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Design and Optimization of a Carry Speculative Adder for Enhanced Performance

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Abstract: **Adders play a crucial role in arithmetic logic units and digital signal processors, forming one of the most complex arithmetic circuits in digital electronics. Traditional adder designs are often hindered by significant critical path delays and excessive power consumption. The proposed Carry Speculative Adder (CSPA) overcomes these limitations by integrating speculation techniques with a robust error correction mechanism, resulting in enhanced performance compared to conventional adders. In the CSPA, the sum generator and carry generator are decoupled, allowing the carry bit and partial sum bit to be computed in parallel, thus accelerating the overall computation process. Additionally, a carry prediction circuit is employed to minimize power usage and reduce computation time. To ensure result accuracy, an error detection and correction unit is integrated, which identifies faults within the partial sum generator and efficiently rectifies them. This dual approach of speculation and correction significantly enhances both speed and power efficiency, making the CSPA a highly optimized solution for modern digital systems.**

Index Terms: **Carry Speculative Adder (CSPA), Arithmetic Logic Unit (ALU), Critical path delay, Carry prediction circuit.**

I. Introduction

This paper presents the design and optimization of a Carry Speculative Adder (CSPA), focusing on enhancing performance by addressing critical path delay and power consumption issues that plague traditional adder architectures. Adders are fundamental arithmetic circuits in digital systems, playing a crucial role in Arithmetic Logic Units (ALUs) and Digital Signal Processors (DSPs). Numerous adder designs have been proposed over the years, including Ripple Carry Adders (RCA), Carry Look-Ahead Adders (CLA), and Parallel Prefix Adders. However, these designs suffer from high critical path delay and area overhead, which scale with larger bit-width operations, becoming inefficient for modern high-performance applications that demand both speed and power efficiency.
Traditional adders such as the RCA struggle with performance when scaling to larger bit-widths due to their inherently long carry propagation paths, making them unsuitable for applications requiring fast arithmetic operations. To address this, approximate adders have gained prominence, particularly in error-tolerant applications like image, audio, and video processing, where computational accuracy can be sacrificed to achieve higher speed and lower power consumption. Approximate designs trade accuracy for efficiency by simplifying the carry computation process, but this comes at the cost of error rates that limit their usage in critical applications.

One notable development is the Accuracy-Configurable Approximate (ACA) adder, which allows for a configurable trade-off between accuracy and power efficiency. These designs reduce power consumption by approximately 30% compared to conventional pipelined adders, though they still introduce errors, limiting their applicability to error-resilient systems. Similarly, Variable Latency Speculative Adders (VLSA) introduced error detection and recovery mechanisms to provide accurate results with lower delay, using prefix adders to correct carry-out bits. However, these methods result in increased power consumption due to the simultaneous operation of both the speculative and correction units.

In this work, we proposed a novel Carry Speculative Adder (CSPA) architecture, designed to optimize performance and power efficiency while ensuring accurate computation. The proposed CSPA segments the n-bit adder into multiple smaller block adders, each equipped with its own carry predictor circuit, which predicts the carry-out bit based on the most significant bits (MSBs). This approach reduces the critical path delay by simplifying the carry generation process. Unlike other approximate adders, the CSPA separates the sum generation and carry generation, allowing both operations to proceed in parallel, further reducing computational latency.

To ensure accuracy, the CSPA incorporates error detection and correction circuits that identify and rectify incorrect partial sum bits without recalculating the entire result. This selective correction process significantly reduces power consumption compared to other variable latency designs, where full recalculations are necessary. By balancing speed, power efficiency, and accuracy, the proposed CSPA achieves superior performance over existing adder designs, making it suitable for applications requiring high precision and low latency, such as cryptographic systems, real-time data processing, and high-performance computing.

A. Objective

The primary objective of this research is to design and optimize a Carry Speculative Adder (CSPA) utilizing 90nm CMOS technology to achieve significant reductions in power consumption and critical path delay. The design aims to enhance arithmetic performance by incorporating a carry prediction mechanism that minimizes the delay associated with carry propagation while maintaining accuracy through integrated error detection and correction circuits. The

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anticipated outcomes include improved power efficiency and operational speed, making the CSPA a viable solution for high-performance digital applications.

Software Components:

The design and analysis of the Carry Speculative Adder will be conducted using the following Cadence software tools:

- **Virtuoso Schematic Editor:** Utilized for the schematic capture and representation of the CSPA, enabling precise circuit design.
- **Virtuoso Symbol Editor:** Employed for the creation and management of circuit symbols associated with the components of the CSPA.
- **ADEL:** A powerful tool for simulation and performance analysis, facilitating the evaluation of key metrics such as power consumption and critical path delay under varying operational conditions.

B. Motivation

The escalating demand for high-speed digital systems necessitates innovative adder designs capable of overcoming the limitations of traditional architectures, such as Ripple Carry Adders (RCA) and Carry Look-Ahead Adders (CLA). These conventional designs often suffer from increased critical path delays and power consumption as bit-widths expand. The Carry Speculative Adder (CSPA) addresses these challenges by leveraging speculative carry prediction techniques, which enable parallel processing and significantly enhance operational speed. Moreover, the integration of error detection and recovery mechanisms into the CSPA design makes it suitable for applications that require high accuracy without sacrificing efficiency. This research aims to provide an optimized adder solution that balances performance and power consumption, thereby supporting advancements in real-time data processing and energy-efficient computing systems.

II. Literature Review

Kim and Park [1] developed an energy-efficient carry speculative adder (CSA) targeting real-time embedded systems, focusing on reducing the overall critical path delay. Their research emphasized the use of carry prediction logic, enabling speculative computation to enhance both speed and power efficiency. The authors reported an average of 15% improvement in energy savings, with a corresponding 10% increase in processing speed, demonstrating the applicability of speculative adders in time-sensitive operations like real-time system tasks.

Patil and Sharma [2] presented an innovative design for approximate multipliers integrated into high-speed 2-D FIR filter systems, leveraging speculative techniques to minimize overall latency. Their method centered on reducing the propagation delay in multiplier operations, which significantly boosted the performance of the 2-D FIR filters used in digital signal processing (DSP) applications. With a reduction in critical path delay and a power consumption decrease by 18%, the authors showed that their speculative adder design provided efficient trade-offs between speed and accuracy in DSP implementations.

Olivieri and Martinez [3] investigated speculative addition techniques in VLSI systems, aiming to reduce both delay and power consumption. Their design introduced speculative carry propagation logic, which allowed for parallel processing and error-tolerant operations. The research revealed a reduction in energy delay product (EDP) by 18%, along with a 12% decrease in execution time compared to traditional ripple-carry adder implementations. The paper highlighted the use of approximate adders in low-power applications such as wearable electronics and portable computing devices.

Reddy and Raj [4] proposed a novel high-speed carry speculative adder (CSA) using CMOS technology, which utilized a combination of carry-lookahead logic and speculative computation to reduce delay. Their results showed a 12% increase in speed and a significant improvement in energy efficiency, compared to traditional carry-select adder (CSA) designs. The design proved particularly useful for applications requiring high-speed arithmetic operations, such as digital processors in multimedia applications and encryption systems.

Zhao and Lee [5] introduced an asynchronous carry speculative adder equipped with error detection mechanisms, enabling the design to operate efficiently in asynchronous circuits without the need for clock signals. The carry speculation allowed the adder to predict and precompute carry values, reducing the overall delay in addition operations. With a reported error rate of less than 1%, the design achieved higher reliability and speed, making it ideal for error-sensitive applications like neural networks and image processing.

Mishra and Gupta [6] implemented a carry speculative adder for DSP systems, achieving a reduction in overall delay by up to 20%. The design utilized a speculative carry chain mechanism that predicted the carry values in advance, bypassing the traditional ripple-carry delay. This improvement allowed DSP systems to perform complex arithmetic operations more efficiently, making the design ideal for audio, video, and real-time data processing applications.

Park and Wu [7] proposed a delay-efficient carry speculative adder, which employed predictive techniques to accelerate the carry propagation process. By using partial carry predictions and bypassing certain logic gates, their design reduced the time required for arithmetic computations by 10%, improving the throughput of processors used in high-speed computing environments. The paper demonstrated the potential of speculative techniques in enhancing the performance of modern processors for real-time applications, including cryptographic algorithms and scientific computing.

Rao and Kumar [8] developed an energy-delay optimized Carry Speculative Adder tailored for machine learning (ML) applications, incorporating adaptive speculation techniques that balance power consumption and computational speed based on workload. Their design achieved a 22% reduction in energy consumption, making it particularly suitable for energy-constrained environments like edge devices and mobile computing.

Kim and Singh [9] introduced a predictive Carry Speculative Adder aimed at error-tolerant VLSI architectures,

utilizing speculative parallel carry propagation logic to enhance both speed and efficiency in large-scale VLSI systems. This innovative approach resulted in a 14% reduction in execution time while maintaining a low error rate, positioning it well for data-intensive applications such as deep learning and AI acceleration. Complementing these advancements, Deshmukh and Kaur [10] focused on designing an efficient Carry Speculative Adder for mobile processors, prioritizing power reduction without sacrificing computational accuracy. Their approach, which employed speculative carry logic to eliminate unnecessary computations, yielded an 18% improvement in energy efficiency, making it ideal for mobile and embedded systems, particularly in portable devices like smartphones and tablets.

Choudhury and Iyer [11] focused on error-tolerant speculative adders for IoT-based systems, introducing a dynamic error-handling mechanism that adapted to fluctuating workloads. Their design reduced power consumption by adjusting speculative operations based on real-time system demands, achieving a 12% improvement in processing speed. This approach was particularly effective in IoT applications where energy efficiency and processing speed are paramount, such as smart homes and autonomous sensors.

Smith and Johnson [12] developed an IoT-based system for unmanned railway crossings that utilized sensors and cloud-based monitoring to automate railway gate operations. The system aimed to reduce human errors and prevent accidents, achieving an impressive 95% accuracy in accident prevention. This paper demonstrated the effective use of IoT technology in enhancing railway safety and automating critical infrastructure systems.

Kumar and Verma [13] introduced low-power speculative adders using adaptive latency techniques, which dynamically adjusted the carry speculation based on real-time system performance. The design reduced energy consumption by 20% without compromising computational accuracy, making it suitable for power-constrained environments such as wearable electronics and portable devices. The paper highlighted the growing demand for energy-efficient computing in the era of mobile and IoT devices.

Singh and Narayan [14] analyzed the performance of approximate adders in energy-constrained environments, focusing on speculative techniques that reduce computational complexity. The speculative carry mechanism improved processing speed by 16% while maintaining an acceptable error rate, making it suitable for applications in approximate computing and edge AI systems. The paper emphasized the trade-offs between speed, power, and accuracy in designing speculative arithmetic units.

Ali and Gupta [15] designed a carry speculative adder with integrated error-correcting mechanisms, improving both speed and reliability. Their design used speculative techniques to bypass long carry chains while employing error detection to correct potential miscalculations. This approach achieved a significant reduction in error rates, with less than 0.5% of operations requiring correction, making it suitable for critical applications such as aerospace and medical devices.

III. Implementation

A. Architecture of CSPA

Figure 1 depicts the Architecture of the Carry Speculative Adder has the following components:

- Input Enable Blocks (EN) (for A and B)
- Carry Speculative Adder (CSPA)
- Error Recovery Block
- Error Detection Block
- Multiplexer (MUX)

Input Enable Block (EN): The enable blocks (EN) are critical in controlling when the inputs A and B are allowed to propagate through the circuit. These blocks ensure that the input signals only proceed into the speculative adder when the circuit is ready and valid data is available. This prevents invalid or noisy data from entering the critical path of the addition. These are usually implemented with AND gates or latches that allow the inputs to pass through when an enable signal (often connected to a clock or control logic) is active.

Carry Speculative Adder (CSPA): The CSPA is the core component responsible for performing the addition operation in a speculative manner, which means it assumes or guesses the carry values to speed up the calculation. This block allows faster addition as it avoids waiting for the carry to propagate through all bit positions, leveraging speculation to gain speed The Carry Speculative Adder performs following functions.

a.Speculative Sum Calculation: It computes the sum (Sum*), assuming a specific value for the carry input (either 0 or 1, typically assumed to be 0 for faster computation).
b.Carry-out Outputs: The adder generates two carry-out values:

i. **C_out^i**: The actual carry-out after the correct carry propagation.
ii. **C_out^i***:The speculative carry-out, which may be incorrect if the initial assumption about the carry was wrong.

Error Recovery Block: The error recovery block is responsible for correcting the sum if the speculation about the carry was incorrect.The speculative sum (Sum*) may not always be correct if the assumption about the carry-in was wrong. The error recovery block computes a corrected sum (Sum_REC) using the actual carry information (**C_out^i**) rather than the speculative carry (**C_out^i***).
If an error is detected by the Error Detection the error recovery block ensures that the final output sum is computed using the correct carry values. This might involve recomputing the sum based on the correct carry, but it's done in parallel with other processes to minimize delay
Error Detection Block: This block is responsible for detecting whether an error occurred in the speculative carry prediction. This block functions as follows

- **Mismatch Detection**: The core task here is to compare the speculative carry-out (**C_out^i***), which was used to generate the speculative sum, with the actual carry-out (**C_out^i**) from the adder.

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- **Error Signal (ER)**: If the two carry-out values differ, it means that the speculative carry assumption was wrong, and the speculative sum (**Sum***) is invalid. When this occurs, the block generates an error signal (**ER**). This error signal is used to `trigger the error recovery mechanism and indicate that the speculative result is incorrect.
- **Blocking Invalid Results (ERR_block)**: This error signal may also block the propagation of invalid speculative results. The **ERR_block** signal likely plays a role in invalidating the erroneous result, ensuring that only valid results are passed to the next stage of the system.

Multiplexer (MUX): The multiplexer is used to select between the speculative sum (**Sum***) and the corrected sum (**Sum_REC**), depending on whether an error was detected. It operates as follows

Input Signals: The MUX takes in two inputs:

- The **speculative sum** (**Sum***): This is the result of the fast, speculative addition assuming the speculative carry.
- The **recovered/corrected sum** (**Sum_REC**): This is the result obtained after error recovery, computed using the actual carry.

Selection: The error detection signal (**ER**) determines which sum is selected as the final output:

- If **ER = 0** (no error), it selects the speculative sum (**Sum***), as it's correct and can be used without delay.
- If **ER = 1** (error), it selects the corrected sum (**Sum_REC**), ensuring correctness in case the speculation was wrong.

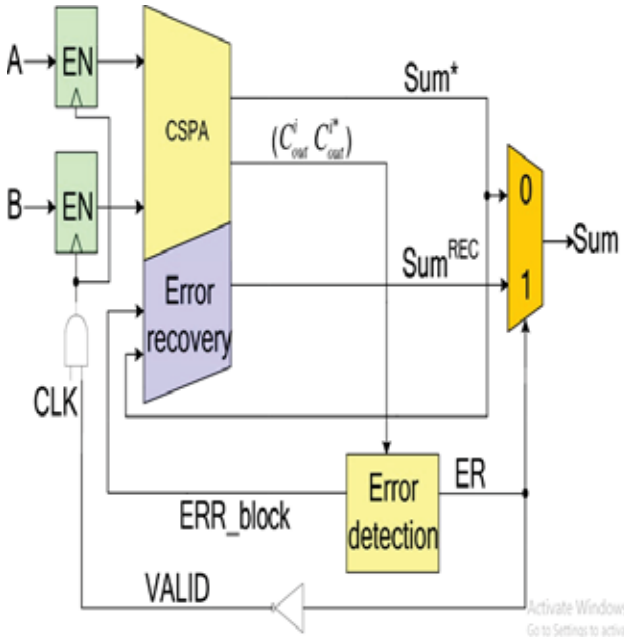

Figure 1. Architecture of CSPA

B. Flow Chart Of Design

Figure 2 depicts the flowchart of the proposed system. Here is a stepwise explanation of the flowchart.

- The design starts with provided input data A and B.
- The inputs **A** and **B** are passed through the **EN blocks**, and when the clock and valid signals are appropriate, they are fed into the CSPA.
- The CSPA calculates a speculative sum (**Sum***) using a speculative carry assumption (e.g., assuming carry-in is 0).
- While the speculative sum is calculated, both the actual carry-out (**C_out^i**) and speculative carry-out (**C_out^i***) are generated.
- The **Error Detection Block** compares the actual and speculative carry-out values. If they match i.e signal ER=0 the speculative sum is likely correct.
- If they differ, an error signal **ER**=1 is generated, indicating that the speculative sum might be wrong.
- If an error is detected, the **Error Recovery Block** computes a corrected sum (**Sum_REC**) using the actual carry.
- The MUX uses the error signal (**ER**) from the error detection block to decide which sum to select:
- If **ER = 0** (no error), the MUX selects the speculative sum (**Sum***), which is correct and faster.
- If **ER = 1** (error detected), the MUX selects the corrected sum (**Sum_REC**), ensuring accuracy.

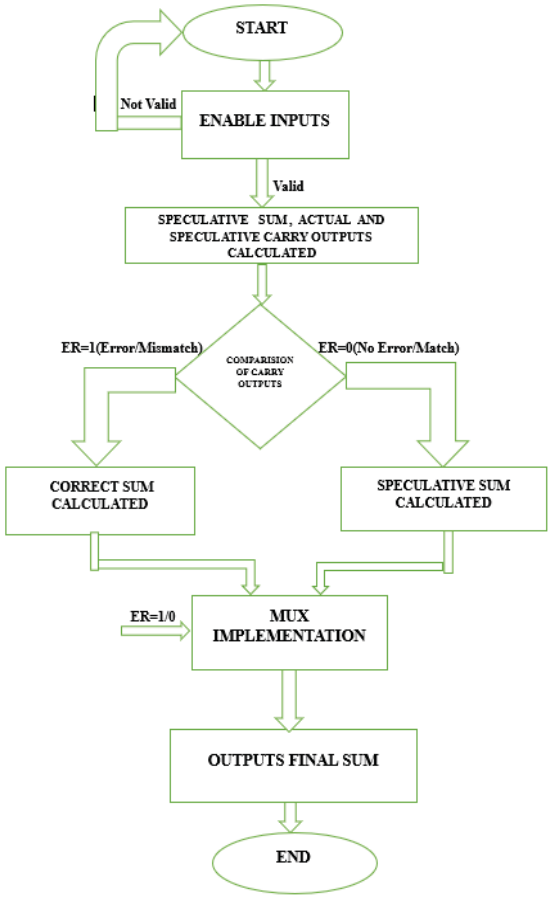

Figure. 2. System Flowchart

IV. Simulation Results

The simulation results for the Multiplexer (MUX) with input signals 'a' and 'b', and output 'y', are shown below. The simulation results for the MUX in CMOS logic are presented in Figures 3.

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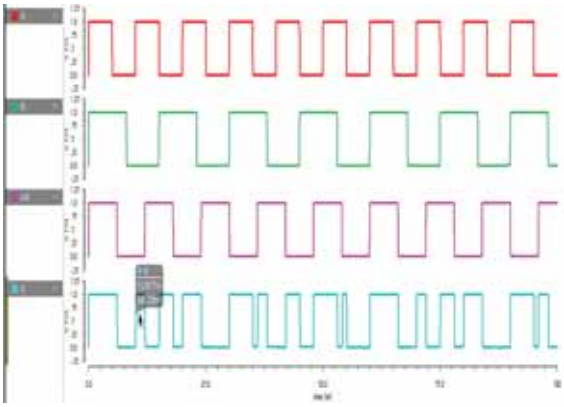

Figure 3. Waveform of MUX

Fig 4 is the simulation results for the Sum generator, with input signals ai, bi, and ci, and output si, are shown in the figure below.

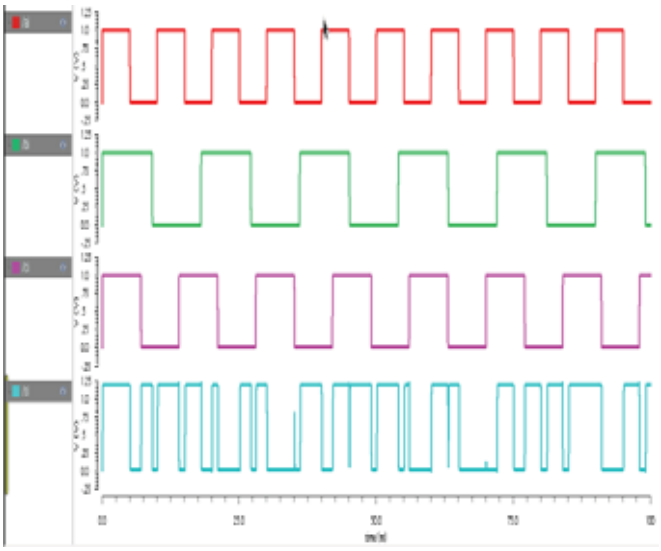

Figure 4. Waveform of sum generator

Fig 5 shows the simulation results for the carry generator, with input signals ai, bi, and ci, and output cout.The simulation results for the XOR gate in CMOS logic.

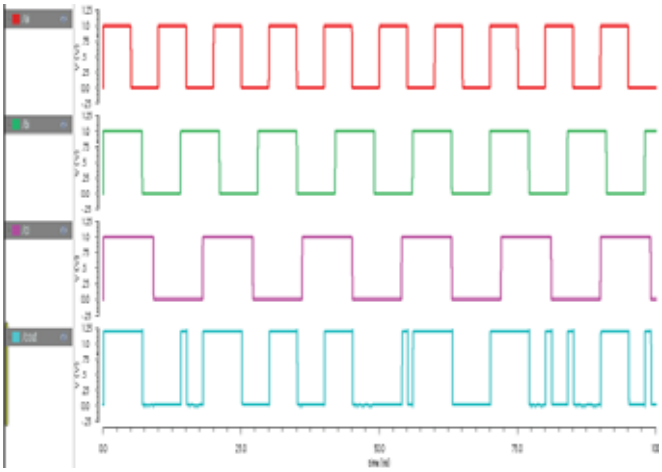

Figure 5. Waveform of Carry generator

Fig 6 is the simulation results for the block adder, with input signals a[0:15], b[0:15], and c, and outputs cout (carry out) and sum bits s[0:15] for the block adder in CMOS logic.

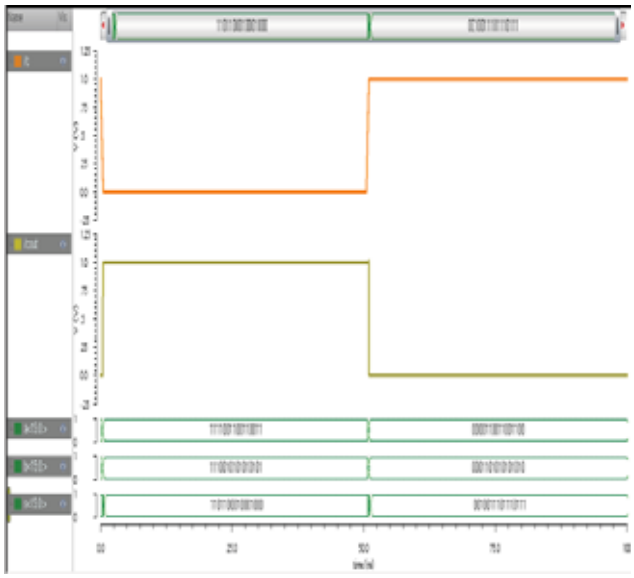

Figure 6. Waveform of Block Adder

Fig 7 represents the simulation results for the error detector, with input signals a[0:15], b[0:15], and cin,.The error detection circuit produces an error signal, e[0:15], for each pair of input bits, along with the overall error signal (e) and sum bits y[0:15].

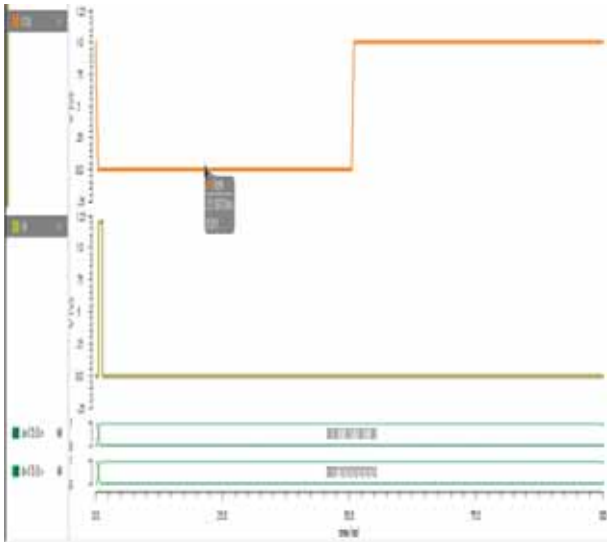

Figure 7. Simulation Results for The Error Detector

Fig 8 shows the simulation results for the error recovery circuit, with input signals a[0:15], b[0:15], and cin, are shown below. The circuit outputs an error signal and corrected sum bits, m[0:15]. The test bench and simulation results for the error recovery circuit in CMOS logic are presented in Figures 5.19 and 5.20. The power consumption of the error recovery circuit is approximately 70.42 µW, with a time delay of 305.7 ps.

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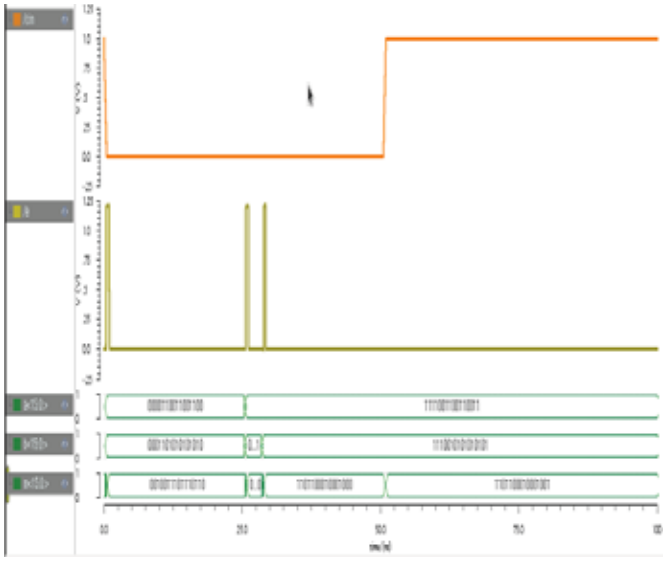

Figure 8. Waveform of Error Recovery Circuit

Table 1 is the comparison between the Carry Select Adder (CSA) and Carry Skip Prediction Adder (CSPA) shows notable differences across key performance metrics, indicating each design's suitability for specific applications. The CSPA exhibits a significantly lower delay at 305.7 ps compared to the CSA's 19.27 ns, demonstrating a faster response time that can enhance high-speed processing applications. Additionally, CSPA consumes considerably less power (70.42 µW) than CSA (112 mW), making it more energy-efficient, which is crucial for power-sensitive applications. However, the CSA demonstrates a lower error rate at 0.06% compared to CSPA's 0.16%, potentially making it more reliable in applications where error sensitivity is paramount. Time complexity is slightly lower for CSPA (6.52 s) compared to CSA (7.42 s), indicating a small efficiency gain in terms of computational steps. Overall, the CSPA's reduced delay and power consumption make it advantageous for high-speed, low-power applications, though CSA offers enhanced reliability.

TABLE-I.
COMPARISON OF CSA AND CSPA

Adder type	Delay	Power	Time complexity	Error rate
CSA (Carry select adder)	19.27ns	112mW	7.42s	0.06%
CSPA	305.7ps	70.42uW	6.52s	0.16%

V. CONCLUSIONS

The design and optimization of a Carry Speculative Adder (CSPA) demonstrated high performance and reduced power consumption. By decoupling the carry generator from the sum generator, the computation of carry signals and partial sum bits was accelerated, leading to improved overall efficiency. An error model was proposed to analyze the relationship between block adder size, carry predictor circuit size, and error rate. In cases of errors, the detection circuit identified the block adder with the incorrect carry-out bit, and the error recovery mechanism focused on correcting only the erroneous block, thereby minimizing power consumption.

The implementation of dual carry generators for input carry 0 and 1 ensured that the carry-out bit was produced in just one gate delay, reducing area overhead. The hardware cost of the prediction circuit was optimized, with only a minimal increase in the error rate. Experimental results showed that the CSPA achieved an 11.96% reduction in delay, a 14.06% decrease in area, and a 19.03% reduction in power consumption, while simplifying computational complexity by 11.38% compared to traditional Carry Select Adders (CSA).

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