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A 32 nm CNFET Model Voltage Controlled Oscillator based ADC Design for Computation-in-Memory Architecture using Emerging ReRAM's

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Abstract: **Applications that are becoming more and more computationally demanding are beyond the capabilities of traditional Von Neumann systems. By adopting new architectural technologies, these flaws can be rectified. Specifically, Resistive Random Access Memory (ReRAM)-based Computation-In-Memory (CiM) holds great promise for satisfying the computational demands of data-intensive applications like database searches and neural networks. In CiM, calculation is carried out analogously; the potential of CiM is hampered by the expensive, time-consuming, space and energy intensive digitalization of the results. To enhance the functionality and energy efficiency of the CiM architecture, an effective Voltage-Controlled Oscillator (VCO)–based analog-to-digital converter (ADC) designed. The proposed ADC can be used per-column rather than sharing one ADC across several columns because of its efficiency. This will increase the CiM crossbar array's overall efficiency and parallel execution. A Multiplication and Accumulation (MAC) technique used in ReRAM-based CiM crossbar arrays is used to evaluate the proposed ADC. The ADC architecture is designed in Cadence Virtuoso, CMOS 45nm technology and then the complete design is implemented using CNFET 32nm Technology, considering its advantages. Figure of Merit, Resolution, delay, signal to noise ratio and power consumption of VCO-ADC are analyzed and compared with other ADCs.**

Index Terms: VCO Based ADC, ReRAM, CNFET Technology.

I. INTRODUCTION

CMOS-based Von Neumann architecture deals with Complementary Metal-Oxide-Semiconductor (CMOS)-based devices, circuits, and architectures that face several challenges [1]. In typical architectures, memory walls, instruction-level parallelism walls, and power walls have a significant negative effect because memory accesses are slow, parallelism is limited, and the clock frequency stagnates due to thermal problems. [2]. However, devices also have issues with high leakage, manufacturing costs that are too high, and reliability. These difficulties are particularly noticeable for data-intensive applications, such neuromorphic computing, where minimizing data transportation and energy consumption is crucial [3]. The necessity to find workable solutions for these application domains has drawn more and more attention. As such, CIM's non volatility , zero-leakage, and high-density characteristics make it a promising candidate to supplant conventional designs and accelerate data-intensive applications. It has been shown that computer systems can function more efficiently and perform better if they are designed with a CiM architecture, which performs operations within the memory and eliminates the need for costly data movement [4]. A CiM can be implemented using both static and dynamic random-access memories (SRAM and DRAM). There are several reasons why memory technologies such as these are suitable for CiM processes, including their unique properties [5]. The physical properties of this resistive memory make it perfect for Multiply and Accumulate (MAC) functions in CiM designs. Resistive random-access memory is a kind of non-volatile storage that functions by adjusting the resistance of a precisely crafted solid dielectric material. It is known that the memristor in the ReRAM device contracts, resulting in a resistance that varies depending on the voltage applied to it. ReRAM is a new technology that many users are implementing. It combines the benefits of RAM and Flash into one unique package. Because of its superior performance and advantages in terms of manufacturability over rival replacement options, it is most likely to replace the flash [6]. ReRAM creates oxygen vacancies, which are flaws in a thin oxide layer that charge and drift in response to an electric field, in contrast to conventional RAM memory types. ReRAM functions by producing resistance rather than storing charge, which makes it like NAND Flash memory. When current is applied, the materials that make up the ReRAM are designed to vary resistance [7]. The NAND-based memory and the RRAM-based memory structure are widely used in memory applications such as computer memories, consumer electronics, smart phones, tablets, and business storage. It is anticipated that the ReRAM application will have additional growth prospects because of technological advancements. ReRAM will find use in deep learning, wearables, automobile infotainment and navigation systems, and the Internet of Things (IoT) in the upcoming years.

The electronic memory market has been controlled by Flash Memory technology for more than 40 years. ReRAM, however, wasn't established until the early 2000s, when certain innovative businesses such as KB-capacity scale

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contributed to its development [8]. To provide a more efficient storage device, manufacturers have developed many types of ReRAM using various dielectric materials. To increase the speed and performance of GPUs, CPUs, and computing processes, RAM memory devices have undergone significant modification over time.

The ADC's job is to convert the analog data that sensors are gathering into digital data that can be processed easily [9]. The voltage-controlled oscillator ADC generates a frequency without giving any input, in contrast to SAR and FLASH ADCs [17,18,19]. ADCs can be used in many ways to implement analog-to-digital conversion. The parameters like sampling frequency, Effective Number of Bits (ENOB), Signal-to-Noise- Ratio (SNR), power consumption, delay, and Figure of Merit (FOM) are analysed by using ADC design. Different ADC architectures are suggested to balance power consumption, SNDR, and conversion speed. The SNDR reduces at lower sampling frequencies due to increased charge leakage by the unit capacitors. The change in frequency is linearly related to change in power consumption [10]. Each type of ADC typically operates optimally within a particular range of resolution and sample rate. While some ADCs are extremely quick but ineffective in high-resolution applications, others, for instance, are efficient at high resolutions but only at low sampling rates. ADCs based on voltage-controlled oscillators show great promise in achieving high energy efficiency. In this system, the first step converts the analog input to a variable-frequency output. For this operation, a voltage-controlled oscillator (VCO) is used. The second stage then uses a reset counter to convert the variable-frequency pulses produced by the VCO into a digital code.

This work is organized in different sections. The introduction of ReRAM and ReRAM based ADC established in Section I. Section II discusses the literature review on VCO based ADC. The internal blocks of conventional VCO based ADC using ReRAMs are presented in section III. The proposed CNFET based VCO based ADC using ReRAMs all architectures and working are discussed in section IV. The simulation results, including a comparison of the performance of important parameters between the current and suggested architectures, are presented in Section V. Section VI concludes with a discussion of the conclusions.

II. Literature Review

The purpose of this work is to demonstrate how analog vital signs can be converted into digital data for digital signal processing using a Voltage-Controlled Oscillator (VCO). A 130 nm CMOS process is used to implement the architecture. It was confirmed that power dissipation was 0.257 mW, active area was 0.007 mm^2, and FOM was 125 dB, all of which are very good results [11]. Analog-to-Digital converters (ADCs) using VCOs are proposed to minimize harmonic distortions. This 40 MHz-bandwidth VCO-based ADC is implemented as an FPGA board with the recommended calibration algorithm, which is based on a CMOS process with a 40 nm CMOS technology [12]. In this brief, an eight-stage pseudo-differential Ring Voltage-Controlled Oscillator (RVCO) built on 65 nm CMOS technology is described for a ten-bit (9.1-bit ENOB) Analog-to-Digital Converter (ADC). As a result, the SNDR is raised to approximately 55 dB because of the 912.9W overall power consumption of the system [13]. This ADC design eliminates the non-idealities of course and fine VCO-based quantizers by using non-linearity cancellation and swing down scaling. Over a 40 MHz bandwidth, the ADC achieved 59 dB SNDR with a 1.2 V supply, yielding 33 fJ/step conversion figure of 1.9 mW. [14]. An ADC based on a VCO is more efficient than an ADC based on a multivibrator. To demonstrate the design working on 65 nm technology, behavioral simulations and transistor-level simulations were used. A power supply noise reduction of 25 dB is reported when the VCO gain is 10% mismatched with a 128 MS/s data rate [15]. The Internet of Things (IoT) wireless sensor node uses a voltage-controlled oscillator (VCO) as a voltage-controlled analog-to-digital converter (ADC). With the use of a resistor-based frequency-tuning technique, VCO's nonlinear transfer characteristic can be reduced, resulting in less odd-order harmonic distortion. An ADC constructed in 28-nm CMOS produces 68 dB SNDR with a 1-Vpp differential sinewave input over a 61-kHz bandwidth, equivalent to an ENOB of 11 using a 1-Vpp input differential sinewave. This device achieves the highest Walden and Schreier FoMs at 167.4 dB and 27.8 fJ/c-s, respectively [16].

The summary from review is different architectures of VCO based ADC presented, the parameters power and delay analysis are poor compared to the proposed work. VCO converts the analog signal to phase domain by producing a continuous output signal whose frequency is proportional to the average analog input signal. The advantage of the VCO based ADC is high Sampling rate, Resolution is high. It is used in gamma ray cameras, sensor applications and ultrasonic applications.

III. Conventional VCO based ADC using Reram's

To transform the crossbar's analog output signal into a digital signal, choose to employ a time-based VCO-based ADC. As a result, it offers the benefits of time-based signaling along with a rather simple design process. With a VCO-based ADC, an analog current must undergo three stages in the phase period before it can be converted to a digital signal. The analog bit-line current must be converted into an analog voltage in the first stage. An analog voltage is then converted into pulses using the VCO. In the final step, a counter is used to count the generated pulses, and a Lookup Table (LUT) is used to map each pulse to the matching digital signal. Power supply voltage can be directly adjusted by adjusting the read voltage (Vread) applied to the crossbar (as row voltages). As a result, turning off the row Vread turns off the ADC and the crossbar. The analogous digital signal that this stage produces is ready for processing by the digital host. Figure 1 depicts the schematic of the entire system, which includes the VCO-based ADC and the ReRAM crossbar. A resistive random-access memory (RRAM) is composed of the parts of a resistive switching memory cell with a Metal-Insulator-Metal (MIM) structure.

The two metal (M) electrodes are positioned between an insulating layer (I) in the construction. High resistance state, or HRS, is regarded as the OFF state or logic 0. Low resistance state, or LRS, is regarded as the logic 1 or ON state.

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The gentle breakdown of the (MIM) structure causes a process that is commonly referred to as "electroforming," and the voltage at which this process takes place is known as the "forming voltage" (V_f). It functions with three volts. The three are read, reset, and set voltages.

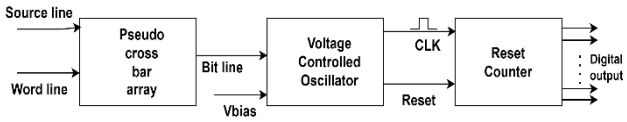

Figure 1. VCO based ADC using ReRAM's

A. Design of Pseudo Crossbar Array

To go from a high resistance state to a low resistance one, SET voltage must be applied. To go from a low resistance condition to a high resistance state, RESET voltage needs to be provided. To read the data from the memory, the READ voltage needs to be applied. When READ voltage is applied, the state remains unchanged.

A pseudo-crossbar array consists of rows and columns of memory cells or logic elements. These cells or elements are arranged in a grid-like fashion, like a traditional crossbar array. Unlike a true crossbar array where each row intersects with each column, in a pseudo-crossbar array, the interconnection is established through a set of switches or multiplexers. These switches control which rows are connected to which columns. Each row and column in the array are addressed individually.

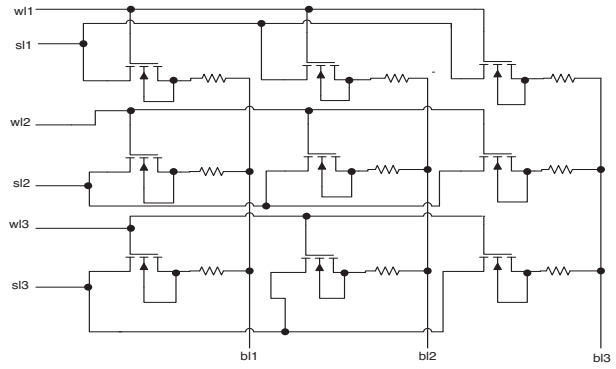

Figure 2. 3x3 pseudo crossbar array

When a particular memory cell or logic element needs to be accessed, the appropriate row and column addresses are selected. To read from or write to a specific cell or element, the corresponding row and column are activated. This activation is typically done by enabling the appropriate switches or multiplexers. Once the row and column are selected, data can be read from or written to the cell or element at their intersection. Fig.2 is a representation of a 3x3 pseudo crossbar array. It has 3 source lines (sl1, sl2, sl3,), 3-word lines (wl1, wl2, wl3) and 3-bit lines (bl1, bl2, bl3,). The data is sent to memory using source lines and it is stored in memory. The control signal is the word line, when word line is high the data can be read. The data is read by using bit lines. The same crossbar array is also designed using CNFET. The proposed array size is 3x3. Each row has 3 basic ReRAM cells, and each column has 3 ReRAM cells. All the column outputs are connected, and they are connected to a single bit line. The output is taken through bit lines. The memory size is scalable according to requirement.

B. Design of Voltage Controlled Oscillator

A ring oscillator is a type of oscillator circuit shown in fig.3 commonly used in digital integrated circuits to generate clock signals or as a frequency source. It is a simple structure comprising an odd number of inverting stages (typically an odd number of NOT gates or inverters) arranged in a ring. A closed loop is produced when the final stage's output is fed back into the first stage's input. Usually, a ring oscillator has an odd number of stages that reverse. This odd number ensures that the feedback loop has a net gain of -1, leading to sustained oscillations. Each stage in the ring is usually an inverter or a NOT gate. This choice of inverting stages ensures that the signal goes through a phase shift of 180^0 with each stage. A closed loop is created by connecting the last stage's output to the first stage's input again.

The feedback loop, combined with the inherent delay of each stage, results in oscillations. The frequency of oscillation is determined by the propagation delay of each inverting stage. As the signal circulates through the ring, it experiences a delay at each stage, contributing to the overall oscillation frequency. Delivering current to each step through the biasing circuit, the first stage made up of transistors MN1 and MP1, is crucial. In transistor MN1, the input voltage control sweep is accepted from least to highest voltage. As a result, the output frequency and drain current (I_d) will both rise in response to a surge in input voltage. The PMOS MP1 transistor reflects the drain current to the steps that follow via a diode connected to it. The output waveform of a ring oscillator is typically a square wave.

C. Design of Reset Counter

A counter is a digital circuit that counts in a prescribed sequence. It can be used to tally the number of clock pulses (or events) that occur. Counters are essential components in digital electronics and find applications in various systems, including frequency dividers, timers, and address generators. A Reset Counter is a circuit that depends on reset for counting the pulses.

It is necessary to comprehend the basic features and functioning of an 8-bit ripple counter in digital electronics to comprehend its theory. Digital circuits that produce a binary count sequence are called ripple counters. A cascade of eight flip-flops, one for each flip-flop that triggers the next in the sequence, makes up an 8-bit ripple counter shown in Fig.4. Following the initial flip-flop, which toggles its output in response to a clock pulse received by the counter, other flip-flops generate a ripple effect. Each counter Consists of a D-Flip flop shown in Fig.5 in which the D-Flip Flop consists of an 3input NAND gate which is designed using transistors is shown in Fig.6.

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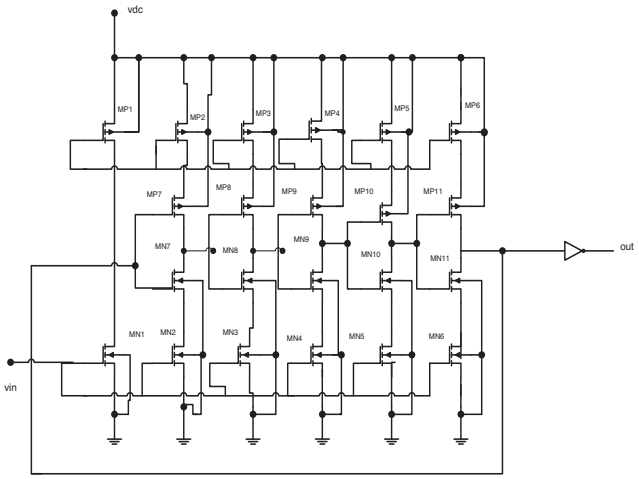

Figure 3. The five-stage current-starved VCO circuit

A ripple counter's primary benefit is its simplicity, as it needs fewer components than synchronous counters. But distinct synchronous counterparts, its disadvantage is the promulgation delay because each flip-flop's output is dependent on the one before it, lengthening the total counting time. Furthermore, because of the propagation delays, ripple counters are prone to glitches, which may call for additional circuitry for error correction. 8-bit ripple counters are nevertheless useful in a variety of digital systems when a trade-off between simplicity and a reasonable counting speed is acceptable, despite these drawbacks.

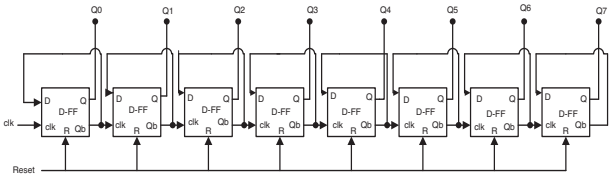

Figure 4. 8 Bit Reset Counter

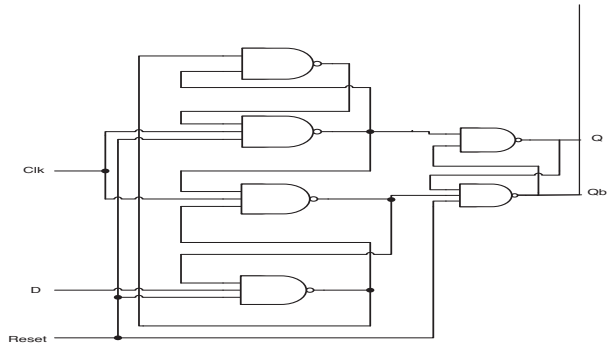

Figure 5. Schematic of D- Flip Flop

Fig. 7 illustrates the usage of a D flip-flop, sometimes referred to as a Data or Delay flip-flop, as a digital storage element in digital circuits for binary data storage.

It is a fundamental building block in digital electronics and is commonly used in sequential logic circuits, such as memory units, registers, and microprocessor components.

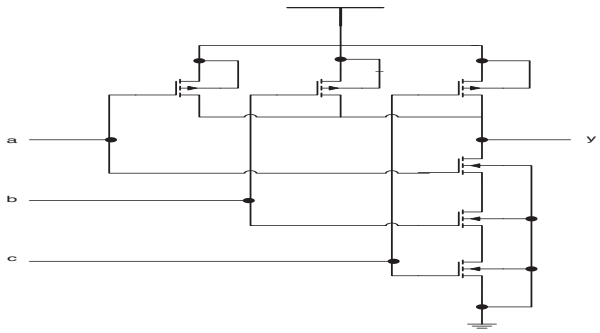

Figure 6. Schematic of 3 Input Nand gate

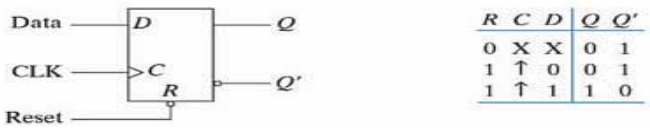

Figure 7. Truth table of D Flip Flop

NAND Gate is a basic digital block in designing a memory element. That performs a Boolean operation called the "NOT-AND" operation. To put it another way, a NAND gate only has a low output (logic 0) when both of its inputs are high (logic 1). If not, a high output is produced (logic 1).

After designing all basic blocks required for VCO-ADC, the task is now to assemble them and make a defined architecture for VCO-ADC. As represented in the above fig.1, 3x3 pseudo crossbar array, Ring oscillator and Reset counter are combined to form a Voltage controlled Oscillator based Analog to Digital Converter using ReRAM's. The working of VCO-ADC is 3x3 pseudo crossbar array have 3 source lines (sl1, sl2, sl3,), 3-word lines (wl1, wl2, wl3) and 3-bit lines (bl1, bl2, bl3,). The data is sent to memory using source lines and it is stored in memory. The control signal is the word line, when the word line is high the data can be read. The data is read by using bit lines. The bit line voltage given to the ring oscillator as an input and the supply voltage value is also given as input itself. The ring oscillator converts the given analog input voltage into frequency. Inverters are typically found in an odd number in any ring oscillator. A sinusoidal waveform is produced by these odd inverters and group ring oscillators . When it is sent through an inverter again it gives a square waveform, which is then used as a clock signal in the counter.

The counter also has a reset input, and the output of the ring oscillator is given as a clock for the reset counter. Based on the different input voltages given, this counter generates an 8-bit digital output. The proposed VCO-ADC uses ReRAM's which can be used for converting Analog input into Digital Output, which has 8 bits.

IV. Proposed CNFET based VCO ADC using ReRAM's

In this work, an effective CMOS architecture for a Voltage-Controlled Oscillator-based Analog-to-Digital converter is used. The advantages of CNFET technology are considered, and the proposed architecture is implemented.

Carbon Nanotube Field-Effect Transistors (CNFETs) stand at the forefront of cutting-edge nano electronics,

representing a pivotal advancement in semiconductor technology. With dimensions on the nanometer scale, CNFETs exploit the exceptional properties of carbon nanotubes (CNTs) to redefine the boundaries of electronic devices. Introduced as a promising alternative to conventional silicon-based transistors, CNFETs offer remarkable potential for enhancing device performance while overcoming the limitations posed by traditional materials. When a voltage is applied to the gate terminal, an electric field is generated across the dielectric layer, which influences the charge distribution within the carbon nano-tube channel. The electrostatic field can be used to control the current flow between the source and drain terminals by varying the gate voltage, which will attract or repel charge carriers within the channel.

CNFETs offer several advantages over traditional silicon based MOSFETs, including higher carrier mobility, lower power consumption, and better scalability. Additionally, CNFETs are less susceptible to short-channel effects, allowing for improved performance at nanoscale dimensions. These advantages make CNFETs promising candidates for future nano-electronic devices, including high-performance computing, flexible electronics, and energy-efficient applications. Ongoing research focuses on optimizing CNFET fabrication processes and exploring novel device architectures to further enhance their performance and functionality.

A lot of digital circuits, including arithmetic circuits, full adder-subtractor circuits, and 6T SRAM, use CNFETs. To enhance the performance of digital or analog designs, MOS and CNFETs are hybridized. Recent years have seen attempts to assess the prospective performance at the device level by modeling and simulating CNT-related devices, such as CNFET. Several optimized approaches are proposed and shown to reduce the impact of parasitic capacitances and increase the CNT ICs' speed.

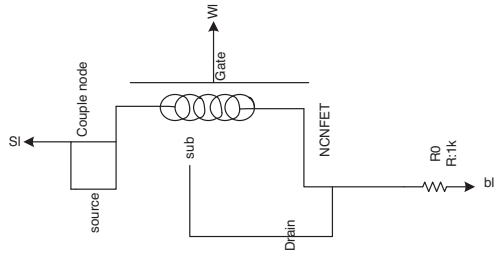

Figure 8. Schematic of ReRAM using CNFET

another important advantage of using a CNTFET device in the nanometer regime is to increase the threshold voltage at 10 nm and beyond the channel length. In the case of the MOSFET while reducing the channel length, the threshold voltage is also reduced, which leads to more leakage power.

Considering the advantages of CNFET over CMOS as discussed, all blocks are designed using CNFET. ReRAM using CNFET, VCO using CNFET, D Flip Flop using CNFET and NAND Gate using CNFET are shown in fig.8, fig.9 and fig.10 respectively. After combining all blocks, the supply voltages V_{dc} and V pulse are applied to memory to all its inputs. The inputs to the memory block are source lines and word lines. These Source lines act as input and they transfer input signal applied to source to bit line, which is acting as output. The word lines act as gates to turn the transistor on and off. Then, the outputs of memory, the bit lines are connected to the input of VCO-ADC. This VCO-ADC now will convert the given analog input voltage into required digital output.

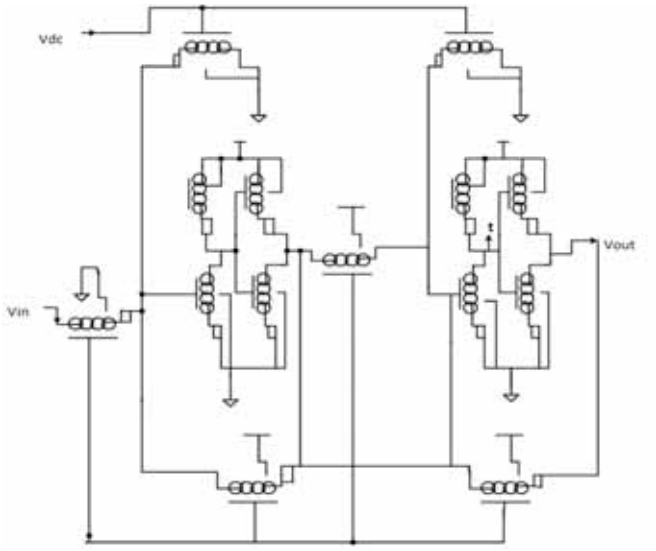

Figure 9. VCO using CNFET

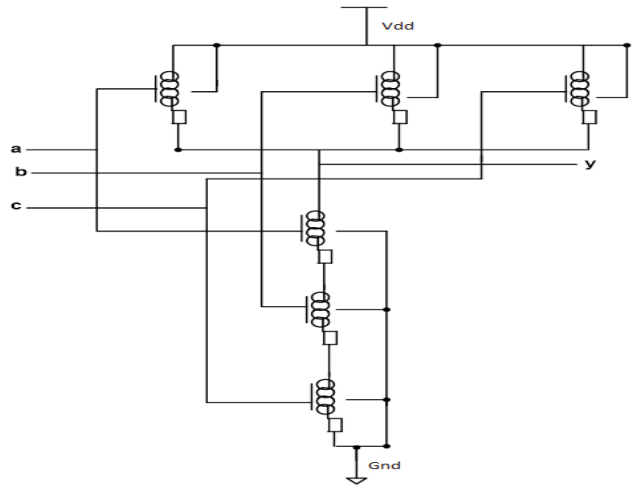

Figure 10. NAND Gate using CNFET

The theoretical calculations of ADC parameters are

1. Figure of Merit (FOM)

The Figure of Merit (FOM) in general is a quantitative measure used to evaluate the performance of any electronic design. It provides a single metric to compare different components based on their key specifications. A lower FoM indicates a more efficient ADC, meaning it can achieve high performance (high ENOB and high sampling frequency) with lower power consumption.

FOM Calculated for P= 9.59 pW, sampling frequency(fs)=3.57 GHz and ENOB=8

$$\text{FOM} = \frac{Power}{2^{ENOB}\ x\ sampling\ frequency} \qquad (1)$$

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$$=\frac{9.59 \times 10^{-12}}{3.57 \times 10^{9} \times 2^{8}}$$

FOM = 0.0104 zJ

FOM Calculated for P= 5.591 pW, f_s=2.2 GHz and ENOB=1.33

$$FOM=\frac{5.591 \times 10^{-12}}{2.2 \times 10^{9} \times 2^{8}}$$

FOM=0.0099 zJ

FOM Calculated for P= 3.972 pW, f_s=1 GHz and ENOB=1.33

$$FOM=\frac{3.972 \times 10^{-12}}{1 \times 10^{9} \times 2^{8}}$$

FOM=0.0155 zJ

2.Signal-to-Noise Ratio (SNR): SNR measures the ratio of the RMS value of the input signal to the RMS value of the noise. It's also expressed in decibels (dB).

SNR = 6.02* N+1.76 (dB). (2)

N= Number of bits

SNR = 6.02* 8+1.76 (dB)=49.92 dB

3.Effective Number of Bits (ENOB): ENOB represents the number of bits that accurately represent the ADC's performance, accounting for noise and distortion. Higher ENOB indicates better performance.

ENOB= (SNR-1.76dB)/6.02 (3)
=(49.92dB-1.76dB)/6.02
=48.16dB/6.02
=8 (Theotical)
ENOB=(45.104dB-1.76dB)/6.02=7.2(practical)

4. Power calculations of proposed CNFET VCO based ADC:

The static power dissipation of an Analog to Digital Converter (ADC) primarily depends on the supply voltage and the static current drawn by the circuit. Static power dissipation occurs even when the ADC is not actively converting analog signals to digital data, as it is the power consumed by the circuit to maintain its ready state.The formula for static power dissipation is:

$$P_{static}=V_{DD} \times I_{static} \quad (4)$$

where:
Pstatic is the static power dissipation,
VDD is the supply voltage,
Istatic is the static current drawn by the ADC.

The dynamic power dissipation in an Analog to Digital Converter (ADC) is primarily due to the switching activity during the conversion process. The formula for dynamic power dissipation is:

$$P_{dynamic}=C_{load} \times V^2_{DD} \times f_{Sampling} \quad (5)$$

where:

- $P_{dynamic}$ is the dynamic power dissipation,
- C_{load} is the load capacitance,
- V_{DD} is the supply voltage,
- $f_{Sampling}$ is the Sampling frequency.

In the context of an ADC, $f_{Sampling}$ is typically the sampling rate or the frequency at which the ADC is clocked. The load capacitance C_{load} represents the total capacitance being charged and discharged during each conversion cycle.

The total power calculated for V_{DD}= 1V, I_{static}= 6.02 pA, C_{load}= 0.001 aF and $f_{Sampling}$= 3.57 GHz

P_{static}= 1 V x 6.02 pA =6.02 Pw
$P_{dynamic}$= 0.001 aF x 1 V x 3.57 GHz = 0.001×10^{-18} x 1V x 3.57 x 10^9 = 3.57 pW
Total Power= P_{static}+ $P_{dynamic}$=6.02 pW+3.57 pW= 9.59 Pw

The total power calculated for V_{DD}= 0.8V, I_{static}= 6.02 pA, C_{load}= 0.001 aF and $f_{Sampling}$= 2.2 GHz

P_{static}= 0.8 V x 6.02 pA =4.816 Pw
$P_{dynamic}$= 0.001 aF x 0.82 V x 3.57 GHz = 0.001×10^{-18} x 0.64 V x 2.2 x 10^9 = 1.408 pW
Total Power= P_{static}+ $P_{dynamic}$=4.816 pW+1.408 pW= 5.591 pW

The total power calculated for V_{DD}= 0.6 V, I_{static}= 6.02 pA, C_{load}= 0.001 aF and $f_{Sampling}$= 1 GHz

P_{static}= 0.6 V x 6.02 pA =3.612 Pw
$P_{dynamic}$= 0.001 aF x 0.62 V x 1 GHz = 0.001×10^{-18} x 0.36 V x 1 x 10^9 = 0.36 pW
Total Power= P_{static}+ $P_{dynamic}$=3.612 pW+0.36 pW= 3.972 pW

5.Power calculations of MOSFET VCO based ADC:

The total power calculated for VDD= 1.2 V, I_{static}= 296.3 μA, C_{load}= 0.1 pF and $f_{Sampling}$= 710 MHz
P_{static}= 1.2 V x 296.3 μA =297.5 μw
$P_{dynamic}$= 0.1 pF x 1.22 V x 710 MHz = 0.1×10^{-12} x 1.44 V x 71 x 10^7 = 102.24 μW
Total Power= P_{static}+ $P_{dynamic}$=297.5 μw + 102.24 μW = 399.74 μW

All these are the Performance Metrics that evaluate any electronic design, to prove it is best than other designs in terms of Power Consumption, Delay, Effective Number of Bits (ENOB), Supply Voltage, Technology used, Figure of Merit (FOM), Signal-to-Noise Ratio (SNR).

V. Simulation Results

The fig.11 is the transient response of 3 input NAND gates Verification is done for both NAND gates using CMOS and CNFET. All the 8 combinations are verified. Fig.12 is the transient response of D flip-flop. Verification is done for both flip-flops i.e., CMOS and CNFET. All the combinations are simulated, and the truth table is verified. Fig.12 can infer that when the clock is triggered the output q is changed according to d input and q-bar is always inverted output of q.

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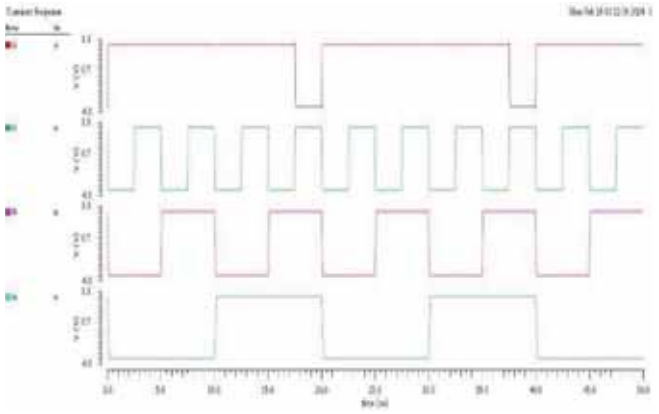

Figure 11. Simulation waveform of 3 input NAND gate

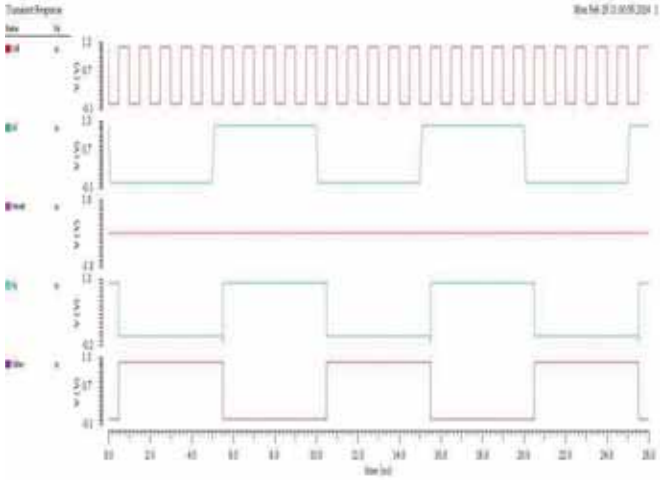

Figure 12. Simulation waveform of D flipflop

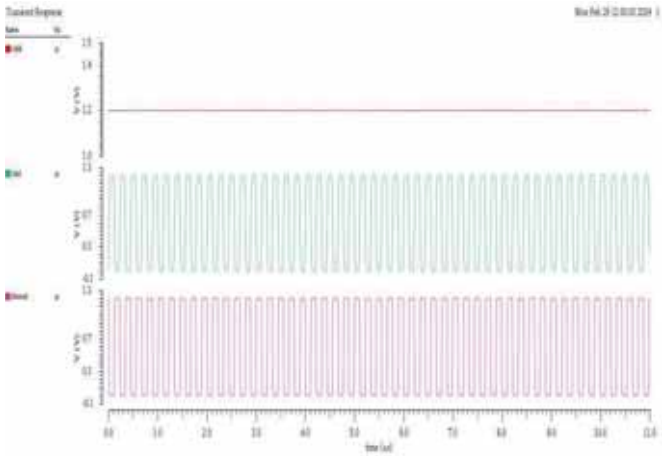

Figure 13. Simulation waveform of VCO

The fig.13 represents the transient response of the ring oscillator. Simulation is done for both the schematics i.e., CNFET and CMOS considering the advantages of CNFET over CMOS. Fig. 13 infers that for the value of vdd of 1 V, the frequency generated is 3.57 G Hz. As discussed in the previous section, it comprises of 8 back-to-back inverters connected to each other. Higher frequencies can be generated using the higher number of stages. ADC satisfied Nyquist criteria that the Nyquist criterion requires that the sampling frequency be at least twice the highest frequency contained in the signal, or information about the signal will be lost.

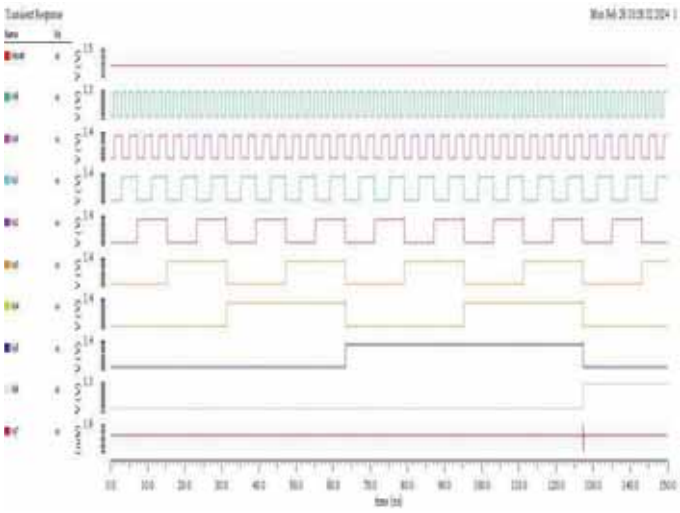

Figure 14. Simulation waveform of Reset Counter

The fig.14. represents the transient response of the reset counter. From fig. 14 it can be inferred that counting starts after reset is zero, and thereafter output is incremented for every clock edge and when output is 255 it becomes zero. The simulation is done for both counters i.e., CMOS and CNFET.

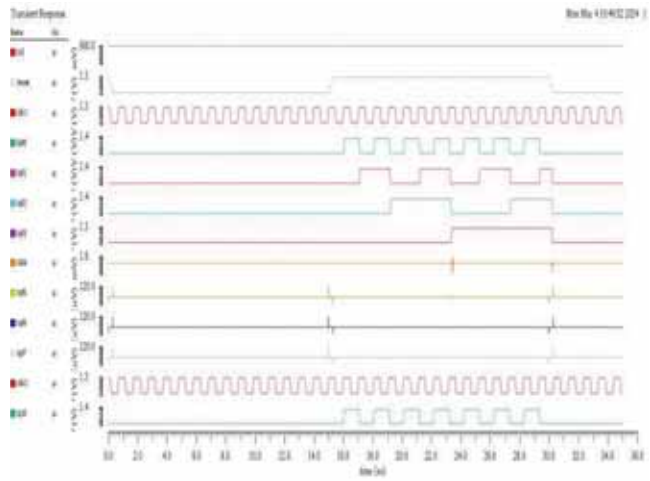

Figure 15. Simulation Waveforms of VCO-ADC for 0.6V Input

The VCO based ADC there is no separate analog input is given so the supply voltage is the controlled volage and it self-act as a input voltage. The input voltage converted into the digital form for this concept, so the input voltage is generated from pseudo cross bar array. Biasing is the setting of DC voltage at operating conditions of an electronic component that processes time-varying signals. Many electronic devices, such as diodes, transistors and vacuum tubes, whose function is processing time-varying (AC) signals, also require a steady DC voltage at their terminals to operate correctly. This voltage is called bias. The pseudo cross bar array inputs are source lines and word lines that are in digital form like logic o and logic 1 to ON or OFF the array switches from that the output voltage generated through bit lines. The bit lines generate the bias voltage that is given to the VCO, and it generates the clock signal that frequency is the sampling frequency mentioned in table.1. For different controlled voltages (input voltages) is 0.6V, 0.8V and 1V the simulated waveforms are shown in this work and

from that clock frequency is the sampling frequency calculated and shown in Table I.

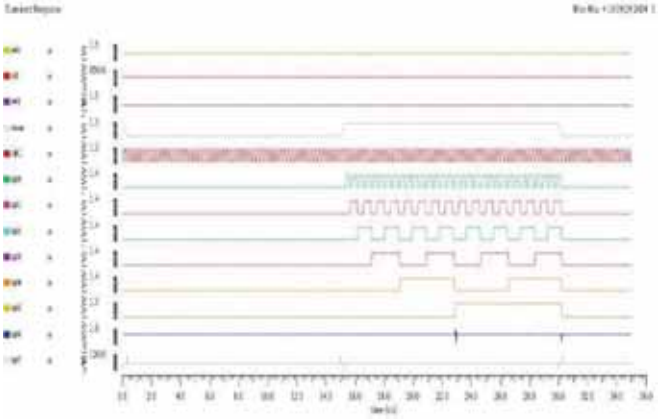

Figure 16. Simulation Waveforms of VCO-ADC for 0.8V Input

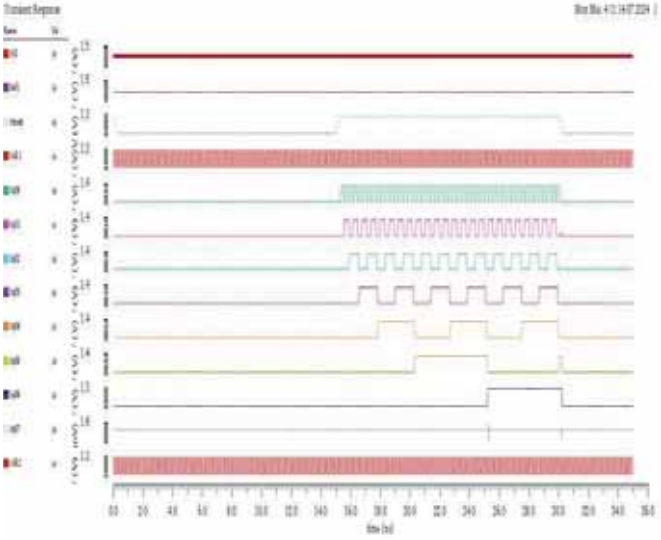

Figure 17. Simulation Waveforms of VCO-ADC for 1V Input

The different input voltages 0.6V, 0.8V and 1V are applied to the VCO based ADC using ReRAM's and the corresponding waveforms shown in fig.15, fig.16 and fig.17 and the digital binary output is analyzed. The Final block of VCO-ADC with ReRAM Memory Architecture is designed using both CMOS and CNFET's. Both the simulation results give Same output digital value for the given analog input voltage. The difference only lies in the performance and advantages of CNFET over CMOS. The comparative analysis of different parameters for proposed and existing is shown in table 1. Observed that the CNFET based ADC power consumption, Delay, figure of merit and SNR is less compared to conventional designs. The limitation of conventional design is under threshold voltage the conversion of analog to digital is not that much accuracy. To overcome that the proposed CNFET based VCO ADC works under threshold voltage and the conversion is more accurate, power and delay is less compared to the conventional designs.

TABLE-I.
COMPARISON BETWEEN PROPOSED AND EXISTING WORK

Parameter	Proposed VCO-ADC with CNFET			VCO-ADC with CMOS	[11]	[13]	[14]
Delay	514.6 p s			16.61 n S	-	-	-
Resolution	8-Bit			8-Bit	4 bit	10 bit	
Technology	32 nm			45 nm	45n m	45nm	45 nm
Supply or input voltage	1 V	0.8V	0.6V	1.2 V	1.2V	1.2V	1.2V
Sampling frequency	3.57 GHz	2.2 GHz	1 GHz	710 M Hz	100 MH z	50 MHz	1.6 GHz
Power	10.94 pW	6.87 pW	4.12 pW	425 uW	0.15 6m W	712.1 2 μW	1.157 mW
FOM	0.020 8 zJ	0.02 1 zJ	0.02 80 zJ	1.37 fJ	125 dB	-	33 fJ
ENOB	1.33			1.33	-	-	-
No. of bits	8			8	4	9.1	-
SNR	49.92 dB			49.92 dB	62 dB	55 dB	59dB

TABLE-II.
COMPARISON BETWEEN THEORITICAL AND PRACTICAL VALUES OF PROPOSED WORK

Parameter	Practical Values of Proposed work			Theoretical Values of Proposed work		
Supply or input voltage	1 V	0.8V	0.6V	1 V	0.8V	0.6V
Sampling frequency	3.57G Hz	2.2GH z	1GHz	3.57 GHz	2.2G Hz	1GHz
Power	10.94 pW	6.87 pW	4.12 pW	9.59 pW	5.591 pW	3.972 pW
FOM	0.0208 zJ	0.021 zJ	0.0280 zJ	0.01 04 zJ	0.009 9 zJ	0.0155 zJ
ENOB	7.2			8		
SNR	45.104 dB			49.92 dB		

The comparison between theoretical and practical work is shown in table 2. Comparing power, FoM, ENOB and SNR parameters of proposed work. Observing that the noise is less in terms of ENOB that is 7.2 bits from this the accuracy of ADC is not that much deviated by using CNFET model. Whenever the ENOB is near to the theoretical value, the lower FoM indicates a more efficient ADC, meaning it can achieve high performance (high ENOB and high sampling frequency) with lower power consumption.

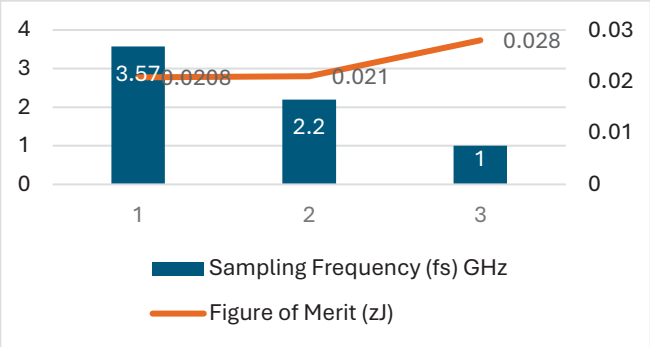

Figure 18. Monte carlo Simulation of VCO-ADC

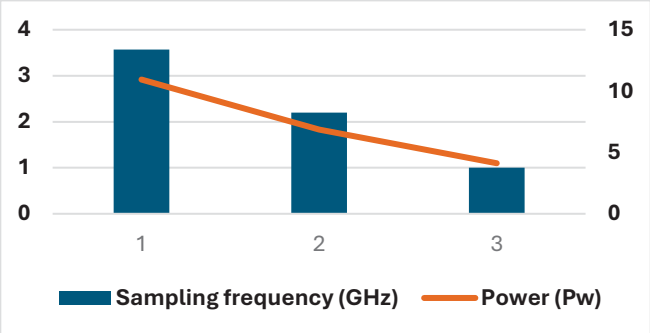

Figure 19. Monte carlo Simulation of power analysis in VCO ADC

The monte carlo simulation of VCO ADC shown in fig.18 observed how the figure of merit is changed for different supply voltages and sampling frequencies. The monte carlo simulation of power analysis in VCO ADC shown in fig.19 observed that the power dissipation is changed linearly for different sampling frequencies.

VI. Conclusions

In this proposed design, VCO-based ADC offers several advantages over traditional ADC architectures. VCO-based ADCs leverage the oscillation frequency of a voltage-controlled oscillator to encode analog signals into digital form, providing a compact, efficient, and high-speed conversion mechanism. This approach is particularly well-suited for CIM architectures, where the proximity of memory and processing elements enables direct analog signal conversion within the memory array, minimizing data movement and reducing latency. By integrating the VCO-based ADC directly with ReRAM arrays, the proposed design achieves seamless integration of analog-to-digital conversion functionality with memory storage. This integration enables efficient processing of analog data directly within the memory array, eliminating the need for separate ADC units and reducing overall system complexity and power consumption. The Development of VCO-ADC systems with wider bandwidth and extended frequency ranges to meet the demands of emerging communication standards and applications, such as 5G and beyond. The resolution of ADCs can further be improved for higher accuracy and detailed digitization of analog signals, using alternate and advanced FET technology libraries.

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