E-ISSN 2581 – 7957
P-ISSN 2277 – 3916

CVR Journal of Science and Technology, Volume 26, June 2024
DOI: 10.32377/cvrjst2609

Comparative Analysis of 5-Level and 7-Level Single-Phase Cascaded H-bridge Multilevel Inverters

Dr. S. Venkateshwarlu[1], N. Koushik[2], V. Ravi Prasad[3], Ch. Sai Karthik[4]
[1]Professor, CVR College of Engineering/EEE Department, Hyderabad, India
Email: svip123@gmail.com
[2]UG Student, CVR College of Engineering/EEE Department, Hyderabad, India
Email: sharmanmk321@gmail.com
[3]UG Student, CVR College of Engineering/EEE Department, Hyderabad, India
Email: vundruraviprasad@gmail.com
[4]UG Student, CVR College of Engineering/EEE Department, Hyderabad, India
Email: saikarthikchevula@gmail.com

Abstract: **The demand for high-performance, efficient, and reliable power electronic systems has been steadily increasing in various industrial applications, including renewable energy systems, electric vehicles, and smart grids. In response to this demand, the Cascaded H-Bridge Multi-level Inverter (CHB-MLI) has emerged as a promising solution, offering advantages such as improved voltage waveform quality, reduced harmonic distortion, and enhanced power handling capabilities. The CHB-MLI is characterized by its modular structure, comprising multiple H-bridge cells cascaded in series. Each H-bridge cell operates with a separate DC power source, enabling the generation of stepped voltage levels at the inverter output. By intelligently controlling the individual H-bridge cells, the CHB-MLI achieves the synthesis of a high-quality multilevel output voltage waveform. The different multi-level inverter topologies are Diode-Clamped MLI, Capacitor-Clamped MLI and Cascaded H-bridge MLI. This paper focused on key aspects like design, simulation, control strategies, performance evaluation, overall comparison and analysis of 5-level and 7-level CHB-MLIs. By addressing these aspects, this paper aimed to contribute to the advancement of power electronics technology and promote the adoption of the CHB-MLI in real-world applications, fostering energy efficiency and sustainability in power conversion systems.**

Index Terms: **Inverter, Multi-level inverter, CHBMLI, switching, SPWM, MCSPWM, gate signal, waveform, harmonics, THD, MATLAB.**

I. Introduction

A. General Concept

To start off, an inverter, in simple terms, is a very widely used power electronic converter which converts fixed DC input to variable AC output. Any inverter uses power electronic switches like SCR or IGBT or MOSFET (based on the application) for its operation. The output of the inverter is varied by varying the switching sequences and firing angles of the switches. Inverters are of 1-phase as well as 3-phase. Figure 1 shows a general classification of Inverters.

B. Classification of inverters

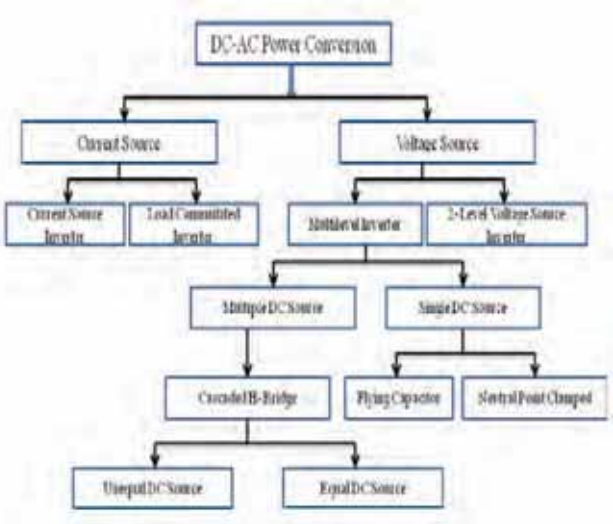

Figure 1. General classification of Inverters

C. Fulfilling the purpose of an Inverter

The main aim of any DC-AC converter is to obtain a smooth variable AC waveform at the output side. This can be achieved by increasing the number of levels in the output waveform. In a simple 3-level inverter with four switches, the possible output values are +Vdc, 0, -Vdc (for a given DC source Vdc). There is an immediate transition in the levels of the waveform whilst it reaches its peak value, which does not give us an output which is near-sinusoidal in nature. As we increase the number of levels, the transition takes place step wise and as a result, we get to observe a waveform which is nearer to a sinusoidal form. The Total Harmonic Distortion (THD) is lesser in those waveforms which are almost sinusoidal in nature. In simple words, the more the number of levels, the better.

Received on 19-03-2024, Revised on 18-04-2024, Accepted on 18-05-2024.

CVR Journal of Science and Technology, Volume 26, June 2024
DOI: 10.32377/cvrjst2609

D. Circuit design requirements

In the case of a CHBMLI, if N is the number of levels in the output waveform, then, Table I shows the design requirements based on the number of levels.

TABLE I.
DESIGN REQUIREMENTS BASED ON NO. OF LEVELS

Design Requirements	Formula
No of Bridges	(N-1)/2
No of Sources	(N-1)/2
No of Switches	2(N-1)
No of carrier waves required (PWM control)	N-1

II. LITERATURE SURVEY

[1] provides an overview of cascaded multilevel inverters, discussing various topologies, control techniques, and applications. It offers insights into the design considerations and performance characteristics of these inverters, serving as a foundational resource for understanding the technology. [2] This work from the University of Tennessee delves into the intricacies of multilevel power converters, covering fundamental principles, control strategies, and emerging trends. It provides comprehensive coverage of multilevel converter architectures and their applications in power electronics systems. [3] The research evaluates the performance of a five-level inverter in the context of solar grid-connected systems. It investigates the efficiency, reliability, and grid integration aspects of the inverter, offering valuable insights into its practical implementation and potential advantages for renewable energy applications.[4] focuses on the simulation of cascaded H-bridge multilevel inverters for photovoltaic (PV) applications. It explores the suitability of multilevel inverter topologies for PV systems, analysing factors such as output waveform quality, efficiency, and grid compatibility through simulation-based experiments.[5] provides a comprehensive overview of multilevel inverter topologies and control strategies. It synthesizes existing research on the subject, highlighting key advancements, challenges, and future directions in the field of multilevel power electronics, offering valuable insights for researchers and practitioners alike. [6] proposes a new cascaded H-bridge multilevel inverter design with improved efficiency. It presents novel circuit configurations or control techniques aimed at enhancing the performance of multilevel inverters, potentially addressing issues such as voltage levels, switching losses, and overall system efficiency. [7] present a comprehensive survey of multilevel inverter topologies, control techniques, and applications, providing a foundational understanding of the field. Kuriakose and Anooja [8] compare the performances of switched DC sources inverters and cascaded H-bridge inverters, contributing to the understanding of different inverter configurations. [9] proposes a symmetrical multilevel cascaded H-bridge inverter using a multicarrier SPWM technique, adding to the repertoire of control strategies for multilevel inverters. [10] offer a comparative analysis of SVPWM and SPWM schemes for NPC multilevel inverters,

enhancing knowledge on modulation techniques. [11] provided a detailed comparative analysis of multi-pulse and multilevel topologies for STATCOM, contributing insights into power quality improvement strategies. [12] introduces a modified hybrid multi-carrier PWM technique for cascaded H-bridge multilevel inverters, advancing PWM modulation methods. [13] discuss the generation of triggering signals for multilevel converters, addressing control aspects crucial for inverter operation. [14] offer a comprehensive review of different multilevel inverter topologies, modulation, and control strategies for grid-connected photovoltaic systems, providing insights into system integration. [15] present multi-carrier PWM strategies for multilevel inverters, contributing to the advancement of modulation techniques in the field.

This literature survey amalgamates diverse perspectives from research articles, surveys, and experimental studies, providing a comprehensive understanding of multilevel inverter technologies, control methodologies, different topologies for their applications, and ongoing research endeavours in the field.

III. 5-LEVEL CHB-MLI

A. Circuit Description

A 5-level CHBMLI has two H bridges connected in series i.e. eight switching devices operate to produce the desired 5 levels in the output waveform. In this case, the reference sine wave is compared with four triangular carrier waves. The frequency of the reference wave is 50Hz whereas that of the carrier waves is in KHz.

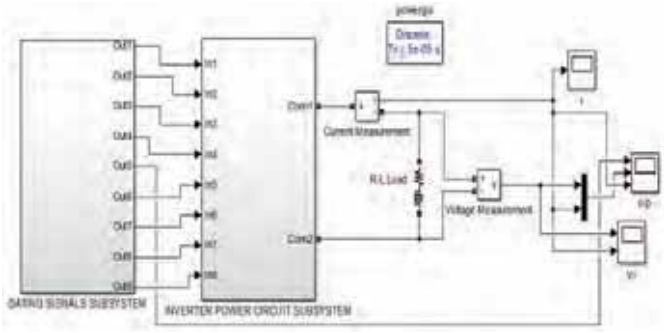

Figure 2. Simulation circuit diagram of 5-Level CHBMLI

Figure 2 shows the MATLAB simulation circuit of a 5-Level CHBMLI which includes the gating pulses subsystem, power circuit subsystem, an R-L Load with V&I measurement blocks and oscilloscopes to observe the waveforms.

CVR Journal of Science and Technology, Volume 26, June 2024
DOI: 10.32377/cvrjst2609

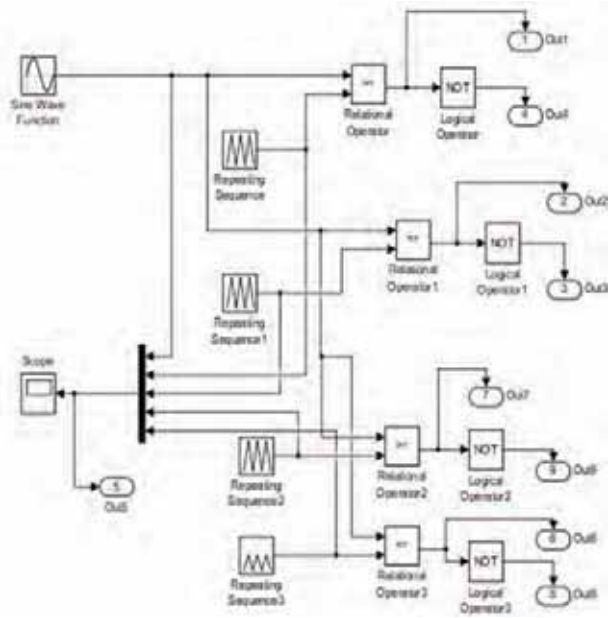

Figure 3. Gating signals subsystem

Figure 3 shows the gating signals subsystem of the 5-Level CHBMLI.

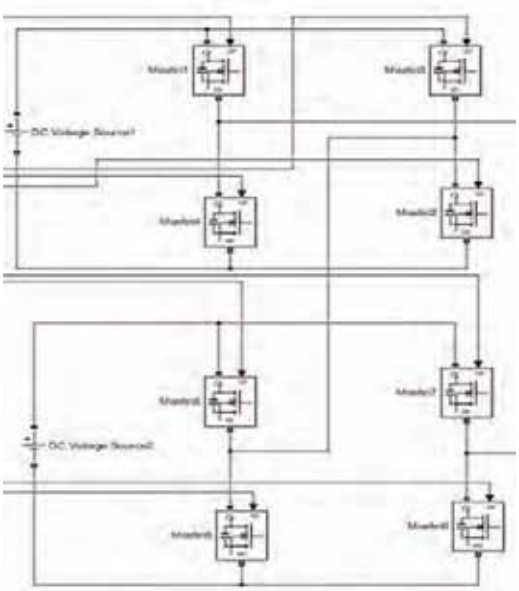

Figure 4. Cascading connections of the two bridges (Power circuit)

Figure 4 shows two H-Bridges in a cascaded fashion. The input fed to the bridges is DC. The switching devices used for the simulation are MOSFETs. The positive end is connected to the Drain terminals of the switches 1,3. The negative is connected to the Source terminals of the switches 2,4. The source of the upper switch is connected to the drain of the switch present below it in the same leg. The switch connections are the same for the second bridge as well. Since both bridges are connected in series, there is a connection between the 2nd leg of bridge-1 and 1st leg of bridge-2. However, the load is connected across the two bridges. One end of the load is connected to a point somewhere in between switches 1,4 of bridge-1 and another end is connected to a point in between the switches 6,7 of bridge-2.

IV. 7-Level CHB-MLI

A. Circuit Description

A 7-level CHBMLI has three H bridges connected in series i.e. twelve switching devices operate to produce the desired 7 levels in the output waveform. In this case, the reference sine wave is compared with six triangular carrier waves. The frequency of the reference wave is 50Hz whereas that of the carrier waves is in KHz.

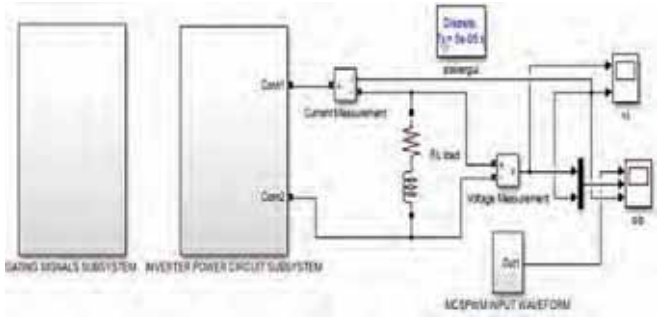

Figure 5. Simulation circuit diagram of 7-Level CHBMLI

Figure 5 shows the MATLAB simulation circuit of a 7-Level CHBMLI which includes the gating pulses subsystem, power circuit subsystem, an R-L Load with V&I measurement blocks and oscilloscopes to observe the waveforms.

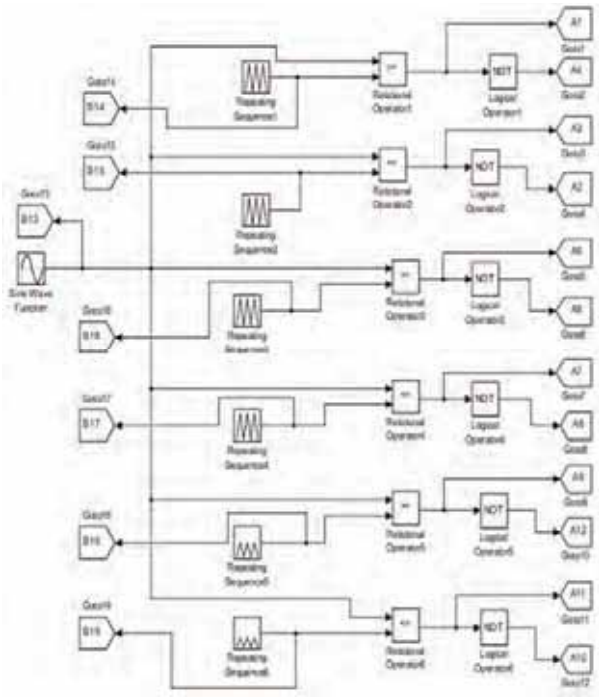

Figure 6. Gating signals subsystem

CVR Journal of Science and Technology, Volume 26, June 2024
DOI: 10.32377/cvrjst2609

Figure 6 shows the gating signals subsystem of the 7-Level CHBMLI.

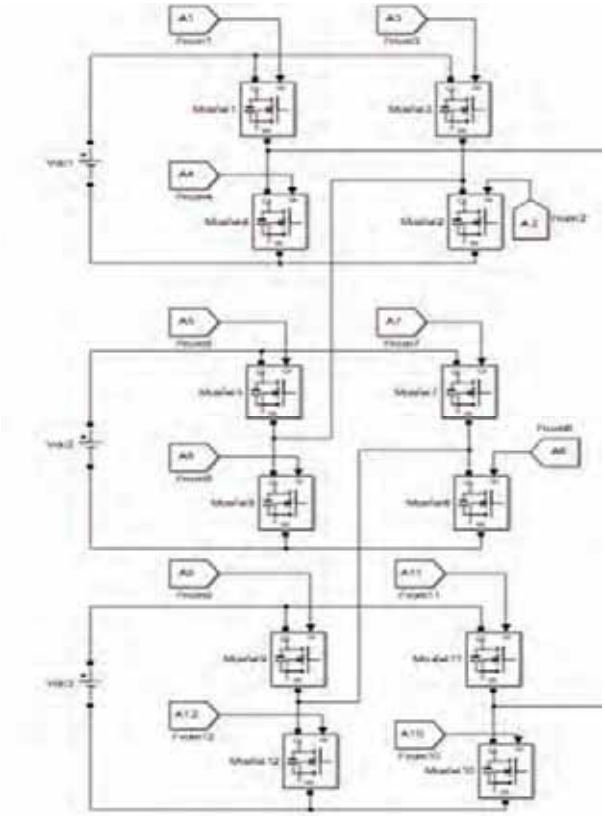

Figure 7. Cascading connections of the three bridges (Power circuit)

Figure 7 shows three H-Bridges in a cascaded fashion. The input fed to the bridges is DC. The switching devices used for the simulation are MOSFETs. The positive end is connected to the Drain terminals of the switches 1,3. The negative is connected to the Source terminals of the switches 2,4. The source of the upper switch is connected to the drain of the switch present below it in the same leg. The switch connections are the same for the second and third bridge as well. Since all three bridges are in series, there is a connection from 2nd leg of bridge-1 to 1st leg of bridge-2, 2nd leg of bridge-2 to 1st leg of bridge-3. However, the load is connected across the first and last bridges. One end of the load is connected to a point somewhere in between switches 1,4 of bridge-1 and another end is connected to a point in between switches 10,11 of bridge-3.

V. Control Strategies

The power electronic switching devices operate i.e. conduct when the gate signal is provided. To trigger the gate terminal, various methods are used. The technique used for this analysis is Multi-carrier Sinusoidal Pulse Width Modulation (MCSPWM). It is an extension of conventional SPWM, which is commonly employed in power inverters to generate AC output from a DC source.

Basic SPWM: In SPWM, a high-frequency carrier signal is modulated by a low-frequency reference signal (sine or triangle wave).The modulation alters the width of the pulses in the carrier signal to create a waveform that approximates a sine wave.

MCSPWM: MCSPWM extends the concept by using multiple carrier signals instead of just one.The idea is to have several carrier waves with different frequencies, each modulated by the same low-frequency reference signal.These carriers are typically evenly spaced in frequency.

Advantages of MCSPWM:

Reduced Harmonics: By using multiple carriers, the modulation spectrum is distributed across different frequencies, resulting in reduced harmonic content in the output waveform.

Improved Performance: Multi-carrier SPWM can provide better harmonic performance compared to single-carrier SPWM, leading to lower Total Harmonic Distortion (THD) in the output waveform.

Based on the control strategy used, the switching gate pulses will be generated and based on this switching, the desired output is achieved.

Figure 8 shows the concept of MCSPWM using a sinusoidal reference signal and two triangular carrier signals.

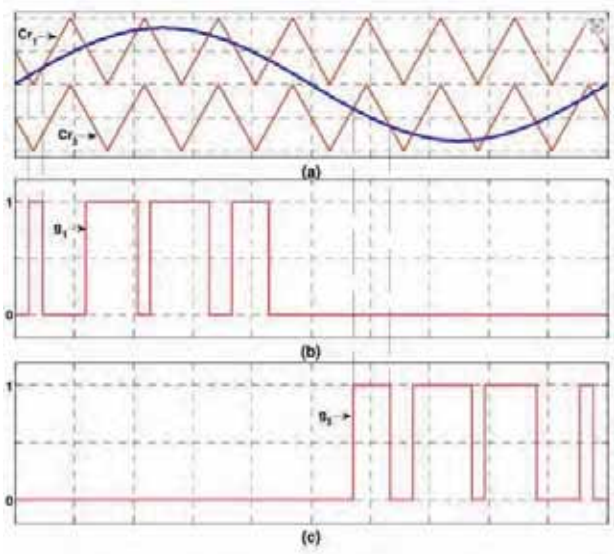

Figure 8. Concept of MCSPWM using a sinusoidal reference wave and two triangular carrier waves

E-ISSN 2581 – 7957
P-ISSN 2277 – 3916

CVR Journal of Science and Technology, Volume 26, June 2024
DOI: 10.32377/cvrjst2609

VI. Switching Sequences

A. Switching sequence of 5-Level CHBMLI

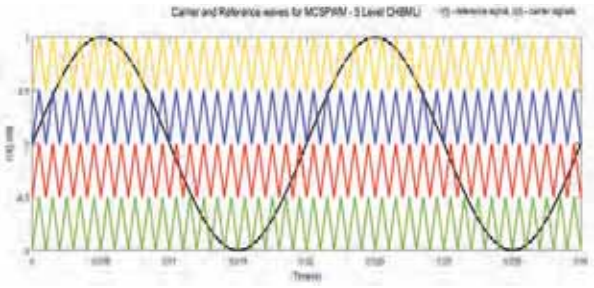

Figure 9. MCSPWM for 5-Level CHBMLI

Figure 9 represents the MCSPWM technique used for the simulation of a 5-Level CHBMLI. As shown in figure 3, a common sinusoidal reference signal (whose frequency is 50Hz and peak value is 1) and since it is a 5-level inverter, 4 carrier signals (2 per each bridge, which are triangular with 2KHz frequency, peak value as 1/2) have been considered. At every instant, the reference and carrier signals are compared with the help of a relational operator and if the reference is greater than the carrier signal, in that case the switches which are not subjected to a NOT operator are turned on and otherwise, the switches which are subjected to a NOT operator are turned on. This is the same for both the bridges.

B. Switching sequence of 7-Level CHBMLI

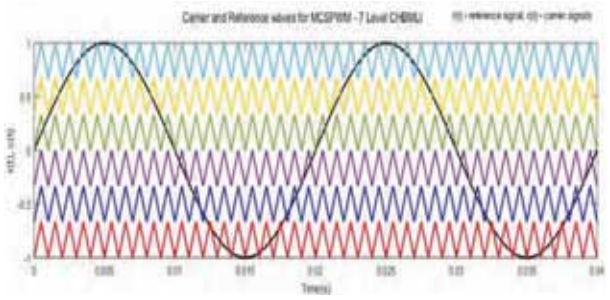

Figure 10. MCSPWM for 7-Level CHBMLI

Figure 10 represents the MCSPWM technique used for the simulation of a 7-Level CHBMLI. As shown in figure 6, a common sinusoidal reference signal (whose frequency is 50Hz and peak value is 1) and since it is a 7-level inverter, 6 carrier signals (2 per each bridge, which are triangular with 2KHz frequency, peak value as 1/3) have been considered. At every instant, the reference and carrier signals are compared with the help of a relational operator and if the reference is greater than the carrier signal, in that case the switches which are not subjected to a NOT operator are turned on and otherwise, the switches which are subjected to a NOT operator are turned on. This is the same for all the three bridges.

For any inverter, the switching order typically follows the modulation index and carrier wave phase relationships to minimize harmonic distortion and maintain waveform fidelity. In this context, switches are activated or deactivated in a pattern that aligns with the modulation scheme, ensuring the desired voltage levels are achieved at the output. The specific switching sequence for these configurations would involve a precise timing mechanism to synchronize the reference and carrier signals and optimize the inverter's performance while meeting system requirements and constraints.

However, the generalized switching of 5-Level and 7-Level CHBMLIs in case of using a microcontroller is determined by a code which works as per the switching sequences shown in the following tables II and III

TABLE II
GENERALIZED SWITCHING SEQUENCE OF 5-LEVEL CHBMLI

Switching sequence								Vdc
S1	S2	S3	S4	S5	S6	S7	S8	
1	1	0	0	1	1	0	0	2Vdc
1	1	0	0	0	0	0	0	Vdc
0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	-Vdc
0	0	1	1	0	0	1	1	-2Vdc

TABLE III
GENERALIZED SWITCHING SEQUENCE OF 7-LEVEL CHBMLI

Switching sequence												Vdc
S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	
1	1	0	0	1	1	0	0	1	1	0	0	3Vdc
1	1	0	0	1	1	0	0	1	0	1	0	2Vdc
1	1	0	0	1	0	1	0	1	0	1	0	Vdc
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	1	0	1	0	1	-Vdc
0	0	1	1	0	0	1	1	0	1	0	1	-2Vdc
0	0	1	1	0	0	1	1	0	0	1	1	-3Vdc

VII. Simulation Results

A. 5-Level CHBMLI

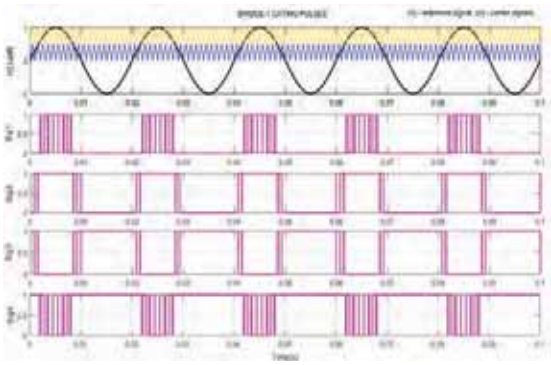

Figure 11. Gating pulses for switches 1,2,3,4

CVR Journal of Science and Technology, Volume 26, June 2024
DOI: 10.32377/cvrjst2609

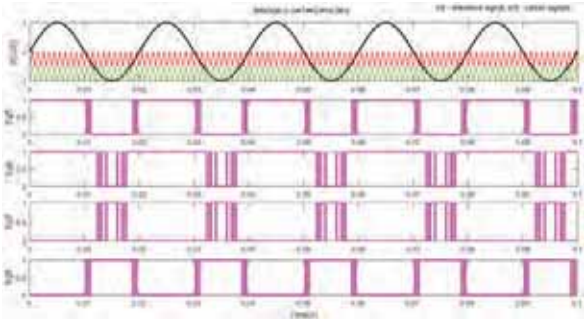

Figure 12. Gating pulses for switches 5,6,7,8

Figures 11,12 represent the switching or gating pulses for the 8 switches present in the 5-Level CHBMLI. These gate signals are generated as per the explanation mentioned in VI. A

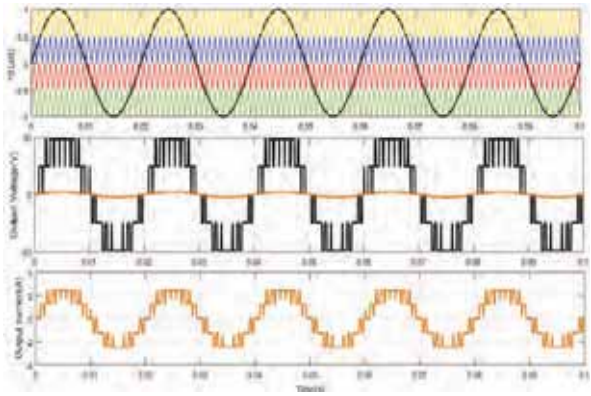

Figure 13. Output Voltage and Current waveforms of 5-Level CHBMLI

Figure 13 represents the simulated 5-level output voltage and current waveform of a 5-Level CHBMLI for a sample R-L load (R=20Ω, L= 0.5mH) and DC input of 25V to each bridge.

B. 7-Level CHBMLI

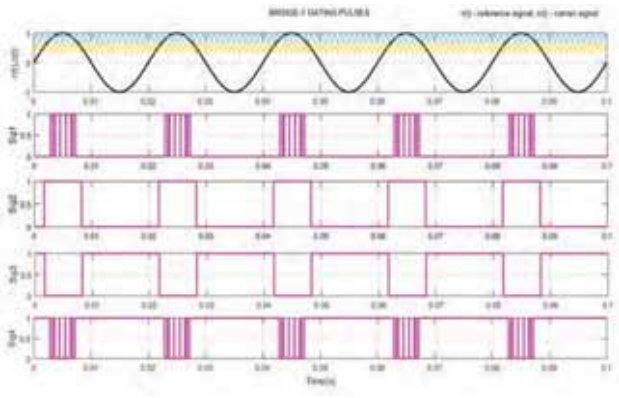

Figure 14. Gating pulses for switches 1,2,3,4

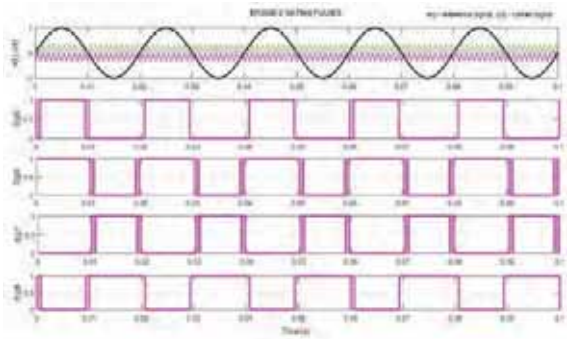

Figure 15. Gating pulses for switches 5,6,7,8

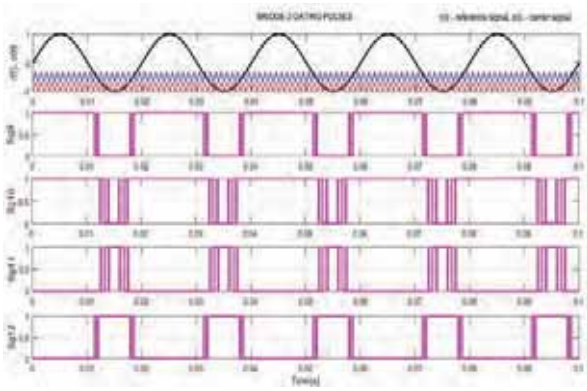

Figure 16. Gating pulses for switches 9,10,11,12

Figures 14,15,16 represent the switching or gating pulses for the 12 switches present in the 7-Level CHBMLI. These gate signals are generated as per the explanation mentioned in VI. B

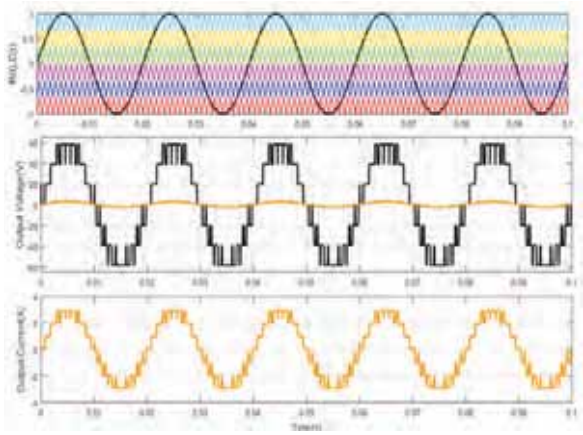

Figure 17. Output Voltage and Current waveforms of 7-Level CHBMLI

Figure 17 represents the simulated 7-level output voltage and current waveform of a 7-Level CHBMLI for a sample R-L load (R=20Ω, L= 0.5mH) and DC input of 20V to each bridge

All the simulations have been performed using MATLAB Simulink, version- R2015a.

CVR Journal of Science and Technology, Volume 26, June 2024
DOI: 10.32377/cvrjst2609

C. FFT Analysis for % THD

In MATLAB, a time-domain signal can be converted into its frequency-domain representation using the FFT-Analysis tool. This tool facilitates spectral analysis tasks such as identifying peak frequencies, measuring frequency components' magnitudes, calculating spectral density, and estimating total harmonic distortion (THD). In this simulation, two cycles of the output waveforms have been considered for THD analysis.

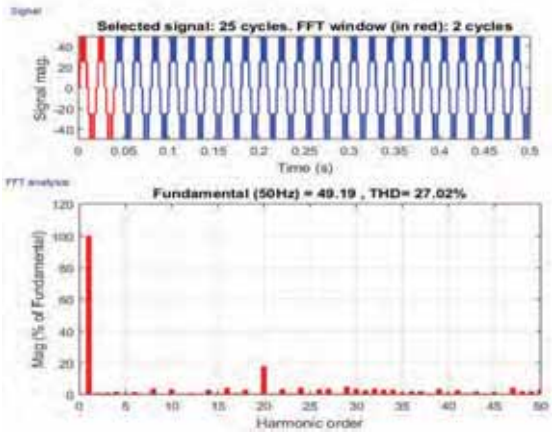

Figure 18. THD in 5-Level CHBMLI output voltage waveform

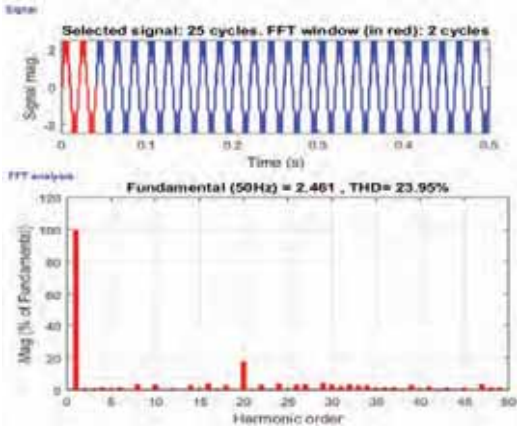

Figure 19. THD in 5-Level CHBMLI output current waveform

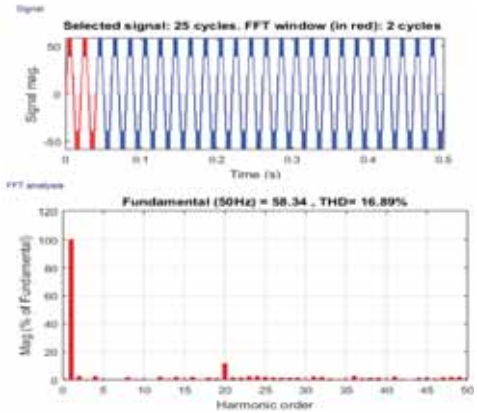

Figure 20. THD in 7-Level CHBMLI output voltage waveform

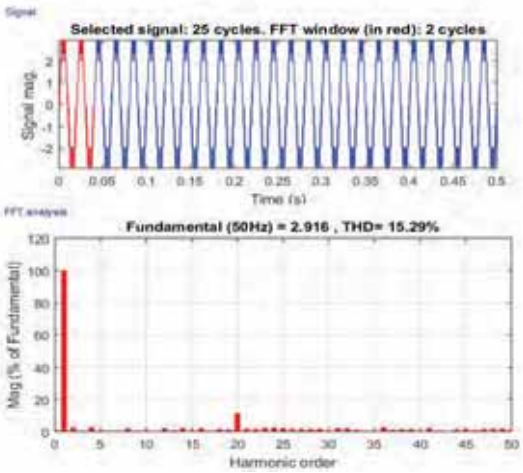

Figure 21. THD in 7-Level CHBMLI output current waveform

Figures 18,19,20,21 represent the %THD in the output voltage and current waveforms of 5-Level and 7-Level CHBMLIs respectively. Figure 22 shows the %THD comparison between the output V&I waveforms of 5-Level and 7-Level CHBMLIs respectively.

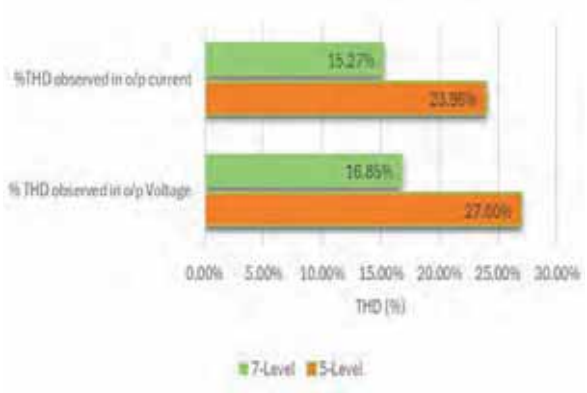

Figure 22. Comparison of %THD in 5-Level and 7-Level CHBMLIs

VIII. CONCLUSIONS

1. A 7-level cascaded H-bridge multilevel inverter offers higher voltage resolution compared to a 5-level inverter, resulting in finer control of the output voltage waveform.
2. The additional voltage levels in a 7-level configuration enable better approximation of sinusoidal waveforms, effectively reducing total harmonic distortion.
3. The finer voltage steps in a 7-level inverter contribute to improved power quality by minimizing voltage fluctuations and waveform distortion. This is particularly advantageous for applications demanding high-quality power supply, such as renewable energy systems and uninterruptible

CVR Journal of Science and Technology, Volume 26, June 2024
DOI: 10.32377/cvrjst2609

power supplies (UPS), grid-tied inverters and motor drives.

4. Implementing a 7-level cascaded H-bridge inverter involves more H-bridge cells and additional circuitry compared to the 5-level counterpart, increasing the complexity and cost of the system.
5. The 7-level inverter may subject its semiconductor devices to higher voltage stress compared to the 5-level counterpart, potentially impacting reliability and lifespan, which necessitates robust device selection and protection strategies.
6. The choice between the 5-level and 7-level cascaded H-bridge inverters depends on the specific application requirements, such as desired output quality, cost constraints, efficiency considerations, and available semiconductor technology. For applications where high-quality output waveform is critical and cost is not a limiting factor, the 7-level inverter may be preferred, while the 5-level inverter could offer a more cost-effective solution for less demanding applications.

REFERENCES

[1] Mariusz Malinowaski, Senior Member, IEEE, K.Gopakumar, Senior Member, IEEE, Jose Rodriguez, Senior Member, IEEE, and Marcelo A. Perez, Member IEEE "A Survey on Cascaded Multilevel Inverters".

[2] Surin Khomfoi and Leon M. Tolbert, "Multilevel Power Converters," The University of Tennessee, pp-31.1-31.50.

[3] Jaysing Ashok Kshirsagar and K. Vadirajacharya, "Performance evaluation of five level inverter for solar grid connected system," International Journal of Current Engineering and Technology, ISSN 2277 – 4106, issue-3, April 2014, pp. 222-225.

[4] Penugonda V. V. N. M. Kumar, P. M. Kishore, R. K. Nema, "Simulation Of Cascaded H-Bridge Multilevel Inverters For PV Applications," ICGSEE-2013 International Conference on Global Scenario in Environment and Energy, International Journal of Chem Tech Research IJCRGG, ISSN : 0974-4290 vol.5, no.2, June 2013, pp. 918-924.

[5] Bindeshwar Singh, Nupur Mittal, Dr. K.S. Verma, Dr. Deependra Singh, S.P. Singh, Rahul Dixit, Manvendra Singh and Aanchal Baranwal, "Multi-Level Inverter: A Literature Survey On Topologies And Control Strategies," International Journal of Reviews in Computing, ISSN: 2076-3328 E-ISSN: 2076-3336, July 2012, vol. 10, pp. 1-16.

[6] Gobinath.K1, Mahendran.S2, Gnanambal.I3 "New cascaded H-bridge multilevel inverter with improved efficiency." International journal of advanced research in Electrical, Electronics and Instrumentation Engineering Vol.2, issue 4, April 2013.

[7] J. Rodriguez. J.-S. Lai, and F.Z. Peng, "Multilevel inverters: A survey of topologies, controls and applications," IEEE Trans. Ind. Electron, vol. 49, No. 4, pp. 724-738, Aug.2002.

[8] Mithun Kuriakose, Anooja V S "Comparison of Performances of Switched DC Sources Inverter and Cascaded H bridge Inverter", International Journal of Science, Engineering and Technology Research, Volume 3, Issue 9, September2014.

[9] Sanjay P.S., Tanaji P.R. and Patil S.K., 2018. Symmetrical Multilevel Cascaded H-Bridge Inverter Using Multicarrier SPWM Technique. International Conference for Convergence in Technology (I2CT), pp. 1-4.

[10] Srivastava S. and Chaudhari M.A., 2020. Comparison of SVPWM and SPWM Schemes for NPC Multilevel Inverter. IEEE International Student's Conference on Electrical, Electronics and Computer Science (SCEECS), pp. 1-6.

[11] Maurya D.S., Jadhav P.D., Joshi R.S., Bendkhale R.R. and Thakre M.P., 2020. A Detailed Comparative Analysis of Different Multipulse and Multilevel Topologies for STATCOM. International Conference on Electronics and Sustainable Communication Systems (ICESC), pp. 1112-1117.

[12] Sarkar I and Fernandes B G 2014 Modified Hybrid Multi-Carrier PWM Technique for Cascaded H Bridge Multilevel Inverter Annu. Conf. Ind. Electron. Soc. 4318–24

[13] Bashi S M, Mailah N and Kadir Z 2008 Generation of Triggering Signals for Multilevel Converter Eur. J. Sci. Res. 24 548–55

[14] Sinha A, Chandra Jana K and Kumar Das M 2018 An inclusive review on different multi-level inverter topologies, their modulation and control strategies for a grid connected photo-voltaic system Sol. Energy 170 633–57

[15] B.P. Mcgrath and D.G Holmes "Multi carrier PWM strategies for multilevel inverter" IEEE Transaction on Industrial Electronics, Volume 49, Issue 4, Aug 2002, pp. 858-867