E-ISSN 2581 – 7957
P-ISSN 2277 – 3916
CVR Journal of Science and Technology, Volume 26, June 2024
DOI: 10.32377/cvrjst2604

Implementation of 5G New Radio Secondary Synchronization on FPGA

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Abstract: 5th Generation New Radio (NR) cellular technology operates at low latency, and higher bandwidths, and makes use of a large number of antennas. NR communication is compatible with a wide range of machine- and human-centered applications. The cell search procedure plays a crucial role in establishing a synchronized connection with the base station (gNodeB) when the user equipment (UE) is enabled, or in the on state. The procedure for cell search finds the physical cell identity of the base station with primary synchronization and secondary synchronization for 3rd Generation Partnership Project (3GPP) 5G NR standards. This paper focuses on identifying the secondary synchronization of Physical Cell Identity (PCI) in the 3rd Generation Partnership Project (3GPP) 5G NR system. Field Programmable Gate Arrays are reprogrammable, flexible, reconfigurable computing circuits and simple to design at very peak frequencies. This suggested architecture employs Secondary Synchronization Signal detection and aims for low power consumption and high speed. The secondary synchronization block has been designed and executed on the Xilinx Zynq FPGA board.

Index Terms: **5G New Radio, FPGA, Cell search, Physical Cell Identity, Primary and Secondary synchronization (SS).**

I. Introduction

The latest fifth generation of wireless technology is produced by the Third Generation Partnership Project(3GPP) for cellular networks. It provides the ability to interact, connect, engage, and experience the world in ways that are similar to those of its predecessors. It enables communication with exceptionally rapid speed, extremely low latency, and millimeter wavelength signals. The 5G New Radio has a frame period of 10 ms. Although the operating frequency is significantly higher than for LTE, the frame structure and OFDM technology are identical to those of the Advanced LTE frame. The 5th Generation NR offers a myriad of applications like signal processing, multimedia, bio-medical, augmented reality, virtual reality, manufacturing, Internet of Things, and transportation, etc.[1]

In 5G New Radio communication, Cell search and signal synchronization are essential elements. The establishment of communication between the base station (gNodeB) and the User Equipment (UE) will be effective if the synchronization is quick and efficient. The synchronization avoids delay spread, inter-symbol interference, and inter-channel interference problems at high frequencies.

Cell search comprises the identification of both primary synchronization signals (PSS) and secondary SSS signals. The Physical Cell Identity is identified, which is then utilized for further demodulation.

This paper primarily focuses on SSS detection for cell identity to establish communication between UE and the base station and the given system is implemented in the Field Programmable Gate Array. The fundamentals of primary synchronization and secondary synchronization are deliberated. Also, the SSS detection is executed using the synchronization block for the 5 New Radio framework [3][4].

Aymen Omri, et al. explained and examined the synchronization process in 5G NR systems. Initially, they discussed 5G NR physical layers, the necessary synchronization techniques, and various synchronization algorithms used for 5G NR that have not been implemented.

J.-C. Lin, "Synchronization Requirements for 5G: An Overview of Standards and Specifications for Cellular Networks," has addressed the importance, requirements, and challenges of synchronization for wireless communications and specified the importance of timing synchronization, frequency synchronization, and space synchronization for the 5G communication.

Chunjing Hu and Yueliang Zhang proposed the algorithm for 5G NR synchronization signal (NR-PSS) detection and implemented it on a field programmable gate array. They reduced the number of multipliers and transformed multiplication into the shift using a preprocessing strategy that reduced the difficulty of the FPGA hardware.

Peng Wang and Fedrick Berggren," Secondary Synchronization Signal in 5G New Radio" proposed a double detection threshold algorithm and simulated it. The 5G NR SSS simulation results are better than LTE SSS but have not been implemented in FPGA.

The proposed architecture is developed by utilizing Verilog HDL with Xilinx VIVADO 2016.4 and executed in the Xilinx ZYNQ FPGA board. The principle of synchronization and the 5G NR frame structure will be discussed thoroughly in upcoming segments.

This paper discussed 5G NR frame structure, synchronization signal for 5G, 5G NR SSS detection algorithm, implementation of 5G NR, simulation results, and conclusion discussed in the coming sections.

Received on 23-03-2024, Revised on 22-04-2024, Accepted on 22-05-2024.

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II. 5G NR Frame Structure

The illustration of the 5G New Radio (NR) frame is shown in Figure 1. The frame period comprises 10 ms and it is subdivided into ten sub-frames with 1 ms. This sub-frame is mathematically shown in equation 1.

Sub frame=Slot2μ (1)

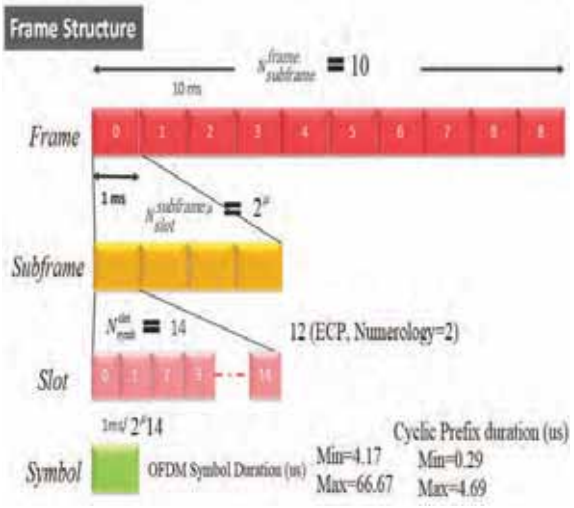

Figure 1. 5G Frame Structure

Each sub-frame is split into slots, with every sub-frame containing 14 slots [5]. Each slot is further divided into symbols, which occupy a small portion of the entire 10ms framework [1]

The frame's mathematical definition is as follows:

Frame=Subclass = 2 μ *14 *10 (2)

When the subcarrier spacing μ =2, then

one symbol = 10 sub-symbols.

One sub-symbol = 2 μ spacing = 2 spaces

One space = 14 OFDM images

symbol = 2*10*14 = 280 OFDM images [6].

Orthogonal Frequency Division Multiplexing (OFDM) images are optimized for the 5G New Radio time frame, making them highly visible at high frequencies, especially with short symbols characteristic of millimeter waves. The synchronization signals PSS and SSS are utilized in the 5G NR system for determining the radio frame boundary and detecting the cell identity (ID) for UE, which is similar to 4G systems. In 5G NR systems, each radio cell is uniquely identified by a cell ID chosen from a pool of 1008 IDs. These IDs are organized into 336 distinct groups. Every group is identified by cell ID group, NID(1)∈ {0,1, …,335}, and comprises three dispa rate segments, specified by the cell ID sector, NID(2)∈ {0,1,2}.

The hierarchical Physical Cell Identity is shown in Figure 2.

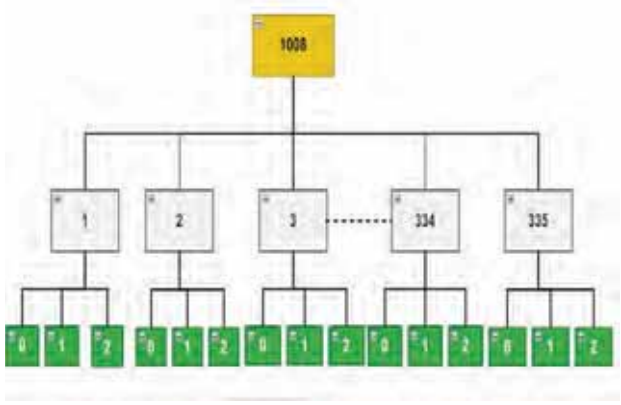

Figure 2: Hierarchy of PSS and SSS

$NID^{(1)}$and $NID^{(2)}$ values from the SSS and PSS, respectively, can be detected by the UE. The UE then uses that information to calculate the serving cell ID in the manner shown below:

$$N_{ID}^{cell} = 3* N_{ID}^{(1)} + N_{ID}^{(2)} \quad (4)$$

Where $N_{ID}^{(1)} \in \{0,1, \dots ,335\}$ and $N_{ID}^{(2)} \in \{0,1,2\}$

III. Synchronization Signal

The initial stage when the user needs to access the mobile network is the 5G NR synchronization process. The primary purpose of this process is to detect the primary and secondary synchronization signals (PSS and SSS). Synchronization is essential for finding a high-quality signal against fading channels, the Doppler effect, inter-channel interference, multi-path interference, and inter-symbol interference scenarios. [7][13]

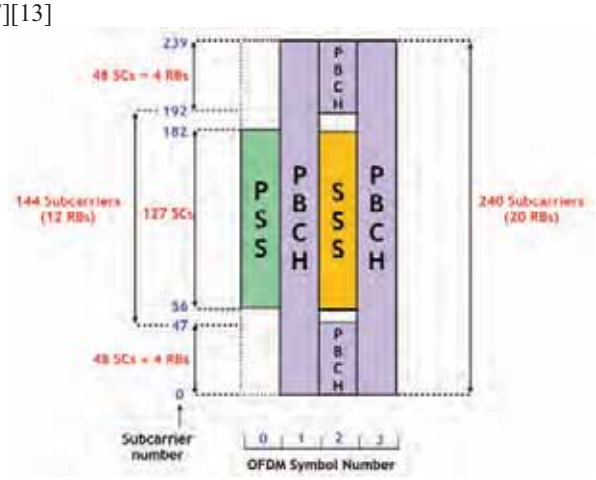

Figure 3: Synchronization Signal block diagram

The synchronization signal block diagram is shown in Figure 3 above. After the generation of PSS, the OFDM symbol0 is generated, and with the PSS value, the SSS value will be calculated at OFDM symbol2.

Physical cell identification of a base station (gNodeB) can be identified by first detecting the PSS value and then determining the SSS value. Figure 4 illustrates the block diagram for finding PCI.

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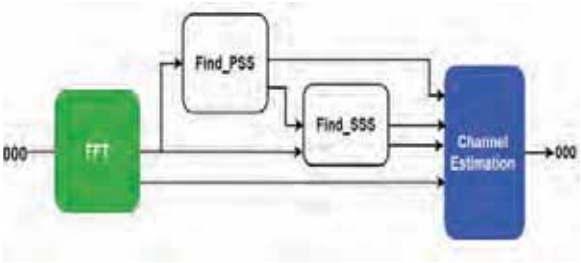

Figure 4: Procedure for finding Physical Cell Identity

The UE first calculates the PSS value and then the SSS value from the received signal will be calculated. PSS provides a radio frame boundary and SSS provides a subframe boundary.

With PSS and SSS values, the Physical layer Cell ID (PCI) will be calculated. The procedure for cell identity calculation is similar, but the number of code groups for SSS is different for finding PCI value compared to LTE.

3.1. Primary Synchronization Signal

The 5G-New Radio (NR) primary synchronization signal is a physical layer-specific signal that determines the radio frame boundary as well as detects the cell ID sector for UEs, e.g., $NID^{(2)}$. the 5G NR PSS, is specifically allocated to the first symbol of each SSB, and 127 subcarriers and it consists of one of three 127-symbol m-sequences PSS has subcarriers with lists ranging from 57 to 183 and is always located in the synchronization block's principal OFDM image. Since the UE oscillator is inaccurate and causes a mismatch with the system reference frequency, the primary goals of PSS are coarse frequency correlation as well as initial symbol alignment. In the time domain, a matched filter of length N= 256 first finds the PSS. To determine the PSS value $NID^{(2)}$, the correlated outputs of the three matched filters of three sectors are maximized.[5]

3.2. Secondary Synchronization Signal

The 5G NR SSS identifies the cell ID group $NID^{(1)}$ and frame identity. However, it is assigned to the third symbol of every SSB, along with the 127 subcarriers, and comprises one of the 336 127-symbol gold sequences. The following definition refers to the 336 potential gold sequences for the SSS:

After PSS detection, the signal proceeds via an OFDM demodulator, recovering the signal from the subcarrier positions in the frequency domain. After that, the receiver can identify the $NID^{(1)}$using SSS detection. Similar to PSS, SSS is always positioned within the third OFDM image of the synchronization block and uses subcarriers that have files ranging from 57 to 183, as shown in Figure 5. [15]

Figure 5. 5G NR Secondary Synchronization Signal Detection Algorithm

The 5G NR Primary SS, however, is allocated to the third image of each SSB and on 127 sub-carriers. It consists of one of three 336 127-image gold successions. The following illustrates the 336 potential gold groupings for the SSS [6]:

$$d_{SSS}= [1 – 2X_0 ((n+m_0) \bmod 127)] [1 – 2X_1 ((n+m_1) \bmod 127] \quad (4)$$

From the above equation 4, SSS ($N_{ID}^{(1)}$is generated by Gold sequence which is derived from a combination of two M-sequences m0 and m1.

$$m0 = 15[N_{ID}^{(1)} / 112] +5 N_{ID}^{(2)} \quad (5)$$

$$m1 = N_{ID}^{(1)} \bmod 112; 0 \leq n < 127 \quad (6)$$

Where

$$X_0(|i + 7|) = (X_0 (|i + 4|) + X_0 (i)) \bmod 2. \quad (7)$$

$$X_1(|i + 7|) = (X_1 (|i + 1|) + X_1 (i)) \bmod 2. \quad (8)$$

And Initial state:

$[X_1(0)\ X_1(1)\ X_1(2)\ X_1(3)\ X_1(4)\ X_1(5)\ X_1(6)] = [1\ 0\ 0\ 0\ 0\ 0\ 0]$
$[X_0(0)\ X_0(1)\ X_0(2)\ X_0(3)\ X_0(4)\ X_0(5)\ X_0(6)] = [1\ 0\ 0\ 0\ 0\ 0\ 0]$

For 5G NR SSS detection, the suggested block diagram is shown in Figure 6. As inputs, the PSS ($N_{ID}^{(2)}$) and pre-SSS are provided.

The pre-SSS signal data is divided into odd and even index blocks in the proposed design for determining SSS. The data sets are then divided into the SSS X0(m0) block and the SSS X1(m1) block.

The SSS block will process the PSS ($N_{ID}^{(2)}$)) data and the even-indexed SSS data by extracting the value m0 from the input signal using the procedure mentioned above from the SSS Generation equations. SSS X1(m1) is nearly identical to the SSS X0(m0) block; to find the value m1 from the input signal, SSS X1(m1) will analyze the odd-indexed SSS data in conjunction with the PSS ($N_{ID}^{(2)}$) information. The outputs of the correlator are fed to the final block, known as the comparator block**.** This block computes the ultimate value of the cell group ID ($N_{ID}^{(1)}$) and finalizes it for the system's output.

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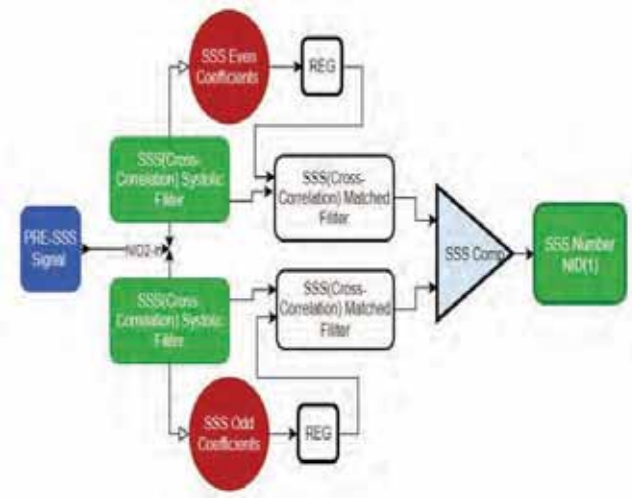

Figure 6. 5G NR SSS detection block diagram

The processing block uses PSS ($N_{ID}^{(2)}$) information and even-indexed SSS data. It extracts the value m0 from the input signal using an algorithm developed from the SSS Generation equations. Similar to the SSS X0(m0) block, the SSS X1(m1) block uses a different algorithm to process odd-indexed SSS data and extract the value m1 together with PSS ($N_{ID}^{(2)}$) information. The outputs of the correlator are fed into the comparator block, the last stage, which generates the system's output by computing the cell group ID ($N_{ID}^{(1)}$) using the previously obtained m0 and m1 values.

The matched filter is designed with Finite Impulse Response Filter. It gives peak output for maximum correlation. [11][12]. The two matched filters' outputs are given to the comparator block. The comparator block will decide the maximum peak value of the SSS number ($N_{ID}^{(1)}$).

After finding the SSS value from the input signal and $N_{ID}^{(2)}$the cell ID will be determined. After finding the cell ID, the next operations are to be performed like the demodulation procedure.

The matched filter is designed with an FIR digital filter. The systolic FIR filter is designed for SSS due to its pipelining and high stability.

3.3 Systolicmatched filter

The systolic FIR filter is an array of processing elements that carries computations on every clock cycle. It is a completely pipelined structure that will offer rapid processing speeds and extremely low latencies. It consists of several processing elements that aim to perform high-speed operations compared to traditional FIR filters within the same period.

The basic definition of the systolic FIR filter is depicted below.

The coefficients are sequenced as {w1, w2, ..., wn}
And the sequences for input {x1, x2, …,xn}

Finally, the resultant sequence is obtained as {y1, y2, …,yn}.

The FIR filter expression is given as:

$$y_i = \sum_{k=0}^{n} w(n)x(k-n) \quad (9)$$

The N tap systolic FIR filter for N=16 taps is designed based on the Direct graph as follows,

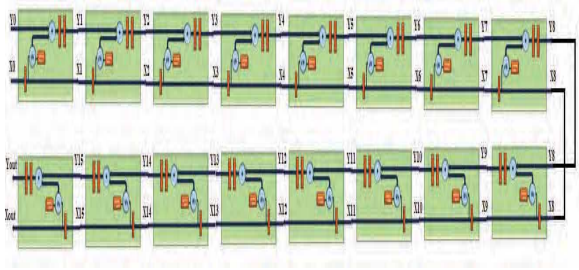

Figure 7: 16 tap Systolic FIR filter block diagram.

16 tap systolic FIR filter consists of 16 processing elements (PE). Each PE consists of a carry select adder, Vedic multiplier, and flip-flops for storage.[12]

The Vedic multiplication algorithm employs a criss-cross technique for n-bit multiplication. It involves splitting the multiplicands into two halves, which are referred to as the Least Significant Bits (LSB) and Most Significant Bits (MSB).

The algorithm is separated into three stages of computation performance. The first stage involves multiplying and providing the product of the LSB bits; the second stage involves multiplying the LSB and MSB bits of both multiplicands in a crisscross fashion and conserving this partial product. The product is obtained in the third stage by multiplying the MSB bits. Ultimately, the final product term is obtained in a single unit step by summing all of the partial products using the corresponding n-bit adder.

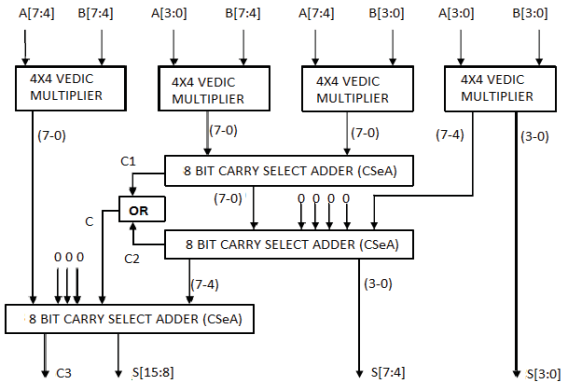

Figure 8: 8-bit Vedic multiplier

The proposed 8-bit Vedic multiplier is designed with a 4 X 4 Vedic multiplier and carries a select adder as shown in Figure 8 above.

The carry-select adder algorithm is implemented in two major stages to perform addition. The general addition is done in the first stage by utilizing the ripple carry process, and the maximum possible carry-in bits are used in the second phase of addition. Consequently, there are two possible outcomes for the carry-in bits: carry-in = 0 and

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carry-in = 1. The determination of the final carry and final sum bits occurs after the second stage has completed its corresponding addition, utilizing the carry-in bits' possibilities. The carry select adder relies on the carry output from the first stage, which feeds into the multiplexer input. By considering the select line bit of the multiplexer, the outcomes are identified or chosen for the addition of the two operands in the second stage. Hereby, the carry select adder is one of the quickest adders that can carry out addition operations in a phase despite the n-bit input.

The carry select adder implementation for the 16-bit data is shown in Figure 9. The proposed carry select adder is a high-speed adder compared to other adder circuits.

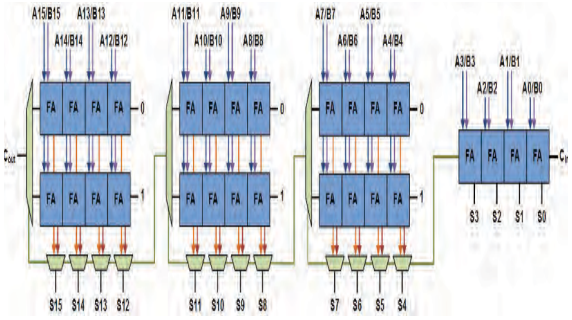

Figure 9. 16-bit Carry Select Adder block diagram.

The proposed systolic FIR is a high-performance and low-power circuit and is considered to be a good choice for the SSS detection system.

IV. Simulation Results

The simulation results for the proposed secondary synchronization block are shown in Figure 10 below. The system processes the SSS input data and $N_{ID}^{(2)}$ value to determine the SSS $N_{ID}^{(1)}$. The data set and the SSS Num value are taken from the system, and a flag head indicates the start of the data symbol. After processing the input data, $N_{ID}^{(1)}$ will be generated and the output flag goes too high to indicate the SSS value is the valid number.

From the simulation results, the calculated secondary synchronization signal value is $N_{ID}^{(1)} = 140(8Ch)$ as shown in Figure 10 below.

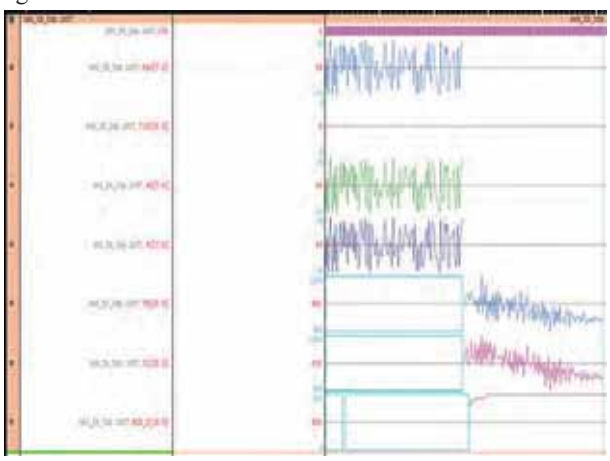
Figure 10: Simulation results of 5G NR SSS.

Finally, the physical cell identity value will be determined with $N_{ID}^{(1)}$) and $N_{ID}^{(2)}$) values. The gate-level schematic diagram for the 5G NR SSS is shown in Figure 11.

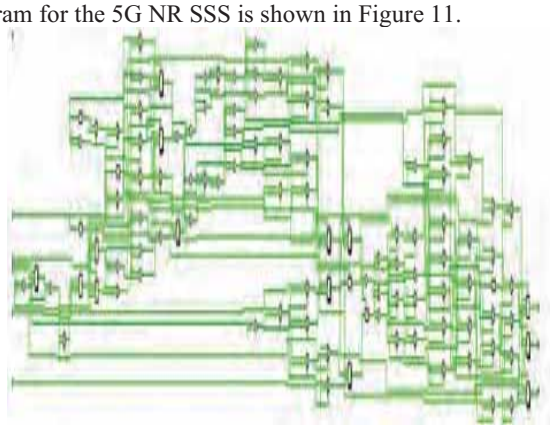
Figure 11. Gate-level schematic diagram of 5G NR SSS

The proposed 5G NR secondary synchronization detection circuit is implemented in the Xilinx ZYNQ board. The FPGA utilization summary is shown in Table 1.

The FPGA utilization summary indicates the resource utilization like flipflops, LUTs, logic blocks, IO blocks, and buffer global clocks, etc.

Table 1: FPGA Utilization Summary

Utilization Summary	Proposed method for SSS		
	Used	Available	Utilization (%)
Number of slice registers	576	17400	3.31
Number of slices LUT'S	773	53200	3.33
Number of flip-flops	264	106400	0.248
No of IOBs	81	200	0.405
No. of BUFGCTRLs	1	32	3.125

From the above FPGA utilization summary, the proposed system uses logic resources with low utilization.

V. Conclusion

The proposed design of a 5G NR Secondary Synchronization Signal for finding Physical Cell Identity is designed, verified, and executed on the Xilinx ZYNQ FPGA board. The outcomes demonstrate that the stated proposition result in the identification of a 5G NR synchronization signal with the proposed technique and also detects the physical cell identity. Also, from the synthesis report, it is observed that logic utilization is reduced. The proposed system has attained low power dissipation and is run at rapid speeds with a minimum of 200 MHz and a maximum of 4 GHz clock rates.

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