E-ISSN 2581 – 7957
P-ISSN 2277 – 3916

CVR Journal of Science and Technology, Volume 25, December 2023
DOI: 10.32377/cvrjst2506

Low Power MIPS-RISC Processor: A Survey

V.Priyadarshini[1], M. Kamaraju[2], U.V. RatnaKumari[3]
[1]Ph.D scholar, JNTUK, Kakinada & Asst. Professor, SR Gudlavalleru Engg. College/ ECE Department. A.P India
Email: darshiniv708@gmail.com
[2]Professor & Mentor (AS&A), SR Gudlavalleru Engg. College/ECE Department, A.P., India
Email: profmkr@gmail.com
[3]Professor of ECE & Vice Principal, UCEK, JNTUK, Kakinada, A.P. India
Email: vinayratna74@gmail.com

Abstract: **This paper describes how low power strategies were used in the design and implementation of low power RISC processors. With the growing demand for energy- efficient computing devices, reduced power usage is now a crucial design factor. The paper provides a detailed analysis of the many low power strategies that can be implemented to lower RISC Processors power consumption. Clock gating, power gating, dynamic voltage and frequency scaling, and instruction set architectural optimizations are a few of these methods. The paper also discusses the impact of these techniques on CPU performance. These techniques introduce the design and implementation of a low-power RISC processor. The results of the experiments demonstrate that the suggested strategies are capable of reducing power usage by up to 50% without adversely compromising processor performance. This paper demonstrates the feasibility of designing low power RISC processors using low power techniques, making them suitable for use in portable and battery-operated devices.**

Index Terms: **MIPS, RISC, Low Power, Clock Gating, Xilinx.**

I. INTRODUCTION

This paper aims to discuss several design methodologies of RISC processor design and to give an overview of low power VLSI techniques that have been employed in the various components of the complete architecture of a processor.

The processor is a crucial component of any device and can significantly affect the battery life. Processors that consume more power will drain the battery life faster than those that consume less power. The battery life of a device is heavily dependent on the type of the processor used. The processors with low power consumption are generally the most battery-friendly. Therefore, choosing a processor that strikes the right balance between performance and power consumption is essential to achieving the desired battery life for a particular device.

Researchers are increasingly calling for surveys and studies to be conducted on low-power processor design with low-power techniques. The main goals of this survey are to identify the most effective low-power design approaches and methodologies, as well as to assess the performance and power consumption of various CPU designs. Based on the results of this survey, the researchers can choose an appropriate method for low-power processor design. This method is essential for advancing processor design and guaranteeing that upcoming gadgets use as little energy as feasible.

The data path is one of the key elements that significantly affect power usage. The power consumption has significantly grown recently since the integrated circuit being built was made to handle heavy computations where data pathways are crucial. As a result of the increased power usage, cooling circuitry will be utilized, which takes up more space. Therefore, a variety of approaches must be employed to lessen the consequences of power dissipation. The circuit is stated to have higher efficiency if the power dissipation is lower. The CMOS logic family is chosen above others due to its low power consumption, which is a straightforward analogue for the aforementioned statement. The consumption of CMOS power can be decreased by introducing a new technique. In this paper, an innovative method for lowering CPU power usage is presented.

The major element of a microprocessor that uses more power is the ALU. Therefore, novel strategies to lessen power dissipation are proposed. There are numerous logic styles available for ALU design. In essence, CMOS logic style (static) can result in lower static power usage. The ALU performs mathematical operations such as addition, subtraction, inversion, shifting, etc., as well as logical operations such as AND, OR, NAND, etc.

The circuits developed with CMOS technology [1], are more power efficient than those developed with other technologies. The power consumption of CMOS technology is superior to that of other technologies.

A CMOS component consumes power only when it switches from one state to another (switching activity). The higher the switching activity, the greater the power consumption.

As predicted by Gordon Moore, co-founder of Intel, transistors getting incorporated into a silicon wafer doubled approximately every 18 months until today. A reduction in the size of transistors results in continuous growth of the semiconductor industry. By improving the performance of the devices, it is transforming the technological world. Typically, a circuit operating at 100 -200 MHz will consume between 15-30 watts of power, and if it operates at 500 MHz, it will consume about 300 watts.

The circuit's operating speed is determined by frequency. Power consumption and frequency requirements are higher for devices that operate at fast speeds. It will become more expensive to cool and pack because of the heat caused by excessive power consumption, which will also degrade the system's performance.

Since 1965, Moore's law has been the driving force behind the fabrication of integrated circuits; however, with the

Received on 31-03-2023, Revised on 03-10-2023, Accepted on 18-11-2023.

CVR Journal of Science and Technology, Volume 25, December 2023
DOI: 10.32377/cvrjst2506

advent of 10 nm technology, the transistor size and atomic size were getting closer, making it difficult to maintain Moore's law, as depicted in figure 1. Power dissipation problems were raised as a result of device scaling. There is a need for alternatives to CMOS technology for the creation of Logic devices in order to address power issues.

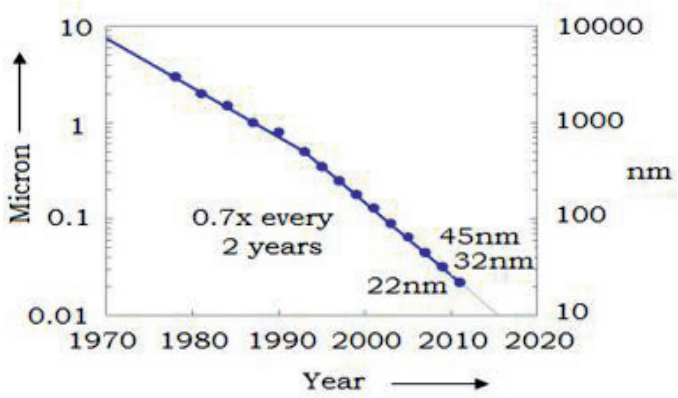

Figure 1. Transistor dimensions scale to improve performance, reduce power and reduce cost per transistor.

High-frequency integrated circuits have been made feasible by the advent of CMOS technology and the ability to fit millions of transistors onto a single sheet of wafer. Additionally, it has decreased the gate latency, increased transistor density, and decreased energy consumption per transistor. According to technical reports, each circuit generation saw a reduction in delay and voltage usage by a factor of 30 percent, a reduction in transistor threshold voltage of 15%, and a doubling of the transistor density on the chip every two years. Despite these benefits, power consumption becomes a problem due to the strong correlation between frequency and dynamic power consumption, which results in a 15% increase in battery's power consumption and 35% percent in overall power consumption.

The size of the devices has been reduced due to technological developments, and now a whole system may be integrated on a single layer of silicon. As a result of their small size and ability to be used anywhere, portable gadgets were in popular demand. However, because they were battery-operated, an increase in power consumption hampered their development. The working frequency of integrated circuits in desktops and servers is being lowered due to overheating, which is reducing chip performance. Power usage has been negatively impacted by the development of portable devices. The frequency of the circuit is also impacted because of the direct relationship between power consumption and frequency of operation. The tremendous need for the creation of portable devices with high computational capability and low battery consumption necessitates power consumption reduction. A sizable amount of the total power consumption is attributed to the data route and clock signal. One of the most important factors in the development of integrated circuits, particularly CPU design, has emerged as power consumption.

II. Motivation

Transistor switching speed has greatly increased in recent years. Despite these benefits, there were several drawbacks as well, including high power consumption and energy waste.

These drawbacks will grow more significant in the future, necessitating the development of further cooling solutions to lower chip package overheating. The transistor density in an integrated circuit has significantly increased, regardless of its size or the application for which it is being created, which results in power consumption of the order of thousands of watts. Systems are overheating and performing worse as a result. Therefore, there is a great need for novel methods that can reduce the system's overall temperature and power dissipation.

The size of the computer system has gradually shrunk from that of a room to a hand-sized device as a result of technical breakthroughs, supporting portability. Power dissipation is one of the performance aspects of these portable gadgets, which is why portability necessitates other features like charged or battery-operated devices.

Data paths are crucial to the operation of processors and power consumption in integrated circuits. There should be some new approaches to lower the power consumption of the data path because it will be higher if the processor is being used for high computational applications. Another criterion for the performance of portable devices is less space. It takes up additional space if cooling circuitry is added to minimize heating and power consumption. New methods that can lower power consumption are therefore needed.

III. Literature Survey

A. Power Management Strategies

The design of a system's flow is composed of several levels of abstraction. The design of a system must be optimized at every stage of the design process in order to run with low power consumption. Power saving can be carried out into any design at three different levels: System level, Logical level, and Technology level. Figure 2 depicts the overall design flow of a system in a bottom-up organization, originating at the lowest abstraction level and working its way up to the highest level.

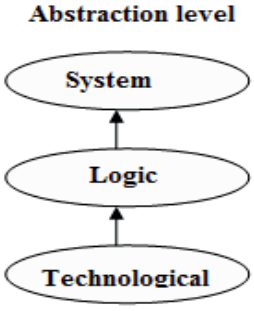

Figure 2. General design flow

Packaging and process technologies are addressed in low power technical level design. This includes:

i) Putting into practice a Silicon on Insulator (SOI) process development with partially or entirely depleted wells to minimize chip and package capacitances. Although this method is incredibly expensive, it has advanced at its own rate since it is so successful. ii) Reducing the supply voltage also reduces power consumption, but it demands new IC fabrication techniques, support circuits for low-voltage operation, such as level converters and DC/DC converters, as well as considerations for signal-to-noise.

Low power logic level [2] design is the level in the general design flow between technologically relevant issues and the system level. This level includes problems with state machines, clock gating, encoding, etc. The fundamental strategy in logic level optimization is reducing switching actions. The methods utilized in logic level design have a significant effect on a system's performance and power usage. Reducing power consumption through effective design techniques is relatively very less expensive than other alternatives, so that's the reason they are frequently adopted.

The system is developed using potential heterogeneous resources individually (electronic, optical, etc.) and will be coupled in a low power system level architecture. Connecting resources for proper functionality in an effective way is the focus of system level design. The chip can be a system if its individual parts are planned and optimized as distinct resources. Partitioning, memory organization, and power management are typical examples at these levels. Depending on the application, several static and dynamic power management approaches can result in significant power savings.

B. Dynamic Power Management

Techniques for reducing power [3] can be divided into two groups: static and dynamic. Static approaches can be used at design time and dynamic techniques during run time. Dynamic Power Management (DPM) [4] [5] [6] [7] refers to the technique of optimizing power consumption in electronic devices by dynamically adjusting the power consumption based on the current workload or usage pattern.DPM is commonly used in batteries, mobile devices and Computer systems to maximize battery life and reduce heat dissipation. In DPM,the system dynamically adjusts the clock frequency,voltage,and other parameters of a processor to minimize power consumption during periods of low activity. When workload or demand increase, DPM boosts performance by increasing frequency and voltage to ensure that the system meets user demands.DPM can be implemented at different levels of the system, including the processor, peripherals, memory and storage. The benefits of DPM include reduced energy consumption, extended battery life and reduced thermal stress, which can prolong the lifespan of components. Additionally, DPM can reduce the system noise, increase performance and decrease the cost of electronic devices by reducing the requirements for cooling and power supplies.

C. Referred Papers:Literature

Aaron P. Hurst [8] developed an approach called Observability Don't Care (ODCs), was used to add clock gating conditions into the design. This paradigm consists of either single-bit registers or single-output combinational logic nodes. This method results in a 7% reduction in the size of the logic network and a 14.5% reduction in dynamic power usage. The disadvantage of this approach is that it is difficult to downsize a large logic network utilizing ODCs.

RananFraer, et al. [9] suggested clock gating analysis, which extracts local or global gating conditions of the state elements that are gated in advance. In order to create a strong gating mechanism for state elements that are not or are gated improperly, certain conditions must be met [10]. Now, all of the state elements have the right propagation of gating conditions. For enabling the state elements, ODC - Observable Don't Care analysis is conducted. In this ODC method, the output from the clock-gated current cycle is an unobservable state. One of the two ways to ODC analysis is the STC approach. This technique allowed for power savings on microprocessor design of up to 28%. ODC and STC analysis have the following drawbacks: (i) they are not beneficial in the designers' approach since they require extra utilities for filtering and sorting; (ii) they must be included into the design cycle.

Macii.E et al. [11] showed leakage and dynamic power reductions might be obtained by combining clock gating (CG) with power-gating (PG). With this method, the same control signal is used to regulate both clock gating and power gating. This strategy results in a 20% reduction in leakage. This technique has two drawbacks: (i) not all circuits may be compatible with it, and (ii) in actual use, the temporal behaviors of the two signals differ.

Rani Bhutada et al. [12] proposed Automated Clock Gating [CG] method. In this case, Automated Clock Gating is implemented directly at the gate level in HDL coding. At different hierarchical levels, the fundamental Register-Based Clock Gating and Complex Clock Gating can be used. The findings indicate a remarkable power loss of roughly 28%.

Hai Li et al. [13] and Brooks D et al. suggested a Deterministic Approach and Value Based Clock Gating respectively. Modern pipeline stages are subjected to Deterministic Clock Gating (DCG). The most important finding is that, for a given cycle, a block's consumption is deterministically known a few cycles in advance for a modern pipeline. Applying DCG results in a 19.9% reduction in CPU power on average without sacrificing performance. This method makes the design verification process more difficult. It is challenging to lower the power using this strategy, especially in SoC designs.

Xiaotao Chang et al. [14] proposed a technique known as programmable clock gating, sometimes termed Intellectual Property (IP) level clock gating. The user can write to activate or disable the IP core clock by changing the flag bits in the control register. The user merely needs to set the control register to 0 to stop the clock when the IP core is not required. When the IP is required, users set the control register to 1, at which moment the clock is activated. The following problems with PCG: i) calls for software control ii) Accurate and efficient user configuration is necessary. System failures or high IP power consumption may be caused by incorrect user settings.

Hans M. et al. [15] suggested a Transparent Clock Gating technique [TCG]. Latches are transparent in this suggested technique. The idea of data partitioning is the basis of TCG. This method allows for a 30% reduction in dynamic power.

Yan Zhang et al. [16] discussed a clock gating approach for optimizing FPGA power. The control enable signal, which is used to turn on or off the clock for unnecessary modules, is received by this multiplexer.

Pi Zhou Ye et al. [17] and Piguet C [18] suggested RISC CPU hardware design core. The PIC 16C6X can use this basic instruction set. 8-bit RISC CPUs are created via a top-down design process. This CPU performs more efficiently than the CISC architecture. This core's shortcomings are that it needs more logic components. In order to lower the power consumption of the CPU core, the chip's frequency is low, low power techniques are not used, and there are fewer on-chip peripherals.

Nalan Erdas et al. [19] used Sea-of-Gates for the development of the 8- bit microcontroller. During the design stage, the logical design and system blocks are implemented at the gate level. The available clock systems are taken into account, and the architecture employs a buffered clock distribution tree. This design has two drawbacks: (i) it operates at a low frequency, and (ii) it uses more power.

Julio C. B. Mattos et al. [20] proposed a stack-based microcontroller. In this manner, a Stack code that uses less bits is required to encode one instruction. In comparison to CISC code, this code is smaller. There is a 31.46% reduction in power consumption possible. This controller's shortcomings include: i) executing fewer instructions ii) processing slowly iii) necessitating more program memory access and iv) generating greater heat.

Dilip Kumar et al. [21] specified a 5-stage MIPS pipelining to determine the delay that is caused by longer paths by employing different processing technologies. The fundamental idea is to shorten the critical path by improving hardware efficiency within the circuit, which leads to an increase in performance. To do this, the pipelines are set up so that high frequency clocks are required for pipelining [7]. Pipelining is the technique of breaking down a logic block into n smaller blocks and inserting latches in between them. This method executes several instructions concurrently. Depending on the processor, the pipeline may have fewer or more phases. Figure 3 depicts the Pipeline Technique's architecture. Multiple instructions are executed concurrently, which reduces power and delay, however, area is impacted.

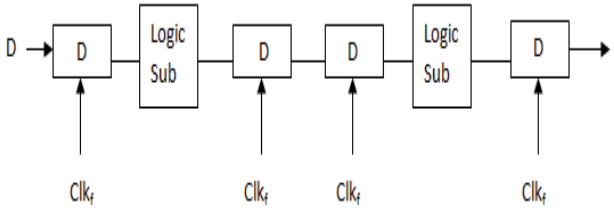

Figure 3. Implementation of Pipelining Technique

V.Prasanth, et al. [22] presented a 28nm, five-stage pipelined MIPS 32-bit CPU. Here, stage registers that toggle flip-flops in the design reduce switching activity between distinct stages. The Harvard architecture processor's speed and performance are improved in this research, which reduces the device's power consumption. In this paper, an innovative RTL clock gating mechanism is used to minimize dynamic power.

G. Jhansi [23] proposed that the power dissipation be taken as a major parameter to consider. Here, a 64-bit RISC CPU is used, and efficiency with great performance is prioritized as a key job. A Latch free based clock gating low power technology [24] is employed to reduce power dissipation.

Clock gating without a latch is depicted in figure 2.2. Basic gates like AND and OR gates can be used to implement this strategy. As long as the clock enable is turned on, the clock will here be triggered to the flip-flop. Clocks are turned off when the clock enable signal stops working [25].

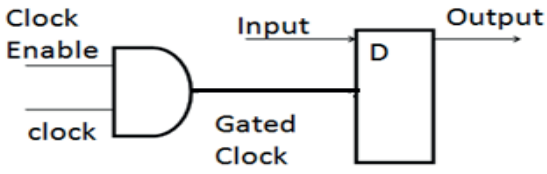

Figure 4. AND gate based Latch free clock gating.

Omkar, et al. [26] proposed the usage of a single precision floating point multiplier at the ALU which is in the execution block. A 32-bit RISC processor is composed of blocks like the instruction fetch, instruction decode, execute block, and write back unit. In this research, a specific power management strategy is applied to reduce static power. For low power applications, it's critical to reduce switching activity because CMOS devices only lose power when switching. One of the best methods for reducing switching activity is power management technique. This power-down method places the circuits in a sleep mode while not in use. It may be utilized at a number of hierarchical levels, including the level of a module, a chip, and even the printed circuit board.

Harpreet Kaur, et al. [27] proposed a MIPS processor with pipelining of five stage architecture that lowers the dynamic power consumption and raises the number of instructions per second for execution. By including NOP instruction, the risks that are introduced by pipelining are also removed. Given that this NOP instruction produces nothing beneficial, all of the power is wasted. As a result, this processor uses its dual write port register file to provide two right-back operations, which lessens the need for NOP in pipelining and results in further power savings. By utilizing a hazard detecting unit in the pipeline to eliminate unnecessary transitions, stalls are decreased.

P. Indira, et al. [28] proposed a MIPS 6 stage pipelined 64-bit RISC processor [29] for hazard free structure by employing a joint effort from the prefetch unit, forward unit, branch and jump prediction unit, and hazard unit. In this study, clock power is reduced using a Dual Edge Triggering Flip-Flop (DETFF) [30]. The Dual Edge Triggered Flip-flop is depicted in Figure 5.

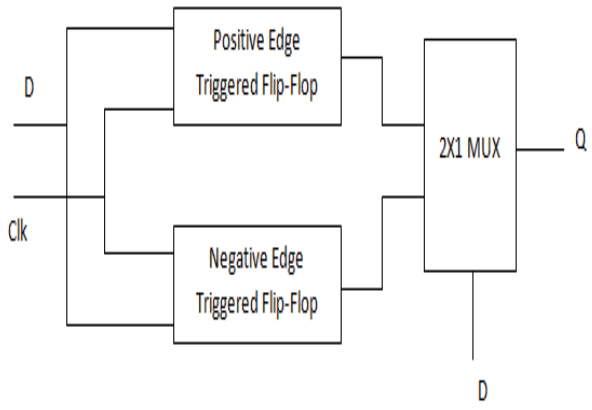

Figure 5: Dual Edge Triggered Flip-flop (DETFF)

Sneha Mangalwedhe, et al. [31] proposed the 5-stage pipelined 32 bit RISC processor [32] has as its primary goals to boost efficiency and decrease power dissipation. The multiplexer-based clock gating approach is used to reduce power dissipation. To improve the efficiency of pipelining a Hazard Detection unit is also included.

Hasan ErdemYantır et al. put [33] a hybrid approximation computing technique for association in memory processors. In order to optimize energy savings within certain rough bounds, this study focused on numerous distributed domains including image processing, machine learning, machine vision, and digital signal processing.

In addition, Duseok Kang et al. presented in [34] A novel method for scheduling deep learning applications on heterogeneous processors in an embedded device. This paper offered a scheduling method based on evolutionary algorithms for deploying deep learning applications on heterogeneous CPUs.

After that Ferran Reverter added [35] a three wire connected resistive sensor interface circuit based on a microcontroller. This article describes a prototype that was created using a commercial microcontroller to measure the resistances of a thermal sensor at various resistance values.

Additionally Cheng-Yao Hong et al. [36] proposed a variation resilient microprocessor with a two level timing error detection and correction system, in which the system was implemented on an ARM cortex- M10 microprocessor with a primary focus on energy savings through operation at lower supply voltages.

For embedded systems, Hyeonguk Jang et al. proposed [37] Integrating Memory Management units (MMU) inside networks on chips. A network on chip that supports multiprocessing and dual RISC-V processors is offered. It provides MMU capabilities without altering the processor design.

A concept for an 8 bit parallel RSFQ microprocessor was provided [38] in a further contribution from Pei- Yao Qu et al. This concept uses fast single flux quantum (RSFQ) circuit technology and a computer to process 8 bits every clock cycle. I also read a work by Swapnil Sayan Saha et al. [39] titled "Machine learning (ML) for microcontroller-class hardware." This emphasizes the prerequisites for enabling on-board machine learning for devices of the microcontroller class.

In addition, Vikkitharan Gnanasambandapillai et al. proposed [40] finding effective parallel instructions for ASIPs, In order to enhance the performance of complex applications. This fully automated approach created to locate parallel instructions for ASIPs also creates FINDER (Flexible Instructions Extensions Instructions), which enhances the performance of huge applications.

Mohammad Attari et al. contributed the work entitled an Application Specific Vector for Efficient Massive Multiple Input and Multiple Output (MIMO) processing [41]. This article introduces an application-specific instruction set processor (ASIP) with multiple inputs and multiple outputs (MIMO). In which the ASIP chip incorporates a parallel memory subsystem.

Further, Marco Crepaldi et al. contributed [42] an innovative multi one instruction set computer for microcontroller applications. a computer with a single instruction set and multiple execution modes that can only execute simple integer instructions are used. Along with RAM, it also has 8 bit I/O. Not all of the aspects of commercial ISA were targeted. On an FPGA, it has been synthesized.

Atef Ibrahim et al. presented [43] a work entitled Systolic processor core for finite field multiplication and squaring. In which the primary emphasis is on a single processor core that executes multiplication and square root operations simultaneously to conserve hardware resources.

In addition, a work challenging Single Instruction Multiple Data (SIMDS) and Very Long Instruction Word (VLIWS) with a reconfigurable architecture proposed by M. Wijtvliet et al. [44], In these reconfigurable architectures, this enables energy-efficient application-specific VLIW- SIMD processors by separating the control and data paths into separate blocks. It has been likened to CGRAC Coarse Grain Reconfigurable Architectures, VLIW, SIMD, low power microprocessors, and SIMD.

IV. Results

Numerous articles have been studied up to this point, and it is clear from them that a number of the strategies that have been described are being employed on MIPS RISC processors, which may be 32- or 64-bit machines with various pipeline topologies. These concepts use various modeling and synthesis techniques along with different processing technologies, such as 28nm, 40nm, 45nm, 60nm, and 90nm.

Let's compare all the parameter findings from the various ideas as indicated in the table to understand what these various strategies lead to in terms of MIPS development. 1.

CVR Journal of Science and Technology, Volume 25, December 2023
DOI: 10.32377/cvrjst2506

TABLE I.
POWER, DELAY AND FREQUENCY COMPARISON OF A PROCESSOR WITH DIFFERENT TECHNIQUES

S.No	Reference/Author Name	Total Power (W)	Delay (ns)	Frequency (MHz)
1	Ref [22] Dr. Dilip Kumar (Apr 2012)	0.031	6.57	178
2	Ref [28] HarpreetKaur (Mar 2013)	0.34	-	193.8
3	Ref [15] (Feb 2013)	0.829	14.348	179.092
4	Ref [27]Omkar (Jul2016)	0.21	0.562	-
5	Ref [24] G. Jhansi (Oct 2017)	0.177	-	-
6	Ref [32]Sneha Mangalwedha (Nov 2017)	0.363	-	401.881
7	Ref [31]P. Razak Hossai (Feb 2019)	0.023	1.143	420.028
8	Ref [29]P. Indira (Oct 2019)	3.60µ	1	255.88
9	Ref [23] Prasanth, V (Mar 2020)	0.129	11.18	285.583

Power, Delay and frequency comparison of processor with different techniques shown in table I. which compares the parameters of the many MIPS designs that have been suggested. Columns 2, 3, and 4 respectively display power usage, delay, and frequency. Table I shows a power reduction from 0.829W to 0.031W.Maximum dynamic power reduction of 90% was obtained for the most recent MIPS CPU.

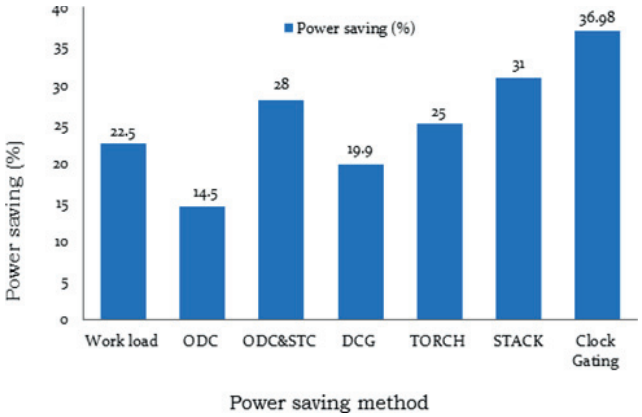

Figure 6. Percentage of Power saving of different MIPS processors using Low Power VLSI Techniques.

The figure 6 shows the percentage of power saving of different MIPS processors using Low power VLSI Techniques. Table II represents a comparison of power consumption with and without clock gating techniques. There is clear evidence from the table that using clock gating technique, there is a greatt possible reduction in the power consumption.

TABLE II.
COMPARISION OF POWER VALUES WITH AND WITHOUT CLOCK GATING TECHNIQUE

References	Clock Gating Technique	Power(W)	
		Without Clock Gating	With Clock Gating
Ref [32]	Multiplexer based Clock gating	0.463	0.363
Ref [30]	Circuit Partitioning	0.94	0.829
Ref [27]	Power Management unit	0.22	0.21
Ref [29]	Flip Flop based clock gating	0.577	0.34
Ref [31]	Dual Edge Triggered flipflop+Multi Vt	4.611 µ	3.60µ

V. CONCLUSIONS

In conclusion, low power RISC processors with low power techniques have become increasingly important in many applications that require energy-efficient computing, such as mobile devices, Internet of Things (IoT) devices, and wearable devices.

Low power RISC processors use reduced instruction set computing (RISC) architectures that have fewer and simpler instructions, which reduces the number of transistors needed and enables higher clock speeds. Low power techniques, such as Dynamic Voltage and Frequency Scaling (DVFS), clock Gating, and Power Gating, can further reduce power consumption by dynamically adjusting the voltage and frequency of the processor and turning off unused circuit blocks.

These techniques have been successful in reducing the power consumption of processors while maintaining acceptable levels of performance, making them well-suited for energy-constrained applications. Additionally, the development of advanced manufacturing processes, such as FinFET and FDSOI, has enabled the creation of low-power RISC processors with even better performance and power efficiency.

Overall, low power RISC processors with low power techniques are a promising area of research and development for energy-efficient computing and are likely to continue to be important for many years to come.

REFERENCES

1. Srinivas.D, and Malik.S, “A Survey of Optimization Techniques Targeting Low Power VLSI Circuits”, Proc. of 32nd ACM/IEEE Design Automation Conf., 1995, pp. 1-6.
2. Li-Chuan.W, Xiao Jun.W, and Bin.L, “A Survey of Dynamic Power Optimization Techniques”, Proc. of the 3rd IEEE Int’l workshop on System-on-Chip for Real-Time Applications (IWSOC) IEEE, 2003, pp. 48-52.
3. Rajesh.K.G, Irani.S and Sandee.K.S, “Formal Methods for Dynamic Power Management ", Proc. of int’l conf. on Computer Aided Design (ICCAD-2003), 2003, pp. 874 – 881
4. Hans Jacobson, Pradip Bose, Zhigang Hu, Rick Eickemeyer, Lee Eisen and John Griswel, “Stretching the Limits of Clock-Gating Efficiency in Server-Class Processors”, Proc. of the

11th Int'l Symposium on High-Performance Computer Architecture (HPCA- 2005) IEEE, 2005, pp. 238-242.
5. Aaron.P.H., "Automatic Synthesis of Clock Gating Logic with Controlled Netlist Perturbation", Proc. of 45th ACM/IEEE Design Automation conf. 2008 (DAC 2008), 2008, pp. 654 – 657.
6. Ranan.F, Gila.K, and Muhammad.K.M., " A New Paradigm for Synthesis and Propagation of Clock Gating Conditions", Proc. of Design Automation Conference 2008 (DAC2008) IEEE, 2008, pp. 658 – 663.
7. Hamid.M, Vishy.T, Matthew.C, and Kaushik.R, "Ultra Low-Power Clocking Scheme Using Energy Recovery and Clock Gating", IEEE Trans. on Very Large Scale Integration (VLSI) Systems, Vol 17, No. 1, 2009, pp. 33 - 44.
8. Aaron.P.H., "Automatic Synthesis of Clock Gating Logic with Controlled Netlist Perturbation", Proc. of 45th ACM/IEEE Design Automation conf. 2008 (DAC 2008), 2008,pp. 654 – 657.
9. Ranan.F, Gila.K, and Muhammad.K.M., " A New Paradigm for Synthesis and Propagation of Clock Gating Conditions", Proc. of Design Automation Conference 2008(DAC2008) IEEE, 2008, pp. 658 – 663
10. . Hamid.M, Vishy.T, Matthew.C, and Kaushik.R, "Ultra Low-Power Clocking Scheme Using Energy Recovery and Clock Gating", IEEE Trans. on Very Large Scale Integration (VLSI) Systems, Vol 17, No. 1, 2009, pp. 33 - 44.
11. Macii.E, Bolzani.L, Calimera.A, Macii.A and Poncino.M, "Integrating Clock Gating and Power Gating for Combined Dynamic and Leakage Power Optimization in Digital CMOS Circuits", Proc. of 11th Euro micro-Conference on Digital System Design Architectures,Methods and Tools, IEEE, 2008, pp. 298 – 303.
12. Rani Bhutada, and YiannosManoli, "Complex Clock Gating with Integrated Clock Gating Logic Cell", Proc. of Int'l conf. on Design and Technology of Integrated Systems in Nanoscale ERA2007, 2007, pp. 164-169.
13. Hai Li etc., "DCG: Deterministic clock-gating for low-power microprocessor design", IEEE Transactions on Very Large Scale Integration (VLSI) Systems 12(3), April 2004, pp: 245-254.
14. Xiaotao Chang , Mingming Zhang, Ge Zhang1, Zhimin Zhang and Jun Wang, "Adaptive Clock Gating Technique for Low Power IP Core in SoC Design", Proc. of IEEE Int'l symp. on Circuits and Systems (ISCAS 2007), 2007, pp. 2120 – 2123.
15. Hans.M.Jacobson, "Improved Clock-Gating through Transparent Pipelining", Proc. of the 2004 Int'l Symp. on Low Power Electronics and Design (ISLPED 04) ACM, 2004, pp. 26-31.
16. Yan Zhang, Jussi Toivanen, and Aarne.M, "Clock Gating in FPGAs: A Novel and Comparative Evaluation", Proc. of 9th EUROMICRO conf. on Digital System Design: Architecture, methods and Tools (DSD06) IEEE, 2006, pp.584-590.
17. Pizhou Ye and Chaodong Ling, "A RISC CPU IP Core", Proc. of 2nd Int'l Conf. on Anti-counterfeiting, Security and Identification(ASID 2008), 2008, pp. 356 – 359.
18. Piguet.C. "Low power design of 8-b embedded cool-RISC microcontroller cores", IEEE Journal of Solid-State Circuits, Vo.32, No.7, 1997, pp. 1067~1077.
19. Nalan.E., and Mustafa.G.C, "Design of an 8 Bit General Purpose Microcontroller with Sea-of-Gates Design Style ", Proc. Of eleventh Int'l conf. on Microelectronics (ICM1999) IEEE, 2002, pp. 177-180.
20. Júlio.C.B, Mattos, MárcioKreutz, and Luigi Carro, "Low-Power Control Architecture for Embedded Processors", Proc. of the 15th Symp. on Integrated Circuits and Systems Design (SBCCI'02) IEEE, 2002, pp. 221-226.
21. Dr.Dilip Kumar and Kiratpal , "Design of High performance MIPS-32 Pipeline Processor",Conference Paper • April 2012 DOI: 10.13140/RG.2.1.4883.6567.
22. V.Prasanth, V.Sailaja, P.Sunitha, B.Vasantha Lakshmi, "Design and implementation of low power 5 stage Pipelined 32 bits MIPS Processor using 28nm Technology", International Journal of Innovative Technology and Exploring Engineering (IJITEE) March, 20, Volume-8, Issue-4S2,ISSN: 2278-3075, pp.502-507.
23. G.Jhansi, " Design of MIPS based 64-bit RISC Processor", International Journal of Engineering and Advanced Technology (IJEAT), October 2017,Volume-7 ,Issue-1, ISSN: 2249 – 8958,pp.48-51.
24. Agineti. Ashok, and V. Ravi, "ASIC design of MIPSbased RISC processor for high performance"Proc.ofInternational Conference on Nextgen ElectronicTechnologies: Silicon to Software (ICNETS2), March2017, IEEE Proceedings, pp. 263-269.
25. Husainali S. Bhimani,. Hitesh N Patel and AbhishekA. Davda, "Design of 32-bit 3-Stage Pipelined Processorbased on MIPS in Verilog HDL and Implementation onFPGA Virtex7," International Journal of AppliedInformation Systems (IJAIS), May 2016.
26. Omkar A. Shastri, "Floating Point Parallel Processing Multiplier Based RISC (MIPS) Processor", International Journal of Advanced Research in Computer and Communication Engineering, July 2016, Vol. 5, Issue 7,ISO 3297:2007 Certified, ISSN: 2278 – 1021,pp.477-481.
27. Harpreet Kaur, Jaspal Singh, "MIPS Processor With Reduced Dynamic Power", IJCST, Jan - March 2013, Vol. 4, Issue 1, ISSN: 0976-8491 (Online) | ISSN: 2229-4333,pp.559-562.
28. P. Indira, M. Kamaraju, "Design and Implementation of 6-Stage 64-bit MIPS Pipelined Architecture", International Journal of Engineering and Advanced Technology (IJEAT), August 2019,ISSN: 2249 – 8958, Volume-8, Issue-6S2,pp.790-796.
29. Liang Geng, Ji-zhong Shen, Cong-yuan Xu "Power-efficient dual-edge implicit pulse-triggered flip-flop with an embedded clock-gating scheme", Frontiers of InformationTechnology and Electrical Engineering,Vol. 17,Issue 9.ISSN 2095-9184 (print); ISSN 2095-9230 (online) pp .962-972.
30. Razak Hossain, Leszek D. Wronski, and Alexander Albicki, "Low Power Design Using Double Edge Triggered Flip-Flops",Ieee Transactions On Very Large Scale Integration (VlSI) Systems, June 1994,Volume. 2, Issue No. 2, 1063-8210/94,pp-261-265.
31. Sneha Mangalwedha, RoopaKulkarni, S.Y.Kulkarni, "Low Power implementation of 32-bit RISC Processor with pipelining", Proc. of Second International Conference on Microelectronics, Computing & Communication Systems (MCCS),November 2017, springer, pp 307-320.
32. Nishant Kumar & Ekta Aggrawal, "General Purpose Six-Stage Pipelined Processor",International Journal of Scientific & Engineering Research, 2013, Vol. 4, Issue 9, pp.294-297.
33. Hasan Erdem Yantır, Ahmed M. Eltawil , and Fadi J. Kurdahi , "A Hybrid Approximate Computing Approach for Associative In-Memory Processors", IEEE Journal on Emerging and Selected Topics in Circuits and Systems, Vol. 8, No. 4, December 2018, PP- 758- 769.
34. Duseok Kang, Jinwoo Oh, Jongwoo Choi, Youngmin Y and Soonho Ha, "Scheduling of Deep Learning Applications onto Heterogeneous Processors in an Embedded Device",Volume 8, 2020 IEEE Access, PP- 43980- 43991.
35. Ferran Reverter, "A Microcontroller-Based Interface Circuit for Three-Wire Connected Resistive Sensors", IEEE

Transactions on Instrumentation and Measurement, Vol. 71, 2022,PP- 2006704.

36. Cheng-Yao Hong and Tsung-Te Liu, "A Variation-Resilient Microprocessor with a Two-Level Timing Error Detection and Correction System in 28-nm CMOS", IEEE JOURNAL of Solid-State Circuits, Vol. 55, No. 8, August 2020, PP- 2285-2294.
37. Hyeonguk Jang, Kyu Seung Han, Sukho Lee, Jae-Jin Lee and Woojoo Lee, "MMNoC: Embedding Memory Management Units into Network-on-Chip for Lightweight Embedded Systems", VOLUME 7, 2019 IEEE Access, PP- 80011- 80019.
38. Pei-Yao Qu, Guang-Ming Tang, Jia-Hong Yang, Xiao-Chun Ye, Dong-Rui Fan, Zhi-Min Zhang and Ning-Hui Sun, "Design of an 8-bit Bit-Parallel RSFQ Microprocessor", IEEE Transactions on Applied Superconductivity, Vol. 30, No. 7, October 2020, PP- 1302706.
39. S. S. Saha, S. S. Sandha and M. Srivastava, "Machine Learning for Microcontroller-Class Hardware: A Review," in IEEE Sensors Journal, vol. 22, no. 22, pp. 21362-21390, 15 Nov.,2022.
40. Vikkitharan Gnanasambandapillai, Jorgen Peddersen, Roshan Ragel, and Sri Parameswaran, "FINDER: Find Efficient Parallel Instructions for ASIPs to Improve Performance of Large Applications", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 39, No. 11, November 2020, PP- 3577- 3588.
41. Mohammad Attari, Lucas Ferreira, Liang Liu, and Steffen Malkowsky, "An Application Specific Vector Processor for Efficient Massive MIMO Processing", IEEE Transactions on Circuits and Systems—I: Regular Papers, Vol. 69, No. 9, September 2022, PP- 3804- 3815
42. Marco Crepaldi, Andrea Merello and Mirco Di Salvo, "A Multi-One Instruction Set Computer for Microcontroller Applications", Volume 9, 2021 IEEE Access, PP- 113454-113474.
43. Atef Ibrahim, "Systolic Processor Core for Finite-Field Multiplication and Squaring in Cryptographic Processors of IoT Edge Devices", IEEE Internet of Things Journal, Vol. 9,No. 2, January 15, 2022, PP- 1354- 1360.
44. M. Wijtvliet, A. Kumar, and H. Corporaal, "Blocks: Challenging SIMDs and VLIWs with a Reconfigurable Architecture", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 41, No. 9, September 2022, PP- 2915- 2928.