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Performance Analysis of Hybrid Comparator using 45nm Technology

Racha Ganesh[1], K. Lal Kishore[2] P. Srinivasa Rao[3]
[1]Ph. D Scholar, JNTUH University, CVR College of Engineering/ECE Department, Hyderabad, India.
Email: rachaganesh@gmail.com[1]
[2]Professor, CVR College of Engineering/ECE Department, Hyderabad, India.
Email: lalkishore@cvr.ac.in[2]
[3]Professor, CVR College of Engineering/ECE Department, Hyderabad, India.
Email: psrao.cvr@gmail.com[3]

Abstract: **In the present real-time world, due to the improvements and innovations of System on Chip (SoC) applications, there is a requirement to integrate multiple technology design topologies. The electronic system design is classified as analog, digital, and mixed-signal design. The comparator is the major building block used in the datapath of System on Chip (SoC) application device. The usage of these devices depends on not only functionality but also on the non-functionality parameters considering different performance estimation metrics. The nonfunctional performance metrics for a transistor level design depends on the number of transistors, switching activities of logic level voltages and delay between input and outputs. These performance metrics are improved by considering the multiple logic families for multiple output generations instead of using a single logic family topology.**

The comparator is the major component in the arithmetic circuits for SoC applications and can be realized by using various design topologies. The vividly used topologies are Conventional CMOS logic, Pass Transistor Logic (PTL), Gate Diffusion Input (GDI) Logic, Stacking technique, Quantum-dot cellular automata, etc. The selection of the design topology for the comparator is made based on the non-functional parameters. The performance of non-functional parameters is improved by combining the topology architectures of different design techniques. In this paper, the comparator is designed using conventional CMOS logic, PTL, GDI, and a hybridized topology for best performance and the same is implemented using 45nm technology. These circuits are designed by using Cadence Virtuoso Electronic Design Automation (EDA) design tools. Non-functional performance parameters are analyzed for different topologies.

Index Terms: **VLSI Design, Comparator, Datapath, EDA tools, CMOS Logic, GDI Logic, PTL Logic.**

I. Introduction

In the present System on Chip (SoC) applications era, there is a requirement to design any system using both datapath and control path. The selection of the electronic system and software elements for data and control paths will decide the improvement in the nonfunctional metrics along with the system design functionality. Hence, the electronic systems related to datapath elements are designed by using arithmetic elements, computational elements for Small Scale Integration (SSI), Large Scale Integration (LSI), Very Large Scale Integration (VLSI), Digital Signal Processing (DSP) AND Embedded Systems application areas.

The Very-Large-Scale Integration (VLSI) is the combination of thousands of transistors that are integrated into a single device called a VLSI chip. The introduction of VLSI technology made a great improvement in the design of electronic systems. This Electronics system VLSI chip consists of data and control path using arithmetic elements, computational elements, memory elements like RAM, ROM, and other logic.

The VLSI technology along with software design together with an integrated single chip device made the possibility of application domain area as System on Chip (SoC) devices. This System on Chip (SoC) application area made the electronic systems design a new development for different system design applications. The different applications for System on Chip applications include Embedded systems, Data Computation systems, Image enhancement and processing applications, communication devices with software applications etc. This cutting edge System on Chip (SoC) application era made the VLSI system design as more important and dominant design technology to meet the needs of present technology applications. Hence, the present VLSI system design based electronic system is an integration of analog, digital, and mixed-signal design components. All the above-mentioned components except ASIC come under digital design, whereas ASIC is the combination of Analog and mixed-signal designs. In ASIC, there are two types of designs semi-custom designs and full-custom designs. The semi-custom uses pre-designed logic cells and libraries known as standard cells. Full-custom design in VLSI is a method of creating integrated circuits that specifies the architecture of each transistor as well as their interconnections. To design a system, there is a requirement for inputs, outputs, datapath and a control unit. The datapath consists of computational elements like arithmetic and logical elements. The control unit consists of control logic using states or algorithms.

This paper implements the design of a basic data path element i.e., comparator using different logic family topologies. The different logic design family topologies used are Conventional CMOS, PTL, GDI and this designed system proposes a hybridized logic model which makes a better design methodology to meet the functionality and nonfunctional metrics. The selection of the logic family is done as per the comparison input output logic and performance metrics for best results.

An overview of the existing design topologies and different arithmetic applications is given in section II. Section III explores the design and modeling of the comparator. Section IV shows the design of a comparator using EDA tools. The simulation input, output relations and performance

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analysis of the comparator are discussed in section V. The conclusions are given in section VI followed by references.

II. Design Topologies and Arithmetic Applications

Overview of the comparator's properties, architecture, and different parameters that must be considered while designing a device, including delay, offset voltage, output impedance, and voltage gain [1]. However, the application and requirements of system design determine which topology to be chosen. The design presents an enhanced technique for designing CMOS comparator based on a preamplifier-latch circuit controlled by a clock [2]. The primary benefit of this design is its ability to boost an ADC's speed while consuming less power. The design is simulated using the Cadence environment in 0.18-micron CMOS technology. The suggested design has high accuracy and uses only roughly 102 W of power when operating at a 125 MHz sampling frequency and a 1.8 V supply. The construction of a 1-bit reverse comparator employing reversible L and M gates and simulation using the TANNER EDA tool is proposed in [3]. The Reverse logic gates are used in digital comparator circuits to cut down on the number of transistors, size, and power consumption. To develop the suggested 1-bit reverse comparator circuit utilizing 180nm technology, L and M reverse logic gates were downscaled using constant electrical field scaling. Power dissipation at 5V supply voltage was estimated to be 0.162mW, which is 10% better than the CMOS circuit design [3]. To provide low power in digital circuits, one of the unique designs (XOR circuit using only n-MOS) has been proposed in [4]. The GDI cell has been used to realize a variety of circuit combinations. Their waveforms have been examined, and numerous performance metrics have been determined based on the results of the simulation. Then, these parameters are contrasted with conventional CMOS logic. The layout and schematics are created using the Dsch tool and 120nm technology file. Microwind 3.1 and the BSIM simulator are used to analyze the results. Utilizing TANNER S-EDIT, the GDI approach has been applied to 250 nm manufacturing technology [5]. After studying several solutions, a multiplexer based magnitude comparator is eventually suggested with optimum VLSI design limitations. The optimal design that results in the lowest transistor count was provided after considering all the potential designs employing multiplexers with a wide range of main inputs as selection inputs. In comparison to current GDI comparators, the transistor count is reduced by 70%, 33%, and 9%, respectively. Two key design strategies are shown in [6]. The former compares CMOS and GDI logic in terms of nonfunctional metrics and provides the design solution using newly designed basic logic cells. The latter discusses the performance concerning the installation of five various modified GDI full adders. In contrast to the current GDI method, CMOS, and pass transistor logic at 250nm technology. The proposed system performance shows improvement in the power and delay parameters using GDI technology. The design summary of the MGDI technology, uses fewer transistors to make digital circuits that use less power and chip space [7]. The complete adder is introduced in this study utilizing the MGDI approach. Using GDI the approach, 2-bit comparator, and complete subtractor were introduced. Then, these digital circuits' power dissipation, transistor count, size, speed, and latency were contrasted with those of conventional CMOS transistors. The S-GDI approach, which is more power-efficient than DCMOS (Differential CMOS) and Energy Economized Pass Transistor Logic, is presented in the work [8]. (EEPL). In comparison to the GDI approach, S-GDI exhibits power efficiency of 96.20%, 93.65%, 97.88%, and 98.22% for XOR, 1-bit adder, 1-bit comparator, and 4-bit up-down counter, respectively. S-GDI exhibits area efficiency of 17.16% and 28.1% for XOR, 41.26% and 53.89% for 1-bit adder, 7.6% and 21.76% for 1-bit comparator, and 6.7% and 28% for up-down counter over EEPL and DCMOS techniques, respectively. S-GDI may be utilized effectively for low-power applications because of its efficiency in terms of the factors that are taken into consideration. The PTL technology reduces the number of transistors required for the design of logic gates. The performance analysis of PTL with CMOS is discussed in [9]. The 2-bit comparator layout is created using semi-automated and automatic methods. The result demonstrates that the semi-custom PTL logic layout uses 35% less space than the CMOS design to give an area-efficient solution [9]. In [10], the circuit methods for constructing a high-speed adder with PTL are discussed. The Double Pass-Transistor logic (DPL) improves the design performance even at a low power supply. The speed is improved because of its symmetrical design and double-transmission properties. This improvement in the gate speed is achieved without increasing input capacitance. The issue of series-connected pass transistors in the carry propagation channel is solved using a Conditional Carry Selection (CCS) carry propagation circuit approach. Combining these methods can decrease a 32-b ALU's addition time from a typical CMOS ALU by 30%. Using these circuit approaches, a 32-b ALU test chip is created in 0.25-um CMOS technology and has a 1.5 ns addition time at a 2.5 V supply. Additionally, it is discovered in [11] that when the threshold voltage is 0.4 V, the low-voltage performance of nMOS-based pass-transistor logic is superior to that of traditional CMOS circuits down to 1 V. [12] proposed a novel methodology for synthesizing large PTL circuits. This also pointed out the need for CAD algorithms for PTL circuit design. It outlined a comprehensive synthesis flow and proposed logic level optimization, that could directly provide efficient PPA.PTL is a natural partner for ambipolar field-effect transistors, and [13] suggests a circuit that uses compact PTL and ambipolar FETs for better energy delay performance compared to the traditional static CMOS logic structure. By combining PTL and GDI approaches, the paper provides a 17T 1-bit hybrid comparator design. Nine NMOS transistors and eight PMOS transistors make up the comparator architecture [14]. This space-efficient 9T full adder module serves as the foundation for the suggested hybrid architecture. DSCH 3.1 and Microwind 3.1 were used to develop and simulate the comparator on a 120nm chip. On the LEVEL-3 and BSIM-4 models, the simulation results are displayed. The suggested design in [14] has an area of 329.3 m2 and uses 120nm technology. The suggested 1-bit comparator circuit operates effectively over a broad frequency range of 2MHz to

400MHz and requires a minimum voltage supply of 0.4V. The 1-bit comparator simulation results demonstrate that the power consumption and current are lower.[15] presented the design of a 2-bit magnitude comparator using Conventional CMOS and PTL. The proposed design in [15] used a PTL-based circuit at input terminals & CCMOS-based circuit at output terminals. The results displayed satisfactory PPA and design efficiency for present microprocessor designs.

In [16], the design of the comparator is implemented by using conventional CMOS logic, GDI logic and PTL topologies. Four P-channel MOSFETs and four N-channel MOSFETs are used in the efficient design. DSCH-3.1 and Microwind-3.1 are the software programs that are being used. Using the 45 nm manufacturing technique, the circuit is developed using DSCH-3.1 and subsequently simulated using Microwind-3.1.

The non-functional parameters considered are power, the area covered, and transistor count. The GDI logic uses less power than the traditional MOS design by around 85.9% and has a smaller latency of roughly 42.1%. Compared to PTL, GDI-Logic uses less power (43.4%) and has an 89% shorter latency. [17] investigates the performance of the fundamental NAND gate utilizing several CMOS approaches. These approaches include Gate Diffusion Input (GDI), Transmission Gate, Domino Logic, and Pass Transistor Logic (PTL). [18] reviewed the performance & efficiency of various design implementation techniques like PTL, GDI, and conventional CMOS by designing a full adder. On comparison of their performance in terms of PPA, showed that an adder designed with PTL & GDI provides less delay & less power dissipation when operated at a higher speed. [19] presented the efficient design of a 2-bit hybrid magnitude comparator using various design topologies. It proved that PTL-GDI techniques provide efficient results in terms of PPA. The simulations are carried out using Tanner EDA tools. The hybrid PTL/CMOS Logic approach produces the best performance at the circuit level when compared to CMOS solo and PTL only. The proposed design in [20] has small power dissipation and low area over various supply voltages. Simulations are built on the BSIM 3V3 90nm CMOS platform. [21] suggests an effective approach for optimizing circuits with closely spaced sequential cycles that concurrently use Shannon decomposition and retiming. Even though the technique can only enhance a small percentage of the circuits (approximately half of the benchmarks are examined), the performance improvement can be significant (7%–61%) with just a little (1%–12%) increase in area.

The algorithm is a useful addition to a synthesis flow since it is also quick. Although retiming is a potent method for accelerating pipelines, it is hampered by close consecutive cycles. It is common practice for designers to manually combine Shannon decomposition and retiming to target such cycles; however, this manual decomposition is error prone. With these above findings in the background, the proposed comparator is designed by using Cadence EDA tools [21].

The design of comparators is used in the applications of image processing for skeletonization using different edge and corner detection algorithms. [22,23]

III. Design and Modeling of Comparator

The electronic system design consists of a data path and a control path. The data path is designed by using arithmetic and logical units in which the comparator is the major building block. The basic design diagram of the comparator is shown in Figure 1. This comparator design diagram consists of A and B as inputs and produces the outputs as A<B, A=B and A>B. This comparator is used mainly in all computational units to calculate the addresses, the table indices for encryption and security application areas.

Figure 1. Block diagram of the comparator

The design of comparators is done by using basic digital logic primitive gates to produce proper input and output relations. The basic input and output relations of a comparator of Figure 1 is shown in Table 1 with all test case possibilities.

TABLE I.
Truth Table of Comparator

INPUT		OUTPUT		
A	B	A=B	A>B	A<B
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

Logic Families

The Logic families used in the design of the comparator are classified into three topologies i.e., Conventional CMOS, GDI and PTL. Finally, the proposed system is designed using Hybrid Logic family to model comparator.

A. Conventional CMOS Logic Style

The conventional CMOS design technique makes use of many transistors. In this logic style three different transistor topologies are used to produce the outputs of comparator. The design of a basic conventional CMOS comparator is shown in Figure 2. This designed comparator consists of a greater number of transistors which results in an increased power analysis. As a result of increase in area and power the overall circuit speed is largely reduced. The main advantages are large fan-out capability (>50), very high noise margins and noise immunity.

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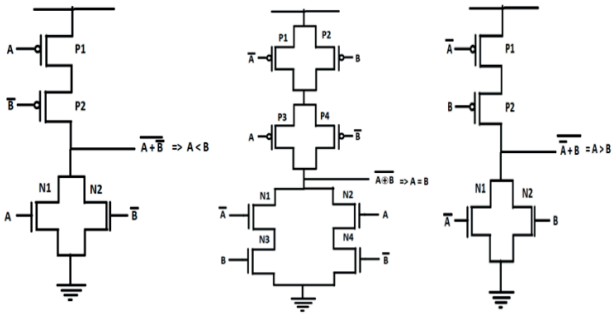

Figure 2. Conventional CMOS Comparator Design

The limitations of this topology are increased cost, less packing density due to a greater number of transistors and their interconnections, which also require the protection for avoiding short circuits among the interconnecting wires.

B. GDI Logic Style

The GDI logic style is used as a new method for digital circuits to achieve low power by considering less complexity in circuit topology. The basic GDI logic design technique makes use of a smaller number of transistors along with different transistor topologies to produce the outputs of comparator. The Figure 3 shows the GDI based comparator design for different output combinations.

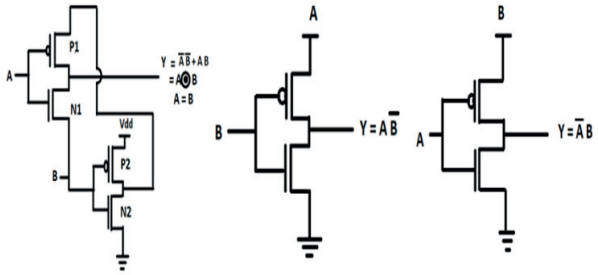

Figure 3. GDI based Comparator Design

The advantages are smaller transistor count, reduced supply voltage, area, power, and delay. This designed GDI logic consists of N, P, G terminals which are connected to VDD, Ground and input or outputs to produce the required logic cell functions. The basic GDI cell functions are listed in Table 2. The GDI logic based output boolean equations along with the logic functions are shown in Table 2.

This designed comparator using GDI has not fixed the problem of low voltage swing which is the major drawback in this topology.

TABLE II.
BASIC GDI CELL FUNCTIONS

N	P	G	OUT	Function
0	B	A	A'B	F1
B	1	A	A'+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT

C. PTL Logic Style

The Pass Transistor Logic (PTL) is used as an alternative logic family compared with Conventional CMOS and GDI logic family. This PTL logic family uses a reduced number of transistors to design the input and output logic function relation. The design of PTL based comparator is shown in Figure 4.

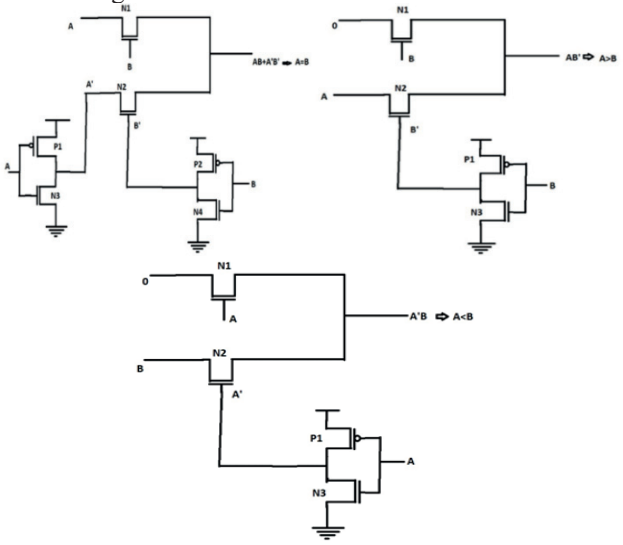

Figure 4. PTL based Comparator Design

The advantages of Pass Transistor Logic are small area and smaller power dissipation. Limitations is larger delay.

D. Proposed Hybrid Comparator

The hybrid model is an advanced technique of designing circuits using two or more design topologies for achieving efficient performance. PTL and GDI have some advantages over static CMOS, such that they can implement a logic function with a smaller number of transistors, smaller delay, and less power dissipation. For full-swing output, level-restoring logic may be required at the PTL and GDI output gates, and this level-restoring logic will slow down the PTL circuits and increase the power dissipation as well. Depending on the application and requirement, the topology for outputs is decided. The block diagram of Hybrid comparator is shown in Figure 5. This hybrid comparator consists of CMOS based design, PTL based design and GDI based designs for different output generations. The advantages of this topology are low-power, delay, power delay product.

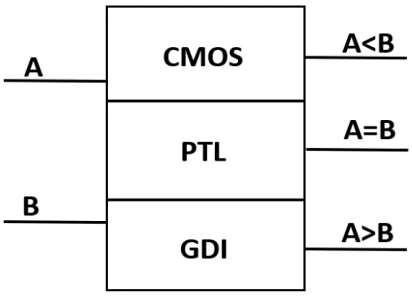

Figure 5. Block diagram of the Hybrid Comparator

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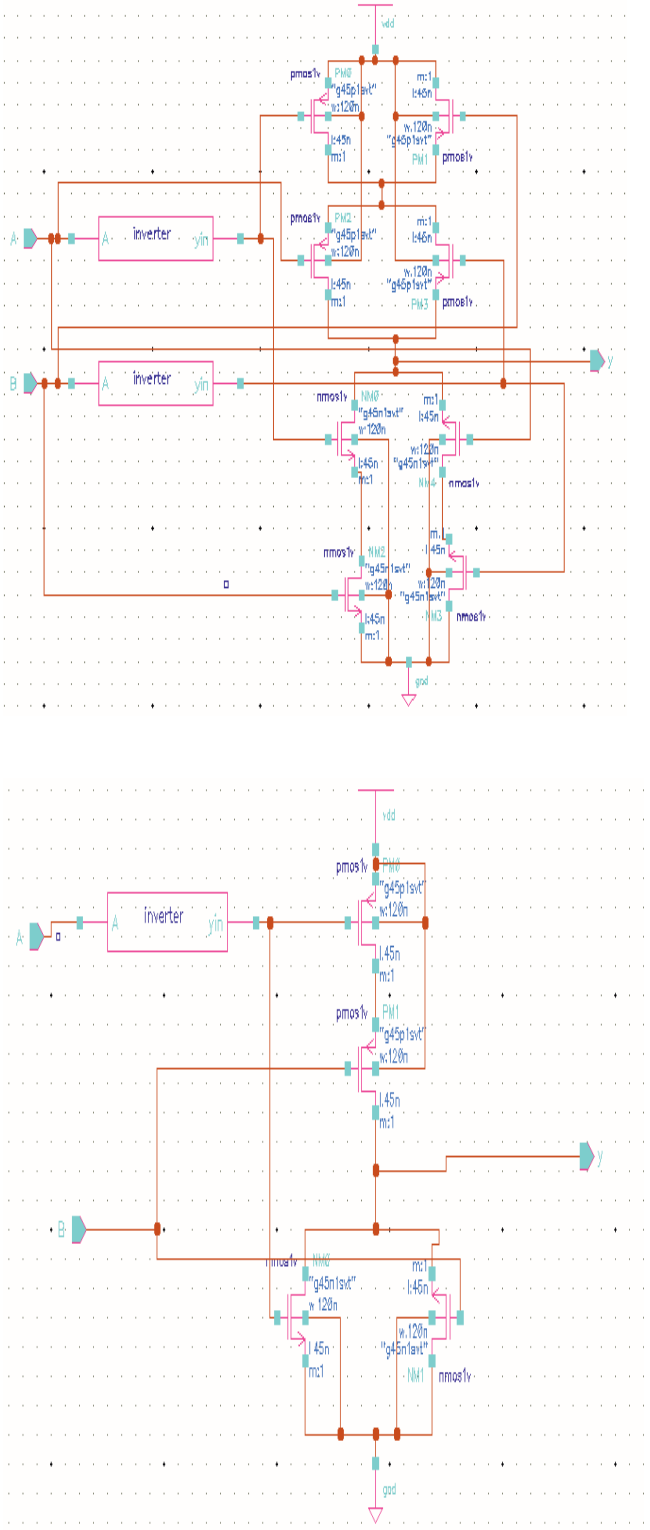
IV. Design of Comparator using EDA Tools

The comparators are designed by using Cadence Virtuoso Design suite EDA tools environment. These comparators are designed by using Conventional CMOS topology, GDI topology, PTL topology and proposed hybrid model.

The Conventional CMOS comparator schematic designs for different output conditions A<B, A=B and A>B are shown in Figure 6.



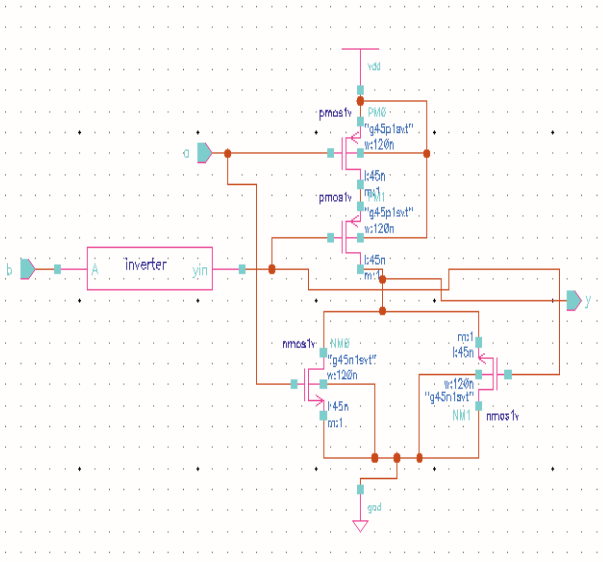
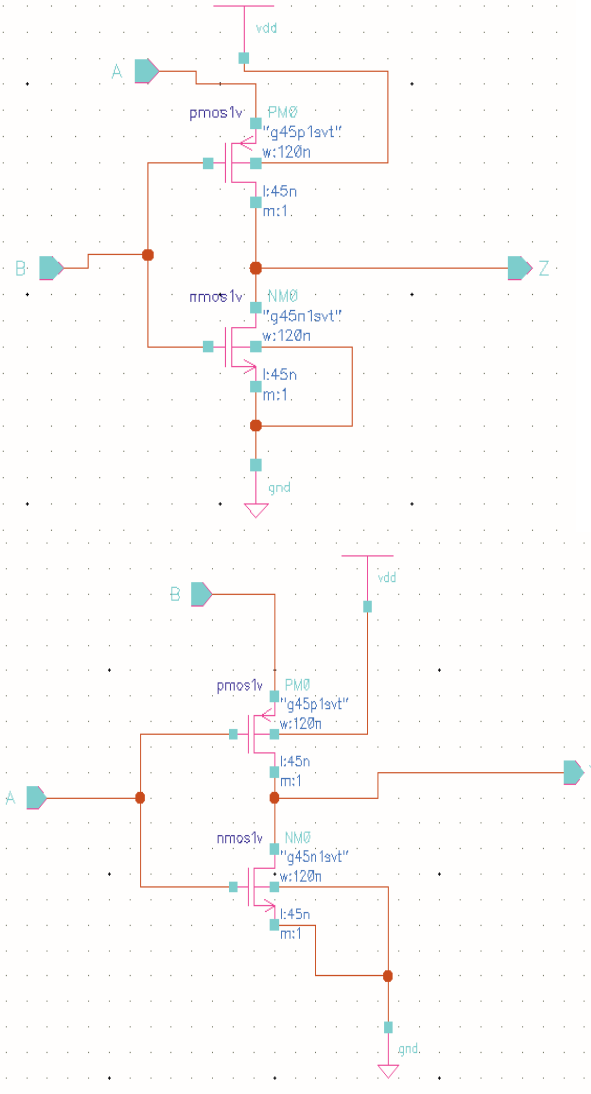


Figure 6. Schematic designs of Conventional CMOS Comparator

The GDI based comparator schematic designs for different output conditions A<B, A=B and A>B are shown in Figure 7.



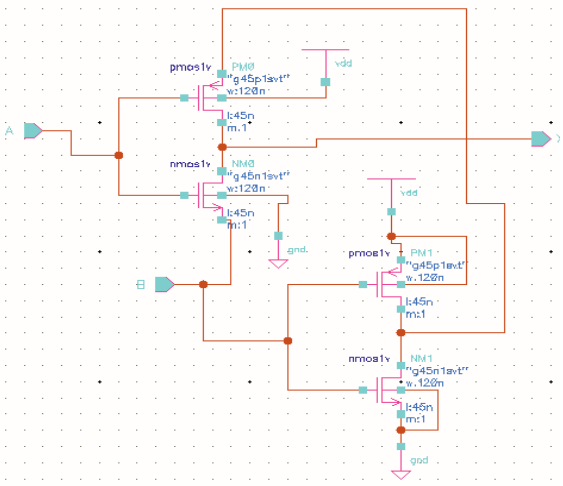


Figure 7. Schematic designs of GDI based Comparator

The PTL based comparator schematic designs for different output conditions A<B, A=B and A>B are shown in Figure 8.

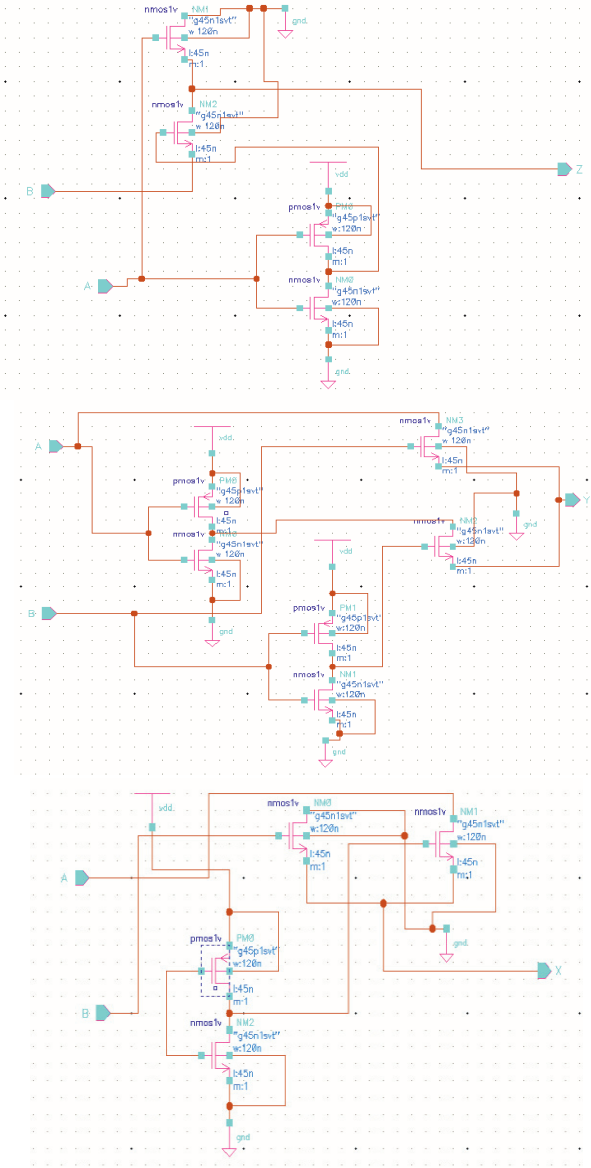


Figure 8. Schematic designs of PTL based Comparator.

The hybrid comparator schematic design using Conventional CMOS, GDI and PTL logic styles for different output conditions A<B, A=B and A>B is selected based on the nonfunctional performance metrics of IC design topologies is shown in Figure 9.

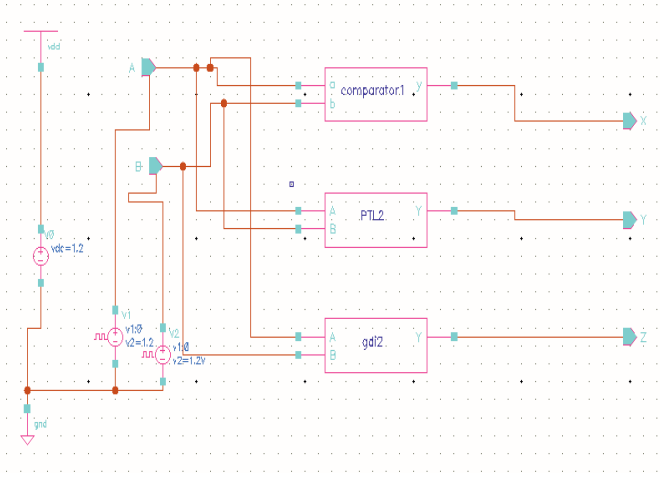


Figure 9. Schematic design of Hybrid Comparator

V. Simulation Results

The simulation results of Conventional CMOS based comparator design are shown in Figure 10.

Figure 10. Simulation of CMOS comparator for A<B, A=B and A>B

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The simulation results of GDI based comparator design are shown in Figure 11.

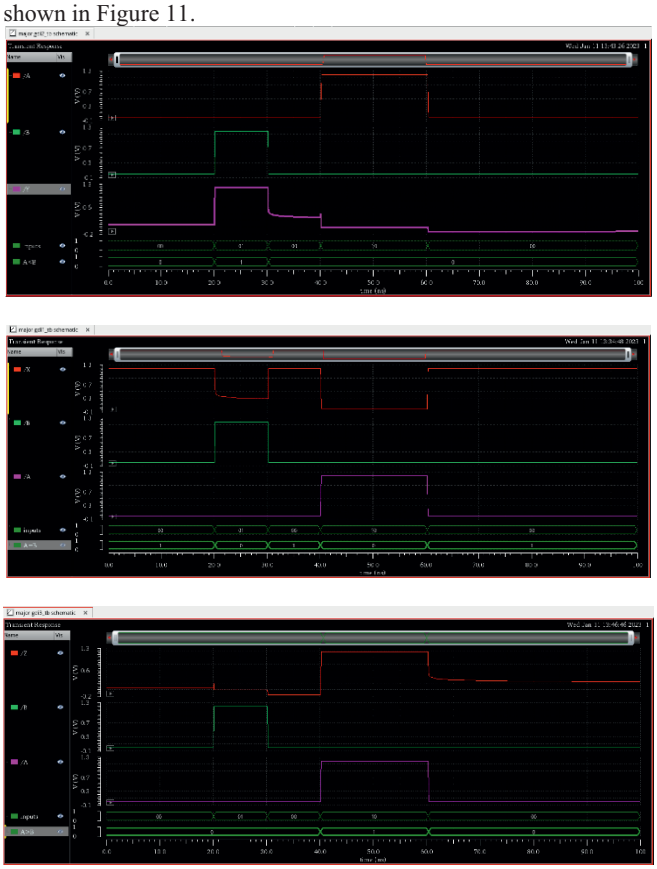


Figure 11. Simulation of GDI based comparator for A<B, A=B and A>B

The simulation results of PTL based comparator design are shown in Figure 12.

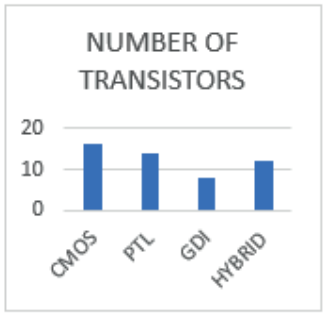
Figure 12. Simulation of PTL based comparator for A<B, A=B and A>B

Figure 13. Simulation of Hybrid comparator for A<B, A=B and A>B

Performance Analysis of Comparator

The Performance Analysis of comparator for area is shown in table III. The Performance Analysis of comparator for delay is shown in table IV and Figure 14. The Performance Analysis of comparator for power is shown in table V and Figure 15.

TABLE III.
AREA COMPARISON OF COMPARATOR



Design Style	Area (Number of Transistors)
MOS	16
PTL	14
GDI	8
HYBRID	12

Performance Analysis of Comparator in terms of Delay

TABLE IV.
DELAY COMPARISON OF COMPARATOR

Design Style	Delay for A<B (ns)	Delay for A>B (ns)	Delay for A=B (ns)
CMOS	9.9	0.056	20
PTL	20	0.351	0.017
GDI	0.02	0.042	19.94
HYBRID	20	20	0.0175

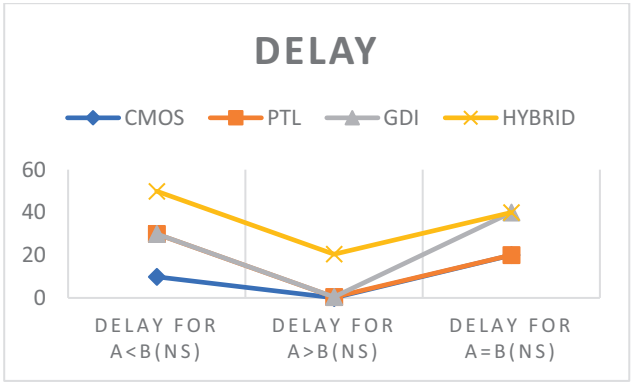


Figure 14. Delay Comparison of Comparator for MOS Logic families

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Performance Analysis of Comparator in terms of Power

TABLE V.
POWER COMPARISON OF COMPARATOR

TOPOLOGY	POWER FOR A<B (nW)	POWER FOR A>B (nW)	POWER FOR A=B (nW)
CMOS	1.62	2.32	36.5
PTL	4.25	30	10
GDI	4.21	7.56	2.1
HYBRID	1.048	0.004	1.04

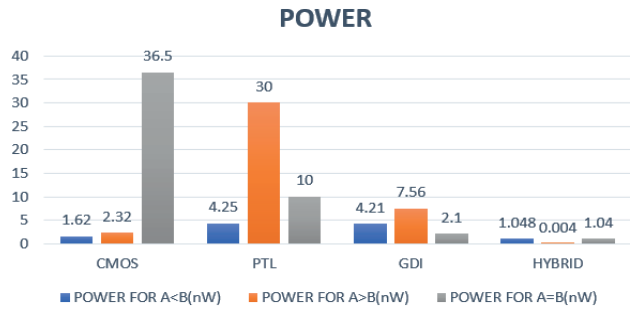

Figure 15. Power Comparison of Comparator for MOS Logic families

VI. CONCLUSIONS

The comparator for arithmetic applications is designed by using Conventional CMOS topology logic, Pass Transistor Logic (PTL), Gate Diffusion Input (GDI) Logic and Mixed hybrid topology logic. The comparators are designed by using Cadence Virtuoso EDA tools with 45nm technology. The nonfunctional area in terms of number of transistors for CMOS logic is 16, PTL is 14, GDI is 8 and Hybrid logic is 12 transistors. The delay and power parameters are also analyzed for the selection of hybrid logic topology. Hybrid logic is having best delay performance for equality comparison, and it also provides low power consumption for equality and inequality conditions compared to CMOS, PTL and GDI logic topologies.

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