E-ISSN 2581 – 7957
P-ISSN 2277 – 3916

CVR Journal of Science and Technology, Volume 24, June 2023
DOI: 10.32377/cvrjst2416

Design and Analysis of a Switched Capacitor Inverter for EV

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Abstract: **This paper focuses on the switched-capacitor converter configurations for a wide range of applications, which have numerous stages which are designed for different voltage levels. A single-phase switching capacitor multilevel boost inverter topology configuration with fifteen levels is discussed using fewer switches and a voltage boost gain. The main goal of this work is to develop a 15L multilevel inverter that can provide AC output voltage with minimal harmonic distortion. The output THD decreases to zero as even the level number approaches infinity.**

Index Terms: **Multilevel inverter (MLI), Cascaded H-bridge, 15 level inverter, reduced switches.**

I. Introduction

The desire for more powerful machinery, which can now produce megawatts of power, has just started to grow in the industry. The medium voltage is typically coupled to a megawatt-sized regulated AC drives network. Currently, it is not possible to link a medium voltage grid directly to a single semiconductor switch. A new family of multilevel inverters has been developed to function at greater voltage levels.

Multilevel inverters use power semiconductor and capacitor voltage sources to produce voltages with stepped waveform. Power semiconductors can only withstand lower voltages, but switch commutation enables capacitor voltage addition, producing a high output voltage. Due to their versatility and flexibility to work at many voltages, multilevel inverters are currently utilised extensively. Several dc voltage sources are used by the multilevel inverter to generate the required output. By using a switching frequency and more dc sources, an inverter's voltage output waveform gets closer to having a symmetrical Frequency [1]. Due to the numerous dc sources, it has little switching losses, low voltage stress, high efficiency, minimal output of Electro Magnetic Interference (EMI), and capacity to operate at high voltage. In addition, multilevel inverters would undergo more procedures. The multilevel approach is based on an inverter with three levels [2–5]. The use of multilevel inverters in power electronic applications is growing because they can satisfy the growing need for power rating and power quality, as well as a reduction in harmonic distortions and electromagnetic interference. Pulse width modulated (PWM) and switching frequency of Multilevel inverters are a variety of ways that make them preferable to two-level inverters [6]. The following are the advantages of a multilevel inverter that stand out the most: a) It is possible to generate reduced dv/dt stress and less distortion in the output voltage. b) There is negligible distortion in the current input drawn. c) There is an incredibly low common mode voltage. d) The switching frequency is incredibly low. The configuration of a multilevel inverter consists of capacitor voltage sources and devices for transmitting power. It is suitable for high voltage applications and voltage waveforms because it can measure the output voltage with greater harmonics to acquire high voltages with maximum device rating. Capacitor-clamped inverters, Diode-clamped inverters, and Cascaded H-bridge inverters are the three primary varieties of multilevel inverters. At each level, fewer cascaded H-bridge inverters, switches, and capacitors are needed.

A cascaded H-bridge with switches and capacitors creates a discrete input voltage in multilevel inverters [11]. One H-bridge cell may deliver voltages at zero, one, and two volts DC. This multilevel inverter's main advantage is that it has fewer parts than the other two types. Compared to the other two types, the inverter is less expensive and lighter. To develop original switching methods, soft switching might be used [7]. Multilevel cascade inverters are utilized to eliminate THD harmonics, the transformer required for standard multilevel inverters, the clamping diodes required for diode-clamped inverters, and the flying capacitors required for flying capacitor inverters all need to be considered. This is the situation if each cell needs a lot more isolated voltage than the other two types [8]. As switching device counts and Total Harmonic Distortion are reduced, the proposed Multilevel Inverter Topology provides greater advantages than current topologies [9] – [10], Switching losses are decreased as a result and improving output effectiveness. We are developing a multilevel inverter with fewer switches, more efficiency, and lower losses. The widespread use of pulse width modulation (PWM) techniques is due to their easy usage, long lifespan, and minimal computational needs [12].

II. Conventional Multilevel Inverter

A number of levels of dc voltages, which are frequently produced from capacitor voltage sources, are combined to create a minute sinusoidal voltage in the fundamental design of the converter with many levels. The synthesized output

Received on 11-03-2023, Revised on 13-04-2023, Accepted on 05-05-2023.

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waveform includes more steps as the level count rises, creating a staircase wave that resembles the desired waveform. The output wave's harmonic distortion lowers and approaches zero when more levels are added to the waveform. The quantity of levels rises, and so does the voltage that can be increased by introducing more levels of voltage. It is possible to determine the output voltage while operating in the positive half-cycle.

A. Cascaded multilevel inverter

An inverter with cascading multilevel is shown in Figure 1 below. A number of H-bridge inverter modules make up the device. This multilevel inverter's primary goal is to produce the required voltage from a number of dc sources, including batteries, fuel cells, and solar cells. It shows how a cascaded single-phase inverter with SDCSs is built from the ground up. Each SDCS is as seen in Figure 1 below, coupled to an H-bridge inverter. The ac terminal voltages of various level inverters are used to connect them in series. Contrary to the diode clamp or flying capacitor inverter, the cascaded inverter does not require any voltage-balancing capacitors or voltage-clamping diodes.

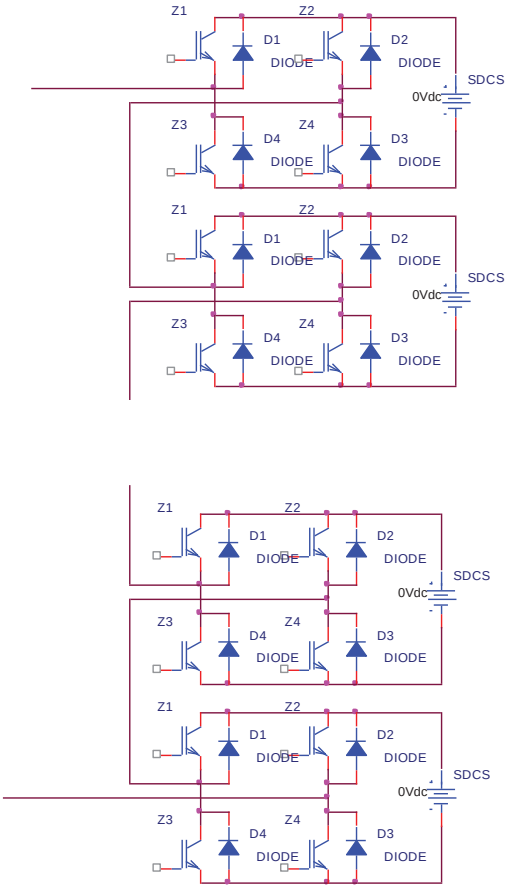

Figure 1. Cascaded Multilevel Inverter.

B. Proposed method

The various topologies of multilevel inverters as they are described in the literature have a lot in common. Their main disadvantage is the circuit complexity of multiple inverter setups, which calls for numerous power switches. Generators or series-connected coordinated power switches are not necessary for the multiple energy supply converters to reach high energies with low harmonics thanks to their distinctive structural design. A multilevel inverter's primary job is to combine various dc power values to create the intended voltage. The enormous power required by large electric drives can be conveniently provided by multilevel inverters. The intended waveform resembles a staircase waveform because as the number rises, the synchronized result pattern has more phases. Just as the level count increases as more levels are introduced to the waveform, the harmonic component of the output wave decreases to zero.

The voltage that can be covered by adding additional inverters rises with the number of levels, so the active devices never have voltage-sharing issues. Utility applications do not use electric motor drives, which employ several inverters. In static var correction, no active power is transferred between the converter and the system, but in motor drives, the converter must manage a bidirectional real power flow. Due to the switching between a number of smaller voltage levels, multilevel PWM drives have a lower dv/dt. Switching losses and the voltage's overall harmonic distortion is still significant. The converter that generates uniformly balanced voltages across the capacitors in the dc link has numerous levels of clamped diodes. As we move to the simpler H-Bridge multilevel inverter, both power devices and circuit complexity will reduce, leading to a reduction in circuit losses. If the trend of technology to make multilevel inverters more affordable is also considered, they can compete with the standard arrangement.

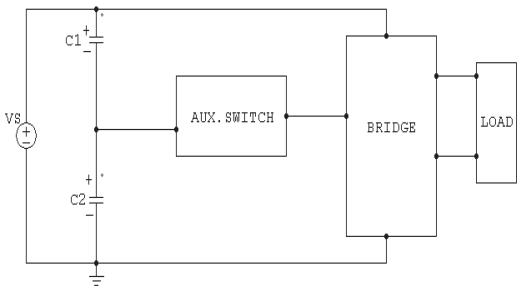

Figure 2. Block diagram of MLI.

A new converter topology is presented in this study which is depicted as a block diagram in Figure 2 (burdensome power stage and complex firing regulating circuit). Using a controller, the firing control circuit was created, and it was used in the design of the seven-level bridge converters shown below.

In this design, the inclusion of an H-Bridge stage and an auxiliary bidirectional switch significantly reduces the complexity of the power circuit.

Standard sinusoidal pulse width modulation is utilized to give switching pulses to the H Bridge circuit (for the generation of positive and negative cycles). The switching pulses for the frontend MOSFETs are produced using the binary priority encoder's logic, which was previously

explained. These pulses are generated when the reference signal crosses the carrier signals. Each switch receives a delay along with the generated pulses. The carrier waves roughly have a frequency of 5 KHz, whereas the Reference Sine waves have a frequency of 50 Hz. Regarding component count and layout complexity, the power stage's innovative converter architecture provides a major improvement. The second-best architecture, the asymmetric cascade arrangement, requires fewer diodes and capacitors and fewer primary switches than the simplified H-bridge multilevel inverter. The FPGA has the ability to conduct all required modulation in the modulator circuit functions, which are demonstrated in Figure 3 below, providing yet another substantial reduction in price and circuit complexity.

The circuit design of the 15-level multi-inverter shown the H-bridge in Figure 3. It is composed of Six auxiliary switches, and four main switches for 15-level output voltage capacitors which are needed.

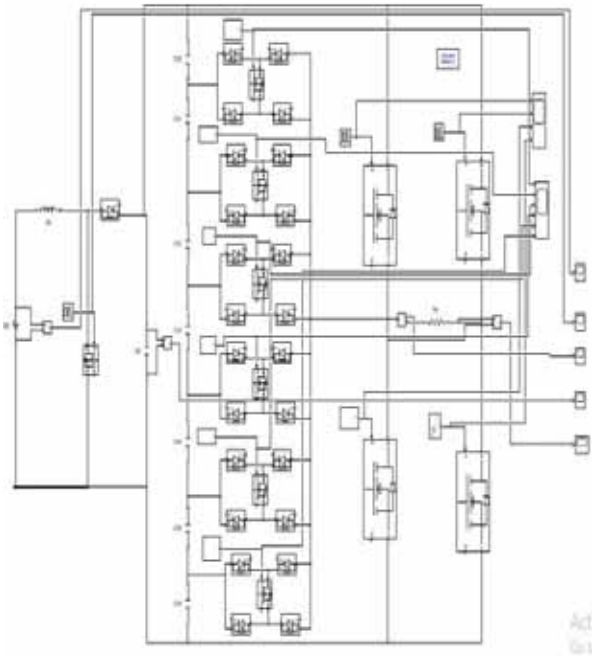

Figure 3. MATLAB Circuit Diagram.

To demonstrate how this streamlined H-bridge multilevel inverter architecture may reduce the number of components, the total number of components was calculated, reducing the number of controlled power switches from the required twelve to just seven, implementing a 13-level simplified H-bridge multilevel inverter and three previously established ones, the diode clamped and capacitor stages, which are considered to be the conventional multi-level stages. Clamped configuration and a new and highly improved multi-level stage with reduced switches achieve approximately requirements for primary switches that are reduced by 40%. The voltage and current ratings of the auxiliary switch are less than those of the regulated switches.

Auxiliary Devices (Capacitors & Diodes): Compared to the diode-restricted configuration, the new configuration needs fewer capacitors and diodes.

Furthermore, since the primary dc power supply is connected to three capacitors in parallel, there is no substantial, during normal operation, capacitor voltage swing range of the previous multilevel.

C. Simulation

In Figure 4 shows the firing pulses to the switches, Figure 5 shows the experimental setup, and Figure 6 shows the cascaded 15-level output waveform.

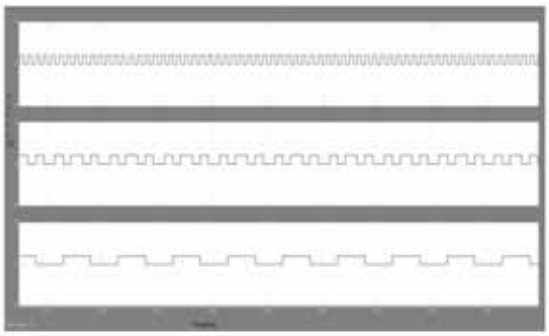

Figure 4. The Firing Pulses to the Switches.

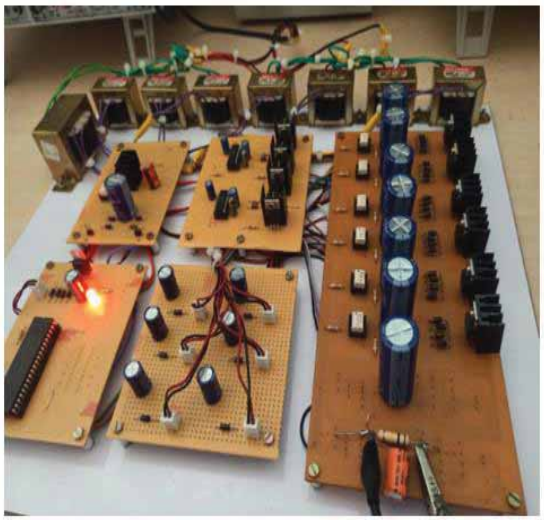

Figure 5. Experimental Setup of Cascaded 15-Level Inverter.

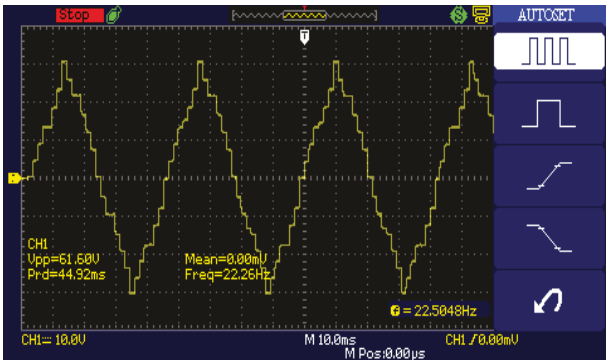

Figure 6. Output waveform

III. Conclusions

To investigate different operating models, an MLI topology with a single phase, and 15 Switches for level lowering are used. An FPGA IP Core Processor-based Hardware prototype is used to verify the simulation results. A cutting-edge SPWM modulation technique is suggested. The inverter can expand while still providing a high output voltage and lowering overall expenses by raising the level with the fewest switches possible. This research proposes an Asymmetric cascaded multilevel inverter with fifteen levels. It generates a high-frequency sinusoidal waveform. A cascaded multilevel inverter's efficiency can be increased by reducing switching losses, and overall harmonic distortion must be decreased.

References

[1] Nabae; I. Takahashi; H. Akagi. ―A new neutral point-clamped PWM inverter‖, IEEE Trans. on Industry Applications, vol. 17, no. 5,pp. 518- 523, 1981.

[2]] C.Bharatiraja, R.Latha, Dr.S.Jeevananthan,S.Raghu and Dr.S.S.Dash,"Design And Validation Of Simple Space Vector PWM Scheme For Three-Level NPC - MLI With Investigation Of Dc Link Imbalance Using FPGA IP Core‖, Journal of Electrical Engineering, vol. 13, edition 1, pp 54-63, 2013.

[3] Rodriguez, J.; Jih-Sheng Lai ; Fang ZhengPeng."Multilevel inverters: a survey of topologies, controls,and applications‖, IEEE Transactions on IndustrialElectronics, vol. 49, no. 4, pp 724-738.

[4] P.Jamuna; Dr.C.ChristoberAsirRajan "New Asymmetrical Multilevel Inverter Based Dynamic Voltage Restorer‖ Journal of Electrical Engineering, vol. 13, edition 1, pp 244-252, 2013.

[5] Nikhil; V.K.; Joseph, K.D. "A Reduced Switch Multilevel Inverter for Harmonic Reduction", Power and Energy Engineering Conference (APPEEC), Asia-Pacific, pp 1-4, 2012.

[6] Al-Judi; A.; Bierk, H.; Nowicki, E."A modified cascaded multilevel inverter with reduced switch count employing bypass diodes IEEE Conference on Vehicle Power and Propulsion, pp. 742-747, 2009

[7] Ebrahim B., Mohammad F., Farshid N."Symmetric and asymmetric multilevel inverter topologies with reduced switching devices, Elsevier Journal of Energy Conversion and Management, Electric Power Systems Research Vol. 86, pp.122-130,2012.

[8] E. Babaei,"A cascade multilevel inverter topology with reduced number of switches, IEEE Trans. Power Electron. Vol 23 no. 6, 2657– 2664, 2008.

[9] M. Calais, V. G. Agelidis, Multilevel converters for single-phase grid connected photovoltaic systems, an overview, in Proc. IEEE Int. Symp. Ind. Electron, vol. 1, pp. 224–229, 1998..

[10] S. B. Kjaer; J. K. Pedersen; F. Blaabjerg. ,"A review of single-phase grid connected inverters for photovoltaic modules, IEEE Trans. Ind. Appl., vol.41, no. 5, pp. 1292–1306, Sep./Oct. 2005.

[11] P. K. Hinga; T.; Ohnishi; T. Suzuki, "A new PWM inverter for photovoltaic Power generation system, Rec. IEEE Power Electron. Spec. Conf., pp.391–395, 1994

[12] Boost, M.A.; Ziogas, P.D.," State-of-the-art carrier PWM techniques: a critical evaluation ,IEEE Transactions on Industry Applications, vol. 24, no. 2,Mar 1998 pp 271-280