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Low Power RF Low Noise Amplifier Design for 5G Wi-Fi Receiver

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Abstract: **This paper presents the design of a differential Low Noise Amplifier (LNA) for a 5th generation Wi-Fi Receiver. The circuit is implemented with 90nm transistors using CMOS technology. The proposed differential LNA for 5G Wi-Fi (IEEE 802.11ac) is designed by combining two single-ended 5G Wi-Fi LNAs with optimized design values. The gate and source degenerated inductance values are optimized to achieve a 5GHz frequency of operation. Noise neutralization capacitors of 10pF are used to reduce the channel noise in the MOSFETs used in the circuit. The differential LNA achieves 93.6% input matching, an input impedance of 45.94Ω, a transducer gain of 25.76dB, a noise figure of 1.52dB, P_{1dB} of -11.7dBm and IIP3 of 3.17dBm.**

Index Terms: **CMOS, Noise Figure, 1dB compression point (P_{1dB}), Third Order Input Intercept Point (II3), harmonic signal, ISM Band**

I. Introduction

IEEE 802.11ac standard is known as 5G Wi-Fi. Modern Wi-Fi technology uses 2.4GHz and 5GHz frequencies. The design of LNA is mainly important in the performance of the overall receiver chain. The noise performance of the LNA should be critical because the same noise is amplified in the succeeding stages. To control the noise in the subsequent stages, LNA gain should be very high. The design of LNA should balance the Gain, Input impedance, Noise Figure and Power Consumption. To design LNA for a 5GHz Wi-Fi receiver, the design factors for LNA are shown in Table 1.

TABLE I.
RF LNA DESIGN FACTORS

Parameter	Value/Range
Input Resistance(R_{in})	=50Ω
Transducer Gain (G_T)	15dB-20dB
Noise Figure(NF)	<=3dB
1-dB compression point (P_{1dB})	>-30dBm
Third-order Intermodulation Intercept Point (IIP3)	>-20dBm
Power Consumption (P_{static})	<5mw
Frequency of operation (f_r)	5 GHz
Input Reflection Coefficient (S_{11})	<-15dB

The inductive degeneration technique is implemented in distributed amplifier design to reduce the noise figure under low power operation state. A common-source amplifier is cascaded to the distributed amplifier to progress the gain at high frequency and encompass the bandwidth [1]. A two-stage ultra-wide-band CMOS LNA is designed with the common-gate configuration as the input stage, the broad-band input matching is obtained, and the noise does not increase rapidly at higher frequencies. By merging the common-source (CS) and common-gate (CG) stages, the broad-band characteristic can be achieved by using two inductors [2]. A CG amplifier combined with a CS amplifier through a current mirror can achieve a high gain due to the additional current amplification. Low noise figure (NF) due to the thermal noise cancellation can be attained with low power consumption without degrading the input matching. The linearity can be improved with low power consumption, a multiple-gated transistor technique for cancelling the IM3 distortion [3]. The T-match technique is applied to achieve simultaneously wideband input and output impedance matching, wideband power gain and a wideband NF [4].

A concurrent dual-band LNA is designed to achieve concurrent gain and impedance matching at both bands. Input and output matching is realized using two-pole matching and LC resonant network [5]. Series inductive peaking in the feedback loop can be implemented to enhance the bandwidth and noise performance of the LNA [6]. The dual-loop feedback configuration can stabilize the LNA's input return loss (S11) at Very High-Frequency (VHF) with small dc blocking capacitors. The body bias control technique is helpful to reduce the power consumption in the inverter-based resistive feedback amplifier [7].

A couple of CS stages are stacked to share the current, and the double transformers are implemented as an RF signal path between the CS stages to improve the gain and stability [8]. Four common-source stages and three transformers are used to connect the drains of the former transistors and the sources of the following transistors to boost the transconductance of the transistors. Consequently, the gain of the circuit is effectively amplified. The NF can be reduced due to the noise contributions of the following stages being further suppressed by the application of the transformers [9].

This paper uses a Cascoded common source topology to avoid Miller's effect and improve the LNA's gain. The various existing impedance matching techniques, such as resistive matching, shunt feedback, common gate input matching and inductive source degeneration techniques, are reviewed [15]. The proposed differential LNA design uses the inductive source degeneration to transfer maximum power from the antenna to LNA. The gain improvement techniques are reviewed, such as Inter Stage Inductive Coupling, Transconductance (g_m) boosting, Partial Positive Feedback, and Cascoding strategies [13]. The cascoding technique is used to design the proposed LNA with optimized design values to achieve the desired gain and improved NF.

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The wireless receiver front end consists of a Low Noise Amplifier (LNA), Mixer and Voltage Controlled Oscillator (VCO). According to the National Frequency Allocation Plan (NFAP), it operates from several MHz to GHz frequencies. In NFAP, 2.4GHz-2.4835GHz frequency is the unlicensed band used for ISM (4G) applications such as Wi-Fi, Bluetooth, Zigbee etc. Similarly, the 5GHz-5.8GHz band is allocated for 5th generation (5G) Wi-Fi IEEE 802.11ac [10]. The present work generally relates to radio frequency (RF) frontend receiver circuit, and in specific relates to a low noise amplifier and mixer circuit design for use in radio frequency (RF) frontend receivers that reduce power consumption without affecting the overall gain of the circuit [16]. Single-ended and staggered-tuned four-stage LNA circuits can work at $f_{max}/2$ frequencies [18].

Wireless receives the signal and converts them into the necessary form with amplification. Typically, LNA is the first block of the receiver chain in a radio frequency system, the first block decides the performance of the remaining receiver chain, and hence LNA plays a crucial role in the receiver front-end design. The front-end block is formed by a Low Noise Amplifier (LNA) and a mixer block for mixing a signal amplified by the LNA with a local oscillator signal, to down-convert the amplified signal to an intermediate frequency. The thermal, flicker and gate-induced noise degrades the noise performance of the circuit [19].

II. Circuit Design

The main objective of this work is to provide a new and improved merged LNA-Mixer circuit with a low power consumption for a Wi-Fi/radio front-end receiver. Figure 1 (Ckt 1) is RF LNA for the 5G Wi-Fi receiver front end.

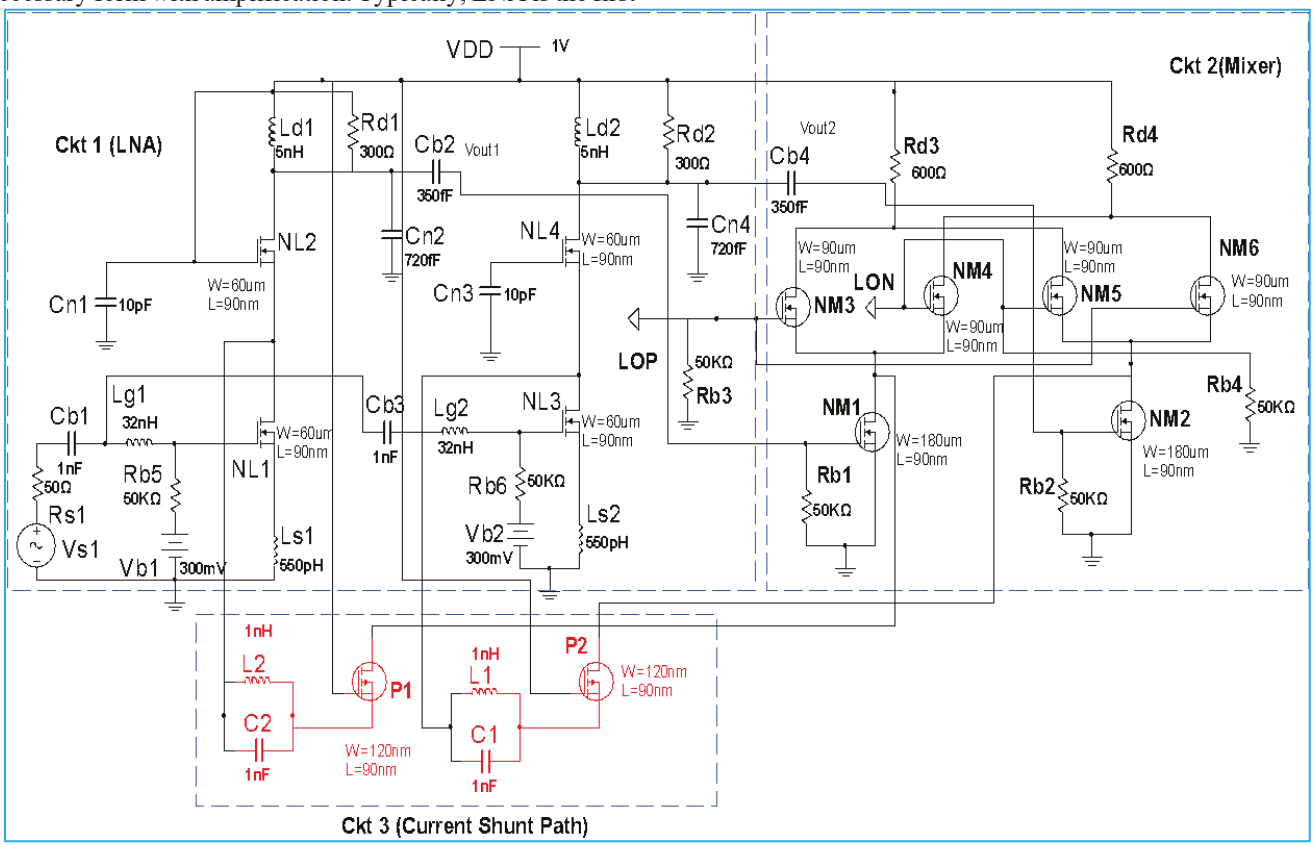

Figure 1. Proposed Novel merged LNA mixer using creative current recycle technique

In Fig 1 (Ckt 1), the Input port source resistance is 50Ω. Coupling Capacitors C_{b1}, C_{b2}, C_{b3}, and C_{b4} are coupling capacitors that couple the a.c input to the MOSFET. Noise Cancellation Capacitors C_{n1}, C_{n2}, C_{n3}, and C_{n4} are used to cancel the noise. R_{d1} and R_{d2} act as load resistors, and R_{b1} and R_{b2} act as biasing resistors. Gate Inductors L_{g1} and L_{g2}, source degenerated inductors L_{S1} and L_{S2} and drain Inductors and L_{d1}, and L_{d2} can series RLC network and be used to provide additional gain to LNA. Here the source degeneration technique is used to achieve impedance matching.

$$Z_{in} = \frac{g_m L_S}{C_{gs}} + j\omega L_S + \frac{1}{j\omega C_{gs}} \quad (1)$$

$$R_{in} = \frac{g_m L_S}{C_{gs}} \quad (2)$$

Differential Cascode Common Source LNA with inductive source degeneration and noise neutralization capacitors shown in Figure 1 (Ckt 1), is used for impedance matching and Gain improvement. The input transistors NL1 and NL3 convert the input voltage into drain current (I_{DS}). The drain current I_{DS} is flowing through a low impedance node available at the source of NL1 and NL3 to cascode transistors NL2 and NL4 to output inductive loads Ld1 and Ld2. The output inductive loads convert this I_{DS} into an output voltage V_{out1} and V_{out2}. In Figure 1(Ckt 1), V_{S1} is the source signal voltage received from the antenna, R_{S1} is the source resistance, the gate bias voltage is V_{dc1}, and the supply voltage is V_{DD}. From the mathematical analysis, the gate-to-source

capacitance and the quality factor can be represented as shown in equations 3 and 4 respectively.

$$C_{gs1} \approx \frac{2}{3} WLC_{ox} + C_{OV} \quad (3)$$

$$Q_S = \frac{1}{2R_S\omega_r C_{gs1}} \quad (4)$$

From the R_{d1}, L_{d1}, C_{b2}, C_{n2} and parasitic capacitances C_{gd2}, C_{db2} a parallel resonant circuit is formed at the output of the LNA circuit. The resonant frequency at the output is shown in Equation 6. C_{gd2} is the gate to drain capacitance, and C_{db2} is the drain to bulk capacitance of MOSFET NL2. C_{n2} is the noise neutralization capacitor and C_{b2} blocking capacitor of NL4. The resonant frequency (ω_r) is shown in Eqn 5.

$$\omega_r = \frac{1}{\sqrt{(L_{d1})(C_{gd2}+C_{db2}+C_{n2}+C_{b2})}} \quad (5)$$

Z_{in} is resistive at resonant frequency (ω_r) with the input resistance (R_{in}) shown in equation 2 by choosing good g_m, L_S and C_{gs} values. So that, the impedance can be achieved is R_{in} = 50Ω. C_{gs} depend upon the MOSFET device dimensions and frequency of operation. Choose the value of L_s according to g_m and C_{gs}. Here L_s is an on-chip inductor, and L_g is an off-chip inductor. The frequency of operation can be represented as shown in equation 6.

$$\omega_r = \frac{1}{\sqrt{(L_g+L_S)C_{gs}}} \quad (6)$$

The gain of the common source or common gate amplifiers can be improved by increasing the transconductance or the output resistance. The output of the common source amplifier is connected to a common gate amplifier known as cascoding, which improves the gain of the circuit. Miller effect can be reduced by using a cascoding structure. The g_m can be improved by increasing the μ_n or C_{ox} or W/L ratio or $I_{DS,}$ as shown in equation 7. An increase in μ_n or C_{ox} or W/L ratio will tend to increase the I_{DS}, which increases the voltage drop across R_D, which reduces the output voltage swing of the circuit. Hence the g_m should be increased without affecting the circuit's gain.

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L} I_{DS}} \quad (7)$$

The typical receiver noise figure is 6 to 8 dB, in that the antenna switch or duplexer contributes about 0.5 to 1.5 dB, the LNA about 2 to 3 dB, and the remainder of the chain about 2.5 to 3.5 dB [12]. While these values provide a good starting point in the receiver design, the exact partitioning of the noise is flexible and depends on the performance of each stage in the chain. The total noise figure of LNA and Mixer is represented in equation 5, where NF_{LNA} is the noise figure of LNA, $\underline{v_{n,mix}}^2$ is mean square noise voltage of mixer, A_{LNA} is the gain of the LNA.

$$NF_{Total} = NF_{LNA} + \frac{\underline{v_{n,mix}}^2}{{A_{LNA}}^2} \cdot \frac{1}{4kTRs} \quad (8)$$

The linearity is represented in terms of 1-dB compression point (P_{1dB}) and Third order Intermodulation Intercept Point (IIP3). Non-linearity in the RF circuits creates harmonic distortion, gain compression, Intermodulation, and cross-modulation [12]. The typical value of 1dB compression point is in the range of -20dBm to -25dBm, of IIP3 of LNA, is -10dBm to -16dBm to achieve better linearity in the LNA design. The nonlinearity expression in a cascaded LNA-Mixer circuit is defined as shown in equation 9, where $V_{IP3,LNA}$ is the third harmonic frequency signal voltage generated by LNA, A_{LNA} is the gain of the LNA and $V_{IP3,mix}$ is the third harmonic frequency signal voltage generated by a mixer. From mathematical analysis, LNA gain and noise factor is represented in equation (10) and (11) respectively.

$$\frac{1}{{V_{IP3,tot}}^2} = \frac{1}{{V_{IP3,LNA}}^2} + \frac{{A_{LNA}}^2}{{V_{IP3,mix}}^2} \quad (9)$$

$$A_V = \frac{-R_{d1}}{2\omega_r L_{S1}} \quad (10)$$

$$F = 1 + \gamma g_{m1} R_S \left(\frac{\omega_r}{\omega_T}\right)^2 + \frac{4R_S}{R_{d1}}\left(\frac{\omega_r}{\omega_T}\right)^2 \quad (11)$$

The differential LNA design values for 5G Wi-Fi receiver are shown in Table II [11]. From Table II the input port resistance of LNA is 50Ω.

TABLE II.
DIFFERENTIAL 5G WI-FI (5GHZ) LNA DESIGN VALUES

Input Port (P_{in1}) Source Resistance	50Ω
Coupling Capacitors (C_{b1} & C_{b2})&(C_{b3} & C_{b4})	1nF &350fF
Noise Cancellation Capacitors (C_{n1} & C_{n3})	10pF
Noise Cancellation Capacitors (C_{n2} & C_{n4})	720fF
Load Resistors (R_{d1} & R_{d2})	300Ω
Biasing resistors (R_{b1} & R_{b2})	50KΩ
Gate Inductors (L_{g1} & L_{g2})	32nH
Source degenerated inductors (L_{S1} & L_{S2})	550pH
Drain Inductors (L_{d1} & L_{d2})	5nH
Length of NL1, NL2, NL3 & NL4	90nm
Width of NL1, NL2, NL3 & NL4	60um

The Proposed Mixer circuit without shunt paths is shown in Fig 1 (Ckt 2) and is implemented with 'NM1', 'NM2' are RF transistors that convert RF voltage into current [17]. This current is steered by LO transistors 'NM3', 'NM4', 'NM5' and 'NM6'. Then this steered current is converted into IF voltage using 'R_{d3}' & 'R_{d4}'. Here 'NM3', 'NM4', 'NM5' and 'NM6' transistors are known as switching quad [14]. At the RF port V_{RF+} and V_{RF-} represent the different phases of RF input. The conversion gain (G_C) of the proposed mixer without shunt paths is shown in Equation 12. It can be defined as the ratio of the IF can be defined as the ratio of the IF voltage (V_{IF}) at the output to RF voltage (V_{RF}) at the input, where g_{m1} transconductance of 'NM1' and 'Rd3' is the load resistor.

$$G_C = \frac{2}{\pi} . g_{m1} . R_{d3} \quad (12)$$

The Proposed Merged LNA-Mixer with current shunt paths is shown in Fig 1. A feedback connection shown in Fig 1 (Ckt 3) is given from the mixer drain terminals of 'NM1' and 'NM2' to LNA drain terminals of 'NL1' and 'NL3' using PMOS current sources ('P1' and 'P2') and two LC tank circuits. The LC tank circuit provides high input resistance from LNA to Mixer, such that the drain current of LNA cannot be entered into Mixer.

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III. Simulation Results and Analysis

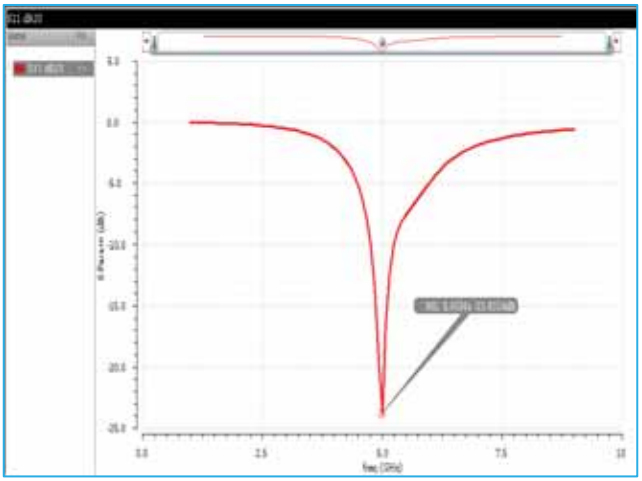

Figure 2. S_{11} of differential 5G Wi-Fi LNA

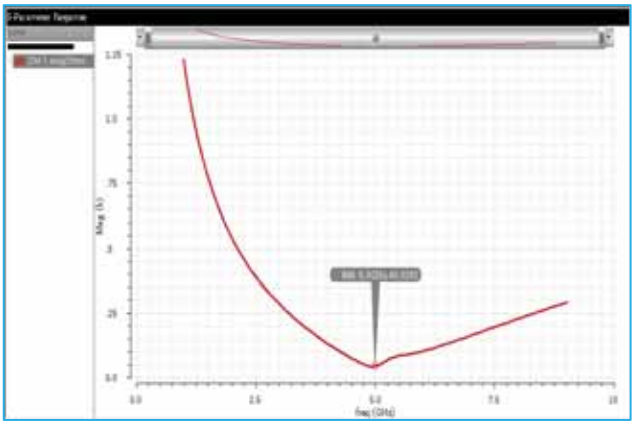

Figure 3. R_{in} of differential 5G Wi-Fi LNA

From Fig 2, the input reflection coefficient is -23.831dB. From that it can be said that in the proposed differential 5G Wi-Fi, LNA delivers 93.6% of input signal to the circuit and 6.4% of incident wave is reflected back as shown in Fig 2. From the port input impedance Z_{M1}=45.94Ω at 5 GHz frequency as shown in Fig 3. From this, it can be said that 91.88% matching occurs at the input of LNA.

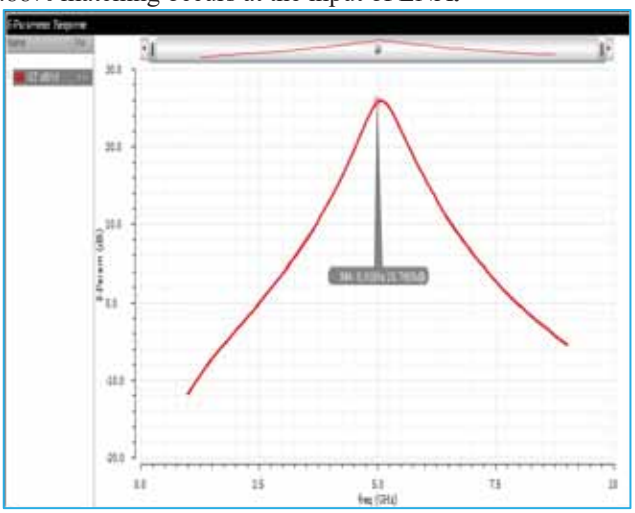

Figure 4. G_T of differential 5G Wi-Fi LNA

The achieved transducer gain is 25.76dB at 5GHz frequency for Differential LNA shown in Fig 1 (Ckt 1).

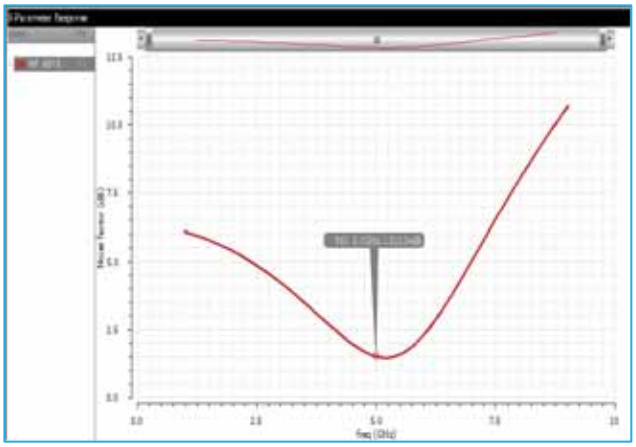

Figure 5. NF of differential 5G Wi-Fi LNA

The target Noise Figure is <3dB and the achieved Noise Figure =1.52dB in Differential LNA shown in Fig 1 (Ckt 1) as shown in Fig 5.

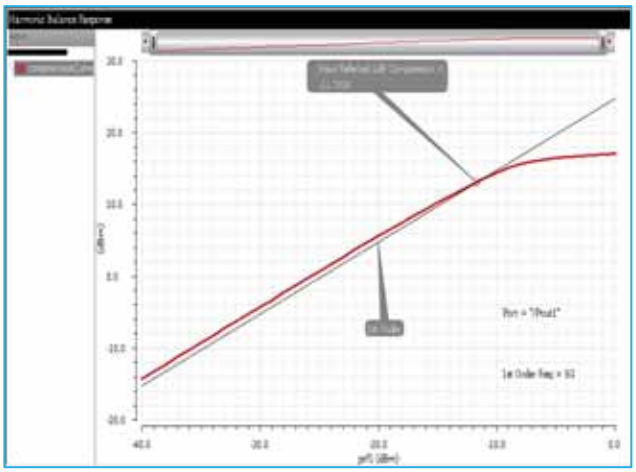

Figure 6. P_{1dB} of differential 5G Wi-Fi LNA

LNA gain in Differential LNA shown in Fig 1 (Ckt 1) is compressed by 1dB from actual value at -11.7dBm i.e. when the input signal power attained to value of 67µW as shown in Fig 6.

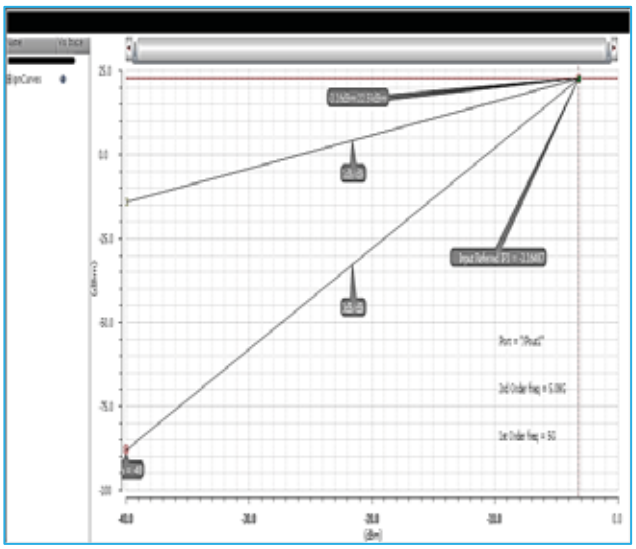

Figure 7. IIP3 of differential 5G Wi-Fi LNA

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IIP3= -3.17dBm of Differential LNA shown in Fig 1 (Ckt 1), when the input signal power reached to -3.17dBm (i.e.) 481µW, the third harmonic signal power meets the input signal power as shown in Fig 7.

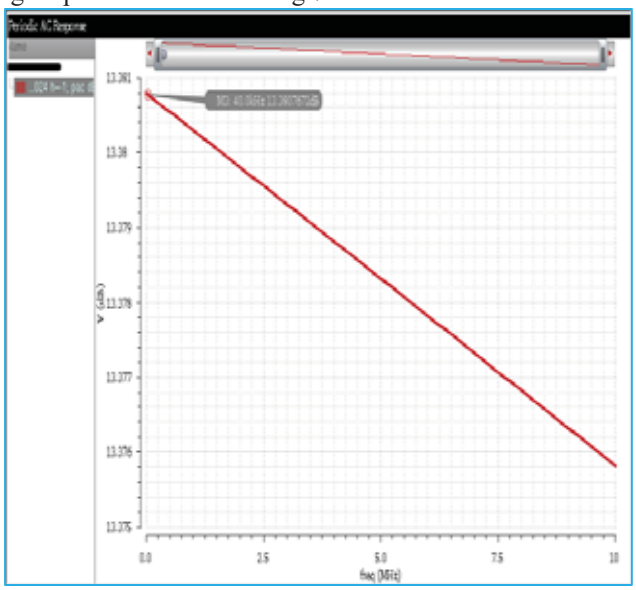

Figure 8. Mixer Conversion Gain

In Table III, the biasing voltages for RF and LO transistors are taken as 300mV. The proposed mixer voltage conversion gain of the Mixer circuit shown in Fig 1 (Ckt 2) is 13.38 dB at 5 GHz frequency. The current flowing through the transistors, drain to source voltages of transistors used in the mixer part and power calculations of proposed merged Differential LNA-Mixer with shunt paths in Fig 1 (Ckt 2) are shown in Table III. The static power consumed in the mixer part of Fig 1 is 1.276mW.

TABLE III.
POWER CALCULATIONS OF PROPOSED LNA-MIXER WITH SHUNT PATHS (MIXER PART)

Parameter	Value
Biasing voltages [$V_{b(RF)}$ & $V_{b(LO)}$]	300mV
Current through N_{M1}&N_{M2}	0.687mA
Current through N_{M3}, N_{M4}, N_{M5} & N_{M6}	0.317mA
Drain to Source Voltage of N_{M1}&N_{M2}	70.13mV
Drain to Source Voltage of N_{M3}, N_{M4}, N_{M5} & N_{M6}	548.9mV
Power consumed by R_{d3} & R_{d4} branch	0.484mW
Power consumed by N_{M1}&N_{M2}	0.096mW
Power consumed by N_{M3}, N_{M4}, N_{M5} & N_{M6}	0.696mW
Static power Consumption in merged LNA-Mixer with current shunt paths (Mixer Part)	1.276mW

The biasing voltage of differential LNA is taken as 300mV. The current flowing through the transistors, drain to source voltages of transistors used in the LNA part and power calculations of proposed merged Differential LNA-Mixer with shunt paths in Fig1 (Ckt 1) are shown in Table IV. The static power consumed by the differential LNA part in Fig 1 is 2.26mW.

TABLE IV.
POWER CALCULATIONS OF PROPOSED LNA-MIXER WITH SHUNT PATHS (LNA PART)

Parameter	Value
Biasing voltages [V_{b1}&V_{b2}]	300mV
Current through N_{L1}, N_{L2}, N_{L3} & N_{L4}	1.13mA
Drain to Source Voltages of N_{L1} & N_{L3}	618.13mV
Drain to Source Voltage of N_{L2} & N_{L4}	381.87mV
Power consumed by N_{L1} & N_{L3}	1.397mW
Power consumed by N_{L2} & N_{L4}	0.863mW
Static power Consumption in merged LNA-Mixer with current shunt paths (LNA Part)	2.26mW

TABLE V.
POWER CALCULATIONS OF PROPOSED LNA-MIXER WITH SHUNT PATHS (SHUNT PATH PART)

Parameter	Value
Current through P1 & P2	0.053mA
Drain to Source Voltages of P1 & P2	548 mV
Power consumed by P1 & P2	0.058mW

The current flowing through the transistors P1 and P2, drain to source voltages of transistors used in shunt paths and power calculations of proposed merged Differential LNA-Mixer with shunt paths in Fig 1 (Ckt 3) are shown in Table V. The static power consumed by LNA, Mixer and shunt path parts and the total static power consumed in Merged Differential LNA-Mixer with current shunt paths in Fig 1 is shown in Table VI.

TABLE VI.
POWER CONSUMPTION IN PROPOSED DIFFERENTIAL LNA-MIXER WITH CURRENT SHUNT PATHS

Parameter	Value
Static power Consumption in LNA part	2.26mW
Static power Consumption in Mixer part	1.276mW
Static power Consumption in current shunt paths	0.058mW
Total Static power Consumption in Merged LNA-Mixer with current shunt paths	**3.594mW**

The transducer gain (G_T) of LNA and the conversion gain (Gc) of the Mixer, the total gain and the total static power consumed in proposed Merged LNA-Mixer (Fig 1) are shown in Table VII.

TABLE VII.
TOTAL STATIC POWER CONSUMPTION AND THE CONVERSION GAIN OF PROPOSED DIFFERENTIAL LNA-MIXER

Result Parameter	Value
Transducer Gain (G_T) of LNA	25.76dB
Conversion Gain (G_C) of Mixer	13.38dB
Total Gain of in proposed LNA-Mixer	39.14dB
Power Consumption in LNA	2.172mW
Power Consumption in Mixer	1.336mW
Power Consumption in proposed LNA-Mixer	3.594mW

TABLE VIII.
COMPARISON OF THE LNA CIRCUIT IN PROPOSED DIFFERENTIAL LNA-MIXER

Parameter/Reference	LNA design factors	REF [10]	REF [15]	Proposed LNA
f_r	5GHz	5.2GHz	5.2GHz	5GHz
S_{11}	<-15dB	-15dB	-10.5dB	-23.8dB
G_T	25.76dB	15.5dB	8.22dB	25.8dB
NF	<=3dB	4.5dB	3.7dB	1.5dB
IIP3	>-20dBm	5.6dBm	4dBm	-3.16dBm
P_{static}	<5mW	10mW	7.6mW	3.594mW

The comparison of the existing LNAs with the LNA circuit in the proposed differential LNA-Mixer circuit in Fig 1 (Ckt 1) is shown in Table VIII. Table VIII compares the results of the existing 5GHz proposed differential LNA with REF [22] and REF [23] and with the LNA design factors. From Table VIII, the input reflection coefficient (S_{11}) of the LNA part is -23.8dB, the Transducer gain (G_T) of the LNA part is 25.88, Noise Figure (NF) is 1.5dB, IIP3 is -3.16dBm and the static power consumed (P_{static}) is 3.594mw are superior to REF [10] and [15].

III. CONCLUSIONS

The differential LNA for 5G wi-fi and mixer circuit can be merged to achieve larger gains. This is a useful feature for the subsequent blocks in the 5G Wi-Fi receiver design. The source degeneration technique is beneficial to achieve impedance matching at the input side of the circuit. The cascoding of a common source amplifier with a common gate amplifier will improve the gain of the circuit while avoiding the Miller effect in common source amplifiers. Cascoding Technique is not only used to improve the gain, but also to improve the noise figure and linearity. The linearity of the LNA can also improve by choosing the differential structures in LNA circuit design. The PMOS transistors are used in current shunt paths. The current shunt paths are used to connect the mixer circuit with LNA to reduce the power consumption without affecting the gain in future.

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