FPGA Design of ECG-SoC System for the Analysis of ECG Applicable for Rural Health Care Centers

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Abstract: Today, **seventy percent of Indians still live in poor conditions in rural areas. Those who live in rural regions have fewer alternatives available to them in nursing care and medical diagnostics since there are only a few institutions equipped with modern medical technology. This situation reduces the number of choices available to them. As a direct consequence of lack of medical facilities, the rural residents do not find enough access to medical treatment. From this perspective, the use of cutting-edge technology to the treatment of their various health problems could prove to be advantageous. In this work, it is proposed that the design and implementation of an ECG-SoC system for the analysis of ECG is applicable to rural health care centers. This system is designed to meet the needs of rural communities. Electrocardiogram (ECG) pre-processing and heart rate variability (HRV) feature extraction are two of the numerous operations that it can do; both the features are appropriate for use in applications pertaining to remote health care. The ECG-SoC was developed by employing a technique known as hardware/software co-design, utilizing an offline dataset obtained from the MIT-BIH database. The design of the system prototype and the testing of the system's functionality both made use of an Altera Cyclone II DE2-115 FPGA platform. Both the processes were carried out to ensure the system's integrity. The results of the computation are shown on the Nios II-Linux terminal, and the task of creating output files for post-processing on the Nios II-Linux terminal appears on the personal computer that is serving as the host. The findings of this research indicate "that the ECG-SoC system developed is capable of performing power spectrum analysis in addition to compiling a raw ECG dataset, detecting QRS, computing R-R intervals, and presenting the FFT output". It is demonstrated that the system can perform these tasks. In addition to this, it can carry out all these activities at the same time. The strategy that has been outlined here will not only bring about a general reduction in the cost of receiving medical care in rural regions, but it will also bring about a lessening in the severity of cardiovascular diseases**

Index Terms: **Electrocardiography (ECG), ECG-SoC System, HRV Feature extraction, cardiovascular diseases**

I. Introduction

According to the information that was gathered and compiled by the World Health Organization (WHO) in the year 2021, cardiovascular disease was the leading cause of death, accounting for almost 68% of all fatalities [1]. It is estimated that coronary heart disease caused 8.3 million fatalities, whereas strokes caused 7.2 million deaths. Cardiovascular disease is responsible for one out of every four deaths, and the proportion of people who die away due to cardiovascular disease is increasing with each passing year [2].

In today's world, enhanced patient monitoring systems have been developed for the goal of tracking the states of patients [3] but very little clinical data has been gathered to estimate the effectiveness of these tactics [4]. Therefore, the standard of care for most medical professionals and healthcare systems remains to be the routine observation of patients' vital signs on a periodic basis [5]. This is the case despite recent developments in new sensing technology. An electrocardiogram, more often referred to as an ECG, is a graphical depiction of the voltage that is produced by the cardiac or heart muscle during the activity of a heartbeat [6]. ECG monitoring systems need to have the capability of extracting the characteristics of an ECG signal in real time [7]. This is a crucial feature. Heart rate variability, sometimes referred to as HRV, is a naturally occurring physiological phenomenon in which there is a change over the course of time in the amount of time that elapses between each of an individual's following heart beats. [8] HRV is an accurate representation of all these different components of heart function, which may be influenced by several physiological factors that can vary the regular beat of the heart. Timing, frequency, and nonlinearity of the HRV signal are the primary processing components that are retrieved from this signal . This signal also exhibits nonlinearity. The features that are obtained from this extraction are useful diagnostic tools that may be used to determine a range of disorders that are linked with the function of the heart [9].

Previous work on ECG analysis may be categorized into the four different kinds of solutions that are as follows: (i) Solutions for traditional, fixed machines (ii) Solutions for System-On-Chip (iii) Solutions for portable device and (iv) Solutions for Application Specific Integrated Circuits (ASIC) [10]. Because all the devices that required to be used to monitor the patient had to be plugged in, prior monitoring systems could not allow for the patient to move freely or conduct remote assessments. In addition to that, the implementation of these solutions necessitated the provision of an excessive number of hospital beds [11][12]. In order to provide a reliable study of the electrocardiogram (ECG), the SoC system may conduct 12-lead investigations entirely inside a single chip. The commercial technique [13], which uses digital signal processing (DSP) to take eighth input sensor lines, produce lead signals, and analyze all of them in one step, does all of this in one step; nevertheless, the procedure is arduous. Electrocardiography (ECG), Electroencephalography (EEG), and respiration signals are examples of the types of biological data that can be captured using a novel approach [14] that makes use of a flexible SoC

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that integrates the capture of multiple biological data with on-chip digital signal processing [14]. This novel approach makes use of a portable ECG measuring and monitoring system that is founded on Linux, in contrast to handheld systems [15] that do little more than receive and send data. Data collection from a 12-lead ECG is one of the features offered by this device, along with internet-based remote diagnostics. Only for the purpose of data collection prior to transmission is the ASIC solution [16] put into use.

Developing an ECG device with System-on-Chip (SoC) technology is one method that is suggested for incorporating an HRV analysis capability onto an ECG device. This method has a few advantages. The end objective of this endeavour will be the manufacture of a portable cardiac monitoring equipment that is suitable for application in contexts associated with home care. This work presents a SoC that is based on the ECG biomedical embedded system. It does this by utilizing a hardware/software co-design technique and the technology offered by Altera (ECG-SoC). The objective of the SoC is to do ECG pre-processing and HRV feature extraction using an offline database that was developed by MIT-BIH [17] .

In this article, a proposal is made for the development of an electrocardiogram (ECG) system that is particularly well suited for application in rural health care facilities. The design of the ECG System is based on FPGA, and it makes use of System-on-Chip technology (also known as ECG-SoC).

II. Proposed Method

The ECG-SoC Cyclone II FPGA architectural design shown in Fig.1 is meant to make it possible for a superior technology to be developed by utilizing a Nios II processor, an Avalon on-chip communication bus, and a Nios II–Linux embedded operating system. All of these components are shown in the figure. The illustration in question illustrates this design.

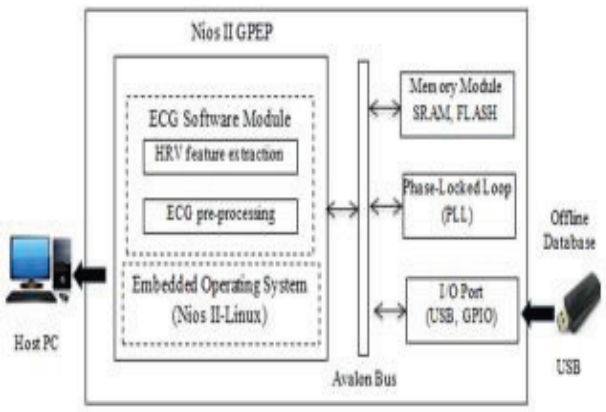

Figure 1. ECG-SoC Cyclone II FPGA

The ECG-SoC was designed primarily for the goal of ECG preprocessing as well as HRV feature extraction. Both aims were pursued simultaneously during development. Because of this, the ECG-SoC will perform computations based on an offline dataset rather than making use of a module for online data collection in order to get the necessary information. The ECG-SoC architecture consists of software and hardware subdivisions working together to form the whole (HW and SW, respectively). Memory modules, a phase-locked loop (often referred to as PLL), and input/output (I/O) ports are all components that are part of the HW partition's make-up. These components each serve a distinct function, some of which include the following but are not limited to the following: to store the image of an embedded operating system, which is composed of programmes, the dataset, and other important files; to control the clock signal of the host computer, the system, and the targeted board; to communicate and transmit data to the outside world; and to accelerate operations that take a significant amount of time within the system. A communication link between these components that is constructed in accordance with established specifications is provided by something that is referred to as a system bus, which is located beside these components.

III. Methodology

An illustration of the ECG-SoC design process is shown in Fig.2. It is composed of four stages, which are the design of system hardware architecture, the design of the Nios II-Linux embedded operating system (OS), the design of ECG-SoC software and the integration of the system". The first stage is the design of the system hardware architecture, and the other three stages are the design, creation, and integration of the OS. In the paragraphs that follow, we will discuss the particulars of each stage. At various stages of the design process, the use of a variety of EDA tools, such as QUARTUS II, SOPC Builder, Nios II IDE, and Nios II-Linux cross compiler, is required .

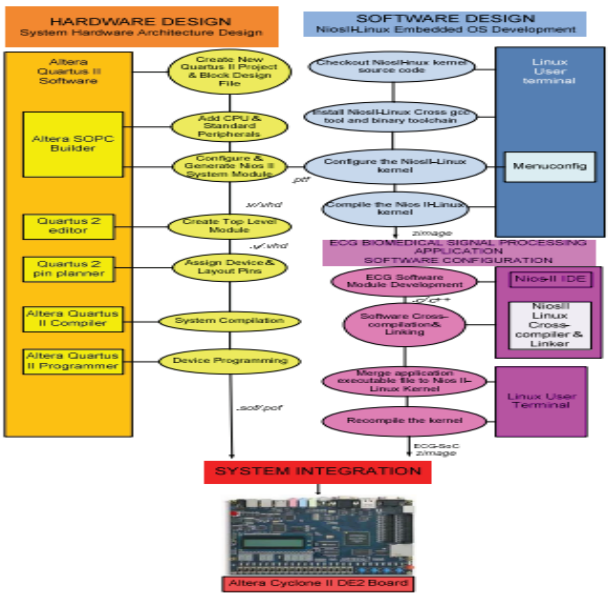

Figure 2. Design Methodology of ECG-SoC

A. System Hardware Architecture Design

Two distinct phases make up the process of designing the system's hardware components from start to finish. SOPC Builder is used at the beginning of the process to define the Nios II GPEP, RAM, and other standard peripherals in order to design a Nios II system module. This is done to ensure that the module will function properly (System-on-

Programmable-Chip). The details of the configuration include the reset vector and the exception vector of the Nios II processor, as well as the base address, the interrupt request (IRQ) assignment of each peripheral, and the source of their clock signal. Additionally, the details include the reset vector and the exception vector of the Nios II processor . Both the process-initiated multiple Verilog HDL (v) files and the system configuration file (.ptf) are going to be utilised in the process of configuring and compiling the software module, and the SOPC Builder is responsible for the generation of both files. In addition, the SOPC Builder is responsible for the generation of the system configuration file (.ptf). During the second stage, the Quartus II will create a top-level file of the Nios II system module. This file will comprise targeted development board, device, and pin selections. The compilation process then does synthesis, fitting, and timing analysis to create the netlist and HW programming file (. sof/.pof), both of which are downloaded to the Cyclone II DE2 FPGA board during system integration .

The hardware architecture of the ECG-SoC system is represented in Fig. 3, which also illustrates the configuration of the system. The whole system that is contained on the Cyclone II DE2 FPGA board makes use of this design in its many iterations during its operation. The marked and coloured block on the chip, which is filled with several different modules, is meant to depict the inside of the chip. To include these modules into the system, SOPC Builder is the tool that is utilised.

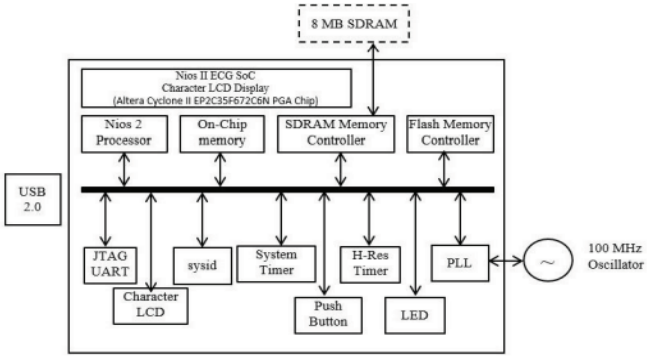

Figure 3. ECG-SoC hardware system configuration

On-chip memory, the SDRAM memory controller, and the flash memory controller are the three basic kinds of memory modules that can be used . On-chip memory is the most common type of memory module. A high-resolution timer, also known as a HiRes. Timer, and a system timer are both utilised for the purposes of improving timing control, simplifying timing problems, and improving the overall structure of the board. The phase-locked loop, also known as PLL, is utilised in the construction of this particular system, and it is responsible for producing a clock signal with a frequency of 100 MHz. The system ID, which is sometimes referred to as the sysid, can get an address that is exclusive to the architecture of this specific system. The JTAG UART is being used as the I/O port for this project. On the other hand, USB 2.0 is being put to use as the peripheral device on the outside.

B. Nios II-Linux embedded operating system

Nios II-Linux is a terminal-based Linux embedded OS that uses Debian 2.6.4-rc6. It can execute Linux programmes and libraries. Distributed versioning, relational databases, debuggers, and cross compilers are included. Cross-compilation condenses information into one file. Linux kernel image is an auto-extractable file (zImage). Cyclone II is programmed using ECG-SoC . The programming file (.sof) must match the board's hardware architecture to work. The hardware system's configuration file (.ptf) is needed to configure the Linux kernel and construct the ECG-Nios SoC's II-Linux kernel.

C. ECG-SoC Software Design

To construct the software portion of the ECG-SoC system, it is necessary to do ECG preprocessing as well as ECG feature extraction, both of which are depicted in Fig.4.

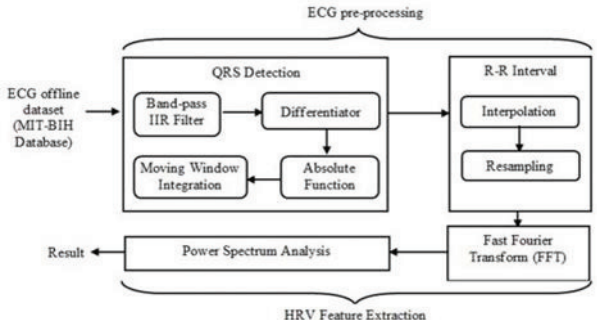

Figure 4. ECG Pre-Processing and HRV Feature Extraction

Eliminating baseline drift, high-frequency noise, and high-frequency random noise created by power line interference is one of the primary goals of pre-processing, along with increasing the signal-to-noise ratio and improving the accuracy of analysis and measurement (50 Hz, 60 Hz) .

During the pre-processing stage, the QRS identification algorithm is modified so that it can correctly identify the ECG QRS complex for HRV analysis. This is done before the processing begins. The band-pass frequency of this detector module is somewhere between 5 and 15 Hz. The slope information needed for peak identification may be obtained from the differentiated filter output. The square function is being phased out in favour of its more efficient counterpart, the absolute function, which may flip between positive and negative peaks. The data is then integrated with a moving window in order to smooth it out. After the QRS complex has been located, the signal from the electrocardiogram is changed into a signal that looks like a valley with two peaks of varying heights. Electrocardiograms determine the presence of heartbeats by focusing on the R peaks of the QRS complex [18]. The R-R interval module of the ECG analyses the current value in comparison to future values in order to determine the peak. The value that is greater than the eight values that follow it and the threshold level is known as the QRS peak. The subsequent block unit does an interpolation between two R-R intervals to provide findings for a continuous R-R interval based on the peaks that were seen.

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To obtain a rapid Fourier transform, the peak QRS signals are resampled at 4 Hz and then linearly interpolated (FFT).

Then, the R-R power spectrum should be obtained. When linear adjustments are incorporated, spectral methods applied to ECG analysis can help explain the behaviour of the time domain model [19]. For power spectrum analysis, both real and imaginary FFT results are necessary. The below mentioned equation (1) demonstrates this point.

$$PS = \frac{\sqrt{(r^2+i^2)}}{N} \quad (1)$$

Where PS is the power spectrum, r is the real, i is the imaginary, and N is for total number of R-R intervals or heart rate (HR) data being transformed.

From the heart rate spectrum diagram, three power bands may be extracted. Power bands range from 0.008 to 0.04 Hz, 0.04-0.15 Hz, and high frequency (HF: 0.15-0.5 Hz). For HF HRV, the power spectrum between 0.15 and 0.4 Hz is integrated. Then, equations (2) (3) (4) are employed, where HR (f) denotes heart rate frequency (HR) .

$$HRV_{VLF} = \sum_{f=0.008}^{0.04} \frac{|HR(f)|^2}{T} \quad (2)$$

$$HRV_{LF} = \sum_{f=0.04}^{0.15} \frac{|HR(f)|^2}{T} \quad (3)$$

$$HRV_{HF} = \sum_{f=0.15}^{0.4} \frac{|HR(f)|^2}{T} \quad (4)$$

HRV is heart rate variability; VLF is extremely low frequency; LF is low frequency; and HF is high frequency. The ECG system's software was created to incorporate ECG-SoC standards for successful ECG pre-processing and HRV feature extraction. 200 Hz sampling frequency and 8 kHz threshold are used. We utilised 12,000 ECG data, and the FFT count was 1024. The 240-second FFT window size .

D. System Integration

The hardware programming file (.sof) and the most recent version of the Nios II-Linux zImage file are both downloaded into the Altera Cyclone II DE2-115 platform during the final step of the system integration process. This is done so that the functionality of the system can be checked, as well as the assessment can be carried out.

IV. Results and Discussion

The descriptions of the ECG system requirements are shown in Table I below [20]. For the ECG signals, we sampled at a frequency of 200 Hz, and the threshold values were set at 8000 Hz. In the meanwhile, a resampling frequency of 4 Hz has been selected with the goal of lowering the dimensionality of the heart rate data. The 120 000 are the offline ECG data that were taken from the MIT-BIH database and stored in a text file format on a pen drive. The increased size of the ECG dataset will result in a greater degree of precision in the processing.

TABLE I.
Specifications of ECG System

Specifications	Values
Sampling frequency	200 Hz
Threshold value	8000 Hz
Resampling frequency	4 Hz
Total ECG data	120 000
FFT count	1024

During the process of verifying the operation of the system, an offline dataset is placed in a portable USB device, and then that device is inserted into the ECG-SoC programme. The results of running ECG-SoC in Nios II-Linux are depicted in Fig. 5 and 6, respectively. At this point, the listings of the execution folders are displayed, and the results are made. The HRV and ECG software are utilized in this section to create the results.

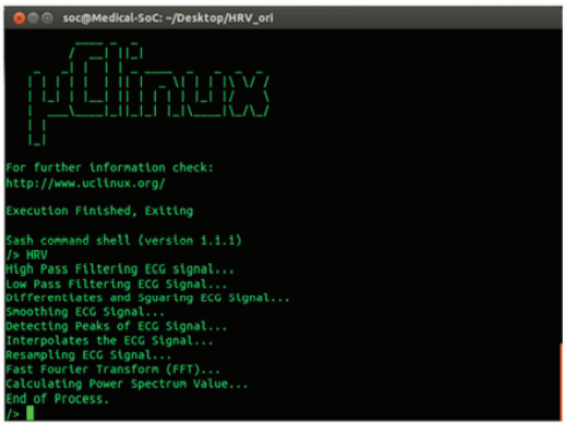

Figure 5. ECG-SoC execution in uCLinux

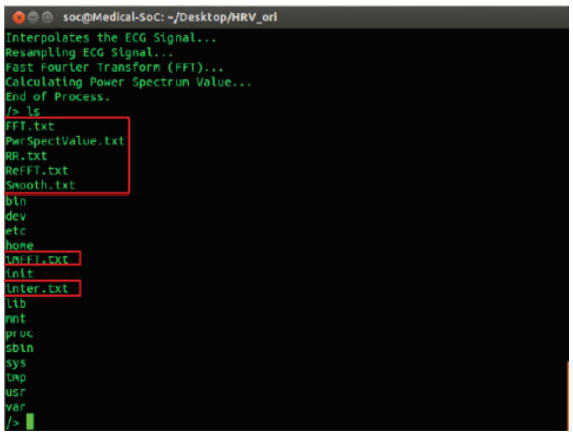

Figure 6. Results file generated from the execution

The electrocardiogram (ECG) data may be seen in Fig. 7 after the programme was developed. To detect negative peaks on an electrocardiogram, each data point is transformed to its absolute value .

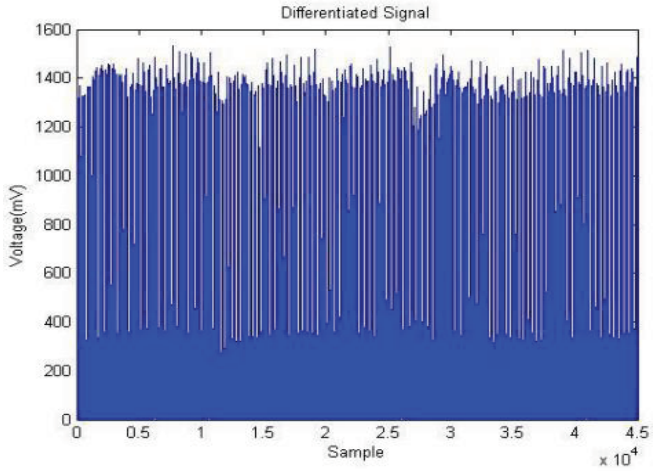

Figure 7. Intermediate results for differentiated signals

The Fig. 8 depicts the output that is obtained when the operation of squaring is carried out immediately prior to the smoothing operation that is carried out by moving window integration. Following performing the squaring procedure, the resultant numbers are greater, and after the integration step necessary to generate a smooth ECG signal, they look like what is seen in the below figure. .

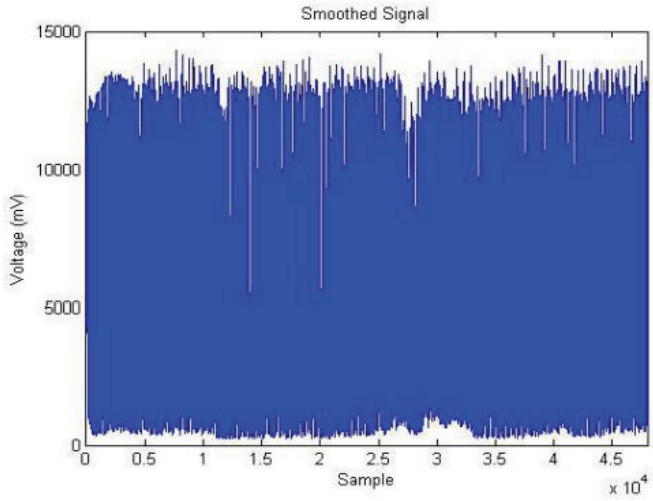

Figure 8. Intermediate results for smoothed signals

Fig.9 shows the QRS peak detected by our proposed method.

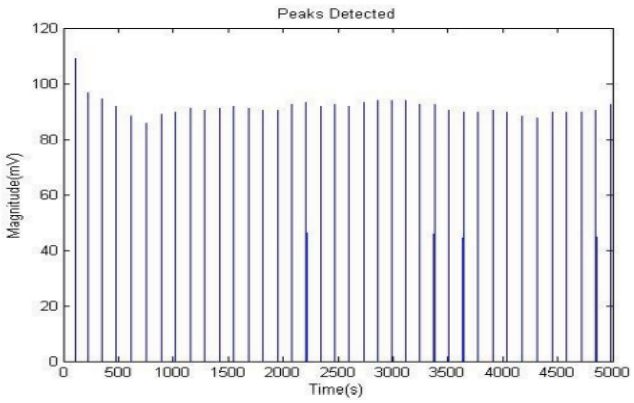

Figure 9. Peak Detection

In Fig.10, linear interpolation has been utilised to the detected QRS peaks for resampling at 4 Hz.

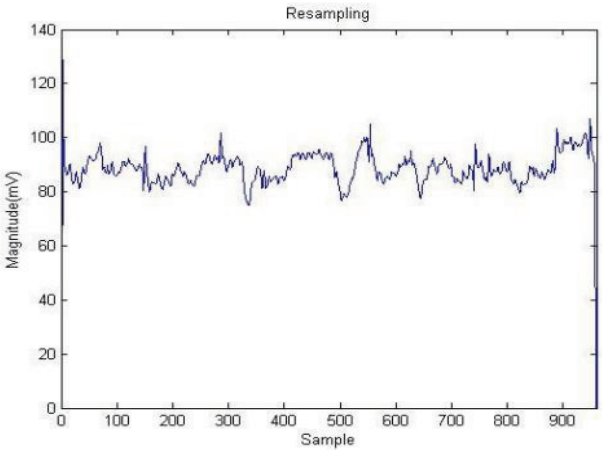

Figure 10. Resampling at 4 Hz by utilizing linear interpolation

The result of the FFT is seen in Fig 11, and it consists of both real and imaginary components. Take note that the negative values appear as a consequence of the fact that an operation was carried out before the FFT was carried out[21] .

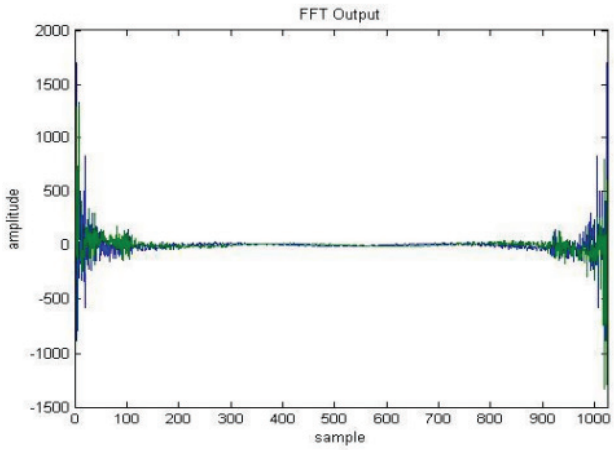

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Figure 11. Fast Fourier Transform

Since this initial process includes subtraction, some numbers will be negative. After FFT results are obtained, Eqn. (1) is used to analyze the power spectrum (1). FFT power spectrum analysis reveals the highest frequency between 0.01 and 0.1 Hz. Inputs include real and imaginary numbers.

The results of power spectrum analysis yields Fig. 12. The graph is plotted for the frequency up to 1 hertz. Maximum VLF, LF, and HF ranges are illustrated by black, green, and black dotted lines, respectively. The highest frequency on this power analysis graph is 0.03 Hz.

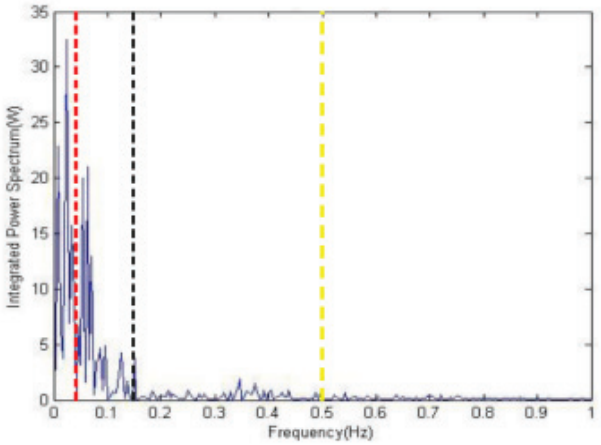

Figure 12. Power spectrum versus frequency

V. Conclusions

In this paper, a System-on-Chip (SoC), which is built on an embedded electrocardiogram (ECG) system is discussed. The ECG-SoC makes use of methodologies that include a co-design of hardware and software as well as technology developed by Altera to carry out ECG pre-processing and extract HRV characteristics from an offline dataset. The fact that these software activities are being carried out is evidence that the ECG-SoC system combines the processes of gathering ECG datasets, storing them, and processing them by utilising integrated hardware and software. All these processes are carried out in tandem with one another. The portability of the system, in addition to the various software enhancements that are capable of being applied are the benefits of the proposed system. The system that has been suggested in this paper can conduct adequate ECG data analysis when it is configured as an ECG-SoC. This enables it to be utilised in a broad variety of cardiac monitoring applications since it satisfies the requirements for such applications in rural areas.

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