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Architecture of Multi-Processor Systems using Networks on Chip (NoC): An Overview

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Abstract: **Network on chip (NoC) is an integrated chip component system with a large scale of integration of components. NoC is an integrated solution in architecture multiprocessor chip. It has metallic wires, ICs, core modules, and components that are used to make products. Specific Integrated Circuits can be classified into three types namely First, Standard IC, second ASSP, and third ASIC. System on chip (SoC) architecture uses communication elements, processors, energy, design applications, modularity, and complexity of the system. The NoC architecture provides operation communication and micro-network components. The NoC architecture is used for processing the data, with multicore on chips (SoC), processing elements(routers), Hardware, network elements, and components. NoC routing chip resources in microprocessor, memory, and Input/Output operations. The SoC chip design is a complex application that requires the design of system components based on requirements, and application specific. The applications are connected to the backbone of the network which uses network topology, NoC chip design, architecture, processors, and it depends on needs and applications. In this study the overview of NoC Architecture elements, topology, routing, flow control, and applications are mentioned. The architecture elements according to the needs to design and development of high-performance systems with optimal utilization of resources. The Future work can be extended to design and develop application-specific standard components in Network on chips.**

Index Terms: **NoC, SoC, Multi-Processor, High-Performance computing, Integrated circuit, Multicore systems, Integration Chip, Communication, Computing**

I. Introduction

Network on-chip communication-based Integrated Chip, the subsystems based on Integrated chip components of the system. NoC is a microprocessor that provides the method to send or receive data. NoC is an approach used to implement VLSI systems. Large scale design, network on a chip is used in the message flow. It contains hardware (routing and switching), topology in different areas of the network.

It minimizes complexity and provides a well-controlled structure with reliability, speed, and High-end systems. Network on-chip is the best integrated solution. Network on Chip (NoC) is an emerging significant on chip design, communication architecture which is used for multi-processor systems where parallel NoC systems are costly and consumes more energy. NoC chip communication scaling is based on application usage, computing advanced integration technologies. The NoC is used in various applications like Artificial Intelligence, big data analytics.

Optical energy with 3D Integrated Circuit solution improves the performance by reducing interconnect length. Section 2 describes the Literature survey, Section 3 deals with the Architecture of NoC and applications, section 4 has discussions, and Section 5 ends with the conclusion and future scope

II. Literature Survey

3D Optical Networks-on-chip (NoC) for Multiprocessor Systems-on-chip (MPSoC), the complexity of multiprocessor system on chip (MpSoc), global communication on the chip is a challenging performance.

Yaoyao Ye et.al[1] studied network communication architecture, which has parallel metallic wires and authors proposed a high bandwidth data transmission in the optical domain. 3D electronic chip integrates optical data transmission network.

Avi Kolodny [2] studied NoC essentials, communication, routing through hops, switches and parallelism. The authors studied a generic architecture with network on chip that route the packets by chip when interconnection is needed. The design model and its characteristics are most important architecture are sensitive to cost, area and power consumption. The custom network design specifications based on requirements like traffic, load, application.

Pingqiang Zhou et. al [3] studied the 3D silicon integration techniques, Network on chip (NoC)architecture design with the 3D environment. The NOC components are used in the building model, the power saving, latency reduction, chip temperature reduction are the parameters.

Mostafa S.Sayed et.al [4] studied the NoC bus architecture, performance and scalability. In NOC design, the authors introduced the architecture which is flexible router with available buffer. The flexible design can achieve better performance by Hotspot, nearest neighbor traffic uniform traffic patterns.

Daniel Gebhardt et.al[5] studied NoC with the interconnection of a large number of Intellectual property cells in the network communication where each cell clock domain has power, latency, and overhead. The authors described asynchronous NoC using flow control, topology, router placement, NOC design, topology, and routing for large routers with network communication latencies.

Adesh Kumar et. al[6] presented chip implementation NOC router by algorithms of architecture with FPGA, VHDL programming and optimized with timing parameters, maximum frequency, and memory.

Youhui Zhang et.a[7] addressed software, hardware hybrid simulation chip multiprocessor system. The NoC simulated FPGA resource. NoC simulation, hardware,

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software-implemented flexible simulation high-performance compact on-chip design, with Xilinxsvirtex 5155T chip. The advantage is increasing the injection rate with the help of hybrid method and improve performance of Chip core by executing CPU.

NoC is the most significant way of communication in Multiprocessor System on Chip (MPSoC). Salma Hesham et.al [14] discussed challenges, design and overview of real time NoC architecture, QoS and fault tolerance.

3D network on Chip problem, the quality mapping methods improve communication efficiency. The IP cores plays most important role in power optimizations. Cui Huang et.al [15] proposed a quantum behaved particle swarm optimization method, where speed and low power consumption in 3D NoC systems. IoT and cloud computing demand, scaling computing with highly efficient, low power process, the NoC is done with packet switched communication. Juan Fang et.al [16] proposed a hybrid NoC framework by buffering and buffer less NoC.

SoC revolution, NoC engineers to designing, dynamic, scalable reliable networks. M.Sujathaet.al [17] reviewed on various NoCs , wired, and wireless and hybrid networks by considering parameters such as adaptability, power and latency and throughput etc.

NoC development on topologies, routing problems Aleksandr Yu et.al [18] proposed a 2D circulant topology design for NoC, characteristics of mesh, torus topologies. Routing NoC with circulant topology and other methods are used. AyasKanta Swain et.al [19] studied a review on demand for home products automation, information sharing, social networks for consumer electronic devices. Multiprocessor SoC and NoC solution helps to improve performance of CE devices.

Parisa Mazaheri Kalahroudi et.al [20] proposed IAM (IWO algorithm mapping), to enhance 2D mesh based NoC mapping IP cores to routers.

III. The Architecture of NoC and Applications

Architectural specification implementation is classified into two types 1) bus-based design 2) NoC-based Design. architectural specification chip, gates and optimize the routing, area, wires, and components in a design where all the things are connected to a bus. Network switches or routers, are capable to take the data and send it to another router, change the locations and send packets to another location. Logical network uses routing methods packet transmissions that has physical design identical to NoC.

Network on chip has following characteristics topology, routing algorithms, switching strategy, and flow control. Metrics: bisection bandwidth, node degree/ diameter. Routers or buffers, wiring delay grow quadratically, buffer insertion can make it linear, but at the heavy cost of buffers, multicycle hops.

Network on Chip architecture: Chip communication improves bandwidth, power efficiency, and scalability. Optical NoC Hybrid architecture was used in optical data transmission at high-speed electronic networks in distributed applications. Optical on-chip router is the most significant component of Optical NoCs. NoC architecture on three-dimensional (3DiC) improves performance by CMOS technology, which supports higher density, and attainment of mixed chip technology interconnections.

System on a Chip (SoC) combines elements in a silicon chip has Very-large-scale integration (VLSI) complex, and high performance core modules and the components technologies used to make the products. SoC processing elements, international technology uses around 4 billion transistors. SoC chip on communication architecture, the processing elements are configured into a single processor. Features of SoC are Physical constraints, bandwidth, synchronization, scheme access pattern, throughput parallel computing, energy consumption proximity, non-determination energy constraints, design specifications general-purpose communication, modularity, and complexity

NoC separated computation from communication, Network on Chip Architecture is shown in Fig.1. Functional Layers: Network on chip architecture, design solution, communication on NoC communication system uses OSI Model, application API and software applications.

Network on Chip architecture: NoC architecture has multiple wires, routes, logic process cores, network interface with clients. ISO/ISI layer has seven layers and functions are described here.

Physical layer. The Communication is done with wire connectivity data link, energy, micro-networks. The physical layer has signal representation with wires, repeaters, circuits, and drivers

***Datalink layer*:** It consists of bits, protocols, error detection, protocols used in network operation. This layer manages system resources, network resources, and quality of services. The data link layer takes the data from the Physical layer as bits and makes into frames. It supports functions like flow control, handing of continuation, correction of transmission errors for the data, The data link layer requires a reliable, signal drivers and receivers, the design technologies are used to restoring signal as technology, error control, utilizing of high bandwidth.

Flow control: Upstream router should know the buffer availability of downstream router and router micro-architecture

Network Layer: Network topology, architecture, which use network resources such as routers, host, heterogenous, cores, architecture. Network layer handles and provides routing algorithms used in message packets transmissions. It provides circuit switch, controller, switch design, virtual channel, channel utilization, multiprocessor networks for end-to-end delivery control Switching is a technique used in a communication network, it needs buffer, store forward virtual circuit needs a buffer, packet has limited buffer size, virtual channels will increase the buffer size. The switching algorithms (i.e., circuit, packet, cut-through switching) were used to another networks.

Routing has deterministic, adaptive routing logic order. In NoC, static routing is used. A Generic Architecture for On-chip route packets interconnections, is the network on Chips where two packets trying to use the same link at same time

will buffer one, maintaining the drop the other is misroute one (deflection).

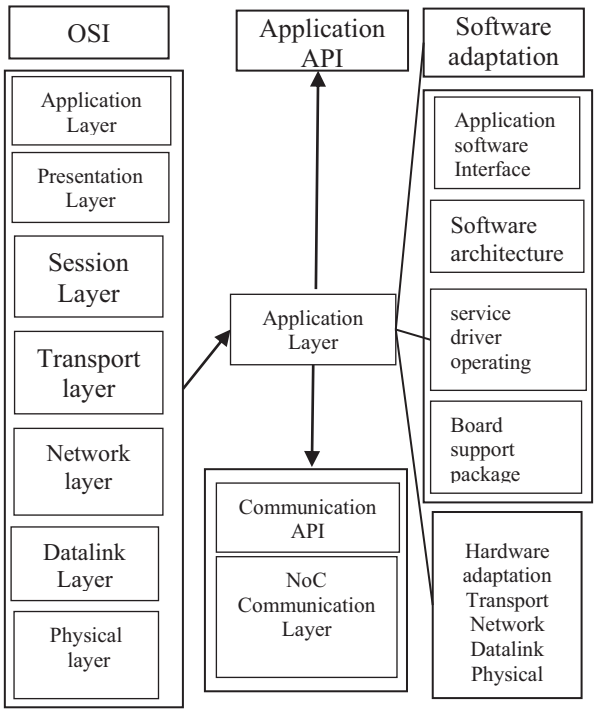

Figure1. NoC architecture (Ref 6)

Transport layer: Transport layer messages decompose the data into a sequence of a message to the destination. The packet standardization, in SoC micro-networks, the traffic management, transportation of packets in NoC, flow control routing algorithms are used for better communication performance. Architecture network, control algorithms are used to provide communication services.

Session Layer: It provides session management, opening, closing sessions between the end-user application process. It provides connections from local to remote system applications.

Presentation Layer: It serves as data translator for the network, mainly concentrating on syntax of user, formatted data, translation with data services. For example, data compression, decomposition, encryption, and decryption.

Application Layer*:* The set of computation, communication tasks, like speed, energy are optimized. Total communication energy is used to recognize service limitations to provide application.

Software Layer: Provided operating system and application layers services. Uniprocessor cannot provide efficient power, and performance.

System software: The system programs on SoC operation.

The NoC architecture provides communication protocols, scalability.

Topology: Topology is the physical organization medium network most common in NoC architecture. Architecture, communication devices have routing and synchronization. The channel communication (if it is asynchronous) then the data is reconstructed. Synchronization of two or more operations can be done at the same time. A direct network is a point-to-point network to each node directly linked with several neighboring nodes. The indirect network is switch-based network nodes that must go to a set of switches. A hybrid network is tightly integrated /connected to computational units with multiple backplanes hierarchical buses.

Topologies, network with new constraints for example 2D mesh has processing element/router link Torus. It shortens distance end to end in either direction into shorter path

The linear set of connection is Hypercube (2 ary,3 cubes), Ring, Octagon etc. The topology in node network connected as bus, mesh, star, etc. The routing algorithms network traffic from node links the data from data link layer to network layer as packets. Network layer uses topologies bus, mesh, tree, torus etc. The switching circuit provides addressing the physical to logical flow of transactions which avoids the distributed deadlocks and improves quality of service. The best services such as best effort, assured throughput, congestion control, flow control end to end communication.

Internet the performance is based on Service Level Agreement (SLA). The RISC, AISC architecture models used Network in Chip, and finds a shortest path routing which optimizes resource scheduling, fast transmission of data. The communication protocols, scalability, topology, computing operations of each process in processor. Network On-chip uses a micro-network protocol which is critical in architecture communication. For SoC design used NoC schemes, SoC architecture.

NoC architecture proposal companies use Free scale, IBM, Intel. The companies to sell it, Sonic (USA),NoC research communities, VLSI/CAD architects, experts use new models, interconnection via transmission message using wires virtual through the NoC. These models' interconnection requires bandwidth, timing, topology, software application, hops that use a router design etc.

NoC platform is scalable, use of billions of transistor chips, many use model VLSI systems with multicore architecture models will improve performance and speed. The 3D Silicon integration technology is a new opportunity design for Network on Chip (NoC) architecture which is developed on System on Chip (SoC). The NoC architecture design uses a 3 D environment and its topology design, 2D, 3D circuits, critical interconnect, all flexibilities are enabled in new system and improve performance system on chip (SoC) structures by 3 D technology. The 3D integrated circuits, with multiple tiers, latency, critical interconnect structure. 2D design rather than 3D circuits give a new high-performance system on chip (SoC) structure 3 D with communication, bandwidth, and parameters.

Architecture of Network on Chip (NoC) is more secured system, the multicore system which depends on switching strategy, topology, and routing methods. The NoC architecture has secured the router. The cryptography message encryption is a Key, the most important in channel security, for multiprocessor systems on chip (MPSoC) and NoC. The secret key encryption algorithms are used in NoC. NoC approach design a network subsystem which has cores,

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SoC, the software application layer in NoC uses resources, microprocessor, OSI layer, network interface, switch, resource for example. connection resources. Network on chip (NoC) uses IP cores, system on chip (SoC), NoC communication stack, chip regions areas each other connected in circuit. A resource in microprocessor, memory, I/O request, ISO /OSI layer model and network services.

NoC based on packet communication, reliable distributed transmission from higher layers to lower layers of abstractions a multi-process chip has hundreds of thousands of cores (ie. Multi-core) has high performance. The traditional systems interconnection with bus interface where network on chip (NoC), communication, architecture, design solve the issues and improve performance, power consumption, scalability, and integrity. The computation time is dominated by gate delay, computer, and unit on ad-hoc basis. The Transistors gates has wire delay. Scalable, structures architecture on-chip is more important design-centric communication design. The Moore's law used in SoC, Chip core chip processing design, the processor is making with hardware designing use application tasks multiple processing elements On /off to save power. Each processing element is optimized to frequency and voltage. And use of load balancing, reliable methods algorithms used for improving performance.

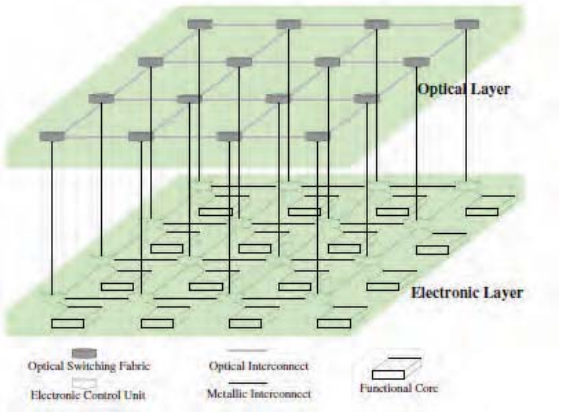

Figure 2. 4X4 mesh-based 3 D optical NoC architecture

The SoC chip designer is a complex application. The communication interconnection with the backbone of the network. The SoC designer uses communication devices that are connected to the backbone of the network which consists of layers, physical interfaces, protocols. The Protocols are used in data transmission, where the network layer routes the Packets from source to destination in a physical path. The routing is forwarded on a per-hop basis, set up optical path, control packets, routing, source-target address etc., The high speed without buffering, is obtained using NoC mesh-based design. Implement physical design is used to control the network Pins. The action of modules provides internal connections, components of SoC multimedia system provides more data transmission on-chip, multi-processor huge data on-chip where a Set of applications on-chip links to modules signals are carried out with global wires. The Architecture-based reusability, scalability for Multiple chip hierarchical processor has more cores on a single chip. SoC architecture has low latency, high throughput, reliable global services. The modern silicon devices shrink to 50 nanometers. For example, network topology 4X4 mesh 3 D optical architecture is shown in Figure.2. which has an optical layer and electronic layer.

NoC has regularity in higher-level abstraction which is like road system, or telephone network systems consisting of Computing module, Network switch, Network links. The network architecture with multiple cores is shown in Figure.3 the resources manager handles tasks.

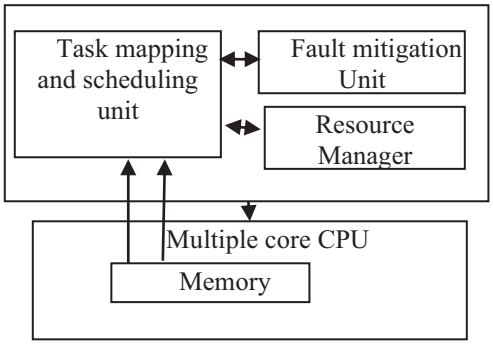

Figure 3. NoC architecture with multiple cores

NoC fundamental concept is a Module where communication packet of bits, point to point link in modules, and the modules are connecting with switch (or router) which sends the packets into several hops via using of switches, which is an efficient use of sharing wires to implement parallelism in communication. The NoC module communication is shown in figure.4. routing the packets through switch control.

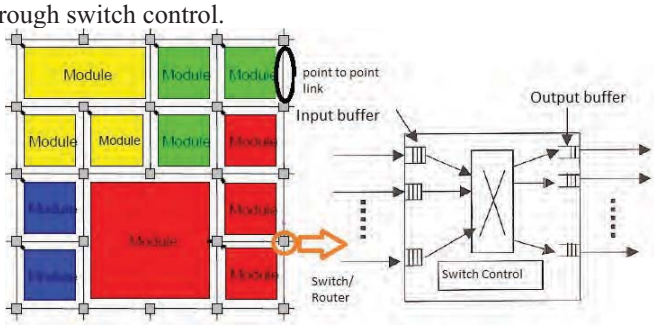

Figure 4. NoC module communication packets connecting to Router.

NoC architecture uses various topologies of interconnections for example bus, advanced bus and multilevel bus are discussed here. Bus Networks: The feature of bus has limited bandwidth, low cost, synchronous, central arbiter. The shared bus architecture is shown in figure.5.

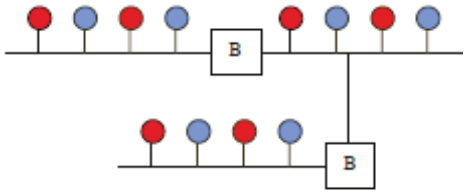

Figure 5. Shared Bus architecture.

Advanced Bus is a segmented One, transaction processed in central arbiter, where it uses limited bandwidth, transfer,

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pipelining features split transactions, with overlapped arbitration, transactions preemption, and resumption transaction reordering. The multilevel segmented bus is shown in figure.6

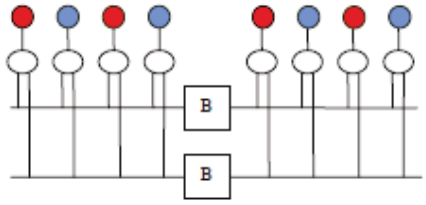

Figure 6. Multilevel segmented Bus

Paradigm architecture will replace with wire by a network to new infrastructure as shown in figure.7. The figure has network link, router link, computing module and bus, power grim clock grid are the components.

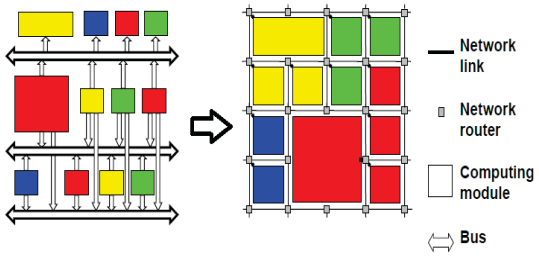

Figure 7. Paradigm the architecture with replacing with wire by packets new infrastructure

The problems are addressed by NoC Global design, system integration and chip multiprocessor with efficient computing. NoC scalability

TABLE I.
NETWORK ON-CHIP AND COST COMPLEXITY

Network on chip	Complexity
NoC	O(n)
Simple Bus	$O(n^3\sqrt{n})$
Point to point	$O(n^2\sqrt{n})$
Segmented Bus	$O(n^2\sqrt{n})$

Table.1 describes Network on chip design and cost complexity of NoC, Simple bus, point to point, and segmented bus and its architecture and cost complexities. NoC and Global wire delay: The wire design for NoC uses NoC links that connects regular, point to point, transmission path with layout and are optimized with power, speed, and noise.

The NoC and GALS system modules may use synchronization method, Asynchronous system has no waste of power in lines where routers are idle in the architecture Chip Multi-Processor (CMP), application-specific standard product (ASSP), application-specific integrated circuit (ASIC)), field-programmable gate arrays (FPGA), the choice depends on the system needs, single application, general-purpose application, configuration during run time, boot time and design time is shown in figure.8. The architecture is based on purpose of application, flexibility with required parameters.

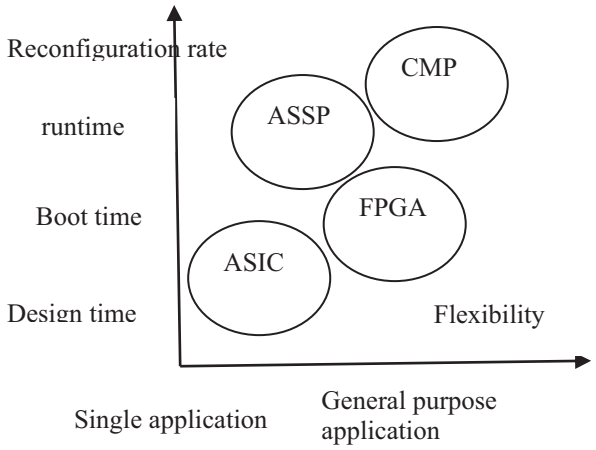

Figure 8. Architecture choice depends on system needs (Ref.12)

Chip multiprocessor (CMP) is a logic design architecture that has multiple processing (i.e., CPU cores) that are integrated onto a single Integrated Circuit. MP figure is shown in figure 9. Single, shared and I/O interfaces.

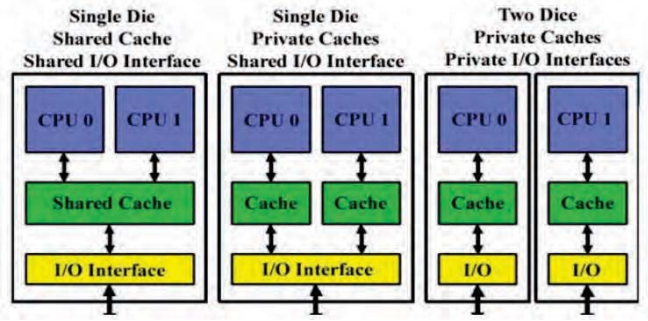

Figure 9. CMP chip Multiprocessor

The application-specific Integrated Circuits can be into three types namely 1) Standard IC 2) ASSP and 3) ASIC
The ASIC figure is shown in figure. 10. ASSP (application-specific standard product) is a product that has a semiconductor device with an integrated circuit. It is used for specific applications in the market. ASIC design built by the specific company.

ASIC design methodology can be designed into full custom design that is extremely slow and expensive. FPGA design is cost effective and fast. The AISC has improved performance with use of mix of analog to digital design, IC, HDL, the limitations are it cannot be upgraded, redesign is complex and expensive.

FPGA is IC programming gateway using semiconductor devices. It is used in application desired functionality requirement after manufacturing. FPGA are available, devices, software, configurable, ready to use IP cores in the market, for example, Defense and aerospace, ASIC prototyping, used in embedded software, SoC systems and in medical, industrial, automotive, broadcast, and consumer electronics applications.

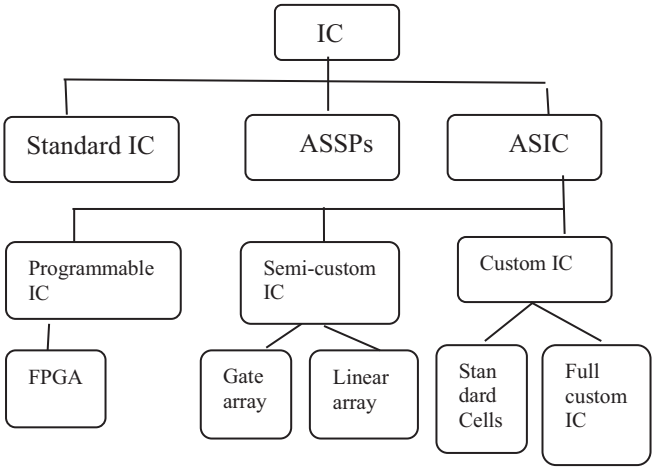

Figure 10. Application-specific Integrated Circuits (ASIC)

Choice of topology can be tree, tours, mesh, ring, bus, star, BFT, Spin, Interconnection. Simple mesh fits planar chip, short links routing, switching, blocking, delay, load, quality of service. NoC aggregate Bandwidth growth, link speed, current spatial reuse, pipelining, distributed arbitration, and separated abstraction layers. sensitivity area of the parameters for example traffic, wires, cost also plays significant role in designing time specialization for custom NoC system.

Bus is off-chip network where the bandwidth is limited, shared, speed grows down if there are more connections, no concurrency, pipelining is difficult, no layer abstraction, cost of links, latency is tolerable, traffic is unknown, changes at run time, Adherence to network standards. To solve critical problems set up connection design we use new tools which minimize the complexity, and design productivity. VLSI problems are mapping application, routing, buffering, timing closure, simulation, and testing. VLSI problems are reframed to NoC application mapping (the task by cores), Placement/Floor planning (is within the network), message routing, buffer sizing (FIFO queue in router), Timing closure(Bandwidth link allocation capacity), simulation(Network simulation, delay/traffic/Modeling power)

Testing and combined problems in the design of NoC(with topology, switching, virtual channels, flow control, arbitration, etc.). Network on the chip is a microprocessor that enables the method to send/receive data in combination. Embedded FPGA interconnections are shown in the figure.11, it has embedded FPGA, input/output connected to Network interconnection, this connects to CPU of the systems and access the memory.

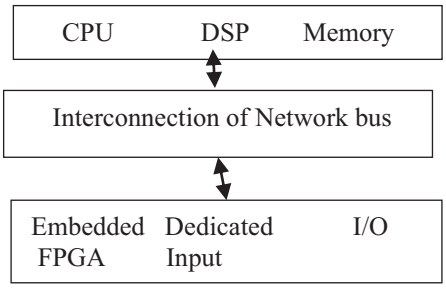

Figure 11. Embedded FPGA interconnection to components operations

Resources: Chip communications improves the bandwidth, power efficiency, and scalability. The optical NoC, Hybrid architecture are used in optical data transmission, it has high speed with distributed operations. The NoC architecture on three-dimensional (3DiC) improves performance by CMOS technology, which supports higher density with mixed chip design technology

The elements are used in NoC which is based on packet communication, interconnects to large IP cells, this can be used in SoC.

Network communicates with cells by clocks, domains, with minimum power, space, latency. NoC elastic protocol, which helps to generate topology, router. SoC design uses binary tree topology. The Process scaling, complex design, fits on System on Chip (SoC). Design is difficult due to multiple clocks, domains are increasing and integrated chip is used in design.

Network of Chip is communication point to point maintaining global clock. NoC design includes topology (star, mesh, etc.), Packet-switched or circuit switch parameters. The design of NoC, topology is mesh, star, tours, packet-switched or circuit-switched

NoC buffer uses optimized buffer size, length of the link, bandwidth NoC design uses Network topology, Heuristic algorithms, Linear programing, capability to topology design, router link, bandwidth, the sender sends the valid data, the receiver receives the data with Network components, Network based protocols, elastics system design with clock, communication channel and sender, receiver's module.

Network fabric work uses Network on Chip (NoC), design, Topology uses packet transmission in routing, throughput, router buffer with NoC fabric, the transmission of data by routing buffer, Network hardware and improves performance. The most important factors are network, topology, design, communication traffic, clocks, IP block, design, topology, router, high bandwidth, minimization function.

In Topology CTG design, each group data structure used is Graph Group where two groups joined by the router. Algorithm. 1 describes NoC topology a path of network routing.

Topology: T (V, E) v is vertices, in physical link E.Map the edge width. The path is critically weights with Network components, the methodology of repeated routing algorithms is used which is described in algorithm.2., Routing algorithm represented in algorithm.3.

CVR Journal of Science and Technology, Volume 22, June 2022
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Algorithm:1 NoC Topology a path of network routing

Begin
Step1. IP router Initialize T, V
Step2. while Vc two or more vertices
find the highest edge
Step3. Create a new router. Group to form new Vc
Step4. Combine both the edges
Step5.Remove route directly
End

The Network router step minimizes the latency in critical paths of communication. Use the directed method to determine router locations by router with path physical length.
Procedure repeated router is represented in algorithm.2.

Algorithm:2 Algorithm for repeated router

begin
Step1.For each edge find the path topology assign router for each router all vectors, move the router in direction.
Step2. Router R
R is sorted in descending area block. Move overlapping router block.
Step3. consider replacement of router on the overlapping block. Block overlapping routers each.
Step4. Move router IP block
Step5. For each router make a new router.
Step6. Find minimum distance move a neighbor while each step run the router if not allowed in the block areas top the edge
Step 7. return
end

NoC framework, bandwidth, pace linked, packet direction data, packets direction total capacity of the link, bandwidth will be considered with needed available systems.

Design SOC for Routing algorithms: The proposed router, Functionality, Module.

Algorithm:3 network routing algorithm FIFO

begin
Input data and output. FIFO flexibility.
Step1. Find the FIFO router to store the incoming packet. FIFO buffer.
Step2. Receive packets from input to output with use of Routing methods packet data with use of routers.
Step3. The operation of the router with FIFO request
Step4. Free slot request, find free hop
Step5. Packet transmission operation
Step6 If deadlock problem, Packet buffer direction, deadlock, avoid deadlock, where the router can store incoming packets,
Step7. Transmit the packets in a specified route.
end

The Communication and Programming model improves performance by Network operations and optimal network. System on chips (SoCs) complexity pushes researchers to come up with NoC bus architecture, the advantages are the scalability, performance, throughput, utilization, and power consumption. In NoC design the overall network design uses the availability of buffer, Virtual channels with power consumption. The NoC performance increase by use of the number of buffers, Router buffer in NoC. If Router increases by use of buffer size, then go for FIFO method and reduce the size of buffers.

The high-performance system increases buffering resources, increase buffer size, Number of VCs, by use of optimization methods. The router uses a large optimization size of the switch, buffer. The architecture use mesh topology, traffic conditions. Finally Analyze dynamic buffer resize with new technique, new router architecture, buffer structure, VC incoming traffic. Flexibility and buffer size. The new router architecture: Flexible router, Buffer, VCs, port. The Router architecture with Input controller, requests, transfer data. Input controller router grants and send internal request transfer packets.

Routing logic is packer director with FIFO, according to designation address the Arbiter receives all requests, grants according to pre specified logic. The router design shown in figure 12.

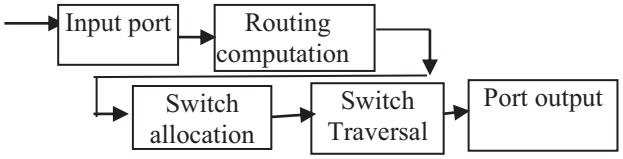

Figure 12. Flow control by Router

For example, Let us take input (N, S, W, PE) with the input port, the input is in the input buffer, the router accepts the input and allocates the channel to process and allocating packets switch and path to outport (N, SW, PE) flow control.

The flow control of networks which improves efficiency by allocation, buffer, packets, control networks and which ensure packet delivery, allocation of adjacent channels without buffer. Flow pipeline, routing, channel allocation, switch, switch traversal will improve the performance. Routing quality of design, reliability, failures, task processing, algorithms, and requirements to be considered based on the design (i.e., correctness, high performance, low hardware cost) etc. helps to improve performance.

IV. Discussions

SoC architecture uses technology and components, NoC address the features, several designs, System on chip(SoC), combine the elements in the chip. The VLSI projects are time to market, high complexity, high performance, Module use of cores, complexity reduced for current digital systems components in the product. The network techniques, VLSI implementation by high throughput with reduced complexity, routing algorithm, packet delivery, message passing, efficiency and the design Network on Chip architecture feasible by satisfying all requirements.2D, 3D meshes, applied SoC developments parameters.

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Computation is an intensive application requires high performance, low power, adding many computing resources, CIP, Ips, on System on chip, interconnection of resources, applications can use bus aces communication, control architecture, utilize efficient resources. The environment bus has large, bandwidth, interconnection. The network on chip architecture is the scalable support chip communication leads to NoC-based solution for many researchers, developers develop a model architecture, circuit-based architecture, on packet-based architecture using routing algorithms incoming outgoing data on control flow.

The figure. 13. The high-level view of Network on Chip architecture, networks with PES, IP, host, memory, and processor cores. The Good algorithms maintains network balancing, design cost.

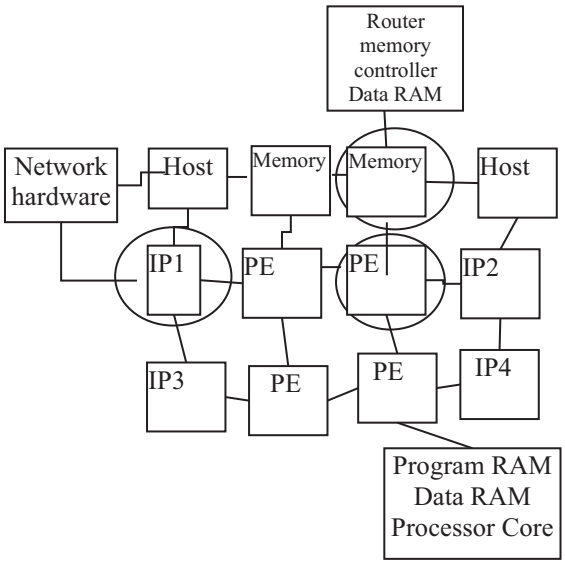

Figure 13. NoC Chip- High level view -Architecture.

The proposed NoC architecture figure14.has feasibility of hardware complexity, protocols, networks controller router capabilities. The cores of communication uses a packet-based network. The performance of system is based on multi-processor, memory modules, several IP-specific processing elements.

Router architecture: Network interconnection requires each PE, data communication, routing algorithm, Virtual channels, Router design, Physical channel, Routing algorithms. Packet is a collection of data received from the data link layer, the message is transmitted through the communication channel, router packet control, flexible for handling, designation of data.

Transfer the packets are flexible with multiple data, has better performance over single data transmission. Network simulation, packet generation traffic patterns using routing algorithm performance. Mesh topology, 8X8 each routing has better performance in each pattern, traffic pattern gives best performance with average latency. Protocol design, router FIFO per input port.

HAL is archive used in scientific documents are used in Hardware, software hybrid simulation technique for system model with chip Multiprocessor. It uses software-hardware interaction modules. Chip design and software with the use of hybrid software in host CPU.

NoC is a time-consuming, high-speed, reconfigurable resources that provides a degree of flexibility. In Hybrid design for hardware and software the resource interface, the performance of CPU improves by multicore architecture framework. CPU speed, NoC phase, design, flow, mesh network, NOC multiple routers, NoC module, the designers are with system software. Levels of the micro-architecture of CMPs Network on the chip has packet-switched, the router design uses Virtual channel flow control, communication access from CPUs cores, are transferred to all cores by local cache. chip memories, parameters, topology, data width, packet length, the latency of router, VC number, FIFO length. NoC module function call, hardware, software interfaces are used in the NoC simulation cycle. The NoC uses multiple nodes which allows communication mode all to all. communication interconnect, design, topology, in current design has required points.

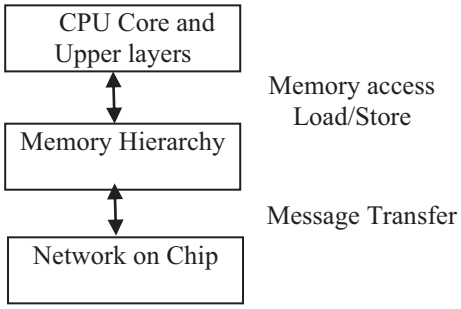

Figure 14. Levels of the micro-architecture of CMPs

The communication each direction which has a node using FIFO channel traffic with the router. Traffic Model, source-destination is with packet transmission. Latency, flow control on the router is controlled with buffer.

Timing model: Each FIFO has multiple channels (VCs), control number of VCs, design, each incoming, queue with internal timing, queue time stamping. The router module has flow control where each router connects to four channels of FIFO, traffic generator. Mesh topology, configuration Interface: Packet injection, which is packet control FIFO, access point, source designation, route the packets. The traffic generator, number of packets received through each route is used to analyze the spots, the clock signal with clock frequency to promote NOC stimulation cycle.

The Signal configuration simulation use of VC number, packet length fields and the Performance model with software, hardware. The NoC sequentially and it is widely used simulator and the simulation cycle is represented in the equation.1

$$simulation\ cycle = HTime + ETime + HStime \quad (1)$$

Where HTime is Hardware time, ETime is Elapsed time and HStime is hardware and software simulation time (interaction time)

The implantation of NoC emulator provides hardware and software interface, topology, mesh comparisons, running chip resources, on-chip resources, NoCscale. For example, 4X4 mesh, NoC, memory hierarchy level, functions, software processor on a chip, the memory space all cores, CPU core, memory access for reading/write from randomly. Memory hierarchy level with L2 cache, NoC design used in different configurations. Input design use target process, 16 core memory hierarchy. NoC computation, access trace CHIP trace for NoC.

V. Conclusions

NoC on chip integration of system components is based on requirement and application. The elements processing, memory, components, I/O, Processing Units, all involved in design, the complexity is minimized by use of software applications like AI, bigdata, and hardware components. NoC functional network architecture uses communication model for ISO/OSI reference model. For multicore systems used in handling tasks, the NoC architecture use various components and network elements, topologies, routing, and other elements. Integrated Chip can be classified into three major categories namely Standard IC, Application specific Standard Product (ASSP), and Application specific Integrated Circuit (ASIC). NoC design combine the Hardware elements such as embedded components, elements, and application software. The high-level micro architecture uses CMPS, CPU cores, and configurations channels, and software applications. In Future we can implement the SOC – Network on Chip for design and develop application-specific standard components in Network on chips.

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