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Comparative Studies on Different Radiation Hardened by Design (RHBD) Memory Cells

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Abstract: **Electronic components and circuits, when they are working in radiation environment undergo radiation impact like Single Event Effects (SEE), Displacement Damage, Total Ionization Dose etc., These effects are mainly caused by deposition of Ionization energy in target material i.e., electronic components and circuits. These effects lead to wrong operation of circuit or may even lead to damage of the circuit. This paper mainly concentrates on Single Event Effects and in these effects, this paper focuses on Single Event Upset (SEU) and Multiple Bit Upset (MBU) phenomenon. Radiation Hardened by Design (RHBD) is a design technique used to design different RHBD memory cells to avoid SEU and MBU. RHBD is a design technique where the number of transistors of the design are increased and arranged in such a way that they avoid these effects by design itself. These different memory cells are designed and simulated using Cadence Virtuoso and Cadence Spectre in 45nm technology. The power, noise, delay analysis of different memory cells is done, and failure rate is calculated using Monte Carlo Simulation. The layouts of different memory cells are drawn using Microwind 3.5 tool. The results of different memory cells are compared.**

Index Terms: **Single Event Effects (SEE), Radiation Hardened by Design (RHBD), Single Event Upset (SEU), Multiple Bit Upset (MBU).**

I. Introduction

The presence of ionization radiation may affect the correct operation of electronic devices [1], both in the Terrestrial environment and Artificial man-made environment. Due to atmospheric neutrons and radioactive essentials inside the chip ingredients or in space, the surrounded particles, which have been released by the Sun and galactic cosmic rays in the terrestrial environment. In Artificial man-made environment, the radiation produced by biomedical devices, nuclear power plants and research on high energy physics, are the causes for radiation effect in electronic devices. The basic aim beyond radiation effect in electronic devices is to deposit energy in the target material. This may lead to different variety of effects like corruption of memory bits, glitches in analog and digital circuits etc., This may increase power and decrease in speed, and in some cases, the complete process of a device may change. The radiation effects mainly occur while scheming electronic systems that operate onboard satellites and spacecrafts. These also occur in high reliable schemes to be used in ground like bank servers, biomedical devices, and automotive machines. In Nuclear environments, like in areas around Nuclear Reactors and Nuclear projects, radiation effects are seen. There are three key classes of radiation effects:

1. Total Ionizing Dose,
2. Displacement Damage, and
3. Single Event Effects.

The first two effects in electronic device parameters are due to deficiency of semiconductor resources which are uninterruptedly hit by many ionizing elements. These mainly happen in space environments and artificial foundations of radiation. The Single event effects are mostly due to stochastic communication of a single ionized particle having high radiation with sensitive regions of the target electronic device. These events happen both in space and terrestrial environments.

There are different types of Single event effects, but this paper mainly focuses on the problem of Single Event Upset and Multiple Bit Upset.

Single Event Upset (SEU): This is corruption of a single bit, due to single ionizing particle in sensitive nodes of a memory cell. It is also known as soft error. The correct logic value can be usually reestablished by simply rewriting the bit.

Multiple Bit Upset (MBU): Corruption of two or more bits due to the passage of a single Ionizing particle. Here, 2 states will change due to radiation effects.

SRAMs carefully follow Moore's law and have developed the perfect standard to study the soft error sensitivity of a technology. In general, the charge formed by an ionizing particle is composed together at a sensitive region of a circuit to yield a trouble. Reverse biased p-n junctions are among the most effective areas in assembling charge. An ionizing component outbreaks one of the reverse biased drain junctions, like the drain of NMOSFET which is off, in the cross coupled inverter in the cell. Consequently, electron-hole pairs are shaped and composed by the depletion region of the drain junction. This causes a transient current, which follows through the junction that is hit while reestablishing transistor source current to the particle induced current. The reestablishing PMOS has a partial amount of current drive and a partial channel conductance, voltage drops at the hit node. If the voltage goes below the switching threshold and the drop lasts for a sufficient time, the response causes the cell to alter its initial logic state, creating a SEU. In the same way if it alters two or more bits due to ionizing particle, it causes MBU. Several features regulate the presence of SEU: radiation transfer through the bank end layers past the reverse biased junction, charge deposition and charge collection. In addition, the circuit response is also of importance.

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II. Literature Review

I.-S. Jung, Y.-B. Kim, and F. Lombardi [2] have proposed two types of 10T SRAM cells that avoid soft errors by using Cadence Virtuoso 180nm technology. But it has high read Signal Noise Margin (SNM). This is the main problem with the design, and it needs two cells to avoid soft errors. S.M. Heinzman , D. J. Rennie, and M. Sachdev [3] projected a quad-node 10T soft error strong SRAM cell that offers differential read process for strong identifying. When associated to a basic 6T SRAM cell, the anticipated cell offers similar noise margin as the 6T cell at the half supply voltage, thus it is positively saving the leakage power. This cell is used as latch to design register files and flipflops. But it cannot avoid soft errors, while working in pure radiation environments. S. Lin, Y.B. Kim, and F. Lombardi [4] proposed a new hardening design of 11 transistor CMOS memory cell. By employing creative access and new mechanisms, the predicted toughened memory cell solves the issues that plagued the previous design. The data stored in the projected hardened memory cell does not change even when subjected to a transient pulse, according to the simulation of the anticipated cell. It costs more than twice as much of a basic memory cell. But this cell consumes high noise margin and speed is low. T. Calin, M. Nicolaids and R. Velazco [5] anticipated a new design strategy for storage which is immune to single event radiation disruptions. This approach is excellent for spreading high density ASICs and static RAMs, which uses submicron CMOS technology. The storage component uses 10 transistors for a simple latch arrangement and 12 transistors for a memory cell building. The problem with this design is, we need to design latch and a memory. S. Gupta, K. Gupta and N. Pandey anticipated the 7T cell with a noise margin free read process that as formerly been anticipated. The new mechanism also aids to decrease power alimentation by reaching a lower data holding voltage idea. A read aid has been anticipated to pointedly increase the act of the read process in subthreshold region. But the write operation capability is very low in it. CH Naga Raghuram, Bharat Gupta and Gaurav Kaushal [7] to reject the SEU and Sing le Event Double Node Upset, have projected a new Radiation Hardened by Design (RHBD) SRAM. The failure probability of SRAM cells is calculated using Monte Carlo Simulations. The predictable RHBD 15T SRAM achieved a zero percent failure chance for the specified charge source when attached to the newly labeled RHBD SRAM cells. The intended SRAM cell's read and write presentations are improved by using separate read and write circuitry at dissimilar nodes. The read, write, and power indulging delays are all reduced. However, they currently use separate circuitry for the read and write processes.

III. Design of Different SRAM Cells and SEU Recovery Analysis

A. Basic 6T SRAM Cell

The Basic 6T SRAM cell shown in figure 1, consists of 6 transistors. Out of these 6, 4 are NMOS and 2 are PMOS transistors [8]. The transistor N2, N4 are access transistors. For these two transistors gate is connected to WL which is high, then only read and write operation will occur. The bit lines BL that are connected to N2 and N4. The Q and Q| are output nodes. The read and write operation are same as 6T SRAM cell. When WL is low, it will be in hold operation and keeps its previous values. But problem with this cell is, it is easily affected by radiation and can change its operation or may be affected by SEU and MBU.

The cell can be easily affected by radiation when it is working in radiation environments and cause SEU and MBU. In order to avoid SEU and MBU, one needs to increase number of transistors or using a technique called RHBD. Using this technique different cells are designed. The figure 6 is the simulation of 6T cell and figure 12 is layout of 6T cell.

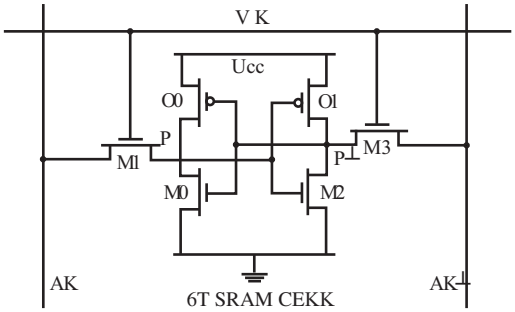

Figure 1. Basic 6T SRAM Cell

B. 10T SRAM CELL

The 10T SRAM cell shown in figure 2 is designed by using RHBD approach to keep away from radiation impacts like SEU and MBU [9]. This cell includes 10 transistors in which 6 are PMOS and 4 are NMOS transistors. The transistors N4 and N3 are access transistors and for these transistors, gate is hooked up to WL. When WL becomes high, both read and write operations will occur. The operation is same as the basic 6T SRAM cell, but it has additional two storage nodes Q, QN, S0, S1. The figure 7 is the simulation of 10T cell and figure 13 is the layout of 10T cell.

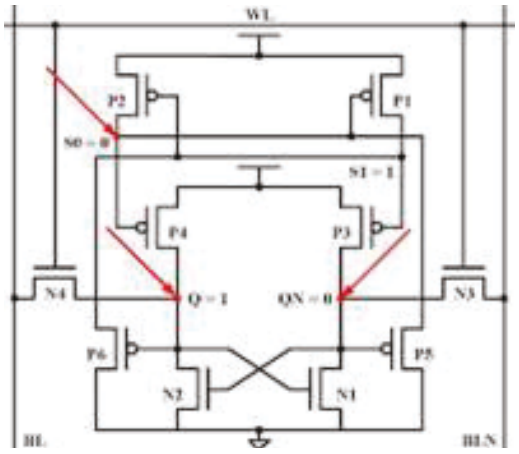

Figure 2. 10T SRAM Cell

The 10T SRAM cell shown in figure 2, is designed by using the RHBD approach to keep away from radiation impacts like SEU and MBU [9]. This cell includes 10 transistors in which 6 are PMOS and 4 are NMOS transistors. The transistors N4 and N3 are access transistors

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and for these transistors gate is hooked up to WL. When WL becomes high, both read and write operations will occur. The operation is same as the basic 6T SRAM cell, but it has additional two storage nodes Q, QN, S0, S1. The figure 7 is the simulation of 10T cell and figure 13 is the layout of 10T cell.

In the SEU recovery analysis of 10T cell, consider following scenario. Nodes Q, QN and S0 are three sensitive nodes in the 10T cell for the reserved value as 1, according to the SEU concept. If a charged element upturns the sensitive node Q to 0, transistor N1 will be tentatively OFF, and transistor P6 will be tentatively ON. However, the size of transistor P1 is 2 times that of P6, the voltage at node S1 will be in its exclusive state. Here to avoid the change of S1 state the transistor size P1 is made twice that of P6. The voltage of node S0 remains unaltered, which is significant. As a result, transistor P4 will turn on, in sequence. Finally, the voltage of the node Q will be compared to the early voltage. Both transistors P1 and P4 will be twisted OFF if the sensitive node S0 is concerned about a radiation element changing the original state. Due to capacitive effect, nodes Q, QN and S1 will be unaffected. As a result, transistor P5 will turn on in sequence, and the voltage at node S0 will be restored.

C. 12T SRAM Cell

The 12T SRAM cell shown in figure 3 is designed by using RHBD technique to avoid radiation affects like SEU and MBU. This cell consists of 12 transistors among which 8 are PMOS and 4 are NMOS. P5, P6 are access transistors and these transistors gate is connected to WL. When WL is low, read and write operations only will take place and the read and write operation is as that of basic 6T SRAM cell. When WL is high, the cell will be in hold operation and holds its previous values. It has four storage nodes Q, QN, S0, S1. Figure 8 shows the simulation of 12T cell and figure 14 shows layout of 12T cell.

In SEU recovery analysis, the drain region of the PMOS transistors P6 and P8, node Q is not a sensitive node and its holding value is 1. Q is a node that exclusively attracts positive pulses. In other words, the 1->1 pulse is utilized to extend Q node while maintaining its retained value. When the QN node is disrupted by the radiation component, the transistors P1 and P4 are turned off. The nodes Q and S1 then remain in a single logic state 1, with no voltage value at the end. As a result, N3 remains on. S0 is in the 0 state, transistors P7 and P2 are switched on, and QN returns to its original 0 state.

The voltage at nodes S0-QN or S1-QN can be restored due to the charge sharing effect. The dumping state of the 12T cell will change because, both P8 and N4 transistors will be replaced. As a result, the node Q will be stressed to state 0. This is like a write 0 process. When a radiation element damages node S0 or S1 or QN or node pair S0-S1 of the predicted 12T cell, damaged data can be amplified from the deposited data which cannot be improved when node pair S0-QN or S1-Qn is distressed. The capabilities of these multiple node upsets scenario can be condensed if the predetermination of the node QN and node pair S0-S1 is excessive enough.

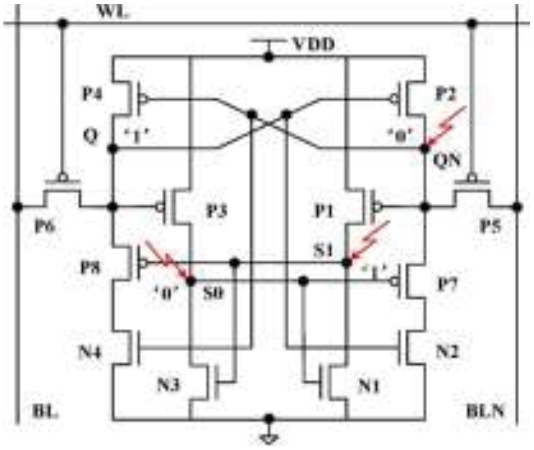

Figure 3. 12T SRAM Cell

D. 14T SRAM Cell

The 14T SRAM cell is shown in figure 4. It is designed by using RHBD technique to avoid radiation affects like SEU and MBU [11]. This cell consists of 14 transistors among which 8 are PMOS and 6 are NMOS. N4 and N5 are access transistors, and these transistor gates are connected to WL. When WL is high, both read and write operation will occur. When WL is low, the cell is in hold its operation and it holds its previous values. The 14T SRAM cell operation is as basic 6T SRAM cell operation. It has 4 storage nodes Q, QB, S0, S1. Figure 9 shows simulation of 14T cell and figure 15 shows layout of 14T cell.

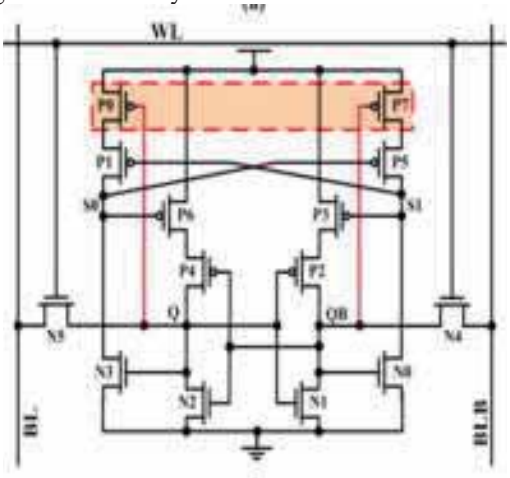

Figure 4. 14T SRAM Cell

Let the stored value be Q=1, QB=0, S1=1, S0=0 and the SEU recovery analysis for 14T cell is done for the same value. when an element hits the drain of P1, it accumulates a positive charge and raises the voltage of node S0, converting S0 from 0 to 1.P6 and P5 will be warped off because of this. However, impact of OFF/On states of extra auxiliary transistors nor it will affect the memory status of the Q and S1 nodes. As a result, the S0 switching pulse cannot be saturated within the cell. After the radiation effect the nodal logic level will be improved. When an element hits the drain of P2, it collects positive charge and raises the voltage at node QB, causing QB to change from 0 to 1. N2 and N0 will be turned on because of this, Q and S1 will be changed from 1 to 0. P0 and P1 will be warped on, and N3 will be OFF, before S0 is changed from 0 to 1. In the end, the storage

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state of the cell will be switched. The parasitic bipolar amplification result of P2 is calmed as the transistors are loaded and the topology is improved. As a result, the quantity of charge gathered by transistor P2 drain is condensed, increasing node QBs SEU tolerance.

E. 16T SRAM Cell

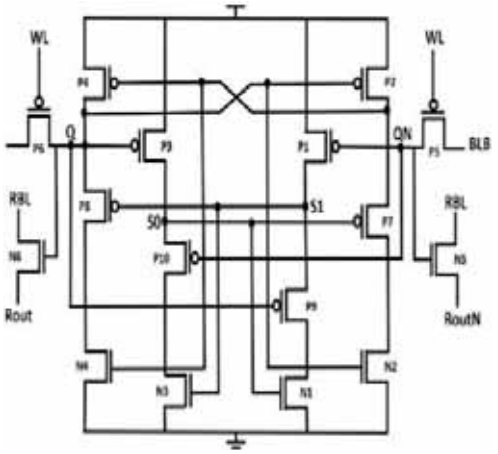

Figure 5. 16T SRAM Cell

The 16T SRAM cell is shown in figure 5 and designed by using RHBD technique to avoid radiation affects like SEU and MBU. This cell consists of 16 transistors among which 10 are PMOS and 6 are NMOS. Here in this P5, P6 are access transistors and the gates of these two transistors are connected to WL. When WL is low both read and write operation will occur. Here for write operation is as basic 6T SRAM cell but for read operation two transistors N5 and N6 are used and the gate of these two transistors is connected to storage nodes Q and QN. While read operation RBL is made high and through Rout and RoutN the value written in cell is read. When WL is high the cell is in hold operation and holds its previous values. Figure 10 and 11 shows the write and read simulation and figure 16 shows layout of 16T cell.

Single node and multi-node upset analysis of the projected RHBD 16T SRAM are reflected as explained below. Two primary and secondary networks are enclosed with PMOS devices. Consequently, only positive transient current has been shaped. So, 0 to 1 upset will happen, but not 1 to 0. Q is the primary linking where 1 is reserved and if component attack happens, only 1 to 1 upset will occur and RHBD 16T SRAM have four storage connections. Eight groups of multi-node upset are likely imaginable. When joining it QN is upset will alter into OFF state. But on the extra side, networks S1 and Q last the same, because P9 and P8 are swapped OFF. So, N3 will be in ON state. P7 and N2 are likewise On, at the same time. QN is pulled back to unique value 0. When connection S0 is inflated by a radiation attack, it will alter ON the device N1 and alter OFF the P7 transistor. But, P9 is swapped OFF, and the S1 value will not alter. P10 and N3 are swapped ON. So, S0 will pull back its original value of 0.

When networks QN and S1 are inflated by radiation elements i.e., 1 to 0 upset will not happen to junction S1. So, the model of the attack is done on P9 and N1 among P9 and N1. Since P9 is in OFF state, it will interrupt the S1 linking. And, as explained before, for QN single node upset, QN linking will drag back to the original value of 0. When S0 and S1 are inflated by element attack, S0 outbreaks will change ON N1 and change OFF P7 transistor. But Q and QN are in its original value P9 and P10 do not modify its state. Finally, also for the extreme group of multi-node upsets, RHBD 16T can advance the dropped data from the corrupted one. When joining pair QN-S0 is upset, the stored data can alter, because PMOS is used among all four inverters, and it takes gate inputs from the storage networks.

IV. Results and Discussion

A. Simulation results of different SRAM cells

The Simulation results of different cells are shown in figures 6,7,8,9,10 and 11.

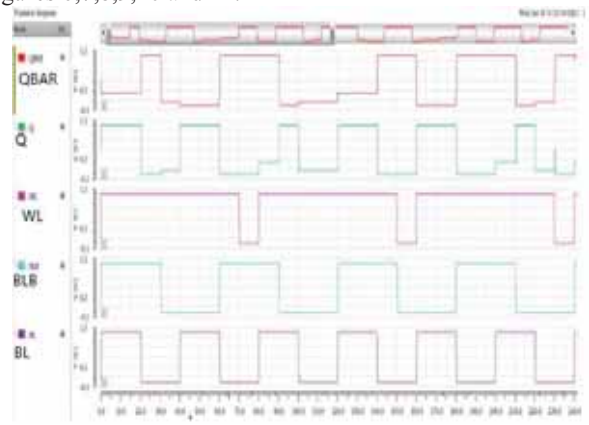

Figure 6. Simulation result of 6T SRAM Cell

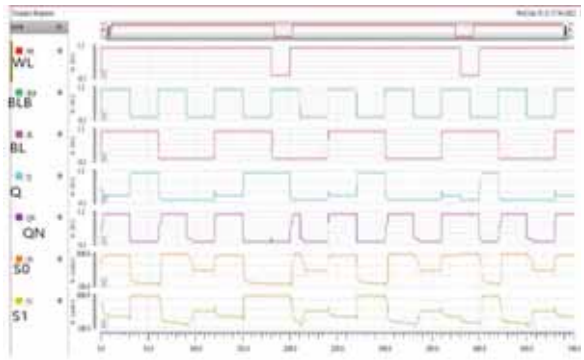

Figure 7. Simulation result of 10T SRAM cell

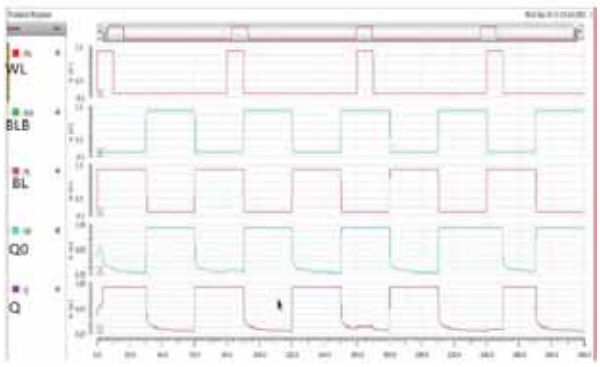

Figure 8. Simulation result of 12T SRAM cell

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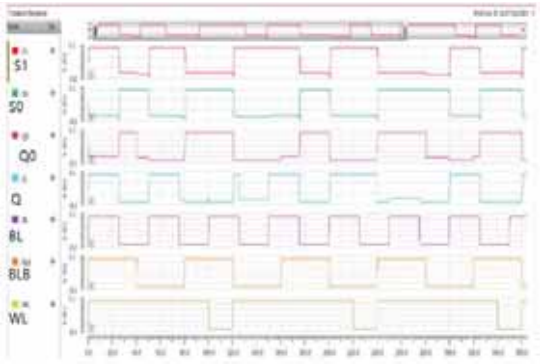

Figure 9. Simulation result of 14T SRAM cell

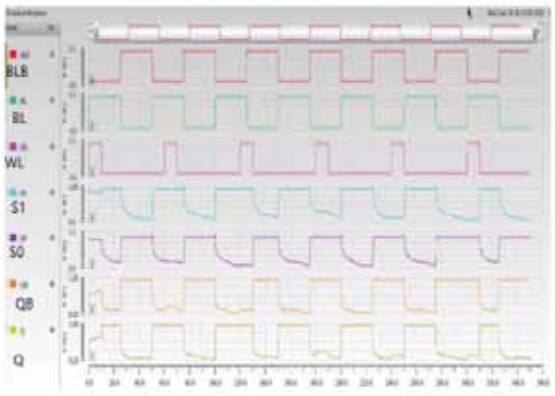

Figure 10. Simulation result of write operation of 16T SRAM cell

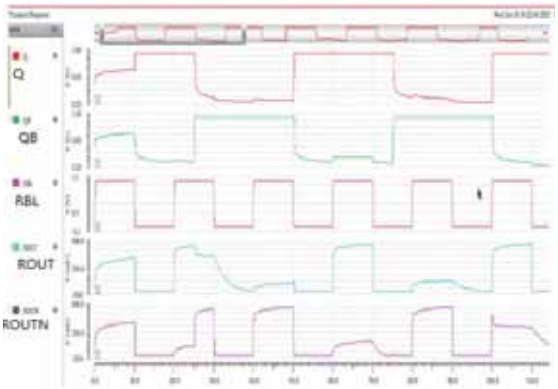

Figure 11. Simulation result of read operation of 16T SRAM cell

B. Noise Analysis

TABLE I.

Memory cell	Noise(mv)
6T	7.811399×10^{-2}
10T	1.813065×10^{-2}
12T	8.91399×10^{-2}
14T	4.26487×10^{-2}
16T	2.203408×10^{-2}

C. Power Analysis

TABLE II.

Memory Cell	Power(nw)
6T	17.47
10T	24.32
12T	33.42
14T	12.21
16T	14.13

D. Delay Analysis

TABLE III.

Memory Cell	Delay(ps)
6T	96.14
10T	30.71
12T	62.48
14T	20.3
16T	7.01

E. Monte Carlo Simulation

TABLE IV.

Memory Cell	Failure Rate
6T	92%
10T	71%
12T	88%
14T	72%
16T	11%

The monte carlo simulation is done to check whether the designed cells will sustain in radiation environment or not. Here 30fc charge is introduced in sensitive nodes of these cells using monte carlo simulation and failure rate is calculated.

The above tables are the results of different analysis like Noise, Power, Delay, and failure rate using Monte carlo Simulation of different SRAM Cells. From noise analysis both 10T and 16T have less noise. In power analysis 14T and 16T cells consumes less power. From delay analysis 16T cell has less delay and from monte carlo simulation 16T cell has less failure rate.

F. Layout Design of different cells

The layout of different memory cells is drawn using Microwind 3.5 Tool and shown in figures 12,13,14,15 and 16.

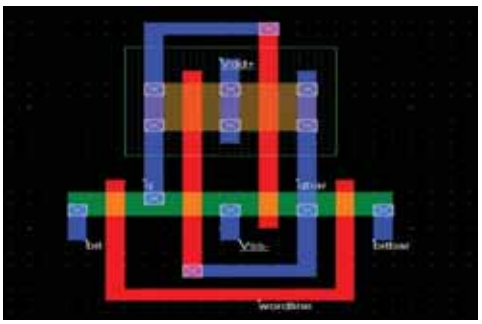

Figure 12. Layout Design of basic 6T cell

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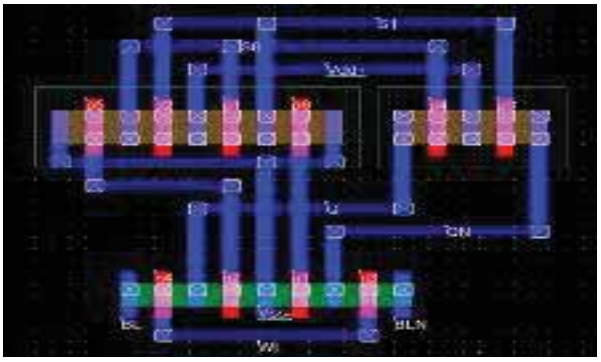

Figure 13. Layout Design od 10T cell

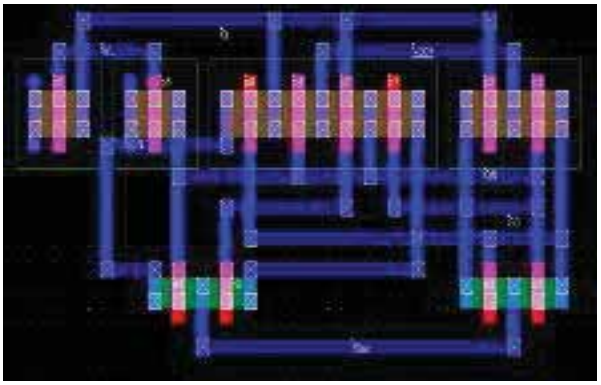

Figure 14. Layout Design of 12T cell

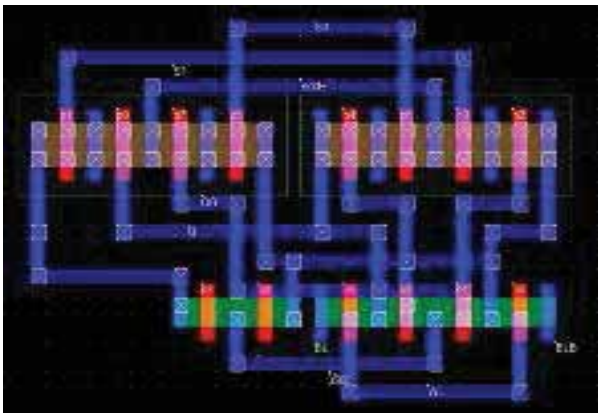

Figure 15. Layout Design of 14T cell

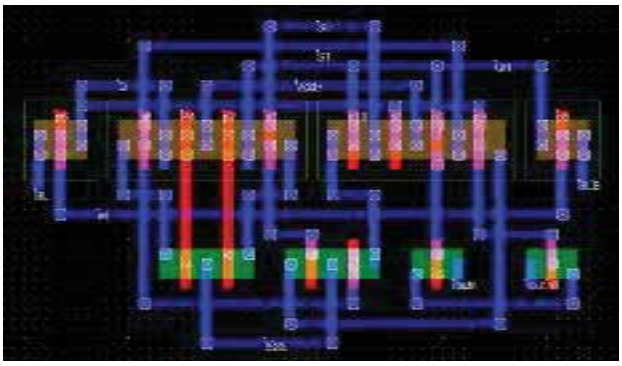

Figure 16. Layout Design of 16T cell

Here, the layout of different cells is drawn for reference to foresee any problems that arise during designing. Compared to all cells 16T memory cell can avoid both SEU and MBU. The 16T cell has less noise, power, delay and its failure rate is very less, when compared to the remaining cells. This cell consumes less power, because the storage junctions are separated by a PMOS device between the inverters. So, when working in radiation environments 16T cell is better compared to other cells.

V. Conclusions

In this work, different cells are designed using RHBD design technique to avoid SEU and MBU by design itself, using Cadence Virtuoso 45nm technology. Basic 6T SRAM cell is simple, but it cannot work properly in radiation environments. 10T cell is designed using RHBD technique. In this cell noise is less but it can avoid only SEU. 12T cell is also designed using RHBD technique. It can avoid both SEU and MBU, but its noise, power, delay, and failure rate are more. 14T cell is also designed using same RHBD technique where one can achieve less power and delay. But it cannot avoid MBU. Lastly, a 16T cell is designed using same RHBD technique. This can avoid both SEU and MBU and its power, noise, delay, and failure rate are very less compared to remaining cells. So, the 16T cell is better for use, when working in radiation environments.

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