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Implementation of Optimized FIR Filter using Reversible Logic

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Abstract: **The Finite Impulse Response (FIR) filter is extensively used in mobile and wireless applications. Low power and low complexity FIR filters architectures are essential to implement these applications. For signal processing applications, FIR Filter is the most frequently used hardware block. The performance enhancement in the FIR filter is a great challenge. In this paper, two different but effectual methods have been implemented in Xilinx software to improve the performance metrics in terms of speed, area and power.**

The first FIR filter is implemented using a normal architecture. The second type of FIR filter is based on Pipelined Technique. In this technique, throughput is enhanced by utilizing the retiming effectively. Due to this performance also increases gradually. Implementing the FIR Filter using Reversible Vedic Multiplier with both adders i.e. Reversible Carry Look Ahead Adder and Reversible Carry Select Adder can optimize the performance in terms of Power, Delay and utilization. The proposed architecture is implemented using IP Integrator in Xilinx Vivado by utilizing the ZYNQ Zed Board which can be used for DSP Applications.

Index Terms: **Carry Look Ahead Adder, Carry Select Adder, FIR Filters, Pipelining, Reversible Logic and Vedic Design**

I. Introduction

FIR filters typically utilized in various applications like biomedical, communications and control because of their stability and linear phase properties. FIR filters have simple and regular structures in correlation with IIR filters which are easy to implement on hardware.

A digital filter is programmable, i.e. a function stored within the processor's memory determines its operation compared to analog filter. The analog filter features are temperature dependent and focus on drift. These problems are not faced by digital Filters, and they are highly stable both in time and temperature.

A Filter is also used to get the filter output with a chain of delays, multipliers, and adders. FIR Filter functions are based on existing and former values of input.

In CMOS VLSI design, Power optimization is often done at various abstraction levels. In 1973, C. H. Bennett concluded that "no energy would be dissipated from a system as long because the system was ready to return to its initial state from its final state no matter what occurred in between." It made us understand that, a reversible gate can shrink power dissipation.

In Reversible logic, system drives in both forward and backward which causes input from output and vice versa. It can recess the process at any stage and return to any point in computation history. There is individual mapping among the input and output signals due to same number of inputs and outputs

Reduction of heat generation and power loss will be attained by decreasing the garbage outputs and constant inputs which upsurges overall circuit performance by using individual inputs and outputs [1].

II. Reversible Gates

A. Introduction

In VLSI parameters like area, speed and power play a vital role as per the emerging technology. By utilizing reversible logic gates having equal number of inputs and outputs can shrink the power consumption and energy leakage which made feedback unessential in the circuit. Due to irreversible gates, the energy carried by the source is altered into heat with every single bit of loss [1].

B. Cost Metrics of Reversible Logic Gates:

1. **Gate Cost:** It indicates the essential number of gates to analyze the cost of a circuit.
2. **Quantum Cost:** It is the accumulation of elementary quantum gates of the circuit.
3. **Ancilla Input:** Transformation of reversible circuit from an irreversible circuit using essential additional inputs are denoted as Ancilla inputs (AI).
4. **Input:** The number of input or wires (n) including ancillary input will assist to estimate design methodology performance.
5. **Garbage Output:** Reversibility of the circuit can be maintained by placing avoidable outputs of the entire circuit into a single output which could be left unused.

The above factors illustrate a straight connection with the area/size and complexity of the circuit which enhances the power dissipation and physical cost [1].

C. Types of Reversible Logic Gates:

Various Reversible gates exist at present. Some of the reversible logic gates are shown below that are used in the proposed design:

a. *Feynman gate*: 2X2 Feynman Gate mainly utilized for fan-out purposes. It achieves complementing and XOR operations are shown in fig 1(a). It is also called a CNOT gate. Quantum cost of this gate is 1.

b. *Peres gate*: It is a 3*3 reversible gate i.e., it has three inputs and outputs. The depiction of Peres gate is shown in fig 1(b). Quantum cost is 4.

c. *Fredkin gate*: It is a 3*3 reversible gate i.e., it has three inputs and three outputs. The depiction of the Fredkin gate is shown in fig 1(c). Quantum cost is 5. Fredkin gate can be designed as Multiplexer.

d. *BME gate*: It is a 4*4 reversible gate i.e., it has four inputs and four outputs. The depiction of BME gate is shown in fig 1(d). The quantum cost is 5[2].

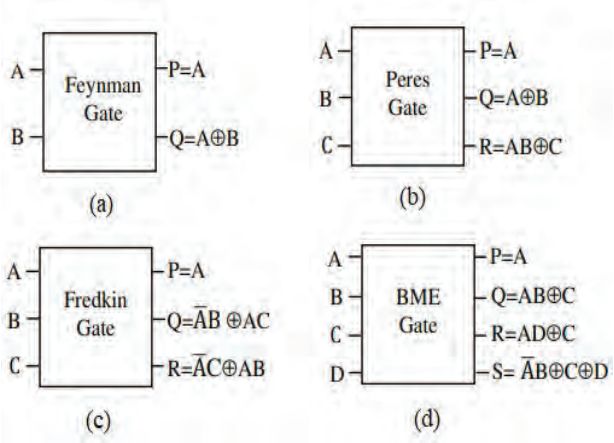

Figure 1. Reversible Gates

III. FIR Filter

The objective of a FIR filter is to realize the coefficients and filter order that match certain necessities. Computation of discrete convolutions i.e. input signal with a known signal is termed as FIR Convolution.

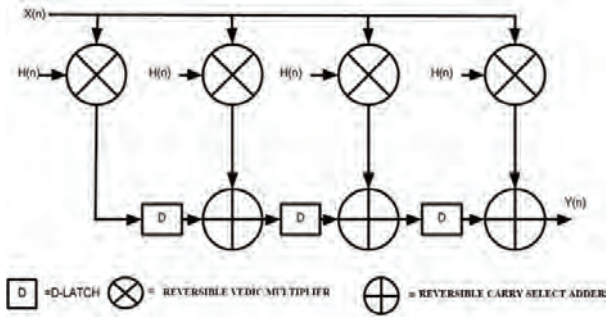

Figure 2 . Reversible FIR Filter

In Direct form FIR filter, length of critical path upsurges with increase in length of filter. The pipelining and parallel processing application will attain growth in input data processing rate or throughput and critical path reduction.

Therefore, it would be more efficient to introduce pipeline filters which improve power and critical path delay along with high throughput than standard filters.

The proposed filter 1 access carry look-ahead adder and proposed filter 2 access carry select adder with carry look-ahead adder for all additions [3].

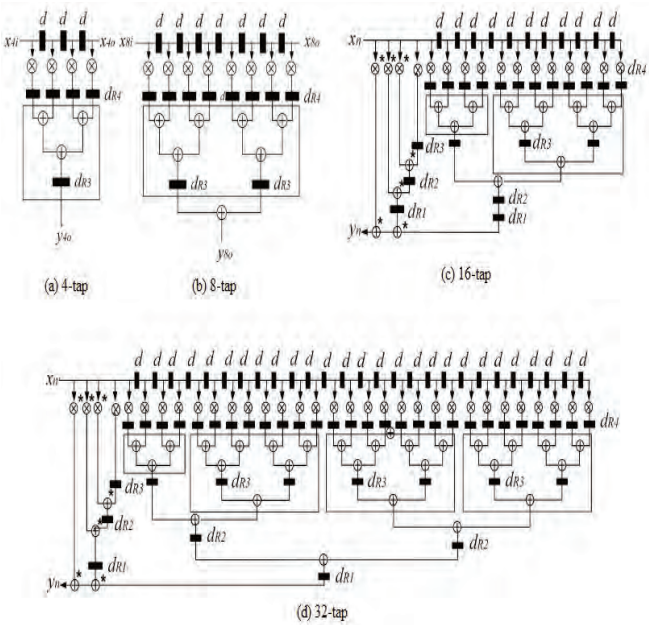

Figure 3. Pipelined FIR Filter

IV. Vedic Multiplier and Adder

In reversible VM, the BME gate and the Peres gate in Fig.4 are substituted with the AND gates and HA in Fig.3. The first BME gate pass in the number of p0, the multiplication of LSB x0 and y0. The two BME gates each have 2 garbage outputs. The inputs to the PERES gate are one of the outputs of both the BME gate and the sum s1, s2 and s3 are attained[4].

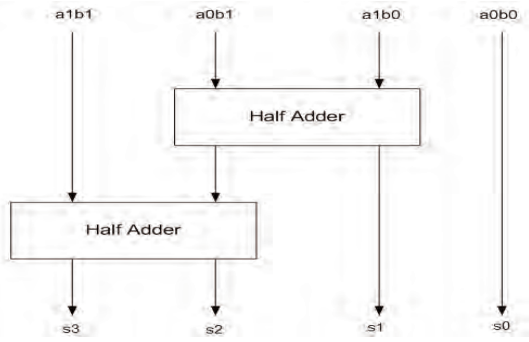

Figure 4. 2-bit Vedic Multiplier

Generating faster partial products can be accomplished using BME gate than the usual Vedic multiplier. In the existing architecture of Vedic multiplier using carry look ahead adder[5], OR gate was added to increase the accuracy and throughput of the output which was specified in below Fig6.

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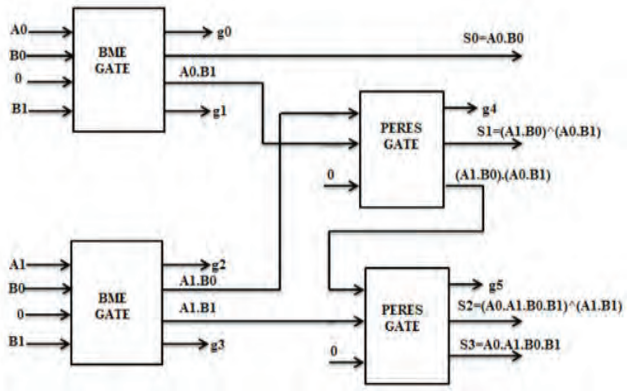

Figure 5 : Reversible Vedic Multiplier

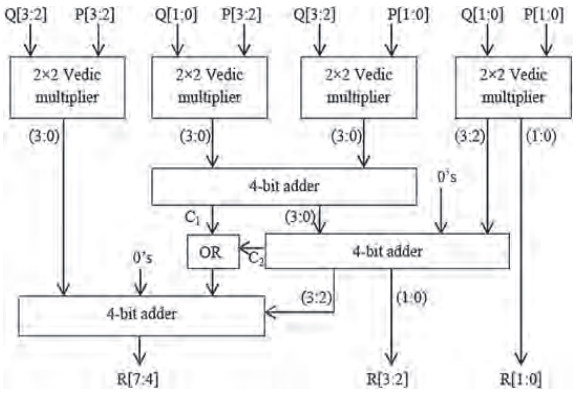

Figure 6. 4-bit Vedic Multiplier

The operation of the above Vedic multiplier is specified as follows. The delay would be reduced by the synchronized partial products measurement. Here, as shown in Fig.5, 4X4 Vedic multipliers can use 2X2Vedic multipliers for generation of partial product. For the partial product addition produced, three adders of 4 bits each are used.

The OR operation achieves the carry output of the first two Adders and its output is set to the next Adder. Where appropriate, zero inputs are pre-arranged for certain adders.

The next adder has two zero inputs along with carry acquired from the former adder. In the above block diagram, the Adders organization is seen, which will diminish the computational time so that the delay can be reduced. Process in Fig.6 for 8-bit VM. It's similar to the VM 4-bit [6].

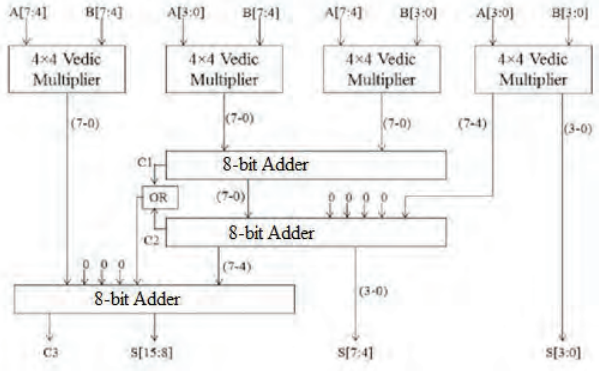

Figure 7. 8-bit Vedic Multiplier

Carry Look-ahead Adder is the fastest adder related to other Adders. It controls the propagation delay, which ascends through addition, by consuming more complex hardware circuitry. The Block diagram of 4-bit Carry Look-ahead Adder is as follows.

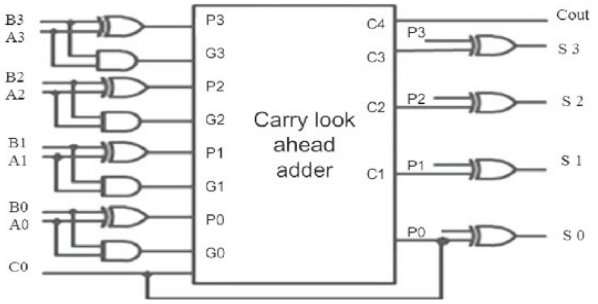

Figure 8. Block Diagram of 4-bit Carry Look-ahead Adder

Carry Look Ahead Adder is aimed for better output as shown in Fig.8 by using reversible gates, i.e., Peres gate for carry propagate, carry generate and sum and Feynman gate for carry. Parameters such as quantum cost, complexity of hardware and power consumption are enhanced compared to traditional and previous current models[7].

The carry look-ahead adder can also be used as a borrow look-ahead subtractor by inserting four Feynman gates at the input terminal [7].

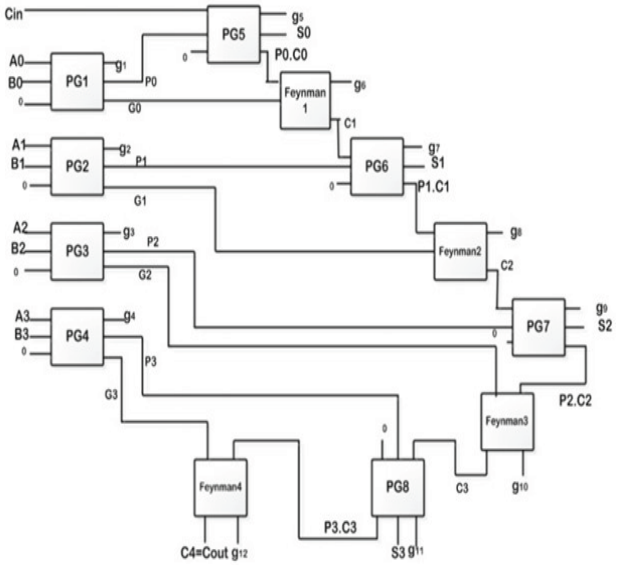

Figure 9. Reversible Carry Look ahead Adder

We need Carry Select Adder, which is speedier than remaining current adders, to succeed arithmetic operations as quickly as possible. Fig.9. reflects the Carry Select Adder block diagram using reversible gates.

Carry select adder was implemented in this paper using Reversible Carry look Ahead Adder, Reversible Multiplexer using Fredkin gate and D-Latch to compensate for parameters of area , delay and power.

The Reversible Carry Select Adder protocol is as follows.

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In the first step, Adder and D-Latch are simultaneously operated using the enable signal with the values 0 and 1 respectively. In the second stage, a multiplexer is fed as inputs with outputs from the adder and latch and carries output from the previous one as a select line[8].

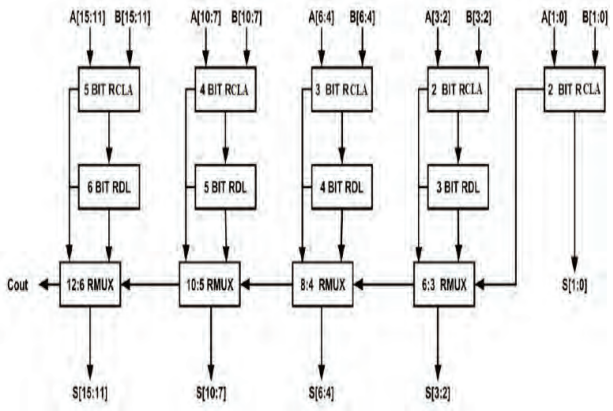

Figure 10. Reversible CSLA using D-latch

V. Design Analysis

These methods are validated for the target device of the Zynq Zed board FPGA. The techniques are simulated and synthesized in Xilinx Vivado software using IP Integrator.

FIR filter was implemented using Carry look ahead Adder and Carry Select Adder in both architectures i.e., Normal and Pipelined. Compared to normal RTL implementation, IP Integrator can optimize parameters like power, delay and utilization.

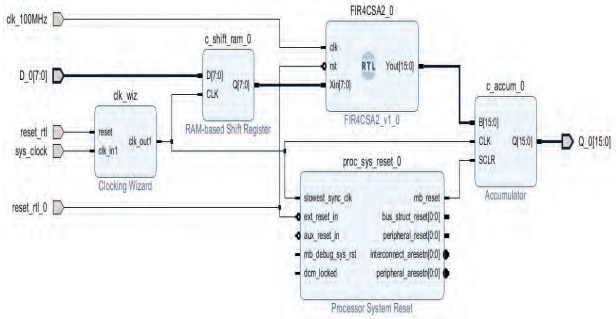

Figure 11. Reversible FIR FILTER using IP Integrator

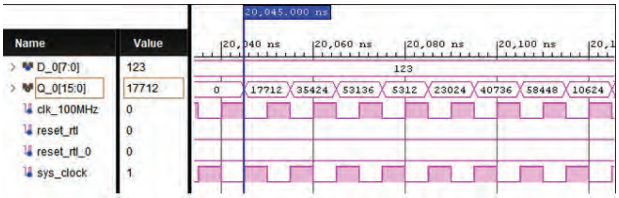

Figure 12. Simulation of 32-tap FIR Filter

The above figure 12 shows Simulation Results of 32-tap FIR Filter using IP BLOCKS and D_0, clock, reset are inputs and Q_0 is output.

VI. Results and Discussion

Experimental results of FPGA performances of VD-CLA-FIR and VD-CSLA-FIR method are as follows.

TABLE I.
Normal Architectutre of Reversible VD-CLA-FIR Filter

FIR FILTER N-TAP	POWER (mW)	DELAY (ns)	FREQUENCY (MHz)	UTILIZATION	
				LUT (53200)	FF (106400)
4	243.867	2.652	141.023	39	73
8	247.944	2.280	135.263	151	76
16	247.884	2.375	137.3060	150	88
32	294.52	2.415	137.3249	149	88

TABLE II.
Pipelined Architectutre of Reversible VD-CLA-FIR Filter

FIR FILTER N-TAP	POWER (mW)	DELAY (ns)	FREQUENCY (MHz)	UTILIZATION	
				LUT (53200)	FF (106400)
4	243.962	2.578	141.203	54	73
8	245.923	2.542	136.724	127	74
16	247.384	2.653	142.5516	186	97
32	249.918	2.48	137.3437	219	105

TABLE III.
Normal Architectutre of Reversible VD-CSLA-FIR Filter

FIR FILTER N-TAP	POWER (mW)	DELAY (ns)	FREQUENCY (MHz)	UTILIZATION	
				LUT (53200)	FF (106400)
4	244.274	2.652	141.037	61	73
8	247.584	2.458	138.1215	144	76
16	247.384	2.325	138.6577	142	88
32	247.333	2.415	132.2401	143	87

TABLE IV.
Pipelined Architectutre of Reversible VD-CSLA-FIR Filter

FIR FILTER N-TAP	POWER (mW)	DELAY (ns)	FREQUENCY (MHz)	UTILIZATION	
				LUT (53200)	FF (106400)
4	244.139	2.650	143.2660	60	73
8	245.933	2.406	138.3700	131	74
16	248.17	2.371	137.3060	189	97
32	248.166	2.345	135.5564	193	98

The results listed in the tables 1-4, depicts the performance metrics. Those are frequency, power, Delay and utilization of the different efficient FIR filter architectures.

In this, the operating frequency of the pipelining FIR Filter is comparatively high and delay along with power consumption of this architecture is more optimized than the normal architecture

Compared to Carry Look Ahead Adder, Carry Select Adder was enhanced the performance of FIR Filter in terms of frequency, delay and utilization.

It is confirmed that pipelined FIR Filters had achieved high throughput along with less utilization than normal FIR Filters. When a number of taps is incremented, the

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difference can be witnessed between the architectures and adders.

VII. Conclusions

In this paper, two types of efficient VLSI architectures required for digital signal processing are designed with different implementation techniques.

Several types of full adders i.e., Carry Look Ahead Adder and Carry Select Adder are involved for the implementation of 4-bit and 8-bit Vedic Multiplier and FIR Filter. All these are executed using Reversible Logic Gates which have condensed the power, delay and area along with utilization parameters.

The Normal architecture of FIR filter using both CLA and CSLA are discussed. The results of CSLA in comparison with CLA make it clear that the CSLA Architecture method reduces the power consumption with the additional area and optimized speed.

The second method called pipelined technique has been applied in FIR Filter to enhance the throughput. There is an increase in power consumption, area and delay along with operating frequency respectively, when compared to the normal FIR Filter.

Despite of normal RTL Implementation, IP Integrator had optimized the architecture in terms of parameters like Power, Delay and Area.

REFERENCES

[1] Ashutosh Kumar Singh, Masahiro Fujita and Anand Mohan, "Design and Testing of Reversible Logic," Springer Singapore, pp. 3-11, 2020.

[2] Md. Belayet Ali, Md. Mosharof Hossin and Md. Eneyat Ullah, “Design of Reversible Sequential Circuit Using Reversible Logic Synthesis”, International Journal of VLSI design and Communication Systems (VLSICS) Vol.2, No.4, December 2011.

[3] Pramod Patali and Shahana Thottathikkulam Kassim, “High throughput FIR filter architectures using retiming and modified CSLA based adders” IET Circuits Devices Syst., 2019, Vol. 13 Iss. 7, pp. 1007-1017.

[4] S.Prema, Ramanan.S.V, R.Arun Sekar and Rajan Cristin “High Performance Reversible Vedic Multiplier Using Cadence 45 nm Technology”, International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-8 Issue-7 May, 2019.

[5] M. Sumalatha , P.V. Naganjaneyulu and K. Satya Prasad ," Low power and low area VLSI implementation of vedic design FIR filter for ECG signal de-noising" in Microprocessors and Microsystems, vol. 71, Elsevier 2019.

[6] C. Durgadevi, M. Renugadevi, C. Sathyasree, R.Chitra, “Design of High Speed Vedic Multiplier Using Carry Select Adder”, International Journal Of Engineering Research and Technology (IJERT) NCIECC – 2017, Volume 5 – Issue 09,2017.

[7] Rahmati, M., Houshmand, M. and Houshmand Kaffashian, M. “Novel designs of a carry/borrow look-ahead adder/subtractor using reversible gates”, J Comput Electron 16, 856–866 (2017).

[8] R. Arun Sekar and S. Sasipriya, "Implementation of FIR filter using reversible modified carry select adder," in Recent Research Challenges in Intelligent Techniques, Big Data and Internet of Things (ITBDIOT2018), Wiley Online Library on, vol. 31, Issue 14, 25 July 2019.