E-ISSN 2581 - 7957
P-ISSN 2277 - 3916

CVR Journal of Science and Technology, Volume 19, December 2020
DOI: 10.32377/cvrjst 1901

Analysis of Switching Losses in Multilevel Cascaded H-bridge and Diode-Clamped Inverter

P. Vinod Kumar[1] and Dr. S. Venkateshwarlu[2]
[1]Assoc. Professor, CVR College of Engineering/EEE Department, Hyderabad, India
Email: p.vinodkumar@cvr.ac.in
[2]Professor, CVR College of Engineering/EEE Department, Hyderabad, India
Email: svip123@gmail.com

Abstract: **Conventional two-level pulse width modulation (PWM) inverters provide good voltage and current output waveforms at the cost of high switching losses during higher frequency operations. Multilevel inverters have emerged very fast as an alternative for medium and high voltage applications. This paper presents the analysis of switching losses estimation of a nine-level cascaded H-bridge and five-level diode-clamped inverter at different switching frequencies. The analysis is also extended to find the comparison of total harmonic distortion (THD) of sine pulse width modulation (SPWM) of currents at different load power factors of cascaded H-bridge and diode-clamped multilevel inverters. This analysis can help in deciding the proper inverter based on the power ratings and area of application. As inverter plays important role in Electric Vehicles, Hybrid Electric Vehicles and Renewable Energy sources, this analysis helps in selecting the better inverter topologies with reduced switching losses.**

Index Terms: **Diode-Clamped Multilevel Inverter (DCMLI), Cascaded H-Bridge Inverter (CHBI), Switching Losses, Total Harmonic Distortion (THD).**

I. Introduction

The demand for multilevel inverters in medium and high-power applications is increasing very fast. They provide high power and voltage with improved power quality. The advancing technology needs high power rating power electronic devices with good power quality. The conventional power electronic circuit can be able to switch input and output only between two possible voltage levels, especially with DC supply. Multilevel inverters are designed to generate a sinusoidal voltage from DC input which can be split into several DC voltages using capacitors. There are three different types of topologies of multilevel inverters. The cascaded H-bridge, capacitor-clamped and diode-clamped multilevel inverters. The main aim of this topology of the multilevel inverter is to produce output waveform with less harmonic distortions without decreasing the power output and switching frequency. The number of levels of the output voltage of the multilevel inverter depends on the input DC sources. THD value decreases as the number of levels of the inverter increases. In a two-level inverter, the output voltage is produced using pulse width modulation [1]-[2]. The output voltage and current of a two-level inverter contains a lot of harmonic distortions, which decreases the quality of the output waveform. In a three-level inverter the THD of the output waveforms decreases compared to two-level inverter. This makes the use of multilevel inverters, which gives the better output voltage and currents with less THD as the levels of the inverter increases. The switching stress also decreases as the level of the inverter increases. The need of filters can be reduced by going for higher levels of the inverter with high switching frequencies. However, this will create another problem, the switching losses of the switches which decrease the circuit efficiency [3]-[4]. As the level increases the number of switches in each leg increases and as to get good output without filters the circuit should be operated at higher switching frequencies. This can be reduced by going for good modulation techniques. In this paper, analysis of switching losses for nine-level cascaded H-bridge multilevel inverter and five-level diode-clamped inverter is done with different switching frequencies. Single phase Nine-level cascaded H-bridge and five-level diode-clamped inverter contains same number of switches. As the analysis will be done on single phase inverter, the five level DCMLI can be considered as nine level inverter. The intention is to study the losses with same number of switches in both the inverters. This helps to compare the performance of inverters in switching stress perspective [5]-[6]. Sine pulse width modulation is used for the analysis. Section-II of the paper gives the details of nine-level cascaded H-bridge and five-level diode-clamped inverter. Section-III gives the details of sine PWM. Section-IV gives the details of the switching losses. Section-V gives the details of results and analysis.

II. Cascaded & Diode-Clamped Inverters

A. Cascaded H-Bridge Inverter (Nine Level)

Cascaded H-bridge multilevel inverter is developed using a full bridge circuit in series connection depending on the number of levels. Four full bridge cells are connected in series to get output as nine-levels. Nine-level cascaded inverter is shown in Figure 1.

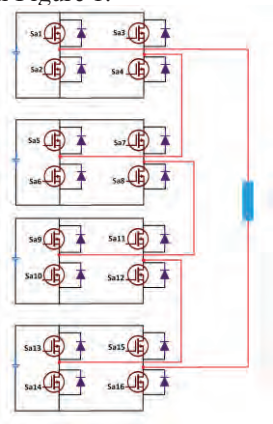

Figure 1. Nine – level CHBI

E-ISSN 2581 - 7957
P-ISSN 2277 - 3916

CVR Journal of Science and Technology, Volume 19, December 2020
DOI: 10.32377/cvrjst 1901

Cascaded H-bridge multilevel inverters are more flexible in selecting switching states compared to other types of inverters. Each bridge contains four switches, in one leg, it contains 2 switches. Four number of DC sources are needed to get a nine-level output. Sine PWM is used in generating switching pulses. Switching states of IGBTs are shown in Table 1.

TABLE I.
SWITCHING TABLE OF NINE LEVEL CHBI

Output Voltage	Active switches
4V	13, 16, 12, 8, 4, 9, 5, 1
3V	13, 16, 12, 8, 4, 9, 5
2V	13, 16, 12, 8, 4, 9
V	13, 16, 12, 8, 4
0	---------
-V	14, 15, 10, 6, 2
-2V	14, 15, 10, 6, 2, 11
-3V	14, 15, 10, 6, 2, 11, 7
-4V	14, 15, 10, 6, 2, 11, 7, 3

B. Diode-Clamped Multilevel Inverter (Five level)

Five-level diode-clamped inverter is shown in the Figure 2. Each leg of the inverter contains 8 switches. Four capacitors are needed to divide the input DC supply to get five levels in the output voltage. But here four separate DC sources are considered like in case of cascaded H-bridge topology. Each leg contains clamping diodes for freewheeling action. The voltage across each device is V, and the total voltage across the leg is 4 times V.

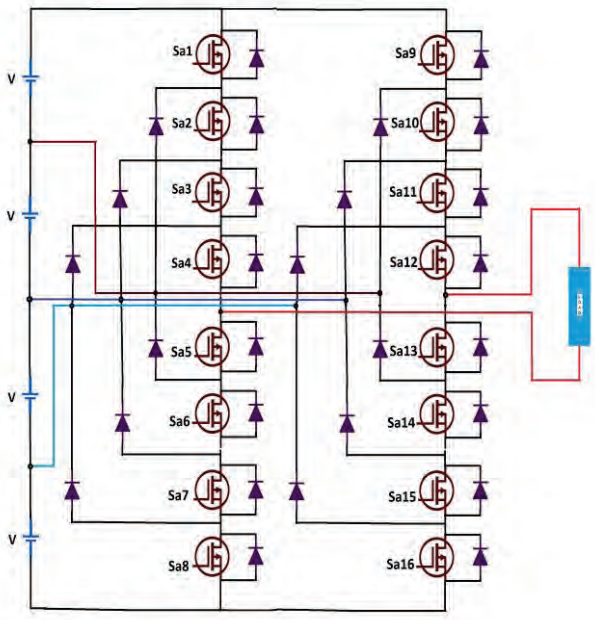

Figure 2. Five-level DCMLI

TABLE II.
SWITCHING TABLE OF FIVE LEVEL DCMLI

Output Voltage (V_{an})	Sa_1	Sa_2	Sa_3	Sa_4	Sa_5	Sa_6	Sa_7	Sa_8
2V	1	1	1	1	0	0	0	0
V	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
-V	0	0	0	1	1	1	1	0
-2V	0	0	0	0	1	1	1	1

III. SINUSOIDAL PULSE WIDTH MODULATION

Sinusoidal pulse width modulation is used for inverters for generating pulses for the switches. This modulation technique compares reference sine wave with the higher frequency triangular carrier waves. Depending upon the level of the inverter, no of carrier waves required will change. In a five-level inverter generally four carrier waves are required to generate pulses to the switches and to produce five-level output. When the sine wave magnitude is greater than carrier wave, then the upper switch will be ON and when the sine wave is having lesser magnitude than carrier then the lower switch will be ON. This makes the inverter get different level in the output. Over a period of one triangular wave, the average voltage applied to the load is equal to the sine wave amplitude during this period. The modulation index is given as m=Am/Ac, where Am is the amplitude of sinusoidal wave, Ac is the amplitude of the carrier wave. By controlling the modulation index, the magnitude of the output voltage can be controlled. Higher switching frequencies produces larger switching losses, typical switching frequencies consider for power system applications are 2-15 kHz. Figure 3. shows the peak to peak nine-level inverter output waveform.

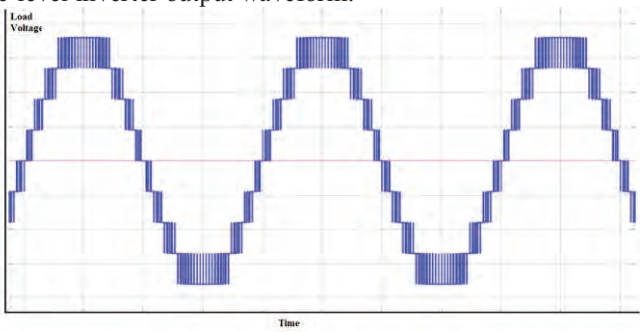

Figure 3. Nine level voltage waveform

IV. CONDUCTION & SWITCHING LOSS CALCULATION

The total losses consist of conduction loss and the switching loss. Switching loss becomes more dominant at high frequencies. Conduction losses are directly proportional to the load current.

Conduction losses occur in the switches and the anti-parallel diodes. Conduction loss in the switches can be calculated using equation (1), and conduction loss in anti-parallel diodes can be calculated using equation 2.

$$W_{cs} = U_{CEo} * I_{Cav} + r_c * I^2_{Crms} \quad (1)$$

$$W_{cd} = U_{Do} * I_{Dav} + r_D * I^2_{Drms} \quad (2)$$

Where

U_{CE0} : On state zero current collector emitter voltage
I_{Cav} : Average switch current
R_c : Collector emitter on state resistance
I_{Crms} : RMS switch current
U_{D0} : Diode approximation with a series conduction of DC voltage sources
I_{Dav} : average diode current
r_D : Diode on-state resistance
I_{Drms} : RMS diode current

E-ISSN 2581 - 7957
P-ISSN 2277 - 3916

DOI: 10.32377/cvrjst 1901

Switching losses will occur in the switches and the anti-parallel diodes. The switching losses in the switch can be calculated using equation 3. And the switching losses in the anti-parallel diodes can be calculated using equation 4.

$$W_{SwS} = \left(E_{onSw} + E_{offsw}\right) * f_{sw} \quad (3)$$

$$W_{SwD} = \left(E_{onD} + E_{offD}\right) * f_{sw} \approx E_{onD} * f_{sw} \quad (4)$$

Where

E_{onSw} : turn - on energy losses in Switch
E_{offsw} : turn - off energy losses in Switch
E_{onD} : turn - on energy losses in diode
E_{offD} : turn - off energy losses in diode
F_{sw} : Switching frequency

V. Results and Discussions

In this paper, analysis of conduction loss & switching loss is done for nine-level cascaded H-bridge inverter and five-level diode-clamped inverter. To simulate the switching losses, a modified half bridge module is taken from Simulink. Thermal model of IGBT-diode and a simscape based heatsink are considered for switching loss analysis [7]. IGBT module no: 5SNE_0800M170100 is considered for half bridge module [8]. The thermal model of IGBT-diode is shown in figure 4. The thermal capacitance of the switch and switch to heatsink resistance are also included in the simulation. The heatsink simscape model is shown in the figure 5. The turn on loss is calculated using voltage before switching and current after switching along with the temperature at junction. The turn off loss is calculated using the current before switching and the voltage after switching along with junction temperature. Conduction losses are calculated using the saturation voltage across collector and emitter multiplied with collector current. This process of simulation of losses was done based on the lookup table taken from the MATLAB sources [7]. The analysis has been carried out at different switching frequencies such as 500 Hz, 1000 Hz, 2000 Hz and 5000 Hz. In both the inverter simulations the same number of switches and DC sources are used. The load is also common in both the cases. Simulation studies have been carried out with the specifications given in the table 3.

TABLE III.
Specifications of Simulink Model

DC voltage	1800 V x 4 sources
Load Power factor	0.9 lag and 0.5 lag
Power	250 KW
Load voltage	5000 V - RMS

This paper mainly concentrates on the switching performance of the two inverters while driving similar loads with the same number of switches. The levels of inverter are chosen in such a way that both should use same number of DC sources with same voltage in two cases.

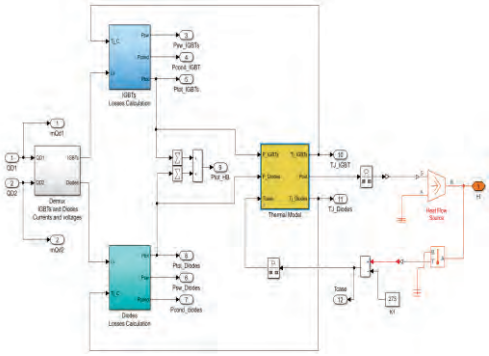

Figure 4. Thermel model of half bridge with IGBTs and diodes

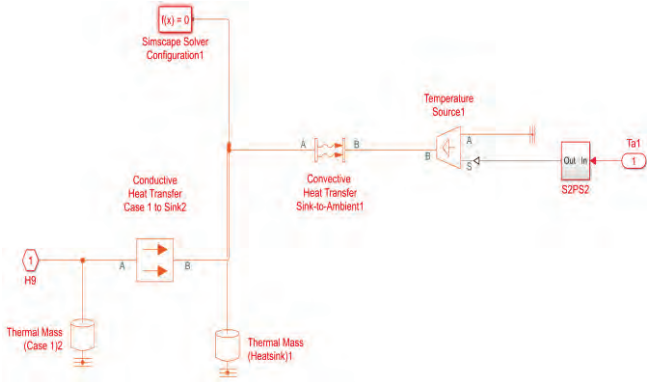

Figure 5. Simscape model of heatsink for half bridge (Two IGBTs)

A. Nine-level Cascaded H-bridge Inverter

Nine-level cascaded H-bridge inverter is tested with sine pulse width modulation at different switching frequencies and the losses are calculated. Figure 6, Figure 7, Figure 8, and Figure 9 give the switching, conduction and total switch losses of CHB five-level inverter at 500Hz, 1000 Hz, 2000 Hz and 5000 Hz. Throughout the simulation the conduction losses remain same as the load considered here is constant. The switching losses are proportionally increasing as the switching frequencies increases. At higher frequencies, the conduction losses appear to be negligible. Figure 10 gives the graph between switching frequencies and the switching losses. Figure 11 gives the graph between switching frequencies and the Voltage THD. Figure 12 gives the graph between modulation index and the load voltage.

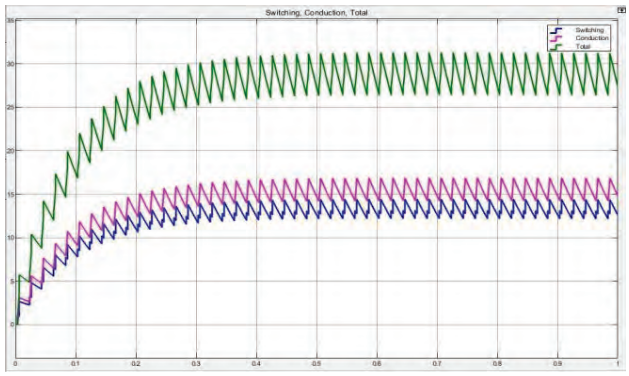

Figure 6. Losses Estimation of CHBI at 500Hz

E-ISSN 2581 - 7957
P-ISSN 2277 - 3916

CVR Journal of Science and Technology, Volume 19, December 2020
DOI: 10.32377/cvrjst 1901

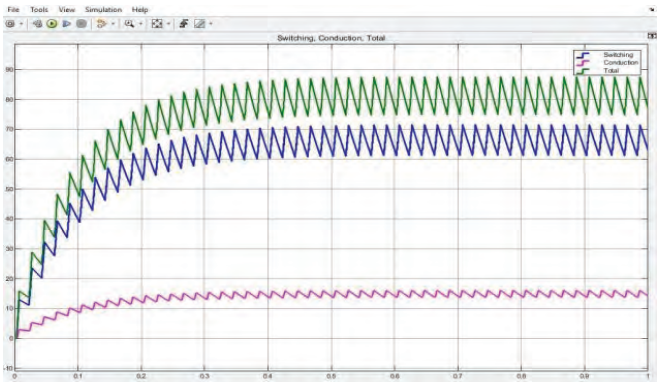

Figure 7. Losses Estimation of CHBI at 1000Hz

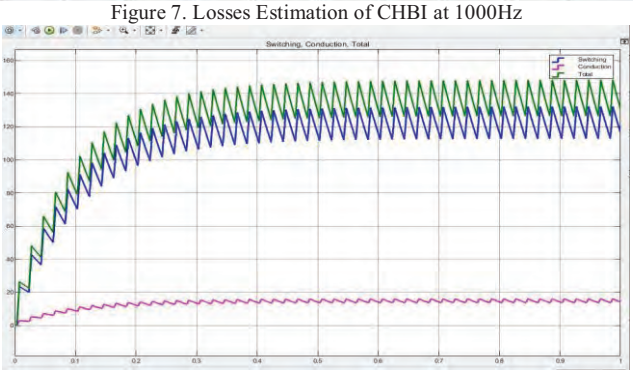

Figure 8. Losses Estimation of CHBI at 2000Hz

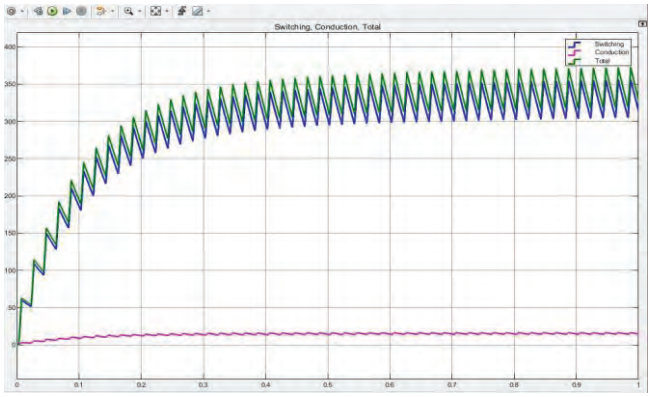

Figure 9. Losses Estimation of CHBI at 5000Hz

A similar analysis is made with 0.5 lagging load and the results are shown in the figures 10, 11 and 12. The orange color curve represents 0.5 lagging load and blue color curve represnets 0.9 lagging load.

Figure 10. Switching frequency verses switching loss for CHBI

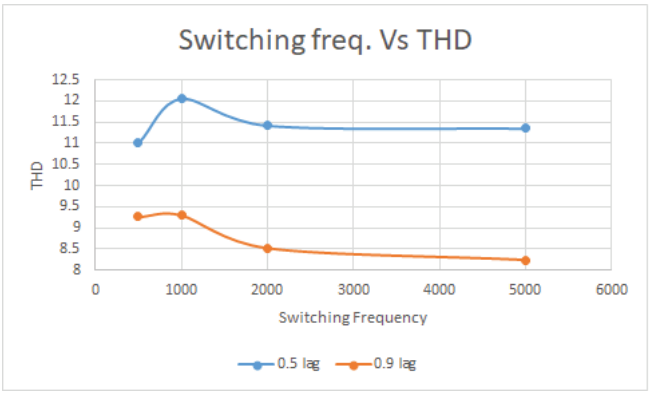

Figure 11. Swtiching frequency verses TDH of CHBI

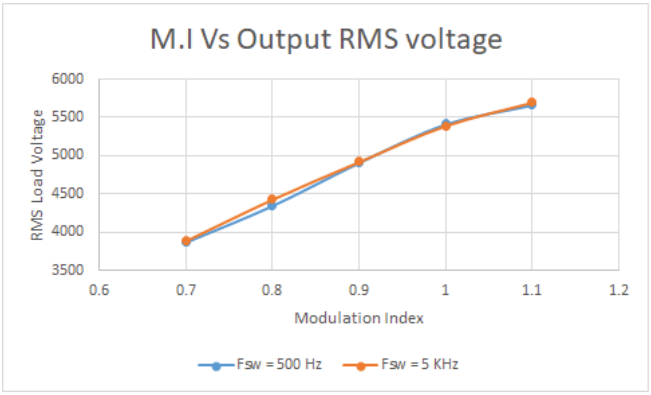

Figure 12. Modulaiton Index verses output RMS voltage of CHBI

B. Five-level Diode-Clamped Inverter

Five-level diode-clamped inverter is tested with sine pulse width modulation at different switching frequencies and the losses are calculated. Figure 13, Figure 14, Figure 15, and Figure 16 gives the switching and conduction losses of diode-clamped five-level inverter at 500Hz, 1000 Hz, 2000 Hz and 5000 Hz. Figure 17 gives the graph between switching frequencies and the switching losses. Figure 18 gives the graph between switching frequencies and the Voltage THD. Figure 19 gives the graph between the modulation index and the RMS voltage.

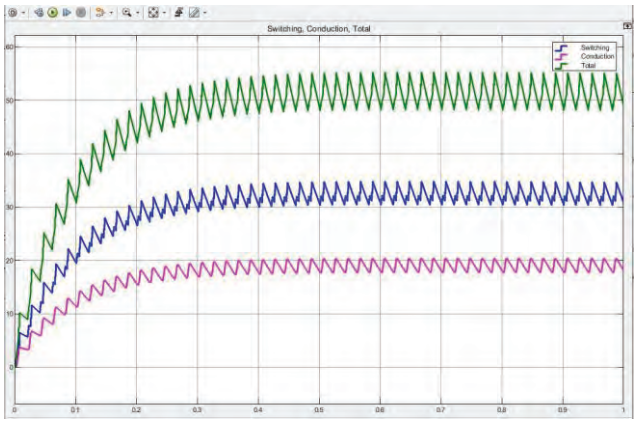

Figure 13. Losses Estimation of DCMLI at 500Hz

E-ISSN 2581 - 7957
P-ISSN 2277 - 3916

CVR Journal of Science and Technology, Volume 19, December 2020
DOI: 10.32377/cvrjst 1901

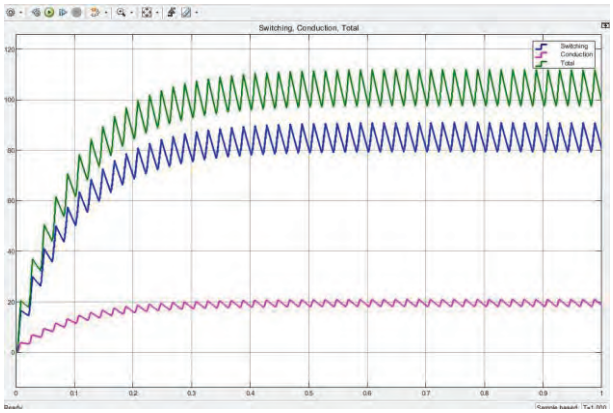

Figure 14. Losses Estimation of DCMLI at 1000 Hz

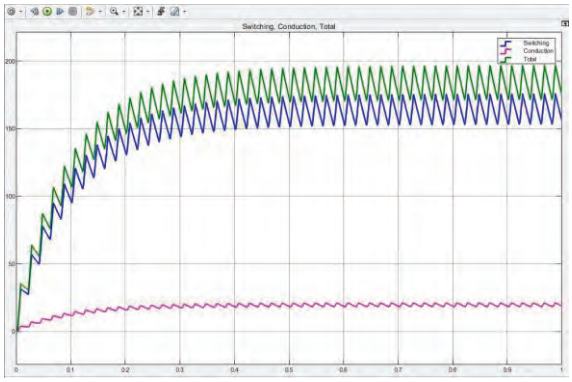

Figure 15. Losses Estimation of DCMLI at 2000 Hz

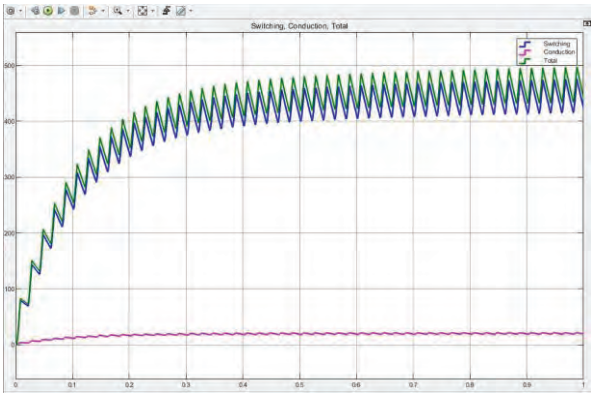

Figure 16. Losses Estimation of DCMLI at 5000 Hz

Figure 17. Switching frequency verses switching loss for DCMLI

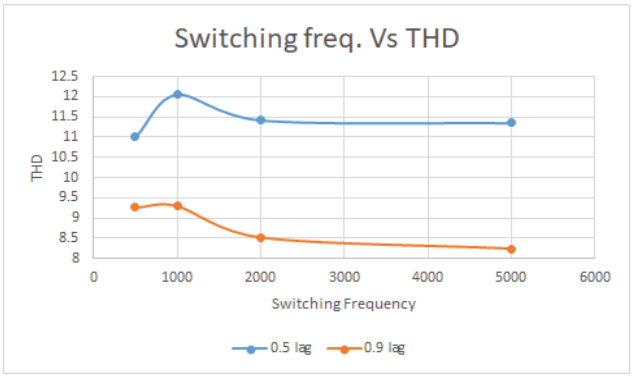

Figure 18. Swtiching frequency verses THD for DCMLI

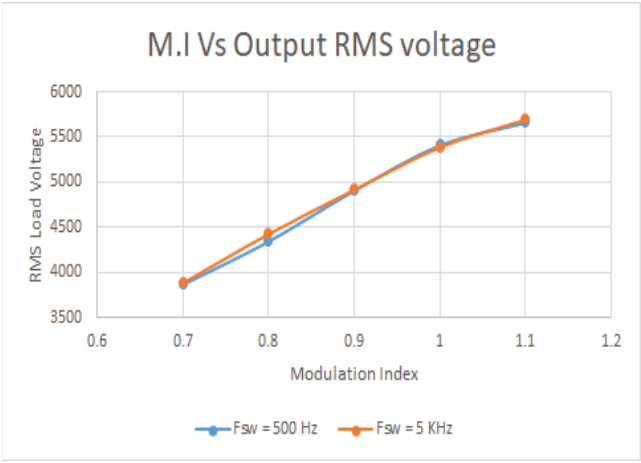

Figure 19. Modualtion index verses output voltage for DCMLI

C. Comparison of CHBI and DCMLI performacnce

The comparison of CHBI and DCMLI inverters are presented here. The switching losses in DCMLI are almost 40 % higher than CHBI driving 0.9 lagging load with same DC voltage sources. Figure 20 shows the loss drop in CHBI operation.

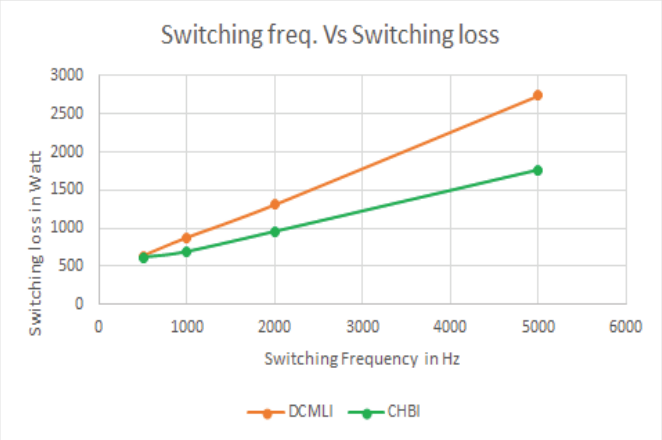

Figure 20. Loss drop in DCML inverter operation

The effect of switching frequencies over individual inverter THDs is almost constant. But when compared both

performances, THD is 90% more in CHBI. Figure 21 shows the THD Vs switching frequencies plot.

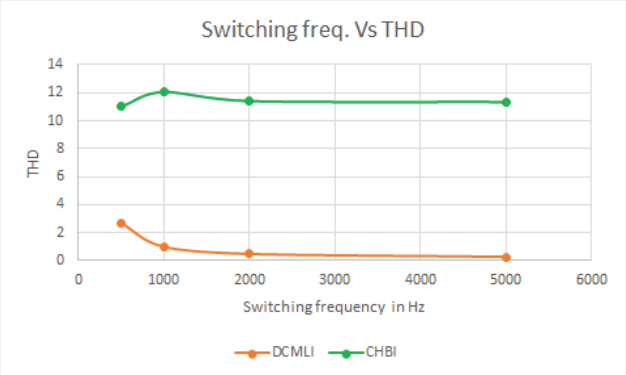

Figure 21. THD Vs Switching frequency for CHBI and DCMLI

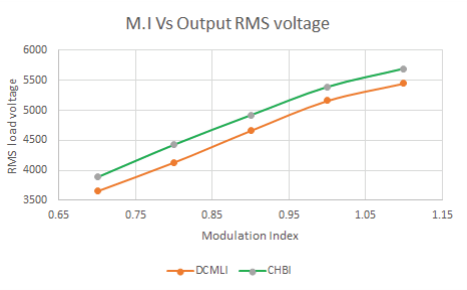

Figure 22. Load voltage Vs Mod. Index for CHBI & DCMLI

CHB Inverter produces more RMS voltage compared to DCML inverter. CHB inverter is delivering 12% more voltage to the load. Figure 22 shows the plot between modulation index Vs RMS load voltage. Switching losses occurred in CHBI and DCMLI while driving 250KW load with respect to the switching frequencies are given in the table 4.

TABLE IV.
SWITCHING LOSS COMPARISON TABLE

Switching Frequency (Hz)	Switching Loss (W)	
	CHBI	DCMLI
500	618	637
1000	696	877
2000	958	1311
5000	1765	2747

VI. CONCLUSIONS

The main aim of this paper was to determine the losses in cascaded H-bridge inverter and diode-clamped inverter circuit in which each circuit has the same number of switches. When same number of switches are there then it is easy to compare the losses in the circuit. This helps to go for methods to reduce losses and the application of each inverter in a particular circuit. The selection of the simscape thermal model of IGBT and heatsink helped a lot in finding the switching losses of the inverters. The simulation mainly emphasized on same number of switches delivering the same amount of power between similar source and load structures. It is observed that for 0.5 lagging and 0.9 lagging loads, the DCML inverter has more switching losses providing a quality sine wave with THD 2% in its current waveform. But the CHB inverter losses are 40% less than DCML inverter with 11% THD.

REFERENCES

[1] A. Nabae, I. Takahashi and H.A. Kagi, “A New Neutral Point Clamped PWM inverter,” IEEE Trans. Industry Application, vol.IA-17, pp. 518-523, sep/oct 9181.
[2] J. Rodriguez, J. S. Lai, and F. Z. Peng, “Multilevel Inverter: A survey of Topologies controls and applications,” IEEE Trans. Industrial Electronics vol.49, no.4, pp. 724-738, Aug.2002.
[3] Mohan Ned, Undeland T.M and Robbins W.P, “Power electronics converters applications & Design,” John Wiley & Sons, Second Edition 2007.
[4] G. Bhuvaneswari & Nagaraju, “Multilevel inverters- A comparative study,” IETE Journal of Research, vol. 51, no.2, Mar-Apr. 2005, pp. 141-153.
[5] Mohammadreza Derakhshanfar, “Analysis of different topologies of multilevel inverters,” Master Thesis, Chalmers University of Technology, 2010.
[6] Akagi H, “Multilevel Converters Fundamental circuits & Systems,” Proceedings IEEEE, 2017, vol.105, pp. 2048-2065.
[7] Mathworks.com – Loss Calculation in a 3-Phase 3-Level Inverter Using SimPowerSystems and Simscape.
[8] http\\abb.com. IGBT Module 5SNE 0800M170100.