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Design of Enhanced PLL for Single-Phase Grid Connected Transformerless Inverters

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Abstract: **Renewable energy sources integrated with conventional sources fed grid to meet the ongoing electrical energy demands. This paper presents design of Enhanced Phase locked loop (EPLL) for single phase grid connected transformer less inverter. The knowledge of phase angle, frequency, voltage magnitude is under consideration to integrate the solar PV to single-phase grid. It is required to track exact utility voltage vector for reliable control of power to the grid. The paper also presents Simulink modeling, analysis of Enhanced PLL and compares its performance with basic phase locked loop (PLL) used.**

Index Terms: **Enhanced phase locked loop (EPLL), Transformerless inverter, single phase grid connected,**

I. INTRODUCTION

Depletion of conventional sources made an inevitable attempt to increase the percentage of renewable energy sources to be used. In this scenario the solar PV places itself on high preferred renewable energy sources, due to its simplified conversion technology [1]. As the renewable energy sources like Photo voltaic (PV) generates DC, it needs a power electronic converter to convert into AC and to feed it to grid. The converter can be DC-DC, to maintain the DC voltage at the DC link of the input of the inverter. The converter can be a DC-AC which feeds the power from PV to grid. A high frequency transformer is used in case of DC-DC converters, on DC side whereas a low frequency transformer in case of DC-AC converter on AC side. In either of the cases the transformer is used which will be integral part of the converter thus occupying space, increases the cost of the system and reduces the efficiency of the system. Thus, to reduce the cost and space occupied by the system the transformerless inverters are into practice [2]. The power electronics converters are used in the conversion of renewable energy sources from dc-dc and dc-ac Solar PV inverters need either a high frequency transformer on dc side shown in Fig.1(a) or a low frequency transformer on ac side to provide galvanic isolation as shown in Fig.1(b) . But by avoiding transformer as shown in Fig.2. efficiency of the conversion can be improved, and size of the inverter can also be reduced considerably. In view of this advantages, research on transformer less inverter has taken a quick pace. To integrate solar PV to single phase grid for low power applications, it is required to track phase angle, amplitude and frequency of utility voltage vector and inverter output voltage. This can be done by using phase locked loop [2].

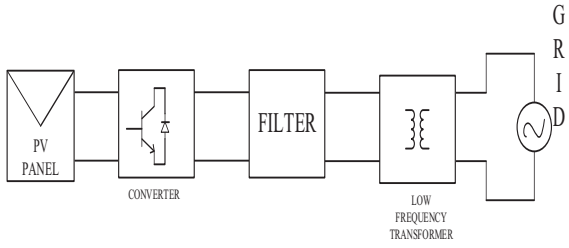

Figure 1(a). Grid connected inverter with low frequency Transformer

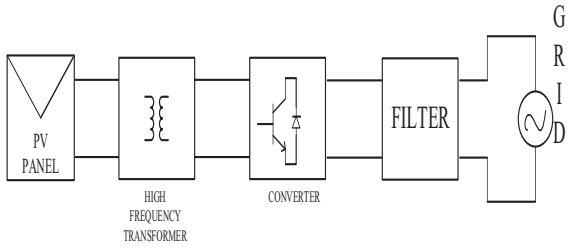

Figure 1(b). Grid connected inverter with high frequency Transformer.

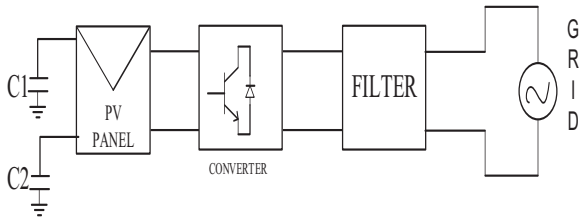

Figure 2. Transformerless Inverter.

In the grid connected inverters the output parameters like voltage amplitude, frequency and phase angle are of greater importance to inject active and reactive power to the grid. In the case if inverters are fed from solar PV it can only supply active power to the grid. To supply reactive power, it needs a distributed static compensator (DStatcom) [3] . In either of the situations to inject active and reactive power to grid decoupled controls of d-axis and q axis components of currents is employed and are controlled separately [3].

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II. PHASE LOCKED LOOP

Phase locked loop identifies and automatically sets phase angle of a voltage or current vector generated by an inverter with that of phase angle of grid voltage or current in grid connected system. The change in frequency of inverter which is required due to change in load can be adjusted with the help of PLL [4]. Besides various other techniques of synchronization of inverter to grid phase locked loop is simple in its implementation. The Fig.3 indicates block diagram of PLL based synchronization of transformerless inverter with grid.

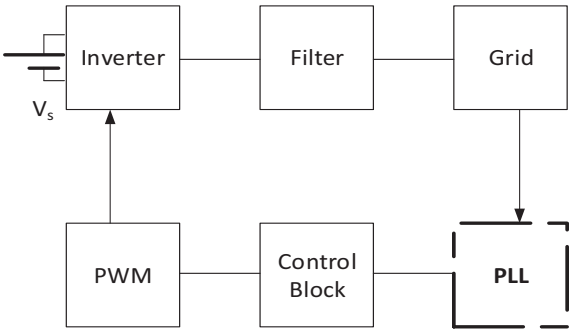

Figure 3. PLL based synchronization of transformerless inverter with grid.

The basic PLL consists of Phase detector loop filter and controller along with a voltage control oscillator as shown in Fig.4..Phase detector compares two input voltages generate an error signal that is proportional to the difference of phase angle between them. This error signal is fed to filter which will further drive voltage control Oscillator [5]. Thus, output is locked to phase at the input.

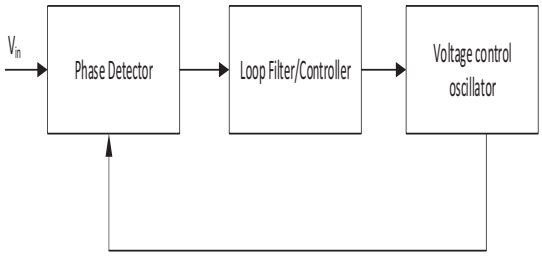

Figure 4. Block diagram of PLL.

In the literature it has been stated that three phase PLL and single phase PLL are designed with different approach. Multiple techniques of synchronization of inverter to grid are surveyed out of which inverse park based PLL is the simplest. It needs to generate a orthogonal component in single phase system unlike in three phase system, where inherently three phase system (a-b-c) can directly be converted into two phase orthogonal stationary reference frame system using Clarks transformation (α-β). Park transformation will convert stationary reference frame to synchronously rotating reference frame which are given by the following equations [6].

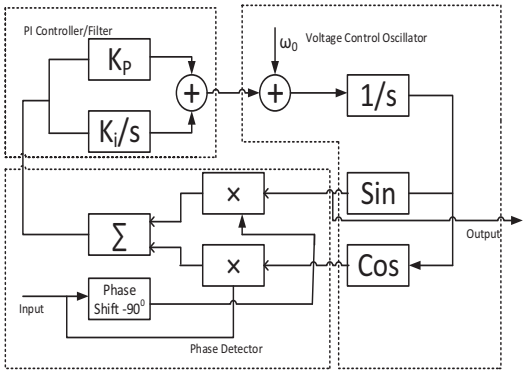

Figure 5. Mathematical modeling of PLL

Basic phase locked loop contains PI controller or filter , voltage controlled oscillator and phase detector as shown in Fig.5 The main focus of this paper is to present a comparison of basic phase locked loop structure with that of enhance phase locked loop in terms of their performances. Enhanced phase locked loop is found be best option for single phase grid connected systems. Further the steady state and dynamic performance of enhanced PLL is analyzed.[8].

III. ENHANCED PHASE LOCKED LOOP

The EPLL overcomes the disadvantage of basic PLL i.e double frequency error. This is done by estimating the amplitude of the input voltage or current signal with an extra loop. Besides EPLL removes double frequency error, it also gives filtered version of input quantity. In other words, EPLL not only acts as PLL but also as filter and controller which helps in direct measurement of phasor.

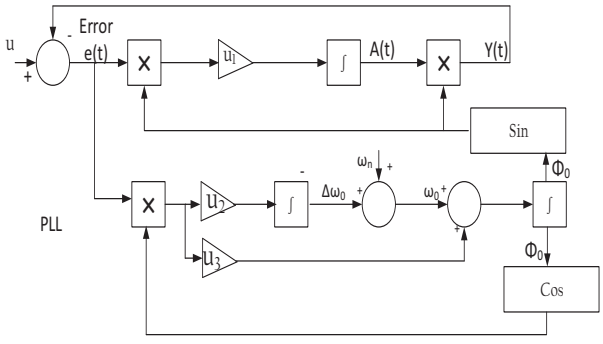

Figure 6. Block diagram of enhanced phase locked loop.

The lower portion of Fig.6 indicates basic PLL and upper loop indicates filtered input signal. Variables u1, u_2 and u_3 are positive gains to control the performance of EPLL [10]. Φ_0 is estimated phase angle, ω_n is reference frequency. In addition to constant estimate of fundamental component of input signal while the amplitude, frequency and phase are varying. It can also provide 90^0 phase shifted signal of fundamental component. Enhanced phase locked loop is best suited for single phase system whereas other techniques of

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synchronization like Recursive Discrete Fourier Transform, Second order generalized integrator etc. [11].
Enhanced phase locked loop is characterized by the following equations in time domain [14] .

$$A(t) = \int e(t).\sin\varphi_0(t).u_1.dt \text{ -----} \quad (1)$$

$$\Delta\omega_0(t) = \int e(t).\cos\varphi_0(t).u_2.dt \text{ ----}(2)$$

$$\varphi_0(t) = \int [e(t).\cos\varphi_0(t).u_3 + \Delta\omega_{0(t)+} \ \omega_n].dt \text{ --} \quad (3)$$

The error signal e(t) is the distortion of the input signal [12].

IV. Simulink Modelling

This section describes the Matlab Simulink modeling of basic PLL and enhanced PLL having varied frequency and amplitude. The variation of phase angle and frequency can be observed. Fig.7. shows the Simulink model of basic PLL having a sinusoidal input with amplitude of 50 and frequency of 50Hz.

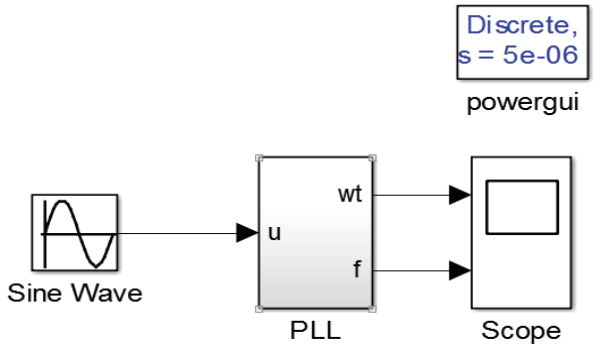

Figure 7. Simulink model of basic PLL

The parameters like input amplitude, frequency, and typical values of gains u_1, u_2 and u_3 are shown in the following Table. I

TABLE I.
DESIGN PARAMETERS OF PLL

S. No	Basic PLL (Ts=5e-6)	
	Parameter	**Value**
1.	Input voltage amplitude	230 Volts
2.	Frequency	50Hz
3.	Kp	400
4.	Ki	2000
	Enhanced PLL(Ts=5e-6)	
1.	Input voltage amplitude	230 Volts
2.	Frequency	50Hz
3.	u_1	200
4.	u_2	20000
5.	u_3	400

Table. I describe the design parameters along with sampling time used basic PLL is T_s=5e-5 sec. and enhanced PLL having a sampling time of T_s=5e-6 sec.

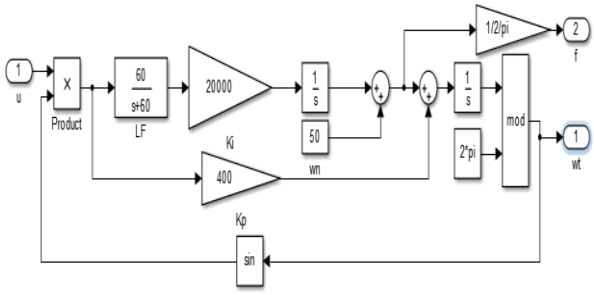

Figure 8. Simulink modeling of PLL

The input amplitude of 230 having a frequency of 50Hz is given. Fig.7. & Fig.8.are showing Simulink models of basic PLL. The Simulink model of basic PLL includes a low pass filter and PI controller as shown in Figure.8.

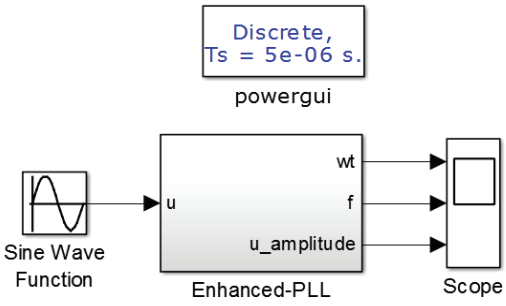

Figure 9. Simulink model of Enhanced PLL.

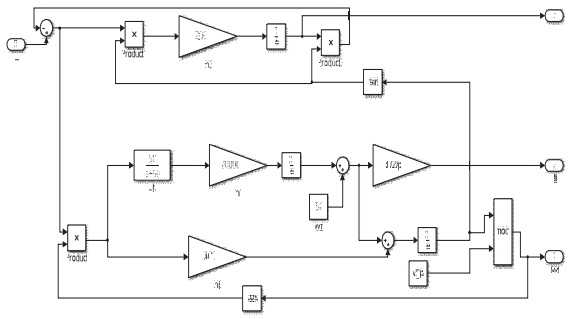

Figure 10. Simulink modeling of Enhanced PLL

Fig.9. and Fig.10. indicates Simulink modeling of enhanced PLL, which includes an extra loop for filtering the input signal so that fine control is possible [11].

V. Results

The Simulink diagrams described above indicating the operation of basic PLL and enhanced PLL. The simulation results of both the types PLL are analyzed and compared in the section V.

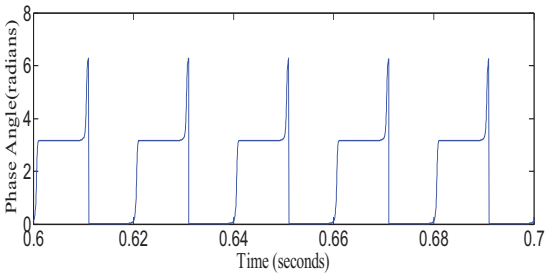

Figure 11. Variation of Phase angle using PLL

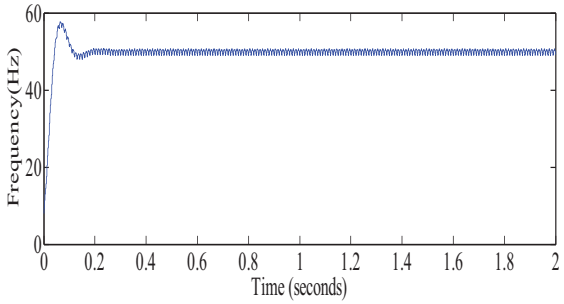

Figure 12. Frequency of basic PLL

The frequency of the given signal is determined by the PLL and is 50Hz as shown in Fig.12.Further the phase angle is determined, its value is mentioned in radians i.e. 6.28 as shown in Figure.11.

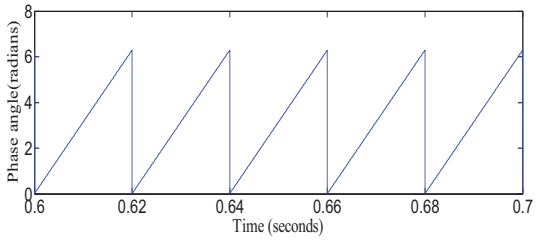

Figure 13. Phase angle of enhanced PLL

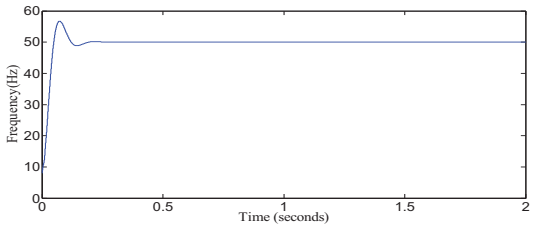

Figure 14. Frequency of enhanced PLL.

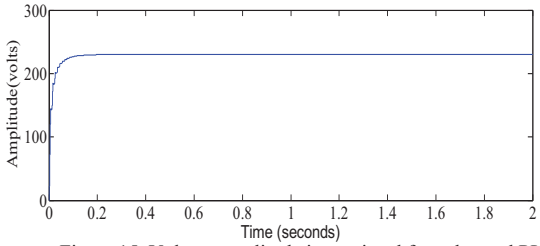

Figure 15. Voltage amplitude input signal for enhanced PLL

Fig.13. and Fig.14 are the simulation results of enhanced PLL describing phase angle and frequency. Figure.15. shows the amplitude of the input signal provided in enhanced PLL.

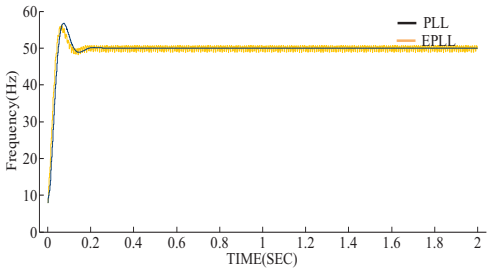

Figure 16. Comparison of frequency in PLL & EPLL.

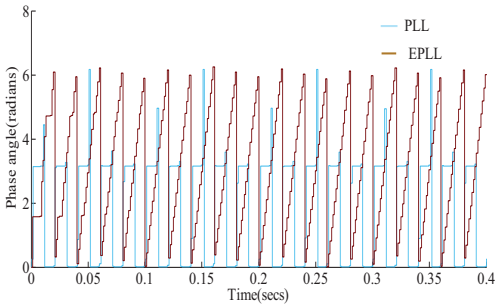

Figure 17. Phase angle Comparison in PLL & EPLL.

The control in the frequency given by basic PLL is compared with EPLL as shown in Fig.16. which describes the performance of EPLL is improved when compared to basic PLL. Fig.17. indicates phase angle variation in PLL and EPLL indicating that tracking of phase angle in EPLL is superior compared to basic PLL [16]-[18].

VI. Conclusions

The phase angle, frequency and voltage amplitude of inverter output signal that is required to feed to grid has paramount importance in view of power control to the grid. By comparing Figure.12.and Figure.13. It can be concluded that the variation of frequency in basic PLL is found to be high i.e.+/-3-5Hz. On contrary the enhanced PLL has negligible (0.1-0.3Hz) variation in its frequency measurements. Figure.11 and Figure 13. indicates the phase angle measurement is not smooth in basic PLL compared to EPLL. Besides the accuracy in measurement and its simplicity in implementation made enhanced phase locked loop (EPLL) much popular when compared with other synchronizing methods.

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