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Detection and Mitigation of Faults in 13–Level Cascaded H-bridge Converter STATCOM

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Abstract: **This paper deals with the detection and mitigation of faults in 13-level converter STATCOM. The FACTS device used is flexible in reactive power compensation, voltage regulation, to reduce harmonics of the grid that must be protected from faults in the switches. Due to frequency switching of the STATCOM, the possibility of the switch malfunction such as open circuit and short circuit faults are predominant. Many static synchronous compensators use multilevel converters to lower the switching faults. The pulse width modulation techniques applied to a proposed cascaded 13-level to detect the faulty switch and mitigate it. In this paper the performance analysis of PWM techniques are computed with dynamic fault conditions.**

Index Terms: **STATCOM, Detection of Faults, Pulse Width Modulation Techniques, Multi-level Converter**

I. Introduction

These days the demand for power has been increasing year after year. Practically when the unpredictable loads that are coupled to the grid system are of unbalanced in nature electrically, the quality of the voltage and current reduces. In order to maintain the quality of the grid system STATCOM is used. With the utilization of STATCOM, reactive power is able to compensate, voltage regulation can be improved.

The control techniques incorporated in STATCOM [1] are generally of two level or three level conventional PWM topologies. With the decrease in the level of the modulated waveform of the Voltage Source Converter, the change in the form of electrical signal is relatively high. So, reactive power will be injected along with harmonics into the grid system with the utilization of STATCOM [2]. The harmonics in the voltage creates large damages to the loads, thereby reducing system efficiency. To overcome this issue a cascaded H-bridge with multilevel is connected. The reason for compelling a multilevel converter topology to the STATCOM is to create an harmonic insertion into the power system. The level of H-Bridge used is a cascaded 13th level STATCOM [3]-[4]. Formulation of the levels of the PWM given as m=2n+1, where m=no of H-bridges. Simplified model of 13-level cascaded H-bridge STATCOM is shown in figure 1. Each phase consists of 6 full bridges and each H-bridge has 4 Insulate Gate Bipolar Transistors (IGBTs) with anti-parallel diode to avoid circulating currents.

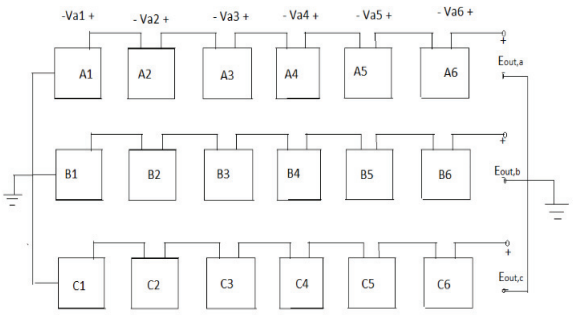

Figure 1. Simplified 13-level cascaded H-bridge STATCOM

As the level of converters used is more, the no of switching devices used also will be more. So it is important fault-lenient STATCOM. The malfunction of power unit in a proposed system will result in the blow up of switch modules which in turn lead to short circuit or open circuit of the respective bridges. These kinds of transient conditions on the power system cause insipient damages like disruptions in the voltages of the grid system and also may create severe dip due to switching. So it is significant to identify the location of faulty bridge and remove it. Early detection of these faults helps to avoid abnormal event progression. With the comparison of capacitor DC voltage to a fundamental value, respective malfunctioned power unit is identified, isolated and removed from service with bi-directional bypassing switch. Several switching technique topologies were applied to the cascaded H-bridge 13 level STATCOM and they are compared with THD spectrum study and identify the technique which gives the best performance.

II. Multilevel Converter

The converter is a power electronic circuit which converts the alternating current into the direct current. Now a days multilevel converters are emerging a new breed of high power switching applications. Multilevel converter consists of several switches, used in industrial applications, Railway Traction Drives and Electrical Vehicle etc. The converter is classified into voltage source and current source. The voltage source consists of multilevel converter and 2-level voltage converter. In this paper we are implementing multilevel with multiple DC sources.

The multiple DC sources with cascaded H-bridge design are implemented. Basically, multilevel inverters are

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classified as Diode Clamped, Flying Capacitor and Cascaded H- Bridge. Of the above, Cascaded H-Bridge converter is the best one to choose because it requires less number of the components in each switching levels. In this paper we are applying Cascaded H-Bridge Multilevel converter (CHB-MLC) [5] which is internal design of a STATCOM.

III. Modulation Techniques

The output voltage of multilevel inverter is obtained using level shifted modulation technique. The PWM include n carrier waveforms for (m-1) level in which magnitude, frequency of waveform is same as that of grid taking sinusoidal waveform as reference for comparison. After comparing, the output signals using comparator are transmitted to the IGBT.

A. Phase Disposition PWM

Figure 2 shows the output characteristics of carrier signal arrangement using PDPWM technique. In this context the entire (n-1) carriers for n level converter are in phase. For thirteen levels three phase multilevel converter we get 12 carrier waveforms which are in phase with same amplitude & frequency.

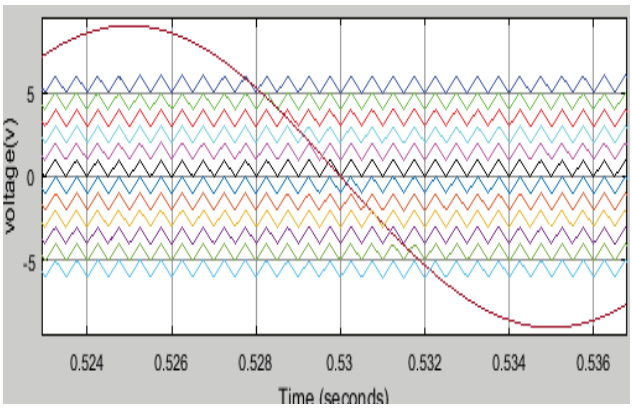

Figure 2. Carrier signal arrangement for PDPWM technique

B. Phase Opposition Disposition (PWM)

In this modulation technique, the output of the carrier signal is above the zero axis with frequency and amplitude in phase with each other. For 180 degree phase shift electrically between frequency and amplitude, same carrier signal is shifted below zero axis. The proposed method has 12 carrier signals to be modulated with the fundamental sinusoidal signal taken as reference is shown in figure 3.

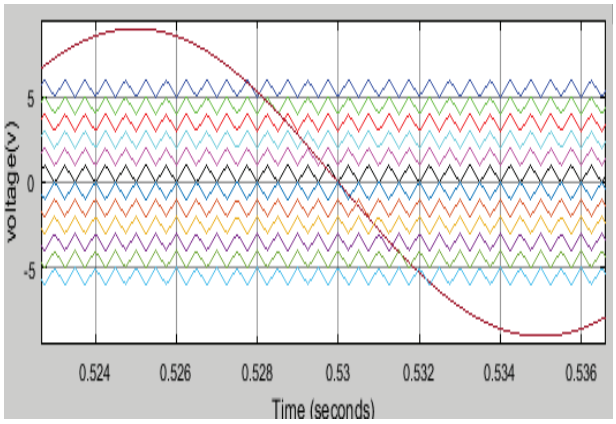

Figure 3. Carrier signal arrangement for PODPWM technique

C. Alternate Phase Opposition Disposition PWM

This modulation technique results in carrier signal out of phase with its next carrier waveform by 180 degree with same frequency & amplitude. Complete phase sequence of thirteen level converter with 12carriers and one reference wave form are shown in Figure 4.

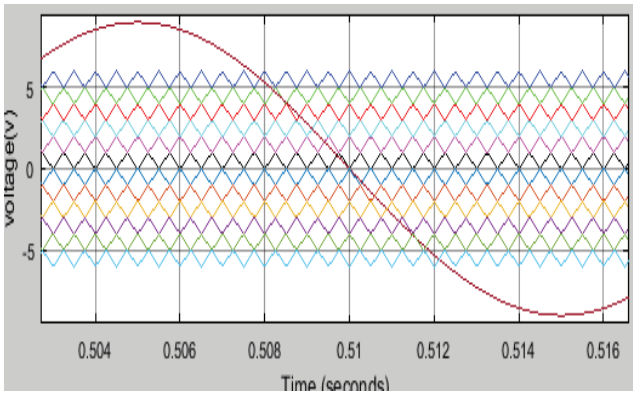

Figure 4. carrier signal arrangement for APODPWM technique

IV. Fault Analysis

The number of switches in the cascaded 13-level STATCOM is more when compare to the conventional control topologies. This is suitable in increasing faults in switching due to the continuous switching operation. This mode of operation results in malfunction of each switch in either of open or close states. The cell with switch faults is shown in below figure 5. The fault detection [7] of any IGBT can be detected by the comparison of capacitor DC voltages to a reference value.

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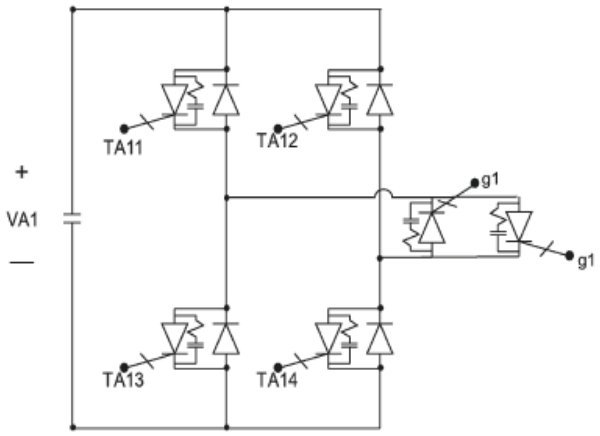

Figure 5. Cell with fault switch

Open circuit fault can be detected if the voltage across the capacitor rises to an infinite value. With dip in the voltage of the system, there is a predominant effect on the performance of STATCOM. An open circuit switch fault is able to avoid by controlling the gate current for the respective switch. In case of any short circuit switch fault, the capacitors will rapidly discharge to zero thereby avoiding the malfunction by using two-way switch.

V. Simulink Model and Results

In figure 6, the complete MATLAB model with STATCOM is shown. The complete system diagram with two buses (V-I measurement) connected one at source side and the other on load side.

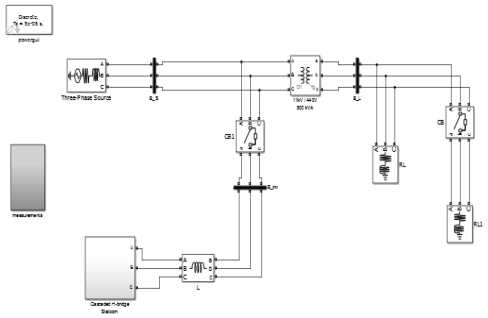

Figure 6. MATLAB model with STATCOM

The internal design of a STATCOM which is 13-level cascaded H-bridge is shown in figure 7. Multilevel STATCOM having 6 H-bridges in each phase to synthesize a staircase waveform is simulated. The converter legs are said to be identical and modular.

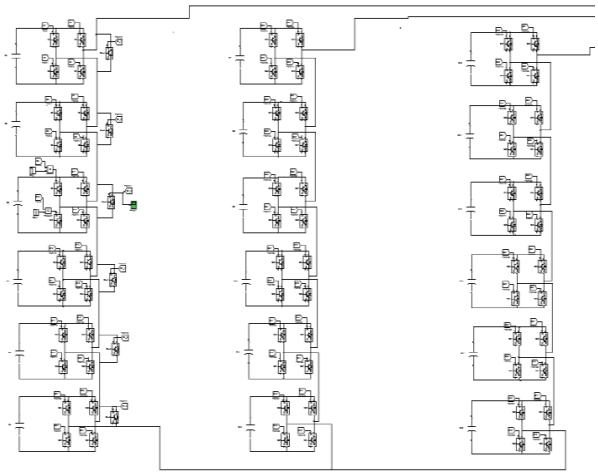

Figure 7. 13-Level Cascaded STATCOM Circuit Design in Simulink

Each H-bridge contains four power electronic switches which are IGBTs with an anti-parallel diode to avoid circulating currents. Each full bridge generates three level voltages (V, 0,-V). DC voltage balancing is obtained by incorporating DC source to each bridge. The Hybrid bridges are connected in a star model with the neutral at mid-point. In order to achieve steady output voltage, the voltages across all the direct current capacitors are to be maintained at a constant value. In this paper we are creating an open circuit and a short circuit switch faults randomly in phase A at third level of the converter which is connected in cascaded manner. The fault is created in circuit by a unit step function at a time interval t=0.5 seconds.

A. Short Circuit Switch Fault

The switch fault in any IGBT can be detected by comparing DC capacitor voltage to a reference value. Using unit step function at 0.5 seconds the fault has been injected into H-bridge.

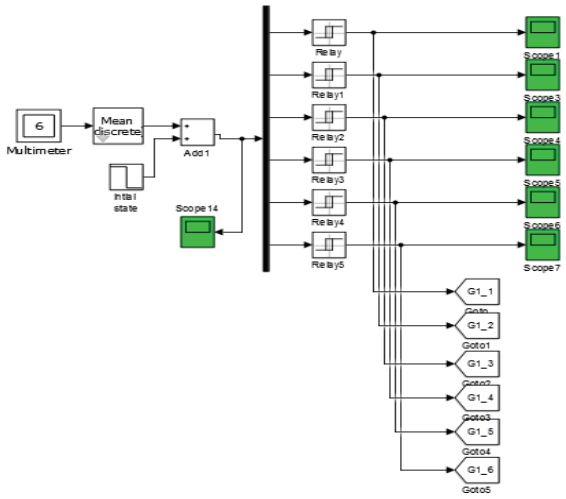

Figure 8. Control Circuit for Detection and Mitigation of the Open Circuit and Short Circuit

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The relay feedback circuit is shown in figure 8. The circuit determines three sets of relays incorporated to generate pulses for each of the switches whose resistance is low. At 0.52 seconds the gate signal of cell 3 by-pass switch is generated as shown in figure 9.

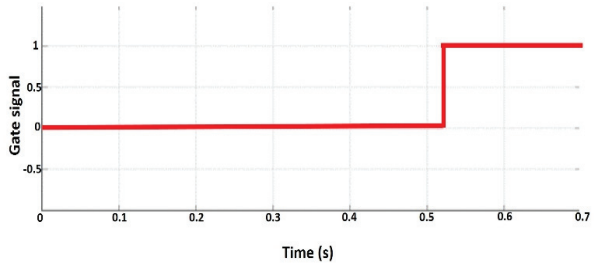

Figure 9. Gate signal generated by relay to by-pass cell No.3

During short circuit switch fault, the voltage across the direct current capacitor reduces to zero. In the figure 10 we can observe that all the voltages across the DC capacitor are same, except at the third hybrid bridge of phase A. This is due to that the voltage across it drops to zero at time interval 0.5 sec where the fault is detected.

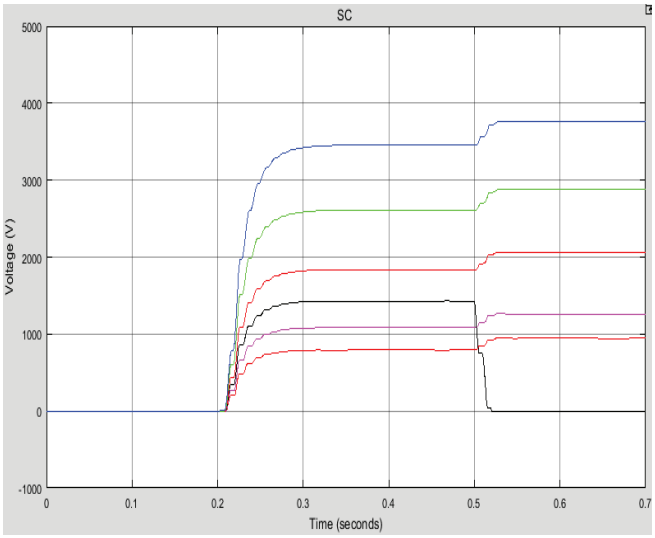

Figure 10. Capacitor voltages during short circuit fault.

Due to the existence of the fault in the system the per unit voltage of the system dropped to certain value. In order to mitigate the detected fault, a bidirectional switch is used to bypass the faulty H-bridge. This method of detection leads to pulse generation at certain signal level for gate bipolar transistor triggering and trips it ON for reduction in fault. The per unit voltages of all the three phases can be observed in figure 11. As soon as the fault is detected or identified, the feedback control circuit is integrated with respective change in the phase voltages as referred in figure 12.

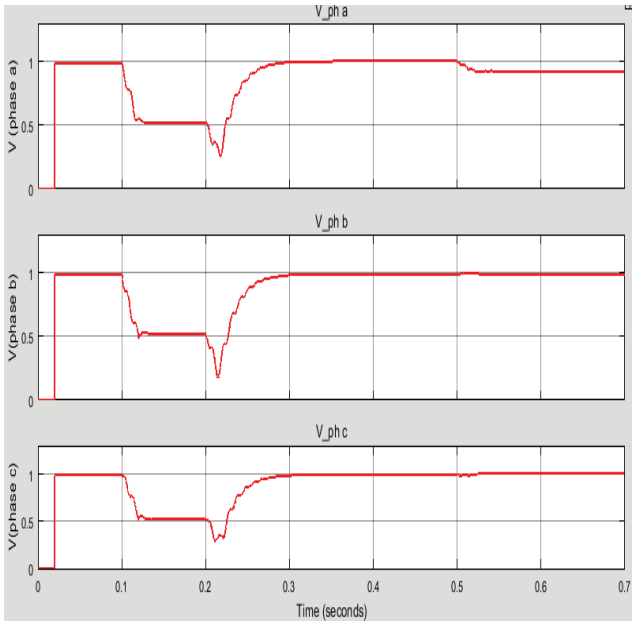

Figure 11. Magnitude of phase voltages during short circuit switch fault

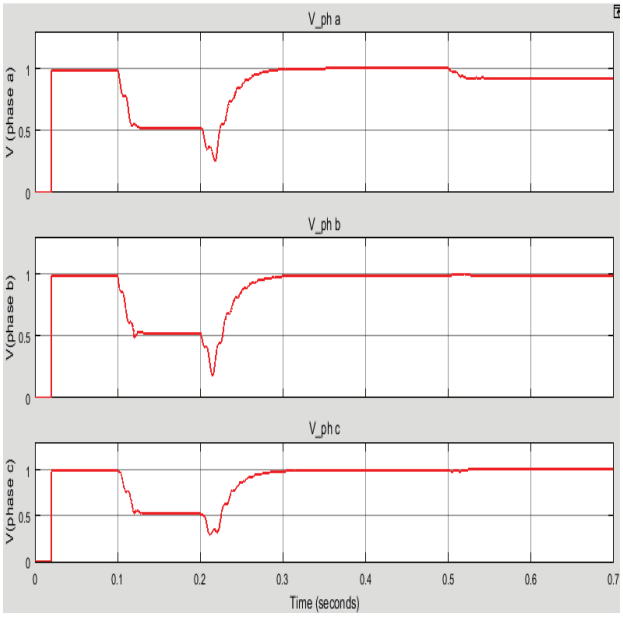

Figure 12. Magnitude of phase voltages in SC switch fault after feedback control circuit

B. *Open Circuit Switch Fault*

During open circuit condition, the potential difference across the capacitor on the direct current side increases to finite value. From the below figure 13 we can observe that all the voltages across the DC capacitor are same except the voltage across the 3rd H-bridge of phase A.

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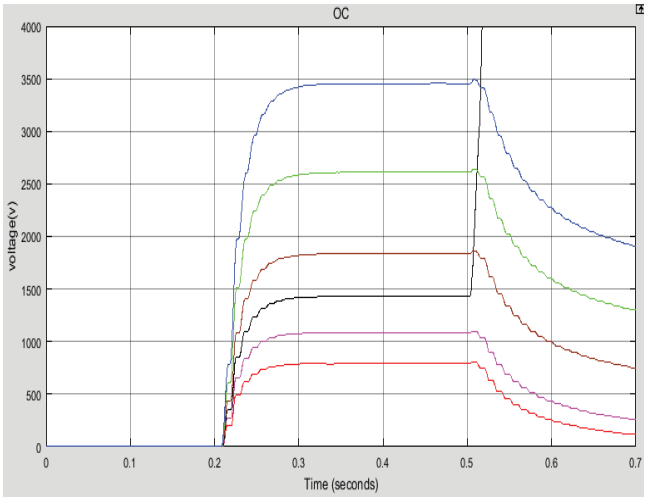

Figure 13. Capacitor voltages during open circuit fault condition.

The voltage across the 3rd H-bridge increases to finite value at t=0.5 sec that means at 0.5 sec the fault is detected. The per unit voltage values of capacitor during and after the open circuit fault can be seen in figure 13 and figure 14 during open circuit switch fault. Due to the existence of the fault in the system, per unit voltage of the system dropped down to certain value.

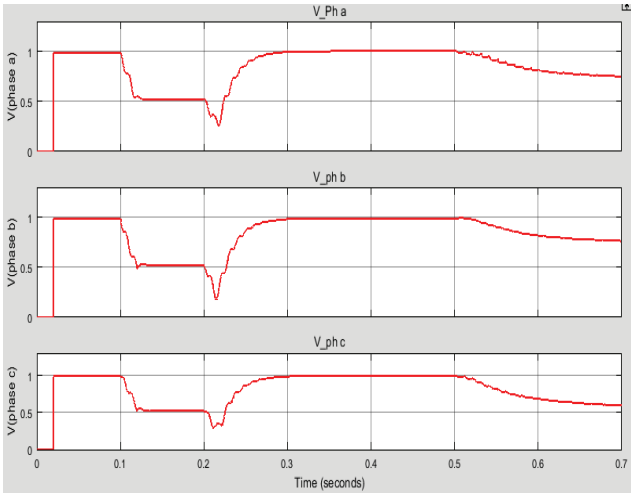

Figure 14. Magnitude of phase voltages during open circuit switch fault

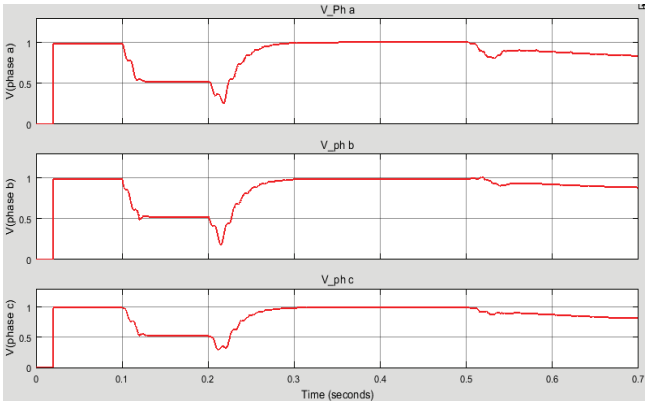

Figure 15. Magnitude of phase voltages in OC switch fault after feedback control circuit

For the injection of reactive power into the system the active power is completely maintained at zero so as to decrease the effect of source. At time interval 0.5sec there is a drop in the value of reactive power by 2MVAR which is due to the switching fault in the system in phase A.

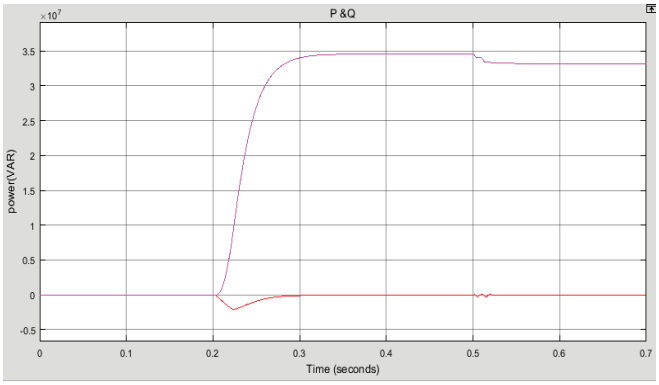

Figure 16. Active and Reactive power of STATCOM

C. *Results*

The following table I shows that comparison of percentage total harmonic distortion values of load voltages for different modulation methods before fault condition and after fault mitigation. From the below observation we can note that the total harmonic distortion in APOD is very less when compare to other PWM techniques.

TABLE I.
COMPARISON OF % THD VALUES OF LOAD VOLTAGES DIFFERENT PWM TECHNIQUES BEFORE, DURING AND AFTER FAULTS

S.NO	PWM TECHNIQUES	%THD LOAD VOLTAGES WITHOUT FAULTS	%THD LOAD VOLTAGES BEFORE FAULTS		%THD LOAD VOLTAGES AFTER FAULT MITIGATION	
			OC FAULT	SC FAULT	OC FAULT	SC FAULT
1	PD	4.26%	51.46%	5.57%	29.42%	5.57%
2	POD	4.78%	51.47%	5.60%	28.31%	5.60%
3	APOD	3.76%	51.26%	5.30%	28.10%	5.30%

VI. CONCLUSIONS

The switching faults in the proposed voltage source converter is detected and mitigated. The harmonic analysis is carried out using PD, POD, and APOD methods. Load voltages were compared by using respective mitigation techniques i.e. before faults and after faults. The THD after creating short circuit fault is said to be very minimal compared to that of open circuit condition and also it is observed that THD of APOD PWM technique is the lowest compared to the other two techniques.

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