Study of Star Connected Cascaded H-Bridge STATCOM using Different PWM Techniques

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Abstract: **Two control algorithms are presented in this paper for STATCOM that meets the requirement of load reactive power and correspondingly voltage balancing of isolated dc capacitors for H-bridge Inverters used in STATCOM. The control techniques used for an inverter in this paper are Sinusoidal Phase Shifted Carrier (SPSC) PWM and Space Vector Phase Shifted Carrier(SVPSC) PWM. The STATCOM performance for the different load changes is simulated in MATLAB environment. The performance parameters such as balancing the DC link voltage, THD for the STATCOM output currents, voltages, and reactive components provided to the load by the STATCOM are compared for both these control strategies.**

Index Terms: **Cascaded Multilevel Inverter, SPSC, STATCOM, SVPSC.**

I. INTRODUCTION

Recently, attention towards the quality of electric power has enhanced due to more preventive guidelines on this area. This curiosity has led to the innovations of multiple equipment, which could progress the energy transmission ability and quality of the voltage in the point of common coupling. These innovative devices are popular as Flexible AC Transmission System (FACTS), which are inventions of modern-power electronics. Considerable work has been carried out using these FACTS devices for high-voltage transmission [1]- [2]. Innumerable FACTS devices, like Static Synchronous Series Compensators (SSSCs), Static Synchronous Compensators (STATCOMs) and Unified Power-Flow Controllers (UPFCs) are extensively used in power systems to stabilize transmission ability of the power system and to enhance power quality in distribution system. STATCOM technology is progressively applied to enhance power transfer ability and improve voltage stability [3].

A STATCOM is fundamentally one of the shunt-type FACTS device. It is one of the inverter with dc-link capacitors on its dc side with control technology, and this device is connected in parallel with the grid. The STATCOM regulates the reactive-power flow in the power line, either by absorbing or injecting it. This reactive-power flow is controlled by regulating the output voltage of the STATCOM [4].

The development of present static switches (IGBT, GTO) and the evolution of new switching devices (IGCT, IEGT, etc.), usage of novel inverter topologies, have facilitated the enhancement in power and voltage ratings of the electronic converters. Because of this, in few situations the inverter may be connected directly to medium voltage buses without coupling transformer [5].

Nowadays multilevel inverters are widely employed for STATCOM as it can enhance the power capacity of the compensator, to make it appropriate for high or medium-voltage bulk power applications [6-7]. There are several types of multilevel inverter topologies used for implementing STATCOMs such as diode-clamped inverter, neutral point clamped inverter, and cascaded H-bridge multilevel inverter. Cascaded H-bridge topology is widely employed due to its several advantages: (1) it can produce nearly sinusoidal voltage waveform and diminishes harmonics, (2) it can respond faster since the removal of the extra transformer to provide the necessary voltage levels, (3) due to modularity in circuit the design and construction is simple [8-9].

Now days the cascaded H-bridge converters in each phase is replacing many other configurations for medium-voltage three-phase multilevel conversion system [10- 11]. This multilevel inverter is preferred as a substitute to the three-level neutral point clamped inverter [12] for variable-speed drive and STATCOM applications.

All the cascaded H-bridge inverters used in STATCOM application are furnished with floating and electrically isolated dc-link capacitors without having any power source in the circuit. This eliminates a large and expensive transformer from the cascaded H-bridge STATCOM. As an example, a 6.6 kV and 1 MVA three phase transformer weights from 3000 to 4000 kg, whereas similar rating three-phase cascaded H-bridge inverter weights from 1000 to 2000 kg only [13].

The problem associated with cascade STATCOM is unequal voltage distribution among all the floating dc-link capacitors. Inappropriate conduction of semiconductor devices, the switching losses in the switching devices employed in the circuit, as well as signal disparity, the resolution issues in the control circuit, and presence of current/voltage sensors, may results into voltage imbalance in the dc-link capacitors.

The converter used in STATCOM acts as an inverter and all the H-bridges produce three different levels of output voltages with the control of four switches. By regulating the phase angle between line voltage and the voltages generated by inverter, results STATCOM to absorb or supply reactive power to the load. The power supplied to a cascaded STATCOM from the dc source should be maintained equal. Therefore, all the H-bridge cells in the inverter are similarly operated. But, due to the semiconductor devices of the inverter are not ideal and have dissimilar acceptance errors, each DC-link capacitor voltages might not be accurately balancing. It is the main drawback for the cascaded H-bridge inverters employed for STATCOM, so it is essential required to use an extra control approach to equalize the DC-link voltages [14-17].

Numerous literatures have considered for the balancing of DC-link voltages of the cascaded H-bridge multilevel inverter. The distinct balancing control is combined with grouped balancing control for regulating DC-link voltages [18]. But, assigning appropriate values to gain parameters is not easy [18].

II. MODULATION STRATEGIES

Based on voltage control Cascade STATCOMs can be classified as pulse width modulation (PWM) and staircase modulation. More Investigations has been done in [17, 19-20] about the staircase modulation and PWM. Mostly PWM is chosen when a transformerless cascaded STATCOM is used. The foremost reason is that the 1.7 kV gate insulated bipolar transistors (IGBTs) may be functioned at a switching frequency higher than 1 kHz through a fewer switching losses. PWM is more advantageous for dynamic performance, more vigorous for line disturbances and faults, and more flexible in applications associated to staircase modulation.

A. Sinusoidal Pulse Width Modulation

Modulation process for multilevel inverters are based on carrier arrangements. The carriers shifted by horizontally is Phase Shifted Carrier PWM(SPSCPWM). Fig 1. Shows the arrangement of carrier and reference signals for the SPSCPWM technique. Mostly phase shifted carrier PWM is chosen for the cascaded multilevel inverters, due to this the power distribution among all the cells is uniform and this is easy to implement separately for any number of inverters. The PSCPWM technique results in the termination of all the carrier and connected sideband harmonics up to 2Nth carrier cluster, here N is the sum of H-bridges in each phase.

The Sinusoidal Phase-shifted carrier PWM having a carrier frequency of 1.2 kHz is applied to a group of two cascaded H-bridge inverters in each phase. Then, the output voltage of each group of H-bridges in a phase has 5-level line-to-neutral PWM waveform with the lowermost harmonic sideband centered at 4.8 kHz (= 1.2Khz x 2 x 2).

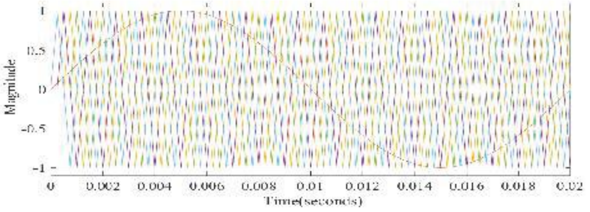


Figure 1. Carrier and reference waveform arrangements for a five level STATCOM with Sinusoidal Phase Shifted Carrier strategy

B. Modified Carrier-Based SVPWM

In the conventional SVPWM technique every outer sector must be mapped with inner sub hexagon sector to evaluate the switching time-period for multilevel inverters. The switching vectors related to the present sectors are turned on and the corresponding time periods are to be calculated from the mapped inner sectors. Because of the presence of more number of inverter sectors realizing this technique will be tough for multilevel inverters. The computational time-period is more in this method during real time implementation.

Before comparing with carrier signals, an appropriate offset voltage is to be added with sinusoidal reference to get the performance of SVPWM in the carrier based PWM technique [21-22]. The finding of offset voltage is contingent on modulus function which depends on the magnitude of DC-link voltage, the phase voltage magnitudes and the number of voltage levels.

A shortened method is defined, where accurate offset times periods are to be calculated for centering the time periods in a sampling interval for the middle inverter vectors. A technique is given in [23] for finding the maximum likely peak magnitude of the fundamental phase voltage in the linear modulation range. The subsequent equations are used to compute offset time $T_{offset.}$

$$T_a = \frac{V_a * T_s}{V_{dc}} \tag{1}$$

$$T_b = \frac{V_b * T_s}{V_{dc}} \tag{2}$$

$$T_c = \frac{V_c * T_s}{V_{dc}} \tag{3}$$

Here T_a, T_b, and T_c are the time periods of imaginary switching, related to the instant value of the reference phase voltages V_a, V_b and V_c.

T_s refers to the sampling time in the above equations.

$$T_{offset} = [\frac{T_0}{2} - T_{\min}] \tag{4}$$

$$T_0 = [T_s - T_{effect}] \tag{5}$$

$$T_{effect} = T_{\max} - T_{\min} \tag{6}$$

T_{max} = Maximum value of the three-phase reference voltages, in each sampling interval.
T_{min} = Minimum value of the three-phase reference voltages, in each sampling interval.

The switching vectors of the inverter are centered in a sampling time-period by the addition of offset voltage values to the reference phase voltages that equates the performance of SPWM technique with the SVPWM technique.

This proposed SVPWM signal generation does not involve look up table, identification of sector, angle information and voltage magnitude of space vector measurement for calculation of switching vectors for the conventional SVPWM technique for multilevel inverters. This technique is further effective when compared to conventional multilevel SVPWM technique. Fig. 2 shows the produced there-phase reference waveforms with the modified SVPWM technique. The generated reference waveforms are compared with triangular carrier signals to produce switching pulses for the switching devices. Fig. 3 Shows the arrangement of carrier and reference waves for the modified Space Vector Phase Shifted Carrier PWM technique.

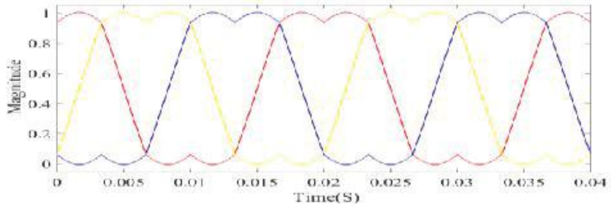


Figure 2. Reference signals for Modified SVPWM

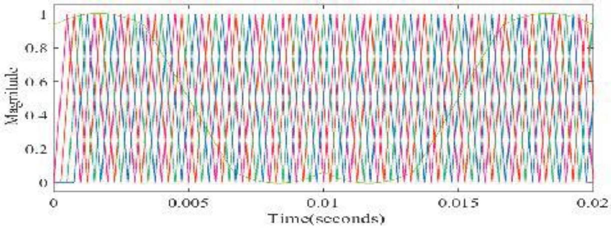


Figure 3. Carrier and reference waveform arrangements for a five level STATCOM with Space Vector Phase Shifted Carrier strategy

III. CONTROL STRATEGY FOR CASCADED FIVE LEVEL INVERTER BASED STATCOM

Fig. 4 shows the five-level cascaded H-bridge multilevel STATCOM. This STATCOM consisting of cascaded five level inverter, which is connected through coupling reactors to the grid. In this topology two single phase H-bridge inverter cells with capacitors as dc-link are connected in series to generate five levels of phase voltage. For an inverter, if N is number of H-bridges present in a phase and m is the number of voltage levels in a phase then the number of levels in phase voltage are 2N+1 and the number of levels in line voltage are 2m-1.

In the design of STATCOM, the three phase quantities v_a, v_b, v_c, i_{al}, i_{bl}, i_{cl}, i_{as}, i_{bs} and i_{cs} are source voltages, load currents and inverter currents, these are transformed in to v_d, v_q, i_{dl}*, i_q*, i_d and i_q in the synchronously rotating reference frame. The mathematical model of the cascaded inverter is transformed to the stationary rotating reference frame. Fig. 5 shows the control block diagram for the generation of reference voltages for various control techniques. The d - q axes reference voltage components of the inverter e_d and e_q are controlled as

$$e_d = x_1 + v_d - \omega L i_q \qquad (7)$$

$$e_q = x_2 + \omega L i_d \qquad (8)$$

Where v_d is the magnitude of source voltage component direct axis and i_d, i_q, i_{dl}*, and i_q* are d-q axes components of current of the inverter and load correspondingly.

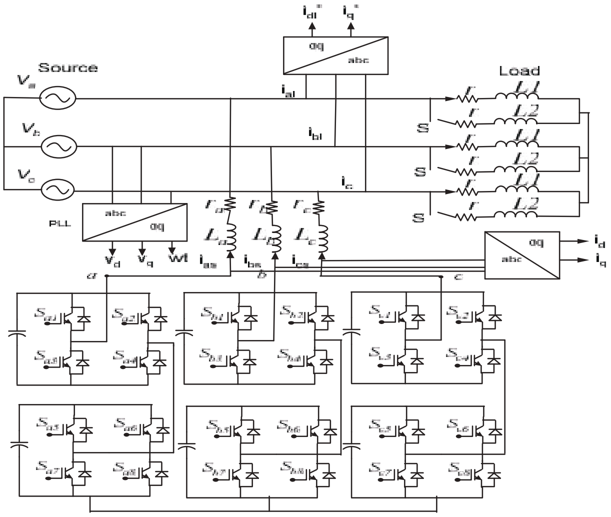


Figure 4. Cascaded multilevel STATCOM.

The synchronously rotating frame and source voltage vector are aligned together so that the q - component of the source voltage v_q is made zero. The control parameters x_1 and x_2 are controlled as

$$x_1 = (k_{p2} + \frac{k_{i2}}{s})(i_d^* - i_d) \qquad (9)$$

$$x_2 = (k_{p3} + \frac{k_{i3}}{s})(i_q^* - i_q) \qquad (10)$$

The d-axis reference current i_d* is

$$i_d^* = (k_{p1} + \frac{k_{i1}}{s})[(V_{dc}^*) - (V_{dc1} + V_{dc2} + V_{dc3} + V_{dc4} + V_{dc5})] \qquad (11)$$

Where V_{dc}* is the reference DC-link voltage and V_{dc1} to V_{dc6} are voltages across the DC-link capacitors in each H-bridge. The unit signals sinwt and coswt are generated by using Phase Locked Loop (PLL) block from the source voltages. The stationary reference frame quantities are converted in to synchronous rotating reference frame as

$$e_{ds} = (\cos\omega t)e_d + (\sin\omega t)e_q \qquad (12)$$

$$e_{qs} = -(\sin\omega t)e_d + (\cos\omega t)e_q \qquad (13)$$

From these synchronous rotating reference frame signals, the reference voltages to control the inverter are generated as

$$v_{ar} = e_{ds} \qquad (14)$$

$$v_{br} = -\frac{1}{2}e_{ds} + \frac{\sqrt{3}}{2}e_{qs} \qquad (15)$$

$$v_{cr} = -\frac{1}{2}e_{ds} - \frac{\sqrt{3}}{2}e_{qs} \qquad (16)$$

The switching frequency ripples in the inverter currents are removed by means of low-pass filter. From V_{dc}* and i_q* loops, the control block produces d-q axes reference voltages, e_d and e_q for the cascade multilevel inverter.

Fig 5. Shows the control block diagram to generate reference signals for the inverter. With these reference voltages, the inverter is controlled to supply the essential reactive currents to the load, and draws required active currents to control the dc-link voltage V_{dc}*.

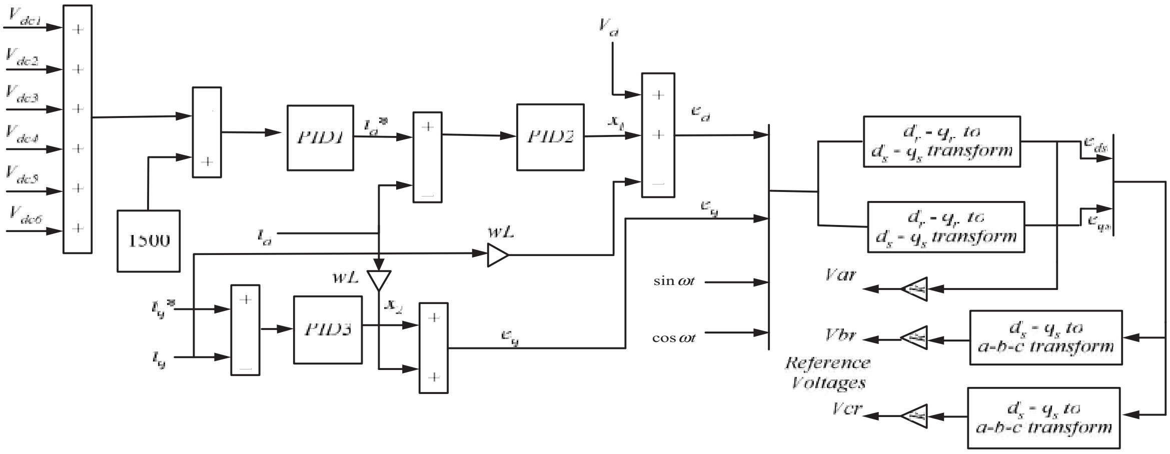


Figure 5. Control block diagram.

IV. SIMULATION RESULTS

The five level Cascaded Multilevel STATCOM is considered for simulation. The simulation of STATCOM is carried out using MATLAB/SIMULINK for different load changes. The inverter is controlled by using Sinusoidal Phase Shifted Carrier (SPSC) PWM, and Space Vector Phase Shifted Carrier (SVPSC) PWM techniques. The system parameters and PI controller parameters for voltage control, current control loops are shown in Table I and Table II respectively.

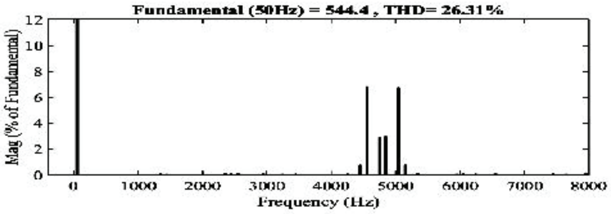
TABLE I
SIMULATION SYSTEM PARAMETERS

Supply Voltage	415 V RMS(Phase-Phase)
DC link voltage	250 V for both control techniques
Load Parameters	R = 4.6 Ω, L = 12.4 mH R = 4.6 Ω, L = 5.01 mH(for half load)
DC link capacitance	10 mF
Fundamental frequency	50 Hz
Switching frequency	1200 Hz
STATCOM Interfacing resistance	0.13 Ω
STATCOM Interfacing Inductance	2.19e-3 H

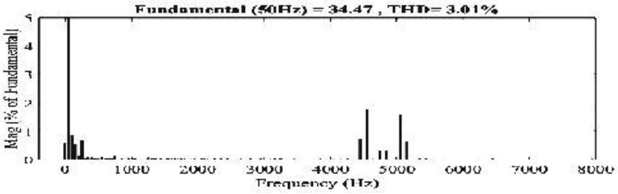
TABLE II
PARAMETERS OF PI CONTROLLERS

PI Controller	**Control Variable**	**Proportional Gain**	**Integral Gain**
PID1	Voltage	0.07	0.2
PID2	Voltage	0.08	0.2
PID3	Current	4	6

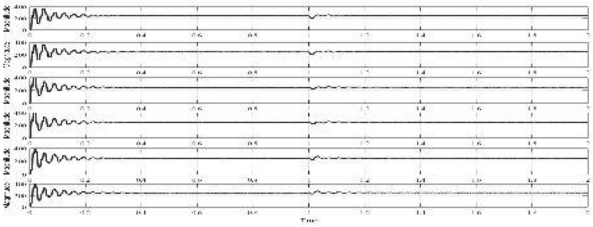
Fig. 6 shows the response of STATCOM for various performance parameters such as harmonic analysis of STATCOM output voltage and current, balancing the DC-link voltages for all H-bridges, Ripple content in DC- link voltage, comparison of reactive components required by the load and supplied by the STATCOM, and Phasor relations between Source voltage and STATCOM current for the variation of load from RL to RC at 1 sec by using Sinusoidal Phase Shifted Carrier PWM technique. It is observed that the STATCOM works perfectly for a reference DC link voltage of 1500 V, this voltage is equally distributed among all the DC-link capacitors of H-bridges and it is observed that the DC-link voltage is balanced for all types of load changes. Even if the load is changed suddenly also STATCOM supplies reactive components required by load. The ripple content in the DC-link voltage is low and it is around 9V. The harmonics in the output current is in the order of 3 % and in the voltage is 26.31%. And no harmonics observed below 4.8 kHz frequency due to SPSC technique. During the change of load from RL to RC the STATCOM currents is changed from lagging to leading with respect to source voltage. But during the change of load the inverter current magnitude values are almost double the normal value. After changing the load from inductive to capacitive at 1 sec, the reactive components supplied by the STATCOM changed from negative to positive, but to reach steady state it takes up to 3 sec.



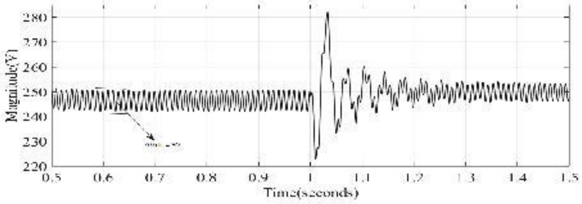
a) Harmonic analysis of STATCOM output voltage



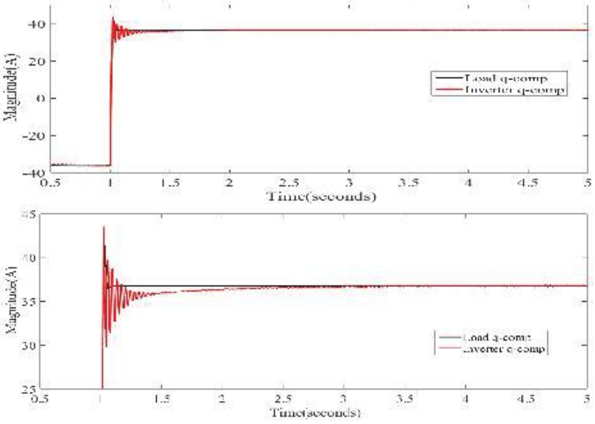
b) Harmonic analysis of STATCOM output current



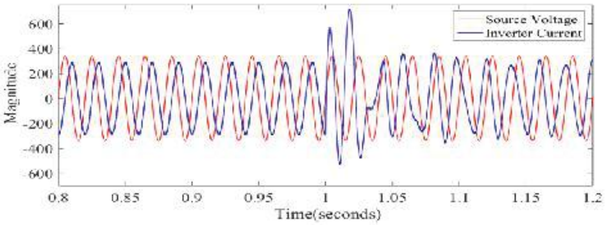
c) DC Link voltages



d) Ripple in DC link Voltage



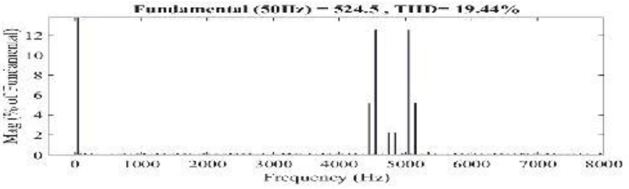
e) Comparison of load and inverter q-components of Currents



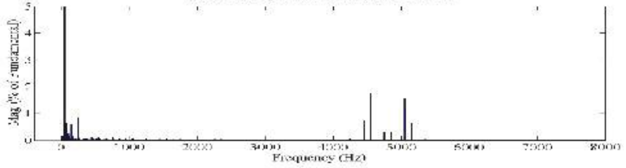
f) Source Voltage and STATCOM current

Figure 6. STATCOM response for variation of load from RL to RC at 1 sec with Sinusoidal Phase Shifted Carrier PWM

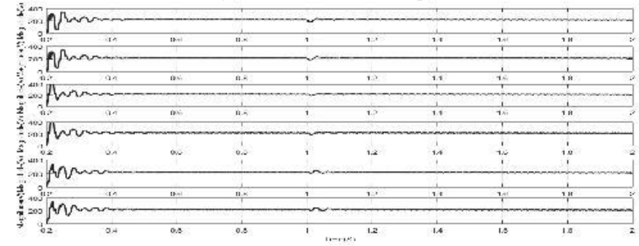
Fig. 7 shows the response of STATCOM for various performance parameters such as harmonic analysis of STATCOM output voltage and current, balancing DC- link voltages for all H-bridges, Ripple content in DC- link voltage, comparison of reactive components required by the load and supplied by the STATCOM, and Phasor relations between Source voltage and STATCOM current for the variation of load from RL to RC at 1 sec by using Space Vector Phase Shifted Carrier PWM technique. It is observed that the STATCOM works perfectly for a reference DC link voltage of 1500 V, this voltage is equally distributed among all the DC-link capacitors of H-bridges and the DC-link voltage is balanced for all types of load changes. If the load is changed suddenly also STATCOM supplies reactive components required by load. The ripple content in the DC-link voltage is low it is around 9V. The harmonics in the output current is in the order of 2.92 % and in the output voltage is 19.44%. And no harmonics observed below 4.8 kHz frequency due to Phase Shifted Carrier technique. After changing the load from inductive to capacitive at 1 sec, the reactive components supplied by the STATCOM changed from negative to positive, but to reach steady state it takes up to 2.5 sec.



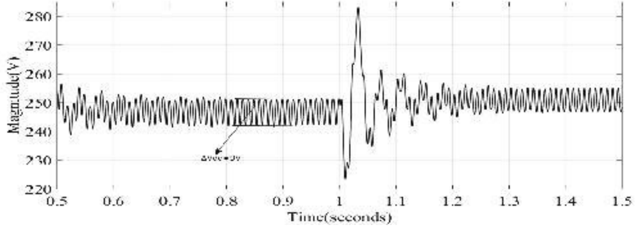
a) Harmonic analysis of STATCOM output voltage



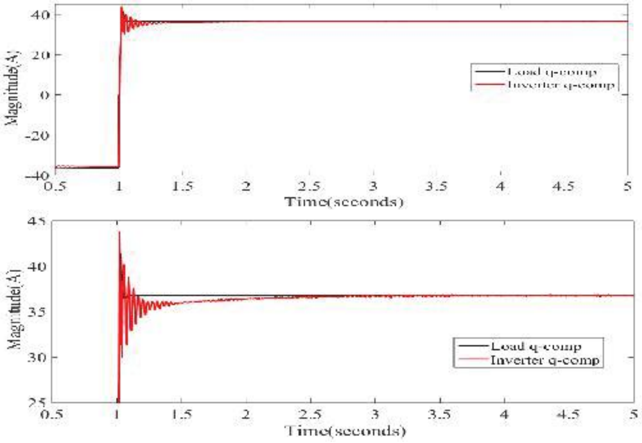
b) Harmonic analysis of STATCOM output current



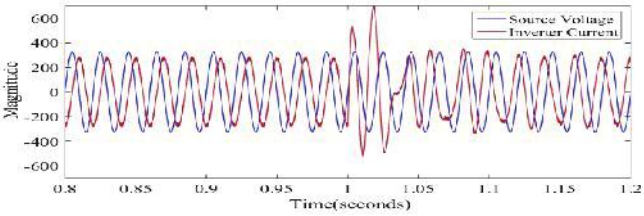
c) DC Link voltages



d) Ripple in DC link Voltage



e) Comparison of load and inverter q-components of Currents



f) Source Voltage and STATCOM current

Figure 7. STATCOM response for variation of load from RL to RC at 1 sec with Space Vector Phase Shifted Carrier PWM

V. CONCLUSIONS

The DC link voltage balancing is one of the major problems in cascaded multilevel STATCOM. In this paper, two control strategies are proposed for cascaded H-bridge five level based STATCOM. With these control strategies, the dc-link voltages of all the H bridges are balanced even if the STATCOM mode is converted from one load to another load. In all the circumstances, the reactive components required by the load are supplied by the STATCOM, and the harmonics in the inverter output current and voltage are reduced. The SVPSCPWM strategy gives 2.92% of harmonics in the output currents of the inverter and it gives 19.44% of harmonics in the output voltage which are less with respect to SPSCPWM technique. During the change of load the settling time required for the reactive components supplied by STATCOM is less in SVPSCPWM. Both methods give almost similar performance i.e harmonics in the output current, DC-link voltage balancing, and supplying of reactive components to load for different load changes.

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