Design and Implementation of Low Power Finite Impulse Response Filters

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***Abstract*— The Finite Impulse Response (FIR) filter is widely used in mobile and wireless applications. For these applications, the low power and low complexity FIR filter architectures are required. The FIR filter is most commonly used hardware block for signal processing in the above applications. The performance improvement of FIR filter is a great challenge. The researchers have proposed many FIR filters to meet above design specifications. In this paper, two different but efficient methods have been implemented in Xilinx software to improve the performance metrics in terms of speed, area and power. The target device is Spartan-3 Field Programmable Gate Array.**

The first FIR filter is implemented using a variable precision two dimensional fine grain pipeline technique. This technique is developed to improve the performance of the existing two dimensional pipeline gating. The second type of FIR filter is based on the technique of a Data transition Power Diminution Technique (DPDT). In this technique, the effective dynamic data ranges are determined and the unused functional blocks are not activated based on the input data. Due to the unused functional blocks, the power consumption is reduced.

***Index Terms* – FIR, DPDT, Low power, Pipeline gating, pipelining.**

I. Introduction

Finite-Impulse Response filters are important building blocks in many digital signal processing systems such as portable wireless systems, mobile phones and battery operated multimedia devices. The design metrics power, area and speed are considered as important parameters for Very Large Scale Integration (VLSI) architectures. The design methodology for high speed and low power is essential in the implementation of all Digital Signal Processing ICs. Generally, the power dissipation can be analyzed at different levels of the design process, such as algorithmic, architecture, circuit and device levels. The minimization of power dissipation depends on the selection of appropriate algorithms and mapping on to suitable architecture. The great extent of power can be reduced by the elimination of redundant and irrelevant computations in the particular system. The proposed architectures are implemented to reduce power dissipation, increasing the speed of operation and minimizing the area of the chip. The total power consumption of CMOS circuit is a combination of static power and dynamic power. Static power defined as the power consumed when the input signal is a constant value.

The dynamic power consumption is the power consumed when the transistors are active and the input signal change the state of the transistors frequently [1]. In the existing methods of FIR filters, lot of power is consumed because of the switching activities in the circuit. The dynamic power can be reduced by proper identification and suppressing the unnecessary activities in the circuit. The speed of the any architecture depends on the longest path delay of the combinational circuit, setup time of the sequential circuits and clock skew. This paper presents two efficient architectures for the solution of the above problems. Variable precision two dimensional fine- grain pipeline gating and Data transition power diminution techniques are working on the reduction of unwanted switching activities to reduce power consumption.

II. Variable Precision Two-Dimensional Fine Grain Pipeline

The variable precision two-dimensional fine-grain pipeline technique is used to reduce the power by decreasing the switching activities in the circuit. In this technique, pipelining is applied to the horizontal and vertical registers. The corresponding register clocks only gated using this pipelining method.

A) Two-dimensional pipeline gating

The two–dimensional pipeline gating technique is an earlier method of the variable precision pipeline gating technique [2]. In this technique, only horizontal clock gating is used to reduce the power consumption in the pipeline digital system. In the two-dimensional pipeline gating technique discussed by Di et al [3], clock gating is used in data path direction in the pipeline. This two- dimensional pipeline gating provides power awareness in the digital system. The global clock or system clock is distributed to the different blocks as a sub clock. This sub clock is based on the input data precision and is connected to one pipeline stage. Each sub clock is driven the registers, which are placed in the pipeline stage. The pipeline gating method based on the input data, disabling the stages, which are not used in the calculation. Those results are diverted to the final output by using multiplexer is shown in the figure.1. This technique decreases the pipeline latency and the power consumption. The power consumption is reduced due to the no transition in the masked pipeline stage. This technique disable the blocks according to the data flow. Here the delay is not fixed, so the gating cannot be applied for overall pipeline system. The pipeline system is implemented for

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fixed latency using clock gating in vertical and horizontal directions to reduce the further power reduction in the digital system. This technique is called variable precision two-dimensional fine grain pipeline gating.

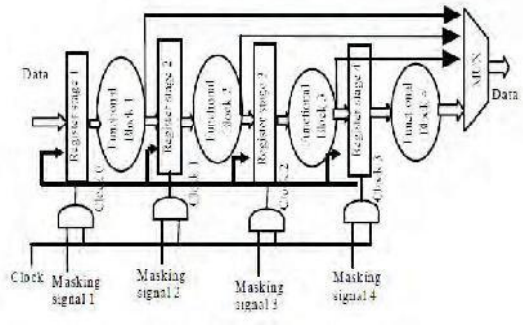

Figure. 1.Two-Dimensional Pipeline Gating Technique.

B) Variable precision two dimensional fine grain pipeline technique for FIR filter

In the variable precision pipeline method two extra features are considered, sub blocks pipelining to maintain the fixed latency and intra pipeline stage gating using variable precision. The variable precision pipeline requires similar additional hardware as conventional pipeline gating technique and with same latency reduction. This section presents the variable precision pipeline fine grain clock gating for multiplier and further FIR filters to reduce the power consumption. The figure. 2 present the variable precision fine grain pipelining for the multiplier. In the multiplier, the zero output-partial products are disabled based on the input combinations. In such case the registers connected to those blocks will not function during multiplication result calculation. The multiplexer selects the correct outputs from the corresponding stages only and remaining blocks clocks are disabled.

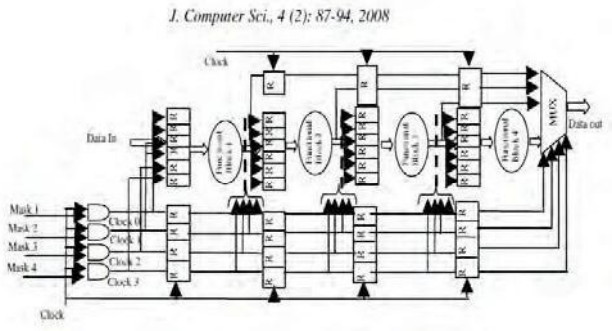

Figure. 2. Variable precision pipeline gating for multiplier.

A set of 8-bit variable precision fine grain pipeline multipliers were used to implement the 8- tap FIR filter and corresponding simulated output windows are shown in figures. 3&4.. In pipelining system, low power and high speed are two main advantages. In the FIR filters, multipliers and adders to be pipelined to improve the throughput [4]. The multiplication time (TM) much larger than the adder time (TA). Hence, proper balancing is required in pipelining stages to get the shorter critical path.

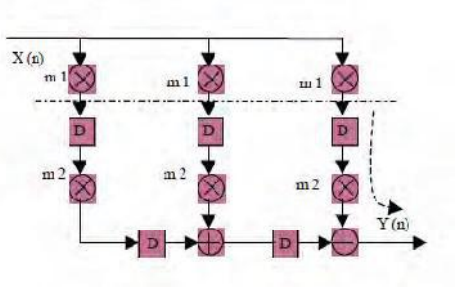

Figure. 3. FIR filter architecture using variable precision Adders and Multipliers.

In the FIR filter architecture, every multiplier is partitioned into two pipeline stages and some extra registers inserted between the sub stage multiplier. The multiplier time TM is divided by TM1 and TM2 and adder time is denoted by TA. If the input data length and the coefficients are small, then TA is enough to operate the filter in high sampling frequency. But, now a days, the FIR filter lengths are 8 to 16 bits and 32 to 64 bits also. For the long word length inputs, the adder also takes considerable time. Now, the pipeline adders are required with including pipeline multipliers for the FIR filter implementation. The pipelining of one adder alters the timing relationship between the two inputs of the next adder. But in the multipliers the relative timing sequence will not change. The pipelining adders are just adding the delay elements between the paths of adders. Hence, extra delay elements are inserted between the pipelined multiplier and its corresponding next adder..

A set of 8–tap variable precision pipelining FIR filter is designed. The variable precision multipliers and adders are used. The overall power consumption is reduced by using two dimensional fine grain adders and multipliers in FIR filter. These results are compared existing pipelining design in [4].

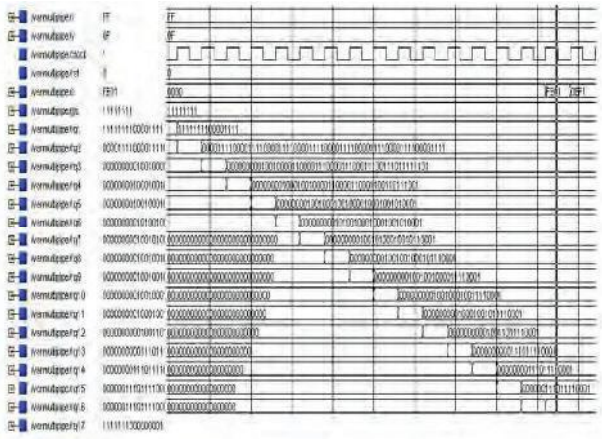

Figure. 4. Simulation Window of Variable Precision Two-Dimensional Pipeline Gating Multiplier

III. THE DATA TRANSISTION POWER DIMINUTION TECHNIQUE IN FIR FILTER

In this method, the data transition power diminution technique for adder, multiplier and FIR filters is introduced. This work is mainly based on the effective data range of arithmetic units. For this method, the Dynamic data range

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determination technique was proposed by Oscal et al [5], is used to reduce the switching activities and corresponding power in the arithmetic units.

The signal or bit switching activities of the two input data, changing from x(n-1) and y(n-1) to x(n) and y(n) respectively cause the switching power. Based upon the each input data, the input data can be divided into effective bits and non effective bits with respect to dynamic range. The entire switching activities are classified into four types, EE- Effective to Effective bits, EN-Effective to Non effective bits, NE- Non effective to Effective and NN- Non effective to Non effective bits. These switching activity styles are always represented in 2's compliment form. The EE, EN, and NE activities are represented in sign magnitude and hybrid, where as NN is represented in only sign magnitude form, because there is no sign extension bits. This proposed work is used to reduce the switching activities of EN and NN styles. [5].

The DRD technique for an adder is presented in the figure. 4. This method can be realized in the 2` compliment representation and sign magnitude representations. Initially, the effective dynamic ranges of every input date can be calculated and higher effective dynamic range will be considered. Hence few blocks of an adder used for the addition process and the result is scaled down for the matching of original word length according to its numerical representation. The less dynamic power is consumed by unused blocks of the adder. Here, the input bits of the unused adder blocks are unchanged states.

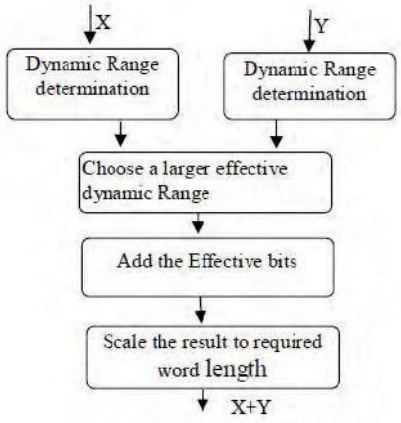

Figure 5. The DPDT for Addition.

For the case of NN, no switching activity and no switching power due to non effective bits of the side by side data are 0 only. The EE, EN, NE, and NN can have the switching activities in 2's compliment representation. The EE and NE are mainly for the DRD technique in the representation of 2's compliment form for the realization of sign magnitude. The NN origination from sign extension bits for the sign change. In the EN case, the switching activities are reduced . These are cannot be eliminated.

A) DPDT Adder Design

The next proposed technique is Data Transition Power Diminution technique (DPDT), which reduces the dynamic power dissipation by reducing the switching activity. The DPDT separates the entire designed circuit into two parts are MSP and LSP. These are most significant part and Least significant part. The MSP circuit turns off whenever they do not affect the results. The 16-bit two's complement adder using DPDT, shown in the figure. 5. In this, the 16-bit 2's complement adder is divided into MSP and LSP at the place between 8^{th} and 9^{th} bits. To control the input data of the MSP some latches are placed in the circuit. When the MSP is turned on, there is no change in the input data. If the MSP is turned off, the previous value is as input. This concept reduces the glitching power consumption. A control logic is required to know whether the MSP affects the computation results or not. This control logic helps to detect the effective ranges of the inputs.

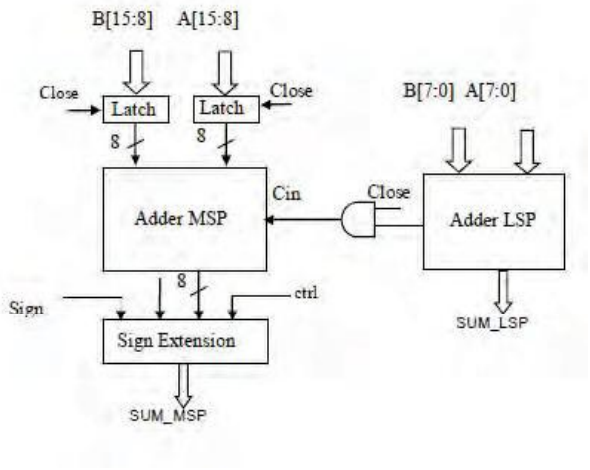

Figure 6. Two's Complement Adder based on DPDT.

B) Multiplier using DPDT

The multiplier design using DPDT is illustrated in the figure. 6(a) and 6(b). According to the Booth encoder, the partial product generator generates the five different partial products, i.e (-2A, -A, 0, A, 2A). These operations are selected and performed on operand B using the Booth encoding method. The partial products, P0 to P7 are accumulated by the adders A1, A2, D1 and D2. Here, the adders A1 and A2 are normal adders used in LSP. The D1 and D2 are DPDT adders, which are used in MSP. The second partial input to all adders are left shifted by 2 bits. The outputs are sign extended by 2bits [6].

The output of the first stage is given as input to the second stage. The output of this stage is sign extended to 4 bits. The output of the second stage is given as input to the third stage. The output of this stage is sign extended to 6 bits. If the Booth encoded value is the small absolute value, then the power dissipation due to data transition will be minimized in the compression tree. According to concept of the redundancy, some of the adders in the multiplier compression tree are replaced with the DPDT adders. The bit-widths of the LSP and MSP are indicated in fraction values nearing the corresponding adder in figure. 6 (b).

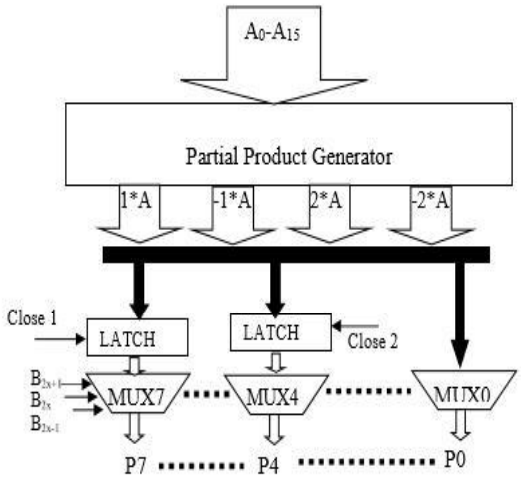

Figure. 7 (a) Booth multiplier using DPDT

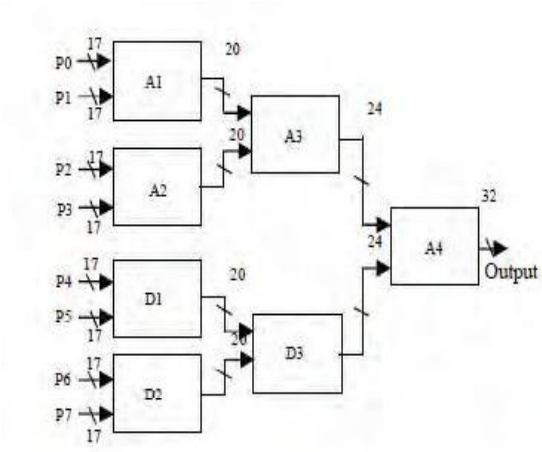

Figure. 7 (b). Low Power Multiplier using DPDT

C) Low-power digital filter design

The FIR filter is implemented using mainly three hardware elements namely, adder, multiplier and unit delay. The function of the unit delay is updating its output once per every sample period. The figure. 7 represents the DPDT low power direct form structure, which is implemented using DPDT adders and DPDT multipliers. The input sequence x(n) is first multiplied by the coefficient h0 using DPDT equipped multiplier [7]. The input sequence is then delayed by unit delay element. After being subjected to each delay, the input sequence gets multiplied by the other coefficients viz. from h1 to hM-1. The multiplied values are then added, to give the output y(n).

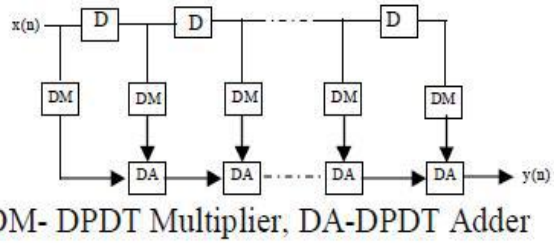

Figure 8. Direct Form Filter Structure using DPDT.

The figures 9 and 10 represents the simulated outputs for the 16 bit adder and FIR filter using DPDT technique.

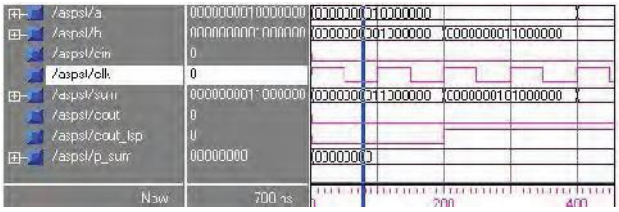

Figure 9. Simulation Result for 16Bit Adder using DPDT

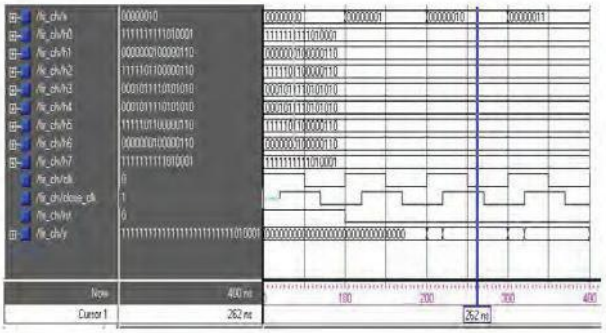

Figure 10. Simulation Result for FIR Filter with Booth multiplier using DPDT

IV. RESULTS

These methods are validated for the target device of Spartan-3 FPGA. The techniques are simulated and synthesized in Xilinx software. The significant high speed and power reduction over traditional Distributed Arithmetic based techniques. The results listed in the table. 1 depicts the performance metrics. Those are frequency, power, delay and area of the different efficient FIR filter architectures.

The bar graph shown in the figure. 11 represents the comparison of the FIR filter parameters. In this, the operating frequency of the variable precision fine grain pipelining FIR filter is comparatively high and delay is very less. The power consumption of this architecture is more than the DPDT FIR filter.

The area of the DPDT fir filter is larger than the Variable precision pipelining FIR filter architecture is shown in the figure. 12.

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TABLE.I
COMPARISON BETWEEN DIFFERENT FIR FILTER PARAMETERS.

	Variable precision pipelining FIR	DPDT FIR
Frequency (MHz)	81.6	25
Power (mW)	350	326
Delay (nS)	12.25	81.21
Area	12036 gate count	27622 gate count

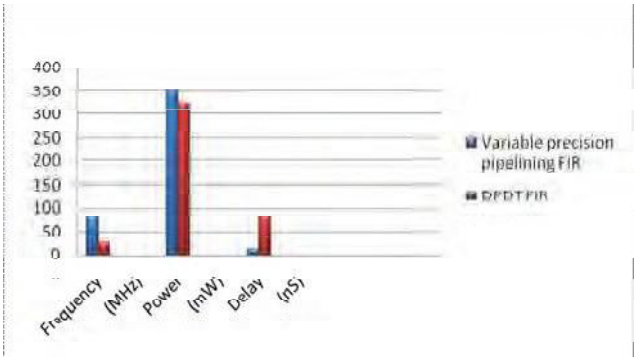

Figure.11 Bar graph for design parametrs of two FIR architectures.

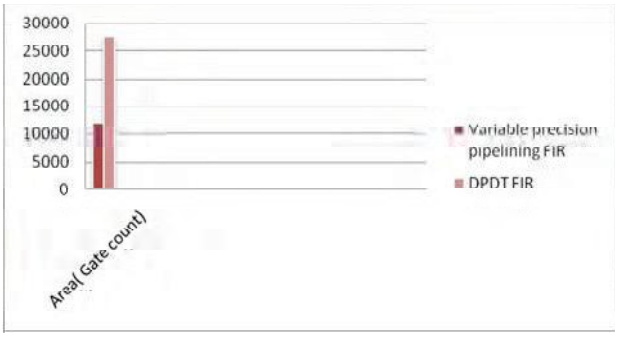

Figure.12 Bar graph for Area comparison of two FIR architectures.

V. CONCLUSIONS

In this paper, two types of efficient performance VLSI architectures required for digital signal processing are designed with different implementation techniques.

The variable precision two-dimensional fine grain pipelining in the FIR filter is discussed. The results-in comparison with the conventional existing techniques make it clear that the variable precision method reduces the power consumption by 18% with 3% additional area. But delay is very much less comparatively with other method. In the area wise, It is the second best architecture.

The second method, called data transition power diminution technique has been applied on adders, multipliers and FIR filter to reduce the power consumption. This FIR filter, using a Booth multiplier with DPDT has been implemented in FPGA. There is a decrease in power consumption, area and delay by 31%, 17.9% and 3%, respectively, when compared to the existing FIR filter, using normal Booth multipliers and normal adders.

For minimum power and high speed applications, the variable precision two dimensional fine–grain pipelining architecture can be preferred. Designing low power System-on-Chip (SoC) for multi-media applications where the less signal correlations, the DPDT is a better method. As DSP continues to make a major impact in many key areas of technology, the two methods have vast opportunities for expansion.

REFERENCES

[1] Michel Keating, David Flynn, Robert Aitken, Allen Gibbons and Kaijian shi (2007), 'Low Power Methodology Manual for System on Chip Design', Springer, New York, USA.

[2] Hoang, Q.D., B.R. Zeydel and V.G. Oklobdzija, 2006. Energy optimization of pipelined digital systems using circuit sizing and supply scaling. IEEE Trans. VLSI Syst., 14: 122-134.

[3] Di, J., J.S. Yuan and R.F. De Mara, 2006. Improving power-awareness of pipelined array multipliers using 2-dimensional pipeline gating and its application to FIR design. Integration the VLSI Journal.,39(2):90-112.doi:10.1016/j.vlsi.2004.08.2

[4] Senthil Kumar A. and Natarajan A.M. (2008), 'FPGA Implementation of Power Aware FIR Filter Using Reduced Transition Pipelined Variable Precision Gating', Journal of computer science, Science Publication (JCS) , USA, Vol. 4, No. 2, pp. 87-94.

[5] Oscal T.C.C., Sheen R. and Wang S. (2002), 'A low-power adder operating on effective dynamic data ranges,' IEEE Transaction on Very Large Scale Integration (VLSI) System., Vol. 10, No. 4, pp. 435-453.

[6] Chen O., Wang S. and Wu Y.W. (2003), 'Minimization of switching activities of partial products for designing low-power multipliers', IEEE Trans. Very Large Scale Integration (VLSI) Syst., Vol. 11, No. 3, pp. 418–433

[7] Chen K.H, Chao K.C., Guo J.I., Wang J.S. and Chu Y.S. (2007), 'A low power Multiplier with the spurious power suppression technique 'IEEE transaction on very large scale integration (VLSI) systems,pp.846-850.