Power Saving and Delay Analysis of Adder Circuit using Adiabatic Logic

A.Anitha
Sr. Asst. Professor, CVR College of Engineering /ECE Department, Hyderabad, India
Email: anitha90@yahoo.com

Abstract— In the implementation of all Integrated circuits (IC), the design parameter power consumption is considered as important parameter. It is considered as top design challenge among all the challenges in the international Integrated Circuit (IC) roadmap technology. The implementation of low power VLSI circuits has been emerged as they are very high in demand because of the rapid growth in technologies.

In the IC chips the transistor count is increasing rapidly and proportionally, as the semiconductor technology entered into nanotechnology scale. The portable and smart electronic gadgets requires more energy efficiency and compact in size. But this improvement increases the clock speed to satisfy the above specifications. Hence, the dynamic power dissipation of the circuits increased. The portable electronic gadgets that are always require high speed clock.

Due to this high speed of the clock the dynamic power dissipation is increased in the VLSI circuits. In the conventional Complementary Metal Oxide Semiconductor (CMOS) techniques, the power dissipation is minimized by supply voltage reduction, reducing the activity of the transistor switches and by considering the less load capacitance. These techniques will be useful to reduce some part of the power dissipation only and still power dissipation is taken place. The further power dissipation can be reduced using adiabatic logic technique.

This paper has presented all the gates (NAND, NOR etc.) implementation using adiabatic logic. The complex circuits such as, full adder and a Carry Look ahead Adder (CLA) circuits are implemented using adiabatic 2PASCL topology and also implemented in conventional CMOS technology. All these implementations are done in 180nm technology using VLSI full-custom cadence tools. The results of the above circuits are compared in terms of delay and power consumption. The comparison states that, the adiabatic logic circuits consume less power with little bit penalty of delay.

***Index Terms*—CMOS logic, adiabatic logic, 2PASCL, power.**

I. Introduction

The word adiabatic is derived from thermodynamics that logic is preferably used to reduce the energy consumption. This process do not use the exchange of heat with the external environment. The main principle of the adiabatic logic is energy reusing. Basically, the stored energy in the capacitor discharging through the ground. But, in this adiabatic logic, this energy is reused itself. The power wastage is taken place in the traditional concept. In adiabatic technology, due to the reusing power saving taken place and power dissipation reduces. This adiabatic logic increases the circuit complexity with advantage of low power [1].

Mainly, there two types of adiabatic structures are mostly used. Those are fully adiabatic logic structure and second is semi or partially adiabatic structures. The design of fully adiabatic logic circuits is very complex due to the complex clock tree design. The advantage of this logic is no losses are occurred. The counterpart, the non-adiabatic logic circuits provides many losses, but design of this style is easy. The trapping of charge at nodes only treated as losses in this structure [2][3].

In the recent years, many adiabatic logic methods are emerged to reduce the power dissipation. Some of them are, trapezoidal waveform at the power supply and QSERL is one of the adiabatic technique that uses two sinusoidal waves, which are 180^{o} phase shift to each other [4]. This technique may consist some limitations regarding to nodes with floating, depletion region of the node capacitor and fan in and fan-out. In some gate implementations, the diodes are needed. These diodes also degrade the output levels and provide power dissipation issues.

Practically, the power or energy consumption associated with charging or discharging of the capacitors in adiabatic components. Hence, the reduction of complete power dissipation may not possible. The adiabatic logic switching approach is conserves the complete energy. But, in the other logics the energy is converted into heat. Hence, these adiabatic type of approaches are used to reduce the power dissipation in digital circuits based on requirements and applications.

A. Conventional Switching

In CMOS circuits, the Dynamic and static power dissipations are mainly contribute for the total power dissipation. The magnitude of the dynamic power dissipation in any circuit is depends on the load capacitance charging and discharging. The static power never depends on the signal switching, which depends on the static current flowing between the power rails. Whenever short circuit is taken place based upon the logic states between VDD and GND, large static current flows and causes to produce more static power dissipation.

The static power dissipation mainly depends on the leakage currents. These leakage currents may be diode leakage, gate oxide leakage and sub-threshold leakage currents. In deep sub-micron technology, the leakage power is the dominant to produce static power dissipation. The expression for the leakage power is given by equation (1)

$$P_{lkg} = I_{lkg} \times V_{dd} \quad (1)$$

During charging of the capacitor the total energy supplied by the power supply CV_{dd}. The 50% of the power is dissipated in the PMOS transistor and its interconnect and remaining 50% power is dissipated or stored in the load capacitor C_L. The load capacitor stored energy is dissipated through the NMOS interconnect as represented in the Figure. 1. Due to the slowly varying of the input signal transitions, the short circuit power dissipation occurs. At that time large static current is flowing through the power rails. That means a short connection is taking place between VDD and GND. The Figure.1 shows the equivalent circuits for the

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charging and discharging of the CMOS logic circuit. The overall power dissipation is determined by equation (2).

$$P_{total} = CV^2 df_{clk} + I_{sc} + I_{lkg}V_{dd} \quad (2)$$

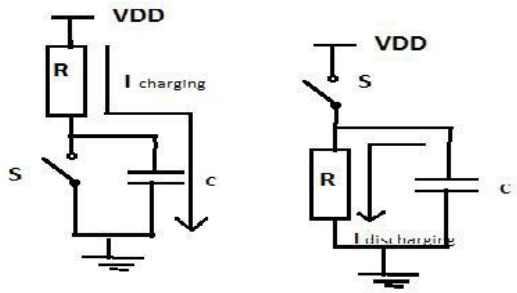

Figure. 1 Conventional CMOS switching.

II. Adiabatic Switching

In this section the adiabatic switching technique to minimize power consumption in VLSI circuits. The time constant RC of the adiabatic logic circuit is very much less than the ramp time period T. i.e., RC << T. Due to this condition, the voltage across the capacitor is nearly follows the VDD supply voltage. Then potential difference is almost zero across the resistor R. The voltage of the capacitor Vc is constant ramp with proportional with slope V/T. Here V means supply voltage and T is the Clock period of the power. The adiabatic circuit charging current and energy dissipated in the resistor are given by the following equations (3) & (4) respectively.

$$i_c = C\frac{dVc}{dt} = \frac{CV}{T} \quad (3)$$

$$E = i_c^2 RT = \frac{(CV)^2}{(T)^2} RT = \frac{RC}{T}CV^2 \quad (4)$$

The Figure. 2 represents the discharging equivalent circuit in the adiabatic switching technique. This is also same as the capacitor charging. But, the voltage in the power supply downs like ramp due to RC << T, and the equation is given by

$$E = \frac{RC}{T}CV^2 << \frac{1}{2}CV^2 \quad (5)$$

This explanation states that the energy of the capacitor is more than the resistor power consumption during the time of capacitor charging and discharging of the capacitor. While the capacitor discharging, the reusing of energy in the capacitor is taken place using returning of supply voltage concept [5][6].

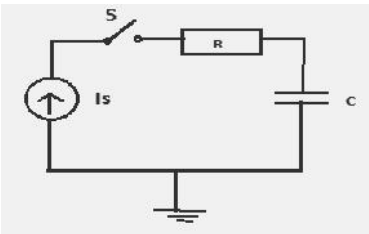

Figure.2 Adiabatic Switching

A. 2PASCL Circuit

The adiabatic logic family is a Two Phase clocked Adiabatic Static CMOS Logic (2PASCL). It contains extra two more transistors only comparatively normal adiabatic logic. In this logic, one transistor is placed in between the Power clock and output terminal. The other transistor is placed beside of the NMOS transistor or pull down logic, which is connected to the other power supply. In this technique, the supply voltage Vdd is replaced by PHI and ground terminal connection Vss is replaced by PHI_BAR respectively. In this method, two complimentary split level sinusoidal wave are used for power clock generation.

The adiabatic circuit operation is divided as two modes, One is evaluation mode and second is Hold phase [7][8]. In the evaluation phase, initially the Pmos logic is turned on. After that, the output becomes low and Load capacitor gets charged for VDD through Pmos transistor and output becomes high logic level. If Nmos transistor is on, the output node Y becomes low and no transition. Whenever, the output node is high the corresponding transistor i.e Pmos also turned on and there is no any transition. Finally, if output node is high, then the corresponding Nmos transistor turned on, discharging is taken place and diode D2 makes the output is low.

In the hold phase, if the output node Y is low, then the transistor NMOS switches to ON, that means no transition. Suppose, the node y is high then the PMOS becomes on then discharging taken place via the diode D1is shown in the Figure 3.

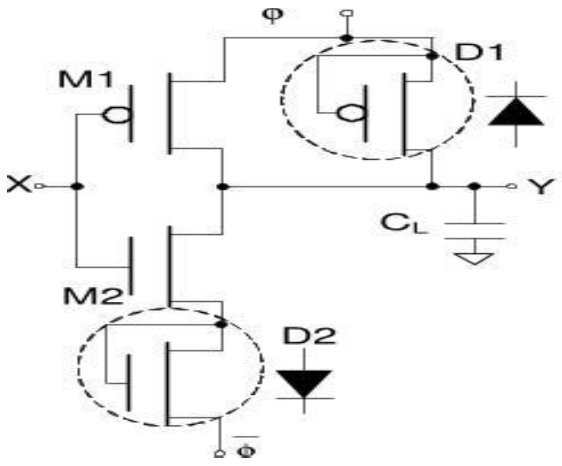

Figure.3 2PASCL Circuit.

III. Simulations and their results

The following Figures from Figure. 4 to Figure 39 are schematics, input and output waveforms, power and delay analysis of NOT, NAND, NOR, EXOR gates, full adder and a 4-bit Carry Look ahead Adder (CLA) circuits [9],[10],[11] using CMOS and adiabatic 2PASCL topology implemented using cadence virtuoso tool in 180nm technology.

Figure 4,5,6 are the schematic diagram, input, output waveforms, power analysis and delay analysis of CMOS inverter circuit.

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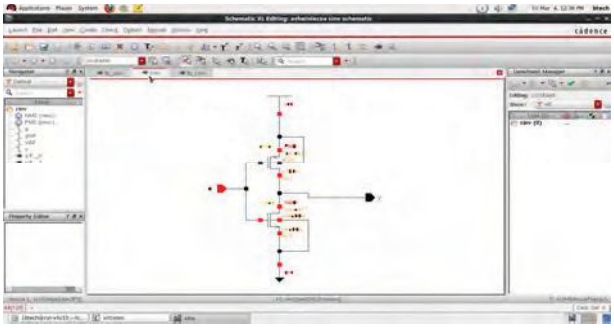

Figure.4 CMOS Inverter Schematic

Figure.5 CMOS Inverter Input ,Output waveforms and Power analysis

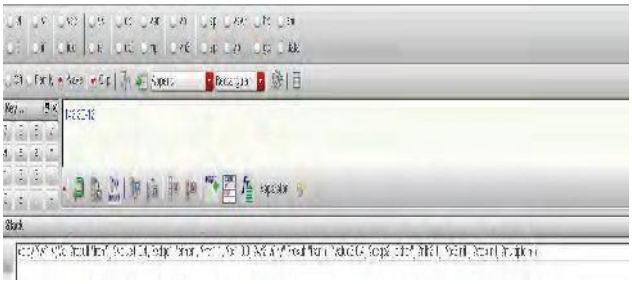

Figure.6 CMOS Inverter Delay analysis.

Figure 7, 8, 9 are the schematic diagram , input, output waveforms , power analysis and delay analysis of adiabatic inverter circuit.

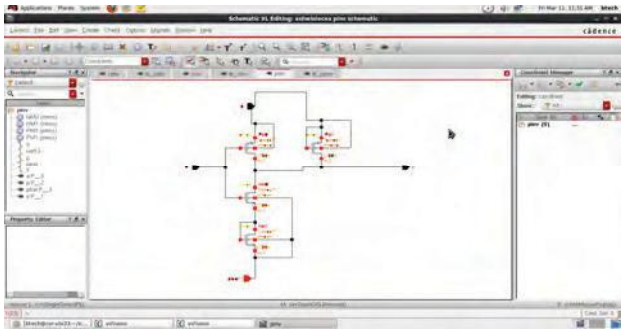

Figure.7 Adiabatic Inverter Schematic

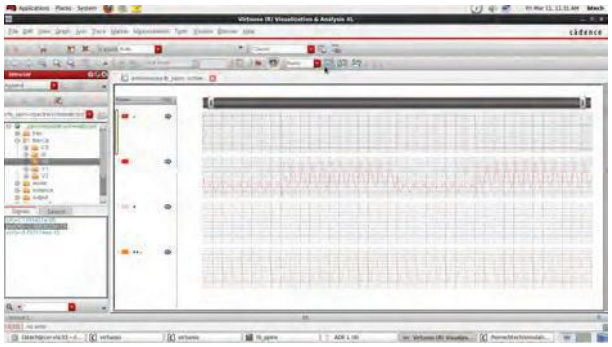

Figure.8 Adiabatic Inverter Waveform & Power

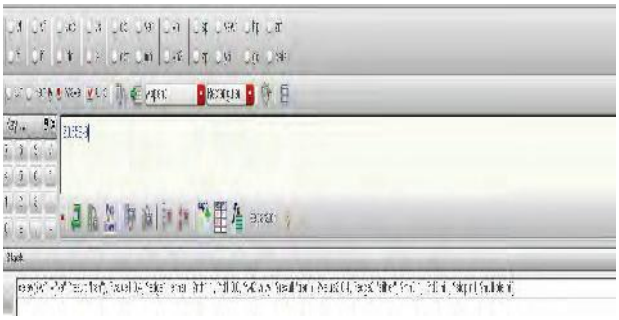

Figure.9 Adiabatic Inverter Delay

Figure 10,11, 12 are the schematic diagram , input, output waveforms , power analysis and delay analysis of CMOS NAND gate circuit.

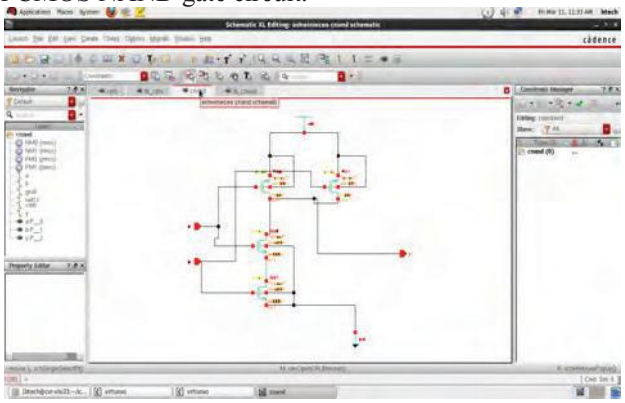

Figure.10 CMOS NAND Gate Schematic

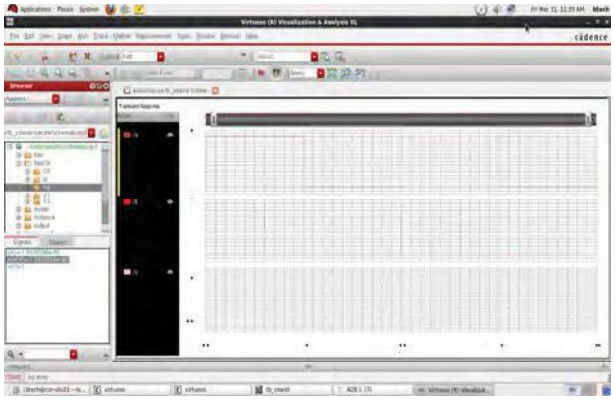

Figure.11 CMOS NAND Gate Input, Output Waveforms and Power

Figure.12 CMOS NAND Delay

Figure 13,14, 15 are the schematic diagram , input, output waveforms , power analysis and delay analysis of Adiabatic NAND gate circuit.

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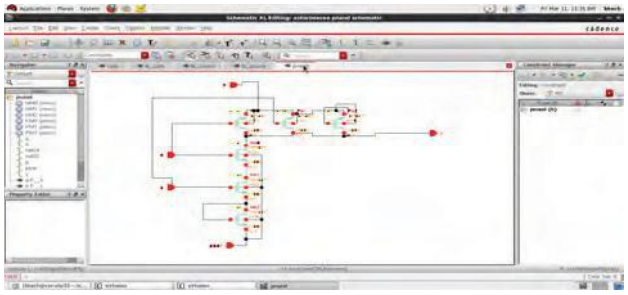

Figure.13 Adiabatic NAND Schematic

Figure14. Adiabatic NAND Waveforms and Power

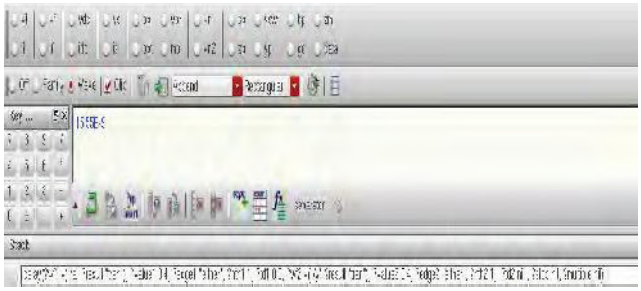

Figure.15 Adiabatic NAND Delay

Figure 16,17, 18 are the schematic diagram , input, output waveforms , power analysis and delay analysis of CMOS NOR gate circuit.

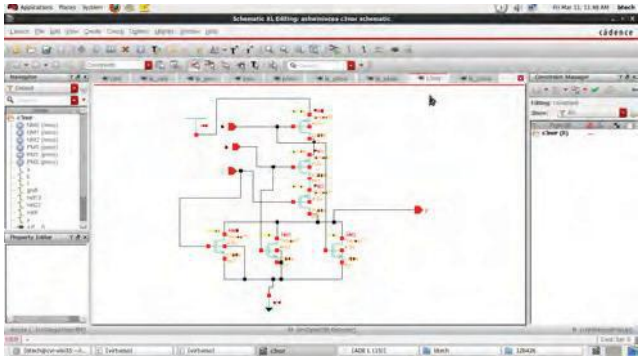

Figure.16 CMOS NOR Schematic

Figure.17 CMOS NOR Waveforms and Power

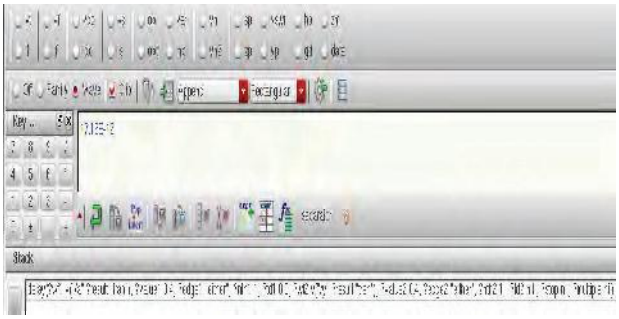

Figure.18 CMOS NOR Delay

Figure 19,20, 21 are the schematic diagram , input, output waveforms , power analysis and delay analysis of Adiabatic NOR gate circuit.

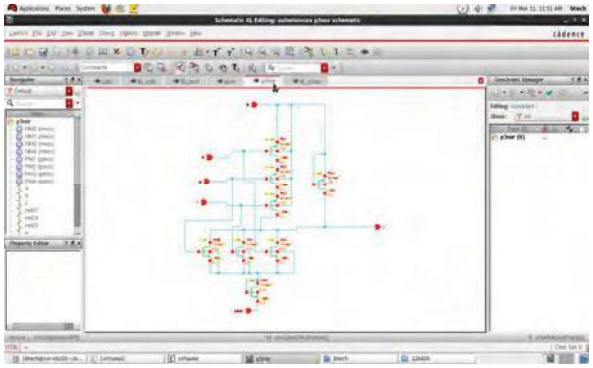

Figure.19. Adiabatic NOR Schematic

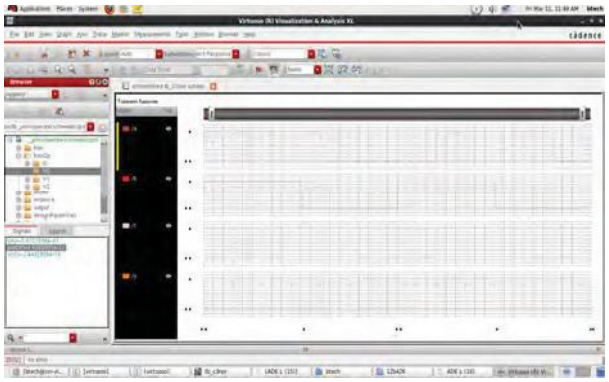

Figure.20 Adiabatic NOR Waveforms and Power

Figure.21 Adiabatic NOR Delay

Figure 22,23, 24 are the schematic diagram , input, output waveforms , power analysis and delay analysis of CMOS EXOR gate circuit.

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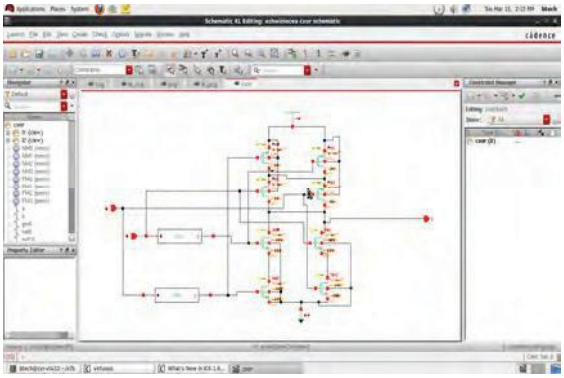

Figure.22 CMOS EXOR Schematic

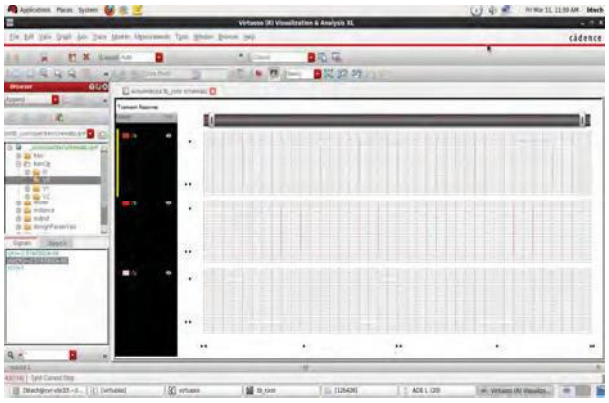

Figure.23 CMOS EXOR Waveforms and Power

Figure.24 CMOS EXOR Delay

Figure 25,26, 27 are the schematic diagram , input, output waveforms , power analysis and delay analysis of Adiabatic EXOR gate circuit.

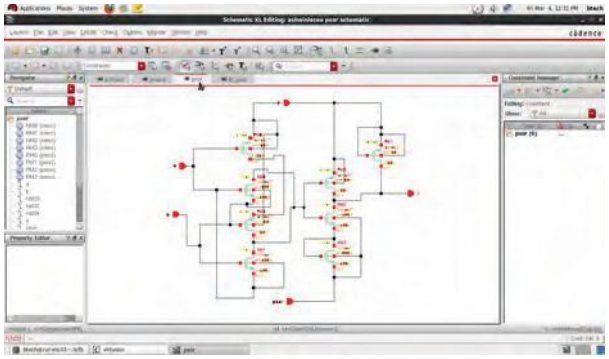

Figure.25 Adiabatic EXOR Schematic

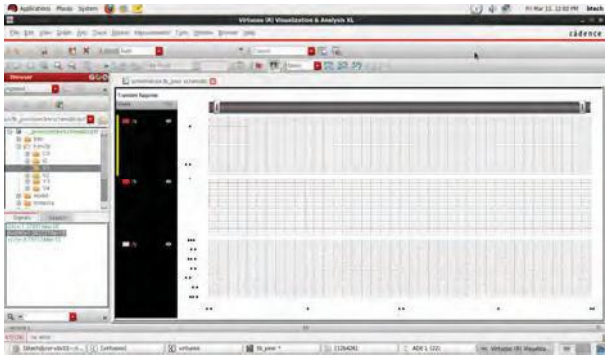

Figure.26 Adiabatic EXOR Waveforms and Power

Figure.27 Adiabatic EXOR Delay

Figure 28,29, 30 are the schematic diagram , input, output waveforms , power analysis and delay analysis of CMOS Full Adder circuit.

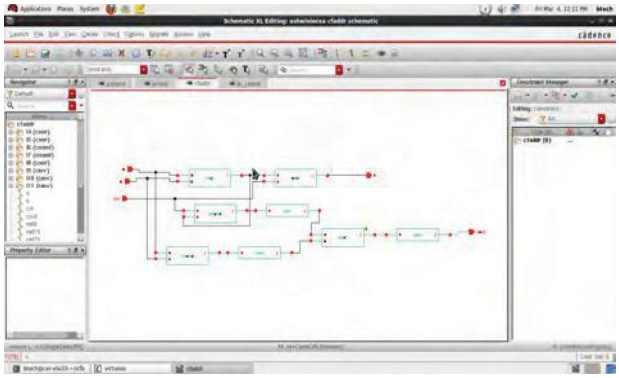

Figure.28 CMOS Full Adder Schematic

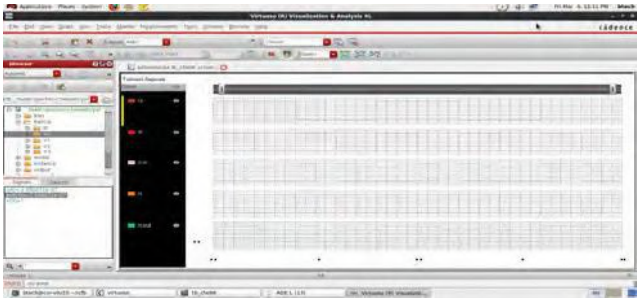

Figure.29 CMOS Full Adder Waveforms and Power

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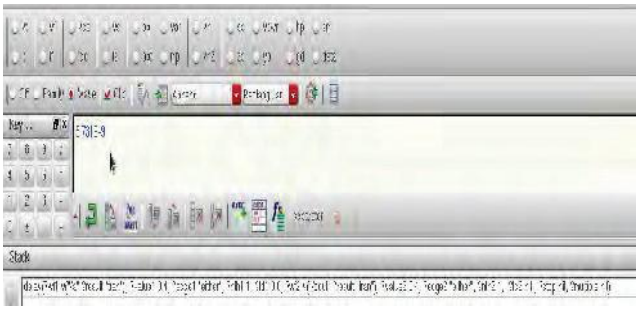

Figure.30 CMOS Full Adder Delay

Figure 31,32,33 are the schematic diagram , input, output waveforms , power analysis and delay analysis of Adiabatic Full Adder circuit.

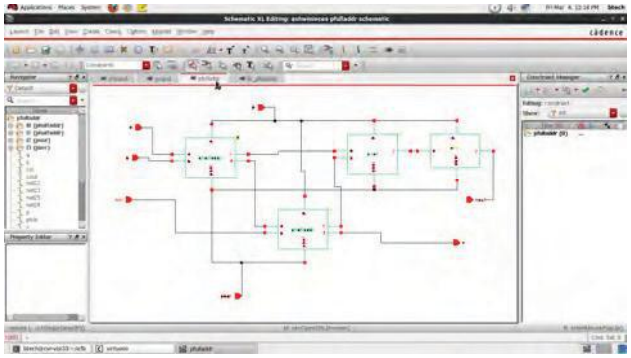

Figure.31 Adiabatic Full Adder Schematic

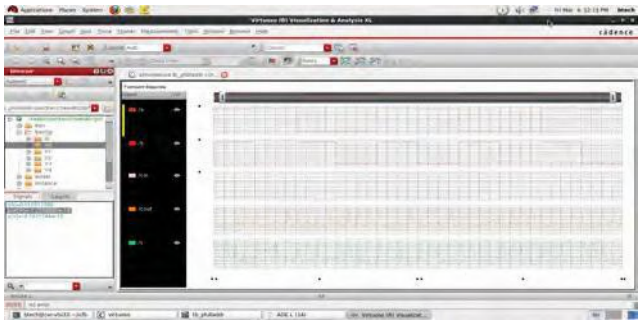

Figure.32 Adiabatic Full Adder Waveforms and Power

Figure.33 Adiabatic Full Adder Delay

Figure 34,35,36 are the schematic diagram , input, output waveforms , power analysis and delay analysis of CMOS CLA Adder circuit.

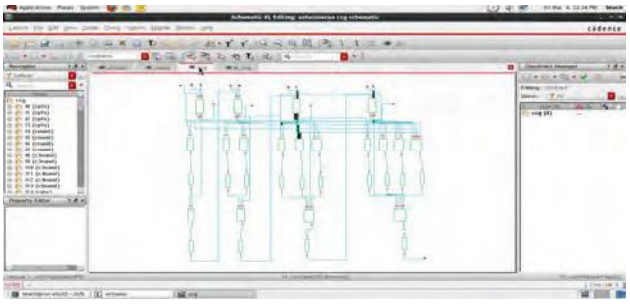

Figure.34 CMOS Carry look ahead adder Schematic

Figure.35 CMOS Carry look ahead adder Waveforms and Power

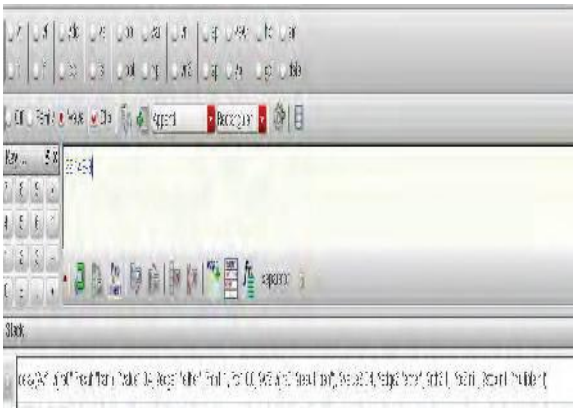

Figure.36 CMOS Carry look ahead adder Delay

Figure 37,38,39 are the schematic diagram , input, output waveforms , power analysis and delay analysis of Adiabatic CLA Adder circuit.

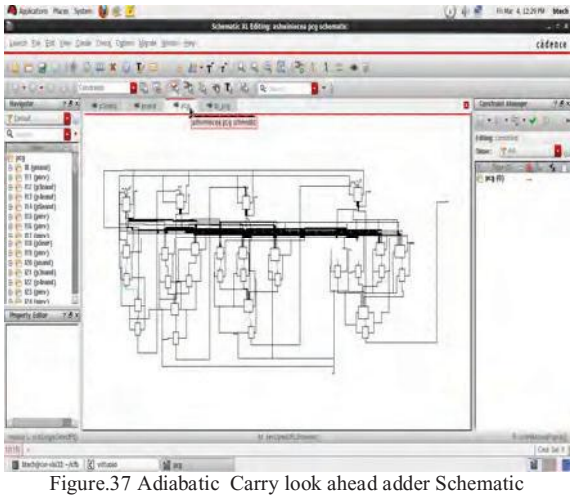

Figure.37 Adiabatic Carry look ahead adder Schematic

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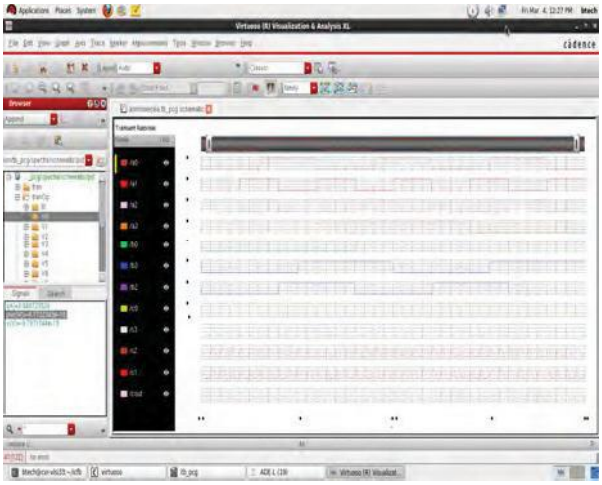

Figure.38 Adiabatic Carry look ahead adder Waveform and Power

Figure.39 Adiabatic Carry look ahead adder Delay

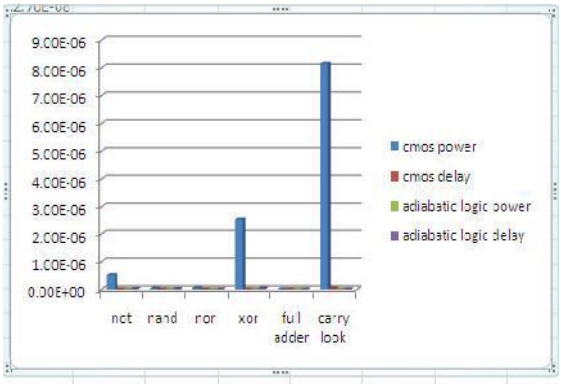

Figure. 40 Bar graph comparison of delay, power of CMOS and Adiabatic logic

TABLE I.
POWER AND DELAY OF CMOS AND ADIABATIC LOGIC

Circuit	Conventional CMOS		Adiabatic Logic	
	Power	Delay	Power	Delay
Inverter	5.44E-07	1.43E-10	6.02E-20	2.05E-08
Nand	3.16E-08	2.58E-10	3.59E-19	1.55E-08
Nor	4.19E-08	1.72E-11	4.60E-19	1.48E-11
Xor	2.57E-06	5.30E-09	1.37E-19	2.70E-08
Full Adder	1.39E-19	5.07E-10	1.38E-19	5.70E-09
Carry Look Ahead Adder	8.15E-06	2.21E-08	4.78E-16	2.68E-10

IV. CONCLUSIONS

In this paper, the logic gates are implemented by adiabatic logic techniques are fully compared with the traditional CMOS logic gates in terms of power and delay. The complex circuits such as, full adders and CLAs also implemented using adiabatic logics and compared with CMOS adders. The power dissipation of the adiabatic circuits are very much less comparatively the CMOS circuits as shown in table.1. The bar graph also shows the power dissipation of the adiabatic logic circuits on Figure 40. Results further affirm that with higher the load capacitance, the power dissipation in the 2PASCL circuits still remain low. From the above simulation results, the 2PASCL circuits consume less power comparatively static CMOS circuits. Finally, these adiabatic logic circuits are fit for the low power VLSI designs. However, in these circuits the delay is little bit increased.

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