Validation of Diagonal Power Routing Approach in Very Large Scale Integration Design for Better Prospects over Orthogonal Routing at Nanometre Era

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Abstract: This paper focuses on top metal layer routing in very large scale integration design in nanometre era, to show that the diagonal routing approach has improvised prospects than the existing orthogonal power routing approach. In this paper, the proposed diagonalised routing and orthogonal routing for an operational amplifier, and both routing techniques are incorporated with HVT swapping. In addition to this diagonal routing implementation, some parameters get affected, i.e., power, delay and length etc. This approach is meant for specific limitation of application areas in very large scale integration design.

Index terms: Diagonal routing, orthogonal routing, operational amplifier, high voltage threshold (HVT)

I. INTRODUCTION

The overall capacity of a chip depends on less glitch, IR drop reduction, compact Area and reduction in delay of the circuit. One approach to reduce the effect of these parameters is by using a top metal layer arrangement. In this approach, metal layer values and design aspects are optimum. Both Manhattan and non Manhattan interconnect routing architectures are implemented with the ACO algorithm [1]. When SSN is produced during the transmission of the signal from one node to other nodes and due to return path currents, led to malfunctioning and degraded performance of the the power distribution in VLSI circuits and it became a challenging issue due to the severe switching noise on the power distribution network. Hence, estimation of the worst case switching noise is essential to ensure the proper functionality of the VLSI circuits [3]. For the varying rise and fall times intended to reduce the performance at high frequency of operation [4, 5]. The IR drop power routing at physical layout is more important to simulate expected outputs in the sense of reducing dreadful conditions of the system. In many cases, researchers investigate to minimize the power dissipation / IR drop, propagation delay and switching activities, etc.. In this conflict, they have mentioned several techniques to identify and investigate the problems. By using several techniques to reduce the cost of fabrication of chip and prediction of several techniques and propose a new technique to implement, for reducing the dynamic IR drop and switching noise during the transmission of the signal [6,7]. In this paper the task to reduce the IR drop using a new technique i.e. diagonal power routing with HVT swapping method is implemented. It is well known that the performance of the chip is significantly affected by power routing technique.

The Maxwell equations relate to E and H fields, that are proportional to the antenna affect in transmission lines of circuit boards and metal layers. Switching activities also affect the various parameters of the device, which is also led to degrading the performance of the device. The inductive effect is more important at high frequency operation [8]. At high frequency of operation, power leakage is reduced by inserting dye caps for static power, whereas in dynamic power analysis the IR drop should vary with R, L & C affects. The present paper analyses the IR Drop with the diagonalized and an orthogonal power grid of dynamic analysis for op-amp. In this paper, mainly focussing the mathematical and simulation of diagonal routing and orthogonal routing top layer routing and comparison of them from obtaining the results to improve the IR drop reduction, reduce the effects of delay, noise and area. This work results will show that the proposed method of diagonal routing is improved in some aspects compared to the existing methods for certain limits, which is implemented to op-amp for validation.

The interconnection delay of the IC is increased and greater than the delay due to MOSFETS [13]. However, these design approaches has increased the speed of the MOSFET to increase the lifetime of the systems few technologies [14]. The increase in the speed of the MOSFET devices has primarily been enabled due to a reduction in their sizes. Metal area of the device reduced is proportional to cross sectional area of devices IC [15]. In scrolling down technology the complexity of the system density with decreases interconnect delay at high frequency of operation [16]. In this work the simulation is done by using diagonal power routing for various blocks and analysis is done over orthogonal routing for a typical 9-metal layer sub NM CMOS technology using Redhawk tools [26]. The methodology applied to validate this approach for all scaling

DOI: 10.32377/cvrjst1210

down technologies in VLSI. In this work it is mainly concentrated on various parameters affecting and the performance of the device with functionalities like antenna effect on metal interconnects [17,18] and the effect of the electromagnetic radiation from the onchipantennas on the MOSFET devices [19], Antenna gain decreases at low frequency range and increases at high and mid frequency ranges in metal interconnects due to the parallel orientation antenna. With the growing technology the devices are very compact and more sensitive to power and delay and area. This has led to many challenges to the designers for interconnection layers in the network.

II. Theoretical Formation

2.1 Orthogonal and diagonal power routing

The modern VLSI has multiple paths at different layers in horizontal and vertical layers. Wires on the same layer cannot cross each other based on the connection establishment. In multiple layers the distance between the components is very less, thus reducing the wire length. To reduce the wire length, cost and power consumption, the wires are routed on the upper layers in a 2D-plane.

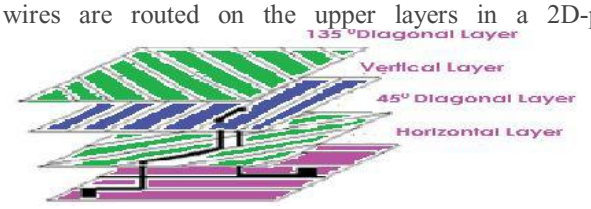

Figure 1. An example of HVHV- Horizontal Vertical Horizontal Vertical layer

In the figure1 shown above to provide connection between layers, horizontal layers allow only horizontal wire route and vertical layers allows only vertical wire route.

$$C = 2\,X\,10^{-6}(\text{wire} - \text{Length}) + 2.3\,X\,10^{-13}(\text{No. of Vias}) \quad \text{m} \qquad (1)$$

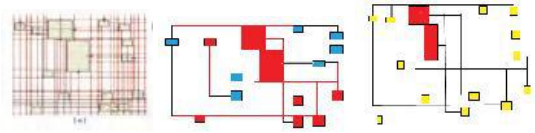

Figure 2.a Figure 2.b Figure 2.c

Figure 2. Three stage routing: (a) The orthogonal visibility graph, (b) The optimal connector routes, (c) The final routes after centering and nudging. Arrows indicate routing direction for connectors.

Right = { E→S,S→W,W→N N→E }-------(2)

Left = { E→N,S→E,W→S, N→W }----------(3)

Reverse= { E→W,S→N,W→E, N→S }-------(4)

in these equations, the distance between two points in orthogonal routing $||(R1, R2)||_1 = |p_1 - p_2| + |q_1 - q_2|$ has been applied to measure the shortest path between any two points R1 = (p1; q1) and R2 = (p2; q2). In this calculation take into the 4 cardinal directions: N, S, E, W. It is assumed that the functions right, left, and reverse defined by the mappings.

The directions of point R2 = (p2; q2) from R1 = (p1; q1) are defined as directions $(R_1, R_2) = \{N \mid q_2 > q_1\} \cup \{E \mid p_2 > p_1\} \cup \{S \mid q_2 < q_1\} \cup \{W \mid p_2 < p_1\}$Note dirns(R1,R2) ={ D} means R2 is on the line in direction D drawn from R1.e in direction *D* drawn from R1.

2.2. Visibility graph of orthogonal routing

The orthogonal visibility graph is used to minimize the penalty function. Let me (p, q) be the set of intersecting points in the diagram i.e, the connecting points and corners of the bounding box of each object. Let P1 and Q1 be the set of p and q coordinates respectively in I. The orthogonal visibility graph VG= (R, G) is made up of nodes. R P, Q1 s.t. p, q∈ R. If q s.t (p, q1) ∈ I think there is no intervening object between (p, q) and (p, q1). There is an edge e∈ E between each nearest neighbourhoods on all the sides and faces without any intervening object in the original diagram.

Observations: This simply takes the route R and "shrink" each segment on the route onto a path in the visibility graph to give R'. By construction R' is no longer than R and has no additional bends.

The orthogonal visibility graph can be constructed using the following algorithm. It has three steps:

1. Generate the interesting horizontal segments

$$H_I = \left\{ \begin{array}{c} ((p,q),(p',q)) \mid (p,q) \in I \;\; s.t. \;\; p \;\; \leq p1 \\ \\ \text{and there is no intervening object} \\ \text{between } (p,q) \text{ and } (p',q) \end{array} \right\}$$

2. Generate the interesting vertical segemnts

$$V_I = \left\{ \begin{array}{c} ((p,q),(p,q1)) \mid (p,q),(p,q1) \in I \;\; s.t. \;\; q \leq q1 \\ \text{and there is no intervening object between} \\ (p,q \text{ and } (x,y')) \end{array} \right\}$$

3. Compute the orthogonal visibility graph by intersecting all pairs of segments from H_I and V_I. The orthogonal visibility graph can be constructed with n objects using the algorithm with time O (n^2). The interesting horizontal segments can be generated in O (n log n) time where n is the number of objects in the diagram by using a variant of the line- sweep algorithm [3,4]. This uses a vertical sweep through the objects, keeping a horizontal "scan line" list of open objects with each node having reference to its closest neighbors. Interesting, horizontal segments are generated, when an object is opened, closed 'or' connection point is reached. Where as vertical segments can generated in O (n log n) time using horizontalsweep. The last step takes O (n^2) time since O (n) horizontal and vertical segments.

***Final placement of orthogonal routing**:*

Finally the layout is to find the exact coordinate points of orthogonal connector segments. This nudges connector route and "alleys" to make shortest path in a given network. The horizontal pass works as explained here

DOI:10.32377/cvrjst1210

and the vertical pass is symmetric, which provides the separate passes

1.Determine a desired horizontal position for all non-end segments in the connector. For the middle segment in an "S" or "Z" bend, this is the middle of the "alley" that the segment is in. For the middle segment in an "⊏" or "⊏"bend, this is the vertex of the object that the segment bends around.

2. Provide a set of horizontal separation constraints to ensure that segments maintain their current relative horizontal ordering with each other and with the other objects in the diagram. The constraints designed led to enforce non-overlap.

3. Project the desired values on to the separation constraints to find the horizontal position of the segments using the approximate projection algorithm satisfy VPSC from [24,25]. The constraints and desired positions can be generated algorithm [3] in O ((n+s) lag (n+s)) time where n is the number of diagram objects and so the total number of vertical connector segments. The approximate projection algorithm has O (⟦ (s + n) ⟧ ^2) worst-case complexity, but in practice O ((s + n) log (s + n)) complexity [5].

2.3. Diagonal routing

A diagonal routing is a technique that uses diagonal wiring which is partially applied to critical nets.To minimize the enhancements needed for the existing CAD system the usage of diagonal wires is limited (Fig.3).

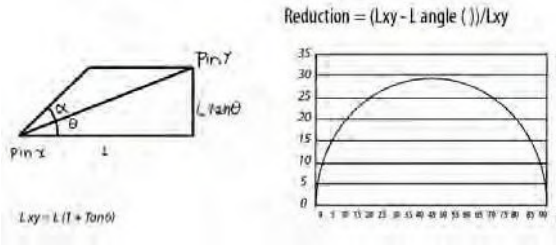

Figure 3. Theoretical Effect of length estimation

The figure 4 represents the theoretical estimation of a given block. In the actual design, the two lengths are compared for 6000 long distance nets. In diagonal routing the net length is reduced by about 12% on average.

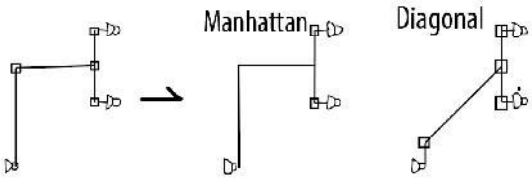

Figure 4. Effect estimation of actual

*The effect of delay estimation:*When a net length is about 1500, the improvement of delay is about 7 pico-seconds.When a diagonal routing is applied to a longer net,then the reduction of delay improved .

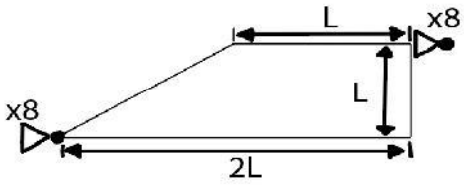

Figure 5. Effect estimation of delay

The diagonal routing can reduce the net length by about 20% in this case (fig. 6).In this paper we are using diagonal routing. The details of Manhattan routing are as follows.

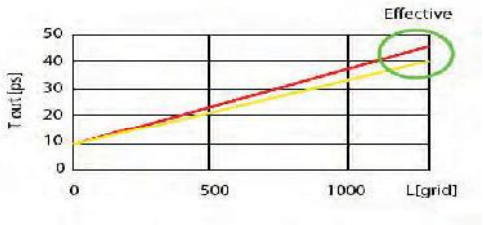

Figure 6 Graphical representations of the diagonal and Manhattan routing

Manhattan routing

The Manhattan routing is a special type of connection lines in graphical modeling tools on the other hand an algorithm for computing networks in VLSI design for integrated circuits. In graphical modeling tools are called with Manhattan routing the layout of connections in which only horizontal and vertical lines can be used with rectangular branches / turns and fixed distances from one another. It is usually not relevant whether crossing lines or may overlap or not. In general, a Manhattan Routing a grid or grid with fixed intervals based on the line extension. In Manhattan routing 45 and 135 degree layers are assigned to upper layers, having smaller wire resistance. With conventional Manhattan routing, the channels are left unused to route regular nets.

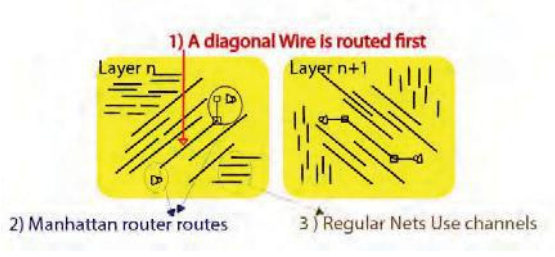

Figure 7: Layer representation of diagonal and Manhattan router Capacitance extraction of the Manhattan routing and diagonal routing

Additional capacitance table, Gapbetween Manhattan wires: 1 gird*N

Gap between Diagonal wires: 1/SQRT(2) grid*N

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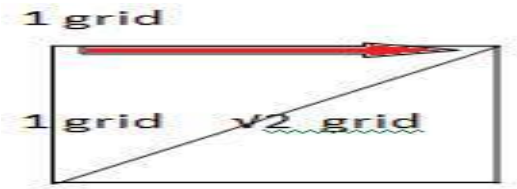
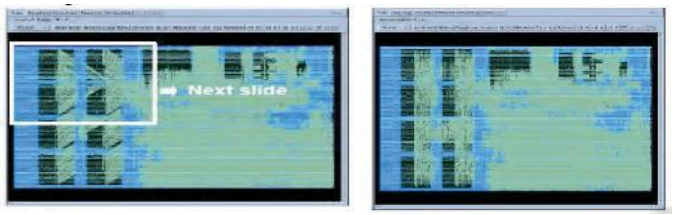


Figure 8. Capacitance table Diagonal wires:

Diagonal wiring directions in integrated circuits are simulated with wires deposed in purely Manhattan directions (e.g., horizontal and vertical directions). A metal layer of an integrated circuit contains at least two pairs of conductors to interconnect one or more points on the integrated circuit.



a. Diagonal b. Manhattan

Figure 9 (a) Diagonal routing and (b) Manhattan routing

III .APPLICATION

Op-amp design using orthogonal routing and Diagonal routing schemes in the nanometre era for validation purpose.

For the above points validation done for op amp using the orthogonal and Diagonal routing approaches, the schematic of op-amp using numberof **nmos** and **pmos** transistors combinations.

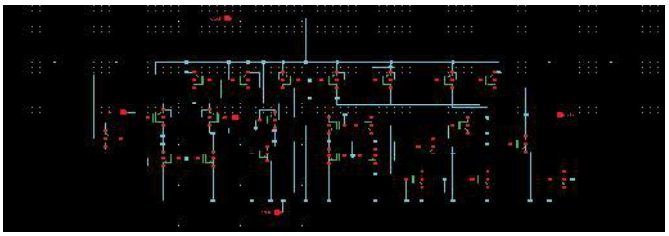


Figure 10. schematic diagram of op-amp

This is the op-amp schematic diagram. It has total 24 transistors(11 PMOS +13NMOS)

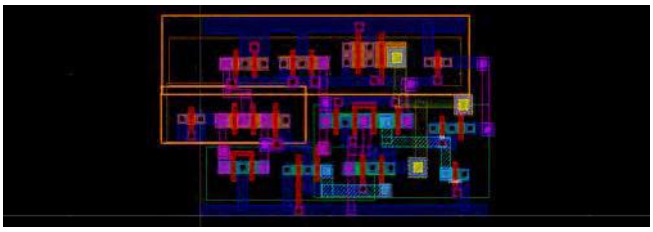


Figure 11. Schematic orthogonal Lay out of op-Amp

The complete orthogonal layout structure for the op-amp is given above. This layout is designed in the conventional orthogonal scheme in 180nm & 90 nm Technology.

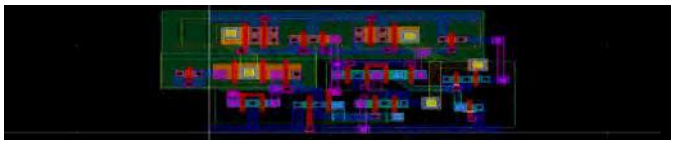


Figure 12. Schematic Diagonal Layout diagram of op-amp

The above image is for the diagonal layout scheme for the op-amp. We can observe some paths are routed in orthogonal manner.

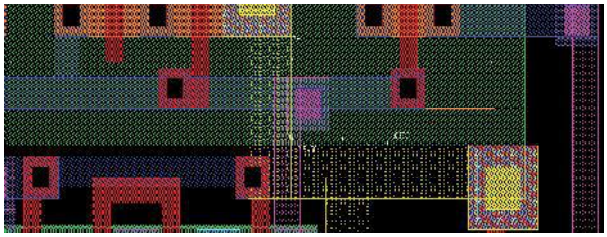


Figure 13.Path length of first path length of orthogonal routing

From above Figure, the path length of the first path is given. Orthogonal routing will take 0.9450+1.0350 = 1.980 micro meters

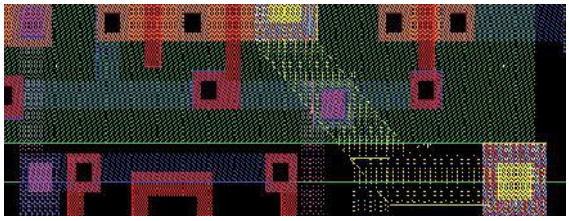


Figure 14.Path length of first path length of diagonal routing

If we observe the same path in the diagonal the length is given bellow. for path 1 - diagonal will take 1.46 micro meters. The difference between the lengths of the paths is 1.980 µm -1.46 µm = 0.52 µm. So from this we can observe that the path length is reduced to 0.52 µm lesser than actual path length when we are using the orthogonal routing.

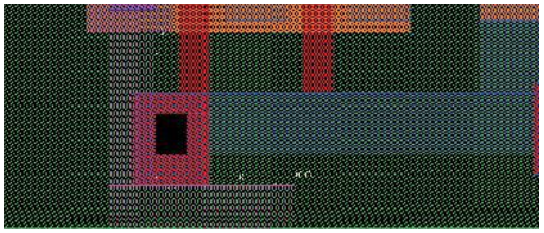


Figure 15.Path length of second path length of orthogonal routing

The second path is taken into consideration and length for orthogonal routing is 1.556 µm .

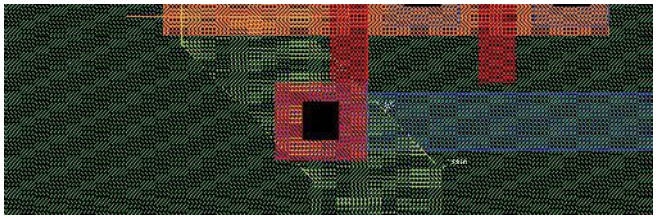


Figure 16.Path length of second path length of diagonal routing

For the diagonal routing the path length is 0.8810 micro meters, The difference between two paths is 1.556-0.88810 = 0.675 µm and this is reduced.

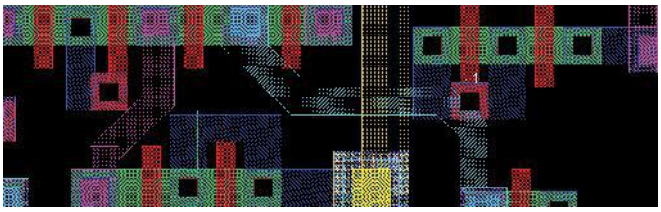


Figure 17.Path length of rest of path length of Diagonal routing for validation

The remaining paths used in diagonal outing. Pink colour path routing and the blue colour path routing.

Figure 18.Simulation output of diagonal routing power calculation

This is power calculation for the orthogonal routing extracted view of the layout. The power dissipation for this routing is 409.5E-3. By converting the floating point into power the power consumption is 409.5 micro watts(µw).

Figure 19 Simulation output of orthogonal routing power calculation

The power for diagonal routing is calculated for the extracted view of the layout. The power consumption is given as 406.3E-6 by converting it into watts we get 406 micro watts(µW). So from this we can observe that the power dissipation is reduced by 3 micro watts(µW). 409.5 – 406.0 = 3.5 µW .

The results describes that the power dissipation is reduced to 3.5 micro watts for a modelling of op-amp .which relates to validated proposal approach in the view of power dissipation reduction and it effects on the other parameters also .

This is the delay consumed by the orthogonal layout the delay value is 509E-9. so this indicates it is taking 5ns delay to produce output

Figure 20.Simulation output of orthogonal routing Delay calculation

The above table shows that the delay calculation for the diagonal is 419.0E-6. It gives the delay of 4.19ns. So from these two values we can get that the circuit is given less delay than orthogonal routing.

The delay is reduced by 1ns approximately. 5.2 – 4.19 = 1.01ns. From the above results describes that diagonal routing delay is low compared to the orthogonal routing for a proposed model of Op-Amp in a VLSI design.

Figure 21.Simulation output of Diagonal routing power calculation

IV.RESULTS & DISCUSSIONS

TABLE I.
VARIOUS PARAMETERS EFFECTED IN 180 NM TECHNOLOGY BY USING DIAGONAL AND ORTHOGONAL ROUTING TO CMOS BASED OP-AMP

Effecting Parameters	Orthogonal routing used in op-amp	Diagonal routing in op-amp	Difference B/w Diagonal & orthogonal	Remarks
Path Length	a)1.556 µM b)1.98 µM	0.8881 µM 1.46 µM	0.6679 µM 0.52 µM	Length reduced in diagonal routing
Delay	5.20 nS	4.19 ns	1.01 nS	Delay reduced
Power dissipation	409.5 µW	406.3 µW	3.2 µW	Power dissipation is better in diagonal

TABLE 2
.VARIOUS PARAMETERS AFFECTED IN 90 NM TECHNOLOGY BY USING DIAGONAL AND ORTHOGONAL ROUTING TO OP-AMP

Effecting Parameters	Orthogonal routing used in op-amp	Diagonal routing in op-amp	Difference B/w Diagonal & orthogonal	Remarks
Path Length	1.236 x10 -6µM	0.687 µM	0.549 µM	Length reduced in diagonal routing
Delay	4.50 x 10nS	3.63 ns	0.87 nS	Delay reduced in diagonal routing
Power dissipation	345.2 µW	337 µW	8.2 µW	Power dissipation is better in diagonal

DOI:10.32377/cvrjst1210

From the above results obtained our approach is justified that to applicable for specific conditional applications for top layer routing in VLSI design Here, the proposed approach is justified that there is no cross over problems, because the approach is meant for only top layer in design so what so ever the routing in orthogonal approach crossover problems the same thing is replica in rest of metal layers ,but overall performance of the systems is better in some specific applications in VLSI design by this proposed approach, since the results confined that to validate with existing approaches.

*1.Effects in length:*In the diagonal routing, net length reduction reduces the net length by 42% on an average. This reduction exceeds the theoretical maximum value 32.4%. This is due to the total detour of the net with diagonal routing is smaller than orthogonal routing.

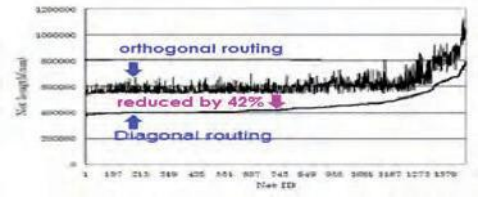


Figure 22: Effects of length

3. *Effects on delay:* Path delay reduction: The path delay is improved by up to about 1.01nano seconds per night on a path when diagonal routing applies to critical paths. This improvement is more than the delay of a gate with no load. The average improvement is about 1nano-second.

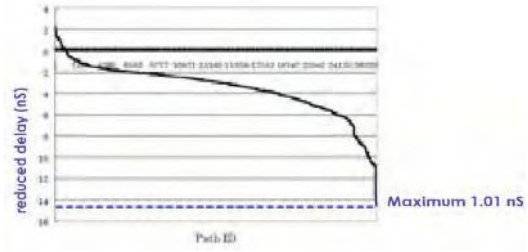


Figure 23: Effects on delay

c. Effects of noise

Noise reduction Coupling capacitance can cause crosstalk noise which is less when diagonal routing is applied. This is due to the associated reduction of net length. Finally, the overall crosstalk is reduced by about 18%.

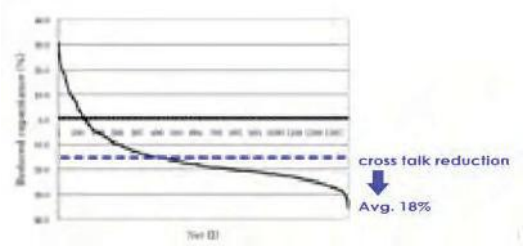


Figure 24: Effects of noise

A diagonal routing function is examined and able to reduce the net length by 42% per net on average, and path delay by up to 1.01nanoseconds.

D. Power dissipation reduction:

Power dissipation reduction is 3.5micro watts by using diagonal routing over orthogonal routing . Finally it is foud that reduction of power dissipation, is better than the orthogonal routing approach.

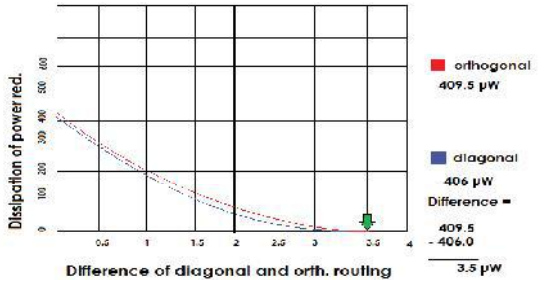


Fig 25.Power dissipation of diagonal and orthogonal approaches

This work is done by using the technology of 180nm and 90 nm in diagonalized and orthogonal routing approaches for design of op – amp uses voltage storm tools. These approaches are compatible with all scaling down technologies for specific application in VLSI design.

V. Conclusions

In this paper, it is presented as the diagonal power routing and orthogonal power routing applied in VLSI design and which has been validated for op-amp device. The results of the proposed approach shows better prospects when compared to the existing method of orthogonal routings. In this approach, there is no cross over problems, because diagonal routing is applied to the only top metal layer and the rest of lower metal layers are arranged same as existing approaches, from this methodology, this is allowing specific limits to be applied this technique in VLSI physical design. In future some fine tuning is needed for more reduction of power dissipation, area, delay for its applications in nanometer era and this approach is compatible with all scaling down technologies in VLSI design.

The authors wish to thank to Mr. Mastanaiah and Srikanth for their supporting to do this work.

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DOI:10.32377/cvrjst1210