PLL Implementation and Reactive Power Compensation

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Abstract: Phase locked loop (PLL) plays significant role in connecting a power electronic converter to the grid. A PLL can be implemented with software or hardware. In this paper, PLL is developed in MATLAB/SIMULINK using harmonic oscillator. The PLL can extract exact supply frequency information under balanced grid voltages. Static Synchronous Compensator (STATCOM) is a shunt connected Flexible AC Transmission Systems (FACTS) device which can able to absorb or generate reactive power. STATCOM is used in power transmission systems for reactive power compensation, load balancing etc. Secondly, a two level voltage source inverter based STATCOM is presented for reactive power compensation. A control strategy is developed for DC link voltage balance and instantaneous reactive power compensation. To validate the effectiveness of the control scheme, simulation study is done in MATLAB/SIMULINK for different load conditions.

Index Terms— Phase locked loop (PLL), two level inverter, reactive power compensation, STATCOM.

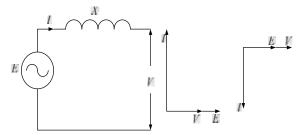
I. INTRODUCTION

The application of power electronic converters in power system is increasing because of improved power quality and providing reliable supply [1]. Power electronic converters are used in, Flexible AC Transmission Systems (FACTS), Grid connected solar PV system, High Voltage Direct Current (HVDC) Transmission and micro grid and so on [2]. For all such major applications, information of grid frequency is essential. Grid frequency is subjected to variations of loads, faults, disturbances in the system [3]. In detecting accurate value of grid frequency, Phase Locked Loop (PLL) plays significant role. Various PLL techniques are used for Synchronization between power electronic converter and grid [10]. An ideal PLL should provide the very fast and accurate value of frequency [4].

Static Synchronous Compensator (STATCOM) is a shunt connected Flexible AC Transmission Systems (FACTS) device which can able to absorb or generate reactive power whose output can be controlled so as to sustain definite parameters of the electric power system [5]. The STATCOM was initially named as advanced SVC (Static VAr Compensator) and then called STATCON (STATic CONdenser) and now a days, it is commonly known as STATic COMpensator (STATCOM).

The STATCOM gives working characteristics like a rotating synchronous compensator without the mechanical inertia. This is due to the STATCOM employs solid state power switching devices [6]. STATCOM also provides voltage support in distribution and transmission network by modulating bus voltages during disturbances [7].

The operation principle of STATCOM is as below. The Voltage Source inverter (VSI) produces a convenient AC voltage source (E). This voltage is compares the grid voltage (V) of the system; when the AC grid voltage amplitude is greater than that of the VSI voltage amplitude, the AC grid looks the STATCOM as an inductance connected to its terminals. Otherwise, if AC grid voltage amplitude is less than that of the VSI voltage amplitude, the AC grid looks the STATCOM as a capacitance connected to its terminals. If the voltage amplitudes are same, then the reactive power sharing between the grid and VSI is zero [3].



If the STATCOM has a DC source on its DC side, it can able to supply real power to the power system. This can be done by varying the phase angle of the STATCOM output and the phase angle of the AC power system. When the phase angle of the VSI lags grid phase angle, then STATCOM supplies real power to the AC system; if the phase angle of the VSC leads the grid phase angle, the STATCOM absorbs real power from the AC system [8]. If STATCOM supplies only reactive power, a capacitor is sufficient at the input of voltage source inverter, and DC link voltage can be maintained by drawing small active power from the grid.

Voltage source fed inverters are recently becoming very popular for FACTS devices due to improved voltage quality, very low voltage drop across the semiconductor device and low switching frequency of the semiconductor device compared to the conventional converters [2].

In this paper, a static VAr compensation system is developed using a two-level inverter as shown in fig.1. For the synchronization of grid to the inverter Synchronous reference frame PLL (SRF-PLL) is used.

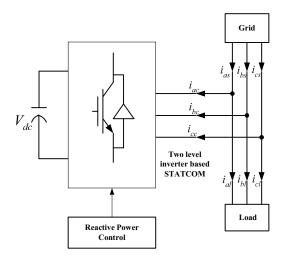


Figure 1. STATCOM with two level Inverter

II. PHASE LOCKED LOOP (PLL)

The emergent use of power electronic converters in both single and three phase applications requires a accurate and fast technique for phase angle evaluation. This is a major parameter in any application where reactive/active power flow control is required [8].

Synchronous Reference Frame (SRF) based PLL is developed in this paper and it estimates the phase angle exactly. The principle of SRF-PLL is estimates both the grid frequency and voltage phase angle for reference signal generation for the control of power electronic converters. The block diagram of three-phase SRF-PLL is illustrated in Fig.2 [9].

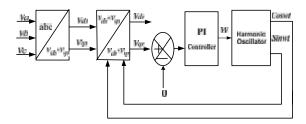


Figure 2. Three phase PLL basic structure

To obtain the phase information, the three phase (V_a , V_b and V_c) AC voltages are transformed into two phases (V_{ds} and V_{qs}) by using equation (1) and these two phases are transfer into direct and qudarature voltages (v_{dr}, v_{ar}) axis by using Equation (2). The phase angle θ is estimated by synchronously rotating voltage vector along d or q axis by using PI controller [10-12].

$$\begin{pmatrix} v_{ds} \\ v_{qs} \\ v_0 \end{pmatrix} = \frac{2}{3} \begin{pmatrix} 1 & -\frac{1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{pmatrix} \begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix}$$
(1)

$$\begin{pmatrix} v_{dr} \\ v_{qr} \end{pmatrix} = \begin{pmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{pmatrix} \begin{pmatrix} v_{ds} \\ v_{qs} \\ v_{0} \end{pmatrix}$$
 (2)

The phase angle θ is expected with θ^* which is integral of the estimated frequency ω^* . The expected frequency is the sum of the PI controller output and feed forward frequency ω [13]. The gain of the PI controller is calculated that, v_q coincide the reference value $v_q^* = 0$. If $v_q = 0$ the space vector voltage is synchronized along the q-axis and expected frequency ω^* locked on the system frequency ω . So that the expected phase angle θ^* is equals to the phase angle θ .

The harmonic oscillator is designed based on the equation (3) and (4).

$$X_{n+1} = X_n + \omega y \Delta t \tag{3}$$

$$Y_{n+1} = Y_{n-} \omega x \Delta t \tag{4}$$

The simulation results for the direct and quadrature axes voltages are shown in Fig. 3. From the result quadrature axes voltage is zero. Fig. 4 shows the PLL generated sin and cos unit signals of same grid frequency. Fig.5 shows the grid frequency in rad/sec. The PLL generated two phase voltages are transferred to three phase by using inverse transformation to know the phase sequence. Fig.6 shows the grid voltage and PLL generated voltages both are in phase.

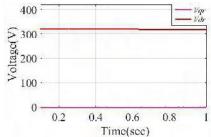


Figure 3. Direct and quadrature axes voltages (v_{dr} and v_{qr})

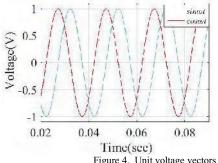


Figure 4. Unit voltage vectors

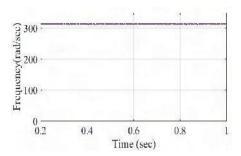


Figure 5. Frequency of grid voltages in rad/sec

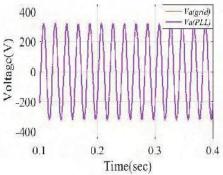


Figure 6. Grid and outupt voltages of pll

III. REACTIVE POWER COMPENSATION

Fig.7 shows two level inverter which is connected to the grid, through coupling inductor. The DC link voltage at the input of inverter is maintained by a capacitor. This is achieved by maintain certain phase angle between the grid and inverter voltages.

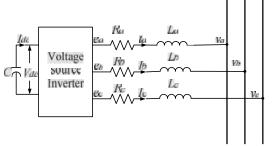


Figure 7. Equivalent circuit of two level inverter based STATCOM

In the Figure v_a , v_b and v_c are grid voltages, R_a , R_b and R_c are the resistances which represent the power losses in the coupling inductor and La, Lb and Lc are inductances of coupling inductors, e_a , e_b and e_c are the inverter output voltages. Assuming $R_a = R_b = R_c = R$ and $L_a = L_b = L_c = L$ and the dynamic model can be derived by writing KVL on AC side as follows [14]

$$\begin{bmatrix} \frac{di_{a}}{dt} \\ \frac{di_{b}}{dt} \\ \frac{di_{c}}{dt} \\ 0 & 0 & -\frac{R}{L} \\ 0 & 0 & -\frac{R}{L} \\ \end{bmatrix} \begin{pmatrix} i_{a} \\ i_{b} \\ i_{c} \end{pmatrix} + \frac{1}{L} \begin{pmatrix} v_{a} - e_{a} \\ v_{b} - e_{b} \\ v_{c} - e_{c} \end{pmatrix}$$
(3)

Equation (3) is transformed to the synchronously rotating reference frame. The reference voltages of the inverter e_d^* and e_q^* are controlled in synchronously rotating reference frame as follows:

$$e_d^* = \chi_l - \omega L i_q + \nu_d \tag{4}$$

$$e_d^* = x_1 - \omega L i_q + v_d$$

$$e_q^* = x_2 + \omega L i_d$$
(4)

The parameters x_1 and x_2 are regulated as follows

$$x_{l} = (K_{pl} + \frac{K_{il}}{s})(i_{d}^{*} - i_{d})$$
 (6)

$$x_2 = (K_{p2} + \frac{K_{i2}}{s})(i_q^* - i_q)$$
 (7)

Where, i_d^* is reference d-axis current and i_q^* is q-axis reference current. i_d^* is obtained from the DC link voltage requirement as

$$i_d^* = (K_{p3} + \frac{K_{i3}}{s})(V_{dc}^* - V_{dc})$$
 (8)

Where, V_{dc}^{st} and V_{dc} are the reference and actual DC link voltages across the capacitor.

The reference q-axis current, i_q^* is obtained by transforming the stationary load current into synchronous rotating frame, using equations (1) and (2). The control circuit is shown in Fig. 8. The reference d-q axes voltages of the inverter, e_d^* and e_q^* are inverse transformed to stationary reference frame voltages e_a^* , e_b^* and e_c^* using equations (1) and (2) [15]. Using this voltages e_a^* , e_b^* and e_c^* as reference signals, high frequency triangular wave as carrier signal and comparing carrier and reference signals gate pulses for the inverter are generated [2].

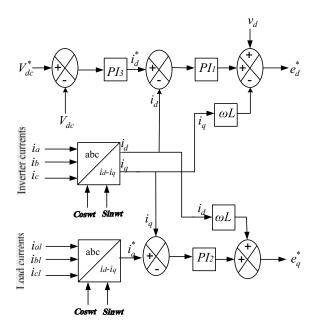


Figure 8. Control circuit

IV. SIMULATION RESULTS

The block diagram shown in Fig.1 is considered for analyzing the system consisting of two level inverter based STATCOM using MATLAB/SIMULINK.

TABLE I SIMULATION PARAMETERS

STATCOM Rating	70 KVA
Grid Voltage	415 (L-L)
Grid Frequency, f	50 Hz
DC Link Voltage, V _{dc}	1000 V
Switching Frequency	10 KHz
DC Link Capacitance, C	1200 μF

A. Capacitive Mode

Initially, the load impedance is set at $(3.4 + j3.4) \Omega$, hence load draws a current of (50 - j50) A. To supply a reactive current of -j50A by the inverter, from (4) and (5), e_d^* and e_q^* are calculated to 375V and 49V respectively. The inverter output voltage $e_i = \sqrt{e_d^2 + e_q^2}$ is 378V. At t = 2 sec, load impedance is changed to $(1.7 + j1.57) \Omega$, then load draws a current of (100 - j100) A.

For load variations, source always supplies active component of current, STATCOM supplies reactive component of current and source always operates at unity power factor as shown in Fig.9 (a). Fig.9 (b) shows variation of STATCOM current when the load reactive component is increased to –j100 A in synchronous rotating reference frame. From the figure, it can be seen that actual current approaches the reference current. Fig.9(c) shows the DC link voltage of the inverter. It can be seen that DC link voltage is maintained at the reference value even after load change. Fig.9 (d) shows inverter output voltage of Phase-A.

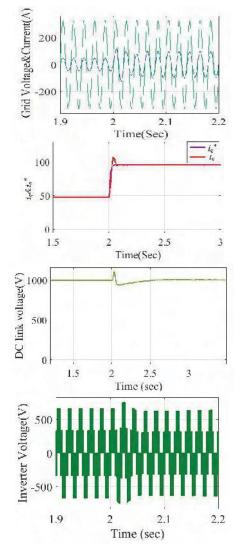


Figure 9. a) Grid current and voltage of phase-A b) Actual and reference reactive component of current c) Dc link voltage d) Inverter voltage

Fig.10 shows the total harmonic distortion of voltage. From the figure it can be seen that fundamental component of inverter voltage is 382.1V. Further, it can be seen that harmonics appear around multiples of switching frequency which is equal to 10 kHz. As discussed in section I the inverter output voltage is greater than the source voltage in capacitive mode of operation.

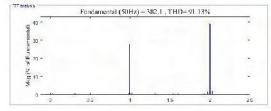


Figure 10. Harmonic spectrum of Inverter voltage *B. Inductive Mode*

In the inductive mode, the load impedance is set at (3.4 + j6.78) Ω and load draws a current of (20 - j40) A. At t = 2

sec, load impedance is changed to $(3.4 - j7.36) \Omega$, then load draws a current of (18 + j38) A. To supply a reactive current of +j38A by the inverter, from (4) and (5), e_d^* and e_q^* are calculated to be 260V and 65V respectively. Output voltage of the inverter is $e_i = \sqrt{e_d^2 + e_q^2}$ is 268V.

For inductive mode also, STATCOM supplies reactive component of current, grid supplies only active component of current and source always operates at unity power factor as shown in Fig.11 (a). Fig.11 (b) shows distinction of STATCOM current when the load reactive component is increased to +j38 A in synchronous rotating reference frame. From the figure, it can be seen that actual load current approaches the reference current. Fig.11(c) shows the DC link voltage of the inverter. It can be seen that DC link voltage is maintained at 1000 V after load change. Fig.11 (d) shows Inverter voltage of Phase-A.

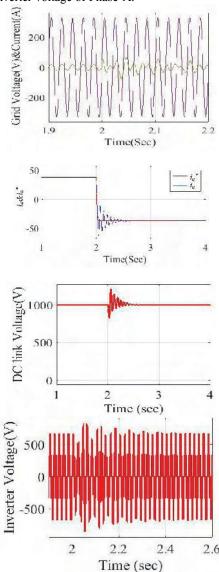


Figure 11. a) Actual and reference reactive component of current b) Dc link voltage c) Grid voltage and currents of phase-A d) Inverter current e)Inverter voltage

Fig.12 shows the total harmonic distortion of voltage. From the figure it can be seen that fundamental component of inverter voltage is 269.4V. Further, it can be seen that harmonics appear around multiples of switching frequency which is equal to 10 kHz. As discussed in section I the inverter output voltage is less than the source voltage in inductive mode of operation.

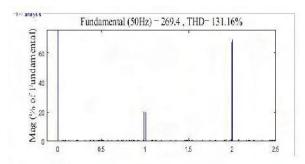


Figure 12. Harmonic spectrum of Inverter voltage

V. CONCLUSIONS

Phase locked loop plays a significant role in connecting a power electronic converter to the grid. In the first part of the paper, PLL is implemented in a grid connected system. The three phase voltages are converted into two phase voltages. The two phase voltages are transformed to synchronous rotating frame. The q-component of source voltage, v_q is made zero using PI controller, which ensures exact frequency information of source at any time.

In second part of the paper, static reactive power compensation is achieved using a two level inverter. Dynamic model of the two level STATCOM is developed. Based on the model the controller was developed. The controller generates reference voltages for the inverter. The effectiveness of the controller is analyzed by doing rigorous simulation studies. From the simulation study, it is concluded that the STATCOM ensures that the source always operates at unity power factor for different load conditions.

REFERENCES

- [1] N. G. Hingorani and L. Gyugyi, *Understanding FACTS*. Delhi, India:IEEE, 2001, Standard publishers distributors.
- [2] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B.Wu,J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," IEEE Trans. Ind. Electron., vol. 57,no. 8, pp. 2553–2580, Aug. 2010
- [3] Y. Liu, A. Q. Huang, W. Song, S. Bhattacharya, and G. Tan, " Small signal model-based control strategy for balancing individual dc capacitor voltages in cascade multilevel inverter-based STATCOM," IEEE Trans. Ind. Electron., vol. 56, no. 6, pp. 2259–2269, Jun. 2009.
- [4] B. Singh, R. Saha, A. Chandra, and K. Al-Haddad, "Static synchronous compensators (STATCOM): A review," IET Power Electron., vol. 2, no. 4, pp. 297–324, 2009.

- [5] M. Saeedifard, R. Iravani, and J. Pou, "Control and decapacitor voltage balancing of a space vector modulated fivelevel STATCOM," IET Power Electron., vol. 2, no. 3, pp. 203– 215, May 2009.
- [6] E. Acha, C. R. Fuerte-Esquivel, H. Ambriz-Perez, and C. Angeles-Camacho, FACTS Modeling and Simulation in Power Networks. New York, NY, USA: Wiley, 2005.
- [7] R. M. Mathur and R. K. Varma, Thyristor-Based FACTS Controllers for Electrical Transmission Systems. Hoboken, NJ, USA: Wiley/IEEE,2002.
- [8] Se-Kyo Chung. "A phase tracking system for three phase utility interface inverters" IEEE Trans. Power Electronics, Vol. 15,No.3, pp. 431-438, 2000.
- [9] V. Kaura and V. Blasko, "Operation of a phase locked loop system under distorted utility conditions," IEEE Trans. Ind. Appl., vol. 33, no. 1, pp. 58–63, Jan./Feb. 1997.
- [10] L. G. B. Rolim, D. R. da Costa, and M. Aredes, "Analysis and software implementation of a robust synchronizing PLL circuit based on the pq theory," IEEE Trans. Ind. Electron., vol. 53, no. 6, pp. 1919–1926, Dec. 2006.
- [11] S. A. O. Silva and E. A. A. Coelho, "Analysis and design of a three-phase PLL structure for utility connected systems under distorted conditions," in Proc. 6th Int. Conf. Ind. Appl. IEEE/INDUSCON, 2004, pp. 218–223.
- [12] S. M. Silva, B. M. Lopes, B. J. C. Filho, R. P. Campana, and W. C. Boaventura, "Performance evaluation of PLL algorithms for single phase grid-connected systems," in Conf. Rec. IEEE IAS Annu. Meeting, 2004, pp. 2259–2263.
- [13] L. N. Arruda, S. M. Silva, and B. J. C. Filho, "PLL structures for utility connected systems," in Conf. Rec. IEEE IAS Annu. Meeting, 2001,pp. 2655–2660.
- [14] C. Schauder and H. Mehta, "Vector analysis and control of advanced static VAr compensators," in Proc. Inst. Elect. Eng. C., Jul. 1993, vol. 140, no. 4, pp. 299–305.
- [15] N. N. V. Surendra Babu, B. G. Fernandes, "Cascaded Two-Level Inverter-Based Multilevel STATCOM for High-Power Applications," IEEE Trans. Power Delivery, Vol. 29, NO. 3, June 2014.