Design and implementation of High Performance Voltage-Controlled Oscillator using CMOS Technology

G.Venkateswarlu
CVR College of Engineering/EIE, Hyderabad, India
Email: venkigummadilli@gmail.com

Abstract— **In recent years, oscillators are considered as inevitable blocks in many electronic systems. They are commonly used in digital circuits to provide clocking and in analog/RF circuits of communication transceivers to support frequency conversion. Nowadays, CMOS technology is the most applicable solution for VLSI and especially for modern integrated circuits used in wireless communications. Additionally, the trend towards single chip implementation makes the circuit design increasingly challenging.**

The main purpose of this paper is to design a high performance voltage controlled oscillator (VCO) using 90nm CMOS technology. In the beginning, a brief study of different VCO architectures is carried out. Next, a wide comparison between different VCO topologies is performed in terms of phase noise and power consumption. The effect of VCO phase noise on RF transceivers is also analyzed. In the following, all the phase noise contributors in a typical VCO are identified to enable design optimization. To meet the state-of-the-art requirements, several circuit solutions have been explored and the design work ended-up with a Quadrature VCO. The design is verified for the intended tuning range and process, temperature, and supply voltage (PTV) variations. The circuit operates at center frequency of 2.4 GHz. The phase noise of QVCO obtained by simulation is -140 dBc/Hz at 1MHz offset frequency which is 6 dB less compared to conventional VCOs. The power consumption is 3.6mW and the tuning voltage can be swept from 0.2 V to 1.2 V resulting in 2.25 GHz - 2.55 GHz frequency range..

Index Terms— **QVCO, Power Consumption, Phase Noise, Tuning Voltage, Communication Transceivers.**

I. INTRODUCTION

Voltage-controlled oscillators are mostly implemented as a component of phase locked loops (PLLs). PLLs can be used in different areas such as clocking of microprocessors, providing carriers for wireless transceivers or other transmission systems. Usually, in communication applications PLLs require VCOs with a wide tuning range to serve up- or down-conversion over the system bandwidth. Interestingly, in PLLs the VCO phase noise requirements can be relaxed. In other words, the noise produced by a voltage-controlled oscillator at the oscillation frequency will be to some extent filtered out by the system. Therefore, VCO topologies with wide tuning range are usually preferred.

In high performance applications where a low phase noise or jitter is required, VCOs using LC tanks are preferred for their high Q-factor. Therefore, LC-based VCOs will be in focus of the presented designs.

To design a VCO, different requirements should be fulfilled. In this section, we define the VCO metrics individually. In particular, we should meet the oscillation frequency, power consumption, tuning range and phase noise requirements which are the most important in a VCO design. The oscillation frequency may vary from one design to another due to different applications and architectures.

The tuning voltage range is determined by required frequency variations in different applications. The other major issues that should be considered especially in a high performance VCO design are phase noise and power consumption. Generally, it is difficult to fulfill all of the requirements at the same time. For instance, there is usually a tradeoff between power consumption and phase noise. On the other hand, some VCO topologies can improve the phase noise performance while other architectures can dissipate less power. Consequently, regarding the design specifications and their priorities, the designers have to choose the appropriate VCO topology but still are exposed to design tradeoffs. The specifications for our ultimate VCO design aimed at 90-nm CMOS technology are as shown in Table 1.

TABLE I
Ultimate VCO design specifications.

QVCO specifications	Value
Center frequency	2.4GHz
Supply Voltage	1.2V
Phase noise at 1MHz offset frequency	< -130dBc/Hz
Power Consumption	<5mW
Tuning Voltage	0.2-1.2
Frequency range	V2.25-2.55GHz

10.32377/cvrjst0614

II. DESIGN AND IMPLEMENTATION OF QVCO

In this section, we present some low phase noise LC architectures. One of the most recent topologies is a quadrature VCO with integrated back gate coupling. Nowadays, quadrature VCOs are widely applicable in transceivers. One of the drawbacks of this topology is higher power consumption than the LC VCO architectures. To get an optimum result regarding the power and the phase noise simultaneously, a much simpler design is presented. At the end of this chapter, we compare all of the benefits and drawbacks of different VCO architectures[1]. Finally, a low noise low power CMOS LC oscillator is designed.

A) Low Phase Noise QVCO

Nowadays, CMOS technology is the most applicable solution for modern wireless communication devices. The challenge of being implemented on a single chip makes the design much complicated. In this topology, high efficient transmission is performed by the help of quadrature-amplitude modulation and the frequency division technique. Recently, some transceivers use quadrature oscillators to drive mixers for performing frequency conversion. However, the signal is susceptible to the phase noise disturbances. There are different methods to produce the quadrature signal. The differential voltage controlled oscillator, the quadrature coupling of two simple LC VCOs, the ring oscillators and the frequency division technique are the most common procedures for producing a low phase noise signal. The quadrature topology is popular among designers due to its high performance regarding the phase noise. The quadrature topology can be done in different ways. Back-gate coupling or adding some transistors to the VCO core are some common procedures. One of these approaches is called source resistive degeneration which has a noticeable impact on phase noise improvement in quadrature VCOs. In this state-of-the-art design, we take advantage of source resistive degeneration and back gate coupling simultaneously. In other words, we put the both procedures into one single model to achieve a significant output with low power dissipation and low phase noise at the same time.

In this section, a 90nm CMOS quadrature VCO with a s ignificant low phase noise is designed. As mentioned in introductory section, we mix two different methods

into one model to achieve the best phase noise performa nce. As observed in the final simulation results, the phase noise and the power consumption have improved significantly in a well designed QVCO[8]. However, a larger area on the chip should be dedicated for the design. Overall, we achieve an optimum performance regarding the phase noise and power consumption.

The phase noise is -140 dBc/Hz at I MHz offset from 2.4 GHz. The QVCO consumes 3 mA from a 1.2V power supply. The QVCO circuit schematic is shown in the Fig. .1. The two CMOS VCOs are coupled back to back by their gates. In other words, the

circuit consists of two CMOS LC VCOs with eight trans istors. In our design the PMOS bulks of each VCO are connected by coupling capacitors as shown in the circuit schematic.

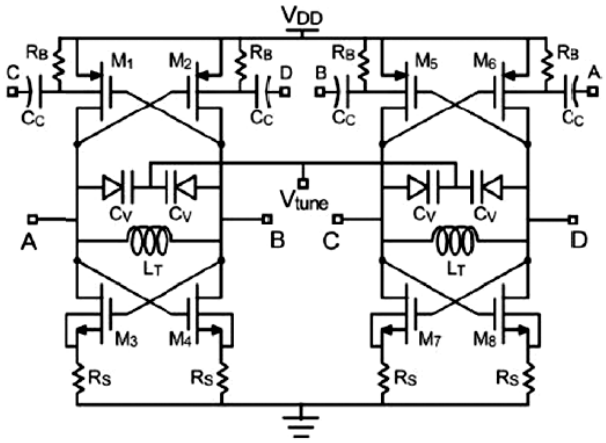

Figure. 1: Circuit schematic of Quadrature VCO

This technique used in our quadrature VCO has an advantage comparing with conventional VCOs. As we notice in old QVCO designs, four more transistors are used as coupling elements [3]. A simple conventional quadrature VCO is depicted in fig.2.

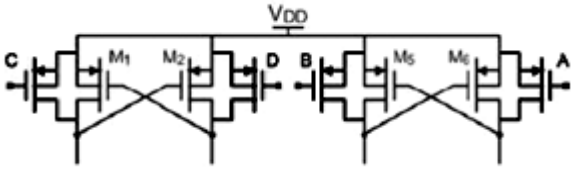

Figure 2:Conventional Quadrature VCO

In our proposed design, these extra transistors are omitte d due to the back-gate coupling technique.

Consequently, the circuit performance improves due to the reduction of noise sources. As described in previous chapters, adding more transistors leads to extra noise of the circuit. Flicker noise of NMOS and PMOS transistors are the main factors that should be considered in our design.

Therefore, the corresponding phase noise can be formul ated as following:

$$L(\Delta\omega) = 10\log\left[\frac{c_0^2}{q_{max}^2}\left(\frac{\overline{i_{n,N}^2}/\Delta f}{2.\Delta\omega^2}.\frac{\omega_{1/f,N}}{\Delta\omega} + \frac{\overline{i_{n,P}^2}/\Delta f}{2.\Delta\omega^2}.\frac{\omega_{1/f,P}}{\Delta\omega}\right)\right]$$

This technique gives more symmetry to the drain current. In this case, more improvement in phase noise is achieved. A designer might think that this technique can be considered for PMOS transistors as well. However, in our circuit, the PMOS transistors should have quite large gm for phase locking. Consequently, this procedure might not be suitable for PMOS transistors. On the other hand, we encounter some limitations when designing the Rsource. High Rsource value can ruin the oscillation initial condition and produce some additional disturbances.

The circuit is designed in CMOS 90nm technology. There is a big challenge for selecting a proper inductance. The quality factor of the inductor should be considered as well. We use a spiral structure for designing the inductor. Its value is 2.1 nH and its corresponding quality factor is 15. As observed in the final results, the value of Rsource is 26 ohm.

The oscillation frequency is functioning between 2.25 to 2.55 GHz when the Vtune is tuned from 0.2 to 1.2 V. Our designed output power varies from -0.5 to -1.6 dBm. In the frequency range of 2.25 to 2.55 GHz, the best result is achieved at 2.4 GHz. The varactor used in our design has a hyperbolic capacitance versus voltage curve. This makes the middle of tuning range a critical point. At 2.4 GHz, the phase noise is -140dBc/Hz at 1 MHz offset frequency. Our designed quadrature VCO consumes 3mA from a 1.2V supply voltage. The equation for calculating the figure of merit for VCO is as following:

$$\mathrm{FOM} = \mathrm{L}\{\Delta\omega\} - 20\log\left(\frac{\omega_0}{\Delta\omega}\right) + 10\log(P_{\mathrm{DC}})$$

As described in the introductory part, we have designed a 2.4 GHz quadrature VCO. Its corresponding phase noise is -140 dBc/Hz at 1 MHz offset frequency. In the design procedure, two simple CMOS LC VCO are coupled together to satisfy the oscillation condition at the desired frequency. The body terminal of PMOS transistors are connected together via coupling capacitors. Additionally, four resistances are added to the source of NMOS transistors to reduce the transconductance as much as possible. Therefore, we have less gm variation at the output. On the other hand, phase noise is decreased as well. This is called source resistive degeneration technique.

III. Low Noise Low Power CMOS LC VCO

Oscillators are inevitable blocks in designing communication systems. There are different LC VCO topologies in communication electronics. LC VCOs are mainly applicable in highly efficient transmitters and receivers. VCOs are used as inputs for the mixers to produce desired outputs. Therefore, they are quite noticeable in highly integrated transceivers. Low noise and high signal amplitude should be achieved for obtaining a reasonable performance in a VCO design. To obtain a state-of-the-art design, two specifications should be met at the same time. LC VCOs are mostly popular due to this issue. They achieve an ultra-low noise with low power dissipation simultaneously. Therefore, the designers are encouraged to design efficient LC VCO topologies. Nowadays, lots of investments have been focused on designing CMOS LC VCOs using on-chip resonators. The drawback is that fully integrated LC VCOs consume lots of power. Therefore, external LC VCO topologies are still used in recent cell phones. In this design, we aim for an optimal circuit using fully integrated VCOs. Our goal is to produce outputs with lower phase noise and power dissipation comparing with conventional off-chip LC VCO topologies[2]. This work mainly concentrates on design of fully integrated VCOs with optimized power consumption and phase noise lower than VCOs with external resonators. For this design, we mainly discuss the complementary LC VCO structure. Then, we compare its performance, regarding phase noise and power consumption, with conventional VCOs.

There are some noticeable advantages that make CMOS LC VCO an identical topology. Complementary VCOs are more economical than their conventional counterparts. Old topologies use only NMOS or PMOS transistors. In our design, we use both type of transistors at the same time. By adding PMOS transistors to conventional NMOS only VCOs, much larger transconductance is achieved. As we know, the tank used in the circuit is lossy. Since we generate a noticeably large transconductance, less current is needed to compensate the resonator loss.

Therefore, much power is saved in this topology. On the other hand, using the PMOS and NMOS pairs simultaneously, we produce symmetrical waveforms at the output. Consequently, the flicker noise upconversion to the 1/f3 region is reduced[6]. The CMOS LC VCO is illustrated in the Fig.3.

If the VCO requirements are fulfilled, the circuit oscillates properly. In the theory, the amplitude increases gradually and stops in a point. Actually, when the negative resistance cannot compensate the resonator loss any further, the output will be stable. However, it is the case when the Vdd is not putting constraints on the output swing at the oscillation startup point. When operating at the current limited regime, the CMOS cross-coupled VCO is the best choice for the state-of-the-art design. Applying the same voltage and bias current, it generates a better phase noise comparing with its NMOS or PMOS counterparts. The phase noise can be analyzed in different aspects. First, the CMOS cross-coupled VCO tolerates a larger charge for the

10.32377/cvrjst0614

output swing. This maximum swing is illustrated as qmax in the Hajimiri's model. As the phase noise is inversely proportional to the maximum charge, the CMOS cross-coupled VCO generates a better phase noise comparing with its conventional counterparts. On the other hand, we can improve it to the Without Tail (WT) structure. The WT structure shows even a better performance than the fixed biasing topology. In the WT topology, the number of transistors is reduced.

In another words, we decrease the number of noise sources. Therefore, the flicker noise sources are just of the cross-coupled pairs. Since switched biasing is applied in the design, the cross-coupled pairs do not affect the phase noise performance that much due to their low flicker noise. Overall, in this design, we improve the phase noise performance by omitting the tail transistor. On the other hand, since the tail transistor is neglected

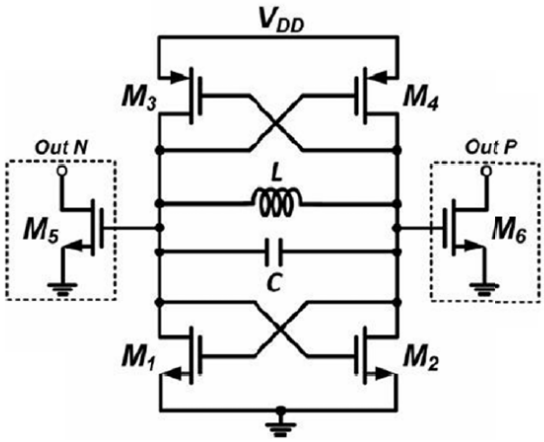

Figure.3: CMOS LC Oscillator cirut schematic

The transconductance produced by cross-coupled pairs should be inversely proportional to the overall resistance of the resonator. As obtained in our experimental simulations, we can optimize the power dissipation by improving the quality factor of our resonator. As a matter of fact, this will optimize the required transconductance as well. However, using fully integrated inductors generates some obstacles for the design. Fully integrated VCOs have low quality factors. On the other hand, there are some boundaries for increasing the quality factor of the inductors.

A. Power Analysis

If we apply Vdd as our supply voltage to the circuit, the voltage measured at the output could be estimated as Vdd/2. Vm represents the output amplitude by which the gate to source voltages can be formulated as following:

$$V_{gs1}=V_{dd}-V_{gs3}=V_{dd}/2+V_m\sin(\omega t)$$

$$V_{gs2}=V_{dd}-V_{gs4}=V_{dd}/2-V_m\sin(\omega t)$$

The NMOS transistors switch on when Vgs≥Vth,NMOS and the PMOS transistors switch on when Vsg ≥ |Vth,PMOS|. As observed in the theory, if we subtract the NMOS and PMOS current from each other the resonator current will be identified. Since one of the PMOS or NMOS transistors is switched on at each cycle, a larger current is conducted into the resonator. Consequently, when the current is driven by one of the M1 or M3 at each cycle, the power dissipation is reduced. On the other hand, since we reduce the number of transistors in each cycle, less noise is driven into the resonator. As observed in above equations, we should consider some limitations for choosing the right supply voltage. If we apply a supply voltage which is larger than the overall threshold voltage of the M1 and M3 transistors (Vth,NMOS + Vth,PMOS), they will be switched on at the same time.

Consequently, the circuit dissipates more power and extra noise will be conducted into the resonator. Increasing the overall noise in the circuit has an inverse impact on the phase noise performance. Overall, to dissipate less power and improve the phase noise performance, we should present a state-of-the-art structure. In this topology, M1 and M3 are not allowed to conduct at the same time in each cycle. This is the same case for M2 and M4 transistors. Now, it is understood the reason to minimize the supply voltage to overall threshold of PMOS and NMOS transistors. Applying the Vdd equal to Vth,NMOS+Vth,PMOS , the output voltage will be estimated as NMOS threshold voltage (Vth,NMOS). This ensures that M1 and M3 or M2 and M4 transistors would not be switched on simultaneously. Therefore, it guarantees that each of the NMOS or PMOS transistors is switched on for half of the oscillation cycle.

The other issue that should be analyzed in details is choosing a right inductor with a suitable resistance. The noise produced by the inductor has a power equal to V_n^2 = 4KTR. Optimizing the inductor's value has several impacts on the performance of the whole circuit. By reducing the inductor's value, its overall resistance will be decreased as well. Consequently, the phase noise performance will be improved because less noise is produced by the resistance. On the other hand, when the inductor generates less resistance, the corresponding transconductance for the transistors will reduce as well.

This leads to less current and hence the power consumption will be optimized. Another advantage of choosing a small inductor is to decrease the reciprocal effect of inductors designed on our chip. On the other hand, when the inductor's size is minimized, a larger capacitor should be chosen to keep the oscillation

frequency at the desired value. Larger capacitors will increase the maximum charge that can be tolerated. Based on Hajimiri's formula[7], increasing the qmax will improve the phase noise performance. If we consider a defined unit area on the chip, the capacitance value that can be allocated to that area is much larger than the inductance that can be specified to that space. Therefore, by reducing the inductor size and increasing the capacitor's value to fix the oscillation frequency at the desired value, the needed area on the chip will be minimized.

However, there are some constraints for decreasing the inductor's value. The tank amplitude can be modeled using a current source which turns on and off very fast from one transistor pair to the other. Since the voltage direction on the resonator changes in every moment, the current direction reverses dynamically through the resonator. Therefore, we can model the whole circuit as current source switching in two directions of Ibias and –Ibias. The current source is feeding the parallel RLCtank all the time. Req is defined as the equivalent resistance of the resonator. At the resonance frequency, the inductor and the capacitor cancel each other due to their admittances.

At the end, what remains is the equivalent resistance of the tank (Req). Since the LC tank mainly weakens the effect of individual harmonics of the input current, the fundamental harmonic can produce a noticeable output swing. Its corresponding amplitude can be estimated as (4/π)IbiasReq. However, the output can be estimated as a sinusoidal waveform at higher frequencies. In sinusoidal waveforms, the output can be estimated as IbiasReq. Therefore, without considering these limitations, reducing the inductor value can be problematic. When decreasing the inductor value, the equivalent parallel resistance decreases as well. Consequently, the tank amplitude decreases noticeably. In our design, the overall resistance in parallel is estimated as $R_p = r_s \times Q^2_{Ris}$ around 320Ω. To fulfill the startup condition, the transconductance should fit in the following formula:

$$g_{m,tank} \geq 1/R_p$$

To minimize the flicker noise upconversion effect, equal transconductance for the NMOS and PMOS transistors should be chosen. The width and length of transistors is decided by following equations:

$$\left(\frac{W}{L}\right)_{NMOS} = \frac{g^2_{m,NMOS}}{I_B \mu_n C_{ox}}$$

$$\left(\frac{W}{L}\right)_{PMOS} = \frac{g^2_{m,PMOS}}{I_B \mu_p C_{ox}}$$

To minimize the short channel noise, proper length and width should be chosen. Regarding phase noise calculation, Hajimiri presents a model as following:

$$L(\Delta\omega) = 10 \log \left[\frac{\frac{i_n^2}{\Delta f} \sum_{n=0}^{\infty} c_n^2}{8 q_{max}^2 (\Delta\omega)^2} \right]$$

Cn represents the coefficients of the VCO Fourier series. As mentioned earlier, qmax shows the maximum charge that can be stored in the capacitor. The noise power spectrum is shown by the term $i_n^2/\Delta f$. As discussed earlier, we can reduce the inductor noise by decreasing its value. Regarding this issue, the current needed for the compensation of lossy resonator will minimize. Consequently, the VCO suffers from less noise which is one of our goals. To meet the desired center frequency, if we reduce the inductor size the capacitor value should be increased[9].

Applying the proper Vdd equal to the overall threshold voltage of an NMOS and a PMOS transistor, only two transistors will conduct in each of the half oscillation periods. This issue saves the power and decreases the overall noise. Overall, the phase noise performance will be improved.

IV. SIMULATIONS AND RESULTS

In this section of the paper, we verify our previous results by a more detailed analysis. Here, we do the final integration of VCO sub-blocks to approach the state-of-the-art phase noise and power consumption. To meet the design specifications precisely, we have tested VCO performance for varying temperature, supply voltage and tuning range. Additionally, a wider comparison is made between different VCO topologies regarding the phase noise and power consumption. As a result, we have obtained a deeper understanding of different VCO topologies regarding their applications and frequency range of oscillation.

A. Phase Noise and Frequency vs. Control Voltage

To verify the frequency range of our designed QVCO, the tuning voltage is swept from 0.2 V to 1.2 V. From the simulation results, the frequency range is observed from 2.25 GHz to 2.55 GHz. The center frequency is 2.4 GHz which matches our specification requirements. Moreover, due to control voltage and frequency variations, the phase noise changes correspondingly[4]. In Fig. 4, the blue plot demonstrates the frequency variation controlled by tuning voltage while the red curve shows the phase noise variation versus frequency and tuning voltage.

As understood from the red plot, the phase noise is considerably high at low tuning ranges. At low tuning voltages, the quality factor of the varactor is quite small. Therefore, the overall quality factor of the resonator reduces and this leads to higher phase noise. However, as the tuning range increases, the phase noise improves and finally it reaches to our desired value at the center frequency.

10.32377/cvrjst0614

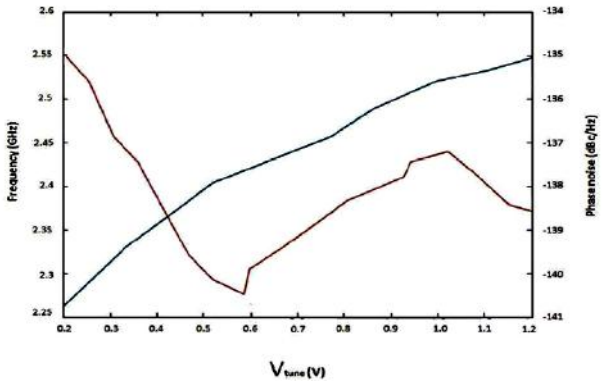

Figure. 4: QVCO Phase Noise and frequency versus control voltage.

B. Reference current source variation

In this section, we have analyzed the Impact of reference current source variation on the center frequency . the supply voltage is set at 1.2 V while the reference current is swept from 150µA to 210µA. As observed from fig.5 there is a small deviation from the center frequency when the reference current is swept from 150µA to 210µA.

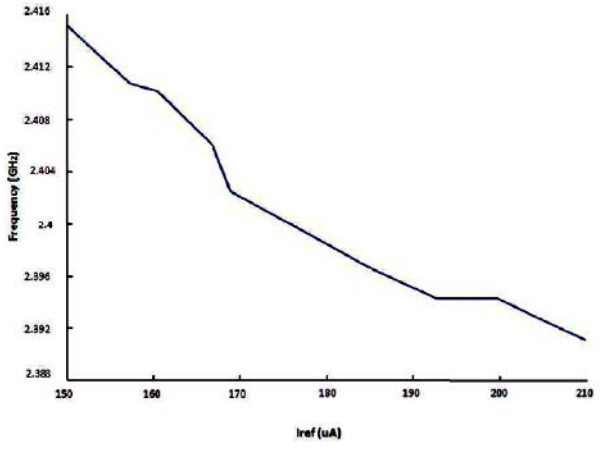

Figure. 5: Impact of reference current source variation on QVCO center frequency

C . Phase Noise and Frequency Vs temperature

In this section , we have analyzed our proposed QVCO performance versus temperature variation . The tall current is set at 3 mA while the supply voltage is 1.2V applying a tuning of 0.6 V, the temperature is swept from -50oC to 175oC . The Fig. 6. demonstrates the phase noise dependency on temperature . as we know the thermal noise is directly proportional to temperature and this leads to poor phase noise performance as the temperature increases .

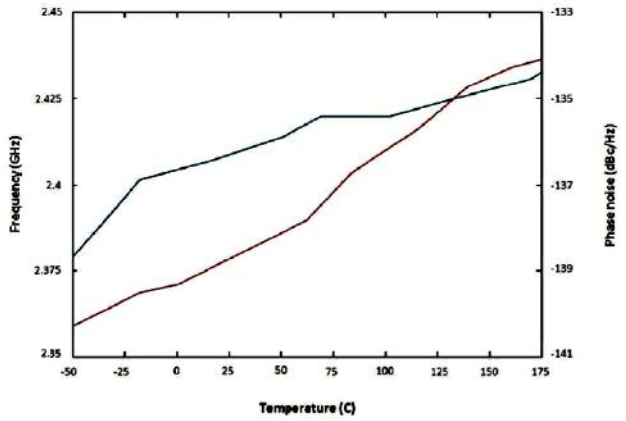

Figure .6: Impact of temperature variation on QVCO phase noise and frequency

CONCLUSION

In this work, we studied the basic theory of an oscillator. In the following sections, the noise contributors affecting the VCO performance are identified. Furthermore, different models interpreting the noise impact on a voltage-controlled oscillator are presented.

The main purpose of this project is to implement a state-of-the-art design considering optimal phase noise and power consumption. Initially, to achieve a high performance VCO, we have designed different high performance LC VCO architectures. Moreover, a wide comparison is carried out regarding the VCO specifications such as phase noise at different offset frequencies, power consumption, FOM and so forth. As a result, a suitable LC VCO topology is chosen for further analysis. Afterwards, we have improved our design to a Quadrature VCO with back-gate coupling and source resistive degeneration.

The designed QVCO oscillates at the center frequency of 2.4 GHz. The phase noise estimated by simulation at 1MHz offset frequency is -140dBc/Hz. The circuit consumes a power of 3.6mW which is less than conventional QVCO architectures. Finally, to verify our design, process, temperature, and reference current variations were tested. As a result, the specification requirements have been met in our design.

REFERENCES

[1] P.K. Rout, U.K. Nanda, D.P. Acharya, G. Panda, “Design of LC VCO for optimal figure of merit performance using CMODE”, 1st International Conference on Recent Advances in Information Technology (RAIT), pp. 761 – 764, March 2012.

[2] S. Zihir, F. Tasdemir, T. Dinc, Y. Gurbuz, “A new resonant circuit for 2.45 GHz LC VCO with linear frequency tuning”, Microwave Integrated Circuits Conference (EuMIC), pp. 390 – 393, Oct. 2011.

[3] P. Liu, P. Upadhyaya, J. Jung, D. Heo, J.-H. Kim, B.-S. Kim, “Dynamically switched low-phase-noise LC VCO with harmonic filtering”, Electronics Letters, vol. 47, pp. 792 – 793, July 2011.

[4] B. Soltanian, P. Kinget, “A Low Phase Noise Quadrature LC VCO Using Capacitive Common-Source Coupling”, 32nd European Solid-State Circuits Conference (ESSCIRC), pp. 436 – 439, Sept. 2006.
[5] Han-il Lee, Tae-Young Choi, S. Mohammadi, L.P.B. Katehi, “An extremely low power 2 GHz CMOS LC VCO for wireless communication applications”, The European Conference on Wireless Technology, pp. 31 – 34, Oct. 2005.
[6] Harikrishnan Ramiah, Tun Zainal Azni Zulkifli, “A Low-Phase Noise and High Output Swing RF LC-VCO in CMOS Technology”, RF and Microwave Conference, pp. 197 – 200, Sept. 2006.
[7] Yang Zhang, Peng Liu, Tang-Nian Luo, Yi-Jan Emery Chen, Deukhyoun Heo, “A low-voltage low-phase-noise bottom-series LC QVCO using capacitor tapping technique”, Microwave Symposium Digest, pp. 237 – 240, June 2008.
[8] M D Wei, S Chang, Y Yang, "A CMOS Backgate-Coupled QVCO Based on Backto- Back Series Varactor Configuration for Minimal AM-to-PM Noise Conversion ", Microwave and Wireless Components Letters, IEEE , pp. 320 - 322, (2009).

10.32377/cvrjst0614