Design of Low Cost Sigma-Delta Analog-to-Digital Converter for Audio Applications

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***Abstract*— FPGA (Field-Programmable Gate Array) based solutions in consumer electronics have gained popularity due to low cost and high performance. The time-to market is also shorter and the financial risk is lower compared to ASIC (Application Specific Integrated Circuit). One component that is missing in a low-cost FPGA is the ability to convert an analog signal to its digital counterpart. The aim of this paper is to implement an ADC (Analog-to-Digital Converter) for audio applications using external components together with an FPGA (Field-Programmable Gate Array). The focus is on making the ADC low-cost and it is desirable to achieve 16-bit resolution at 48 KS/s. Since large FPGA's have numerous I/O-pins, there are usually some unused pins and logic available in the FPGA that can be used for other purposes. This is taken advantage of, to make the ADC as low-cost as possible.**

This paper presents two types of converters an Σ-Δ (Sigma-Delta) converter with a first order passive loop-filter and an Σ-Δ converter with a second order active loop-filter. The solutions have been designed on a PCB (Printed Circuit Board) with a Xilinx Spartan FPGA. Both solutions take advantage of the LVDS (Low-Voltage-Differential-Signaling) input buffers in the FPGA. First converter achieves a peak SNDR (Signal-to-noise-and-distortion-ratio) of 62.3 dB (ENOB (Effective number of bits10.06 bits)and it is very low-cost but is not suitable for high-precision audio applications. Second converter achieves a peak SNDR of 80.3 dB (ENOB 13.04) and the cost is more comparatively first one but it is more suitable for mono audio and for stereo audio applications.

***Index Terms*- FPGA, ADC, SNDR, Sigma-Delta converter, ENOB, Xilinx Spartan, LVDS.**

I. INTRODUCTION

An FPGA is an integrated circuit, which have a large number of logic resources that can be configured to implement complex digital algorithms. The configuration can be done after manufacturing and is specified using a HDL (Hardware description language). This paper will take advantage of the strength of the FPGA. The aim of this paper is to implement an ADC (Analog-to-Digital Converter) for audio applications using an FPGA together with external components. Two solutions are presented: (1) a **Σ**-Δ converter with a first order passive loop-filter and (2) a **Σ**-Δ converter with a second order active loop-filter. In both solutions, the FPGA will mainly **b**e used to implement digital filters.

The main objective is to try eliminating the external ADC and replacing it with external components and using the power of the FPGA. The goal is therefore to make it low-cost and it is desirable to achieve CD quality, i.e. 16-bit resolution at 44.1 KS/s. In this design will use 48 KS/s and the goal is to achieve 16-bit resolution. The term "low-cost", in this paper, is only focusing on the external components. The goal is to keep the total cost of the external components at a minimum. However, the FPGA resources used should also be kept at a minimum. Since large FPGA's have numerous I/O-pins, there are usually some unused pins and logic available in the FPGA that can be used for other purposes. This is taken advantage of, to make the ADC as low-cost as possible.

In this section, the fundamental operation of an ADC is described. Furthermore, it describes the basic operation of an **Σ**-Δ converter and in particular the CT **Σ**-Δ converter. Since the **Σ**-Δ converter is a oversampling converter, there is a chapter about digital filtering and decimation (down sampling). The main objective of an ADC is to convert an analog signal into its digital counterpart, so it can be further processed by digital circuits. An analog signal is in its nature continuous in both time and amplitude, while a digital signal is discrete in both time and amplitude. This process can be divided into two sections: Sampling and Quantization See Figure.1 for an illustration of the ADC system.

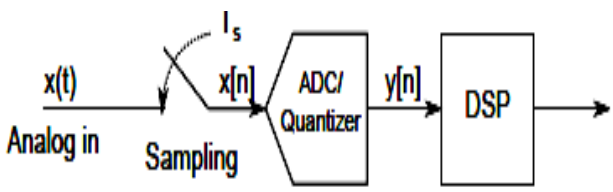

Figure.1: From analog input signal, $x(t)$, to output, $y[n]$, which is later processed by e.g. a DSP .

Sampling is a process that converts a continuous time signal into a discrete time signal. The signal, $x(t)$, is sampled at a uniformly spaced time intervals, Ts. An anti-aliasing filter is usually placed before the sampling [1], to prevent the overlapping. The Nyquist theorem sets a boundary for the sampling frequency. A/D-converters that operates close to the boundary is called Nyquist-rate converters and converters that operate at a much higher frequency is called oversampling ADCs. The analog signal must also be mapped to discrete levels. This is done by the quantization process. The word length, in number of bits N, decides the resolution of the ADC and the number of levels is $2N$.

II. Implementation of a Passive Σ-Δ Converter

This section will describe the implementation of a low-cost passive **Σ**-Δ converter. First there will be a section about the system overview. Thereafter there will be a section about the implementation of the modulator itself. The System Overview is illustrated in Figure. 2 and the specifications for the proposed ADC are listed in the Table.1.

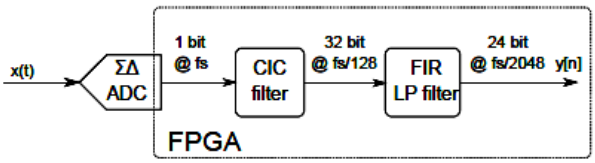

Figure 2: System overview of the passive **Σ**-Δ ADC.

TABLE I
SPECIFICATION FOR THE PASSIVE Σ-Δ ADC.

Specification	Symbol	Value
Sampling frequency	f_s	98.304MHz
Oversampling ratio	OSR	2048
Output sampling rate	f_{OUT}	48KS/s
Supply voltage	V_{dd}	3.3V (Single supply)
Input bandwidth	f_B	20KHz
Input voltage amplitude (max)	A_{in}	1.65 V

A. *The Passive Σ-Δ Modulator*

In order to cut the cost of an **Σ**-Δ ADC, the loop-filter consists only of passive components. The loop-filter of a typical (active) **Σ**-Δ is employing integrators with high gain (e.g. RC-integrators). One can make an integrator of passive components with e.g. a RC-filter, a so called "lossy integrator" with no gain. The linearization of the passive **Σ**-Δ is shown in Figure 3. The gain G is the gain of the quantizer /comparator [2].

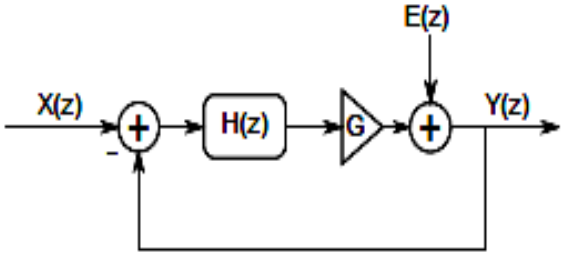

Figure 3: Linearization of the passive **Σ**-Δ ADC.

The transfer function becomes:

$$Y(z)=\frac{GH(z)}{1+GH(z)}X(z)+\frac{1}{1+GH(z)}E(z)$$

The gain factor G is assumed to be constant. [3] estimates the value of G by nulling the input, x. The 1-bit output, y[n], will alternate (ideally) between 0 and 1 at a rate of fs=2. This signal is then passed to the (low-pass) loop filter by a DAC. If the sampling frequency is high enough the signal is attenuated by a factor jH (f = fs=2) j, and this G is roughly:

$$G\approx\frac{1}{\left|H(f=f_s/2)\right|}$$

A first order RC-filter with transfer function

$$H(s)=\frac{1}{RCs+1}=\frac{1}{\frac{s}{w_p}+1}$$

The total system of the passive **Σ**-Δ converter is illustrated in Figure.4.

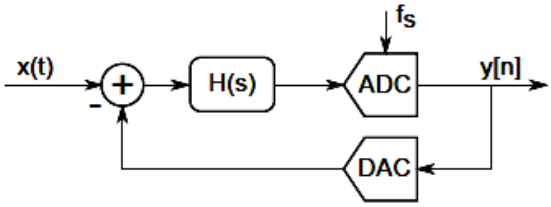

Figure 4: The passive **Σ**-Δ converter.

The ADC in Figure 4 is chosen to be a 1-bit quantizer, employing the LVDS buffer in the FPGA, sampled at fs = 98:304MHz. The DAC is chosen to be a 1 bit DAC, which only uses one pin on the FPGA. Figure 5 illustrate the 1-bit DAC. Here, the output of the FPGA is chosen to be a tri-state buffer and therefore the output of the DAC can either be Vdd, GND or T. This tri-state buffer can be used to create NRZ, RZ and HRZ DAC pulses. T stands for tri-state and is a high output impedance state (no current can flow out of the FPGA). NRZ pulses are either "high" or "low" for the whole sample period, i.e., it doesn't employ the T-state. On the other hand, the T-state can be used to implement RZ

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and HRZ pulses which are "off" for half of the sample period. One thing to take into account is the parasitic capacitance associated with the pad, Cp. This capacitance is max 10pF [9]. This implies that the time constant, $R_{DAC}C_p$, is low.

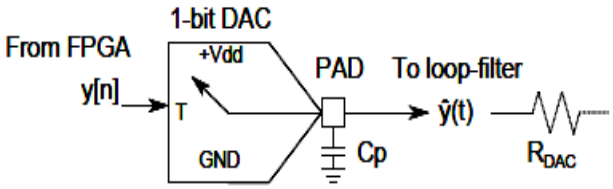

Figure 5: Simple illustration of an 1-bit DAC.

The chosen 1-bit DAC will use NRZ pulses because of the simplicity and "minimal" impact of the parasitic capacitance. The converter is therefore only using three pins on the FPGA: two for the LVDS buffer and one for the NRZ DAC.

B. *Realization of the Passive Σ-Δ Converter*

The Figure .6 illustrates the realization of the **Σ-Δ** converter. The 1-bit digital out will be further processed (filtered and decimated) by the CIC and FIR filter. The reference signal (vref) is mid-range, i.e. $Vdd=2 = 1{:}65V$. The chosen component values are presented in Table 2.

TABLE II
COMPONENT VALUES FOR THE PASSIVE **Σ-Δ** MODULATOR

Component	Value
RIN	6:8*K*
RDAC	6:8*K*
C	1*nF*
R	6:8*K*
CIN	1*μF*

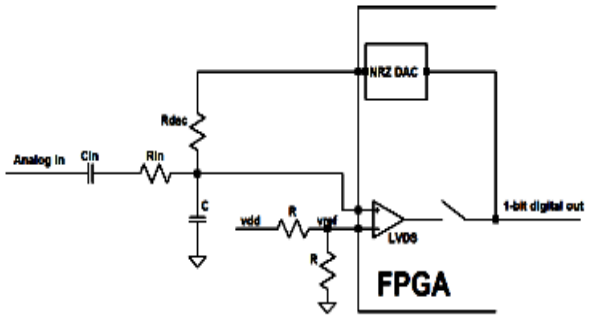

Figure .6: Realization of the passive **Σ-Δ** converter [6].

III. IMPLEMENTATION OF A SECOND ORDER Σ-Δ CONVERTER.

This section will describe the implementation of a second order **Σ-Δ** converter. The **System** Overview of the complete system of the second order **Σ-Δ** converter is illustrated in Figure. 7 and the system specifications are shown in Table 3.

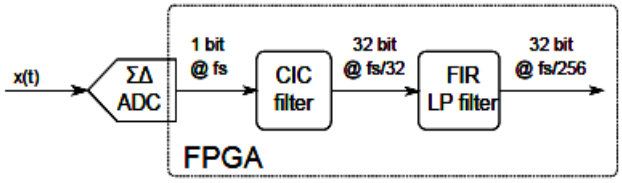

Figure 7: System overview of the second order **Σ-Δ** converter.

TABLE III
SPECIFICATION FOR THE SECOND ORDER **Σ-Δ** ADC.

Specification	Symbol	Value
Sampling frequency	*fs*	12.288MHz
Oversampling ratio	OSR	256
Output sampling rate	*fOUT*	48KS/s
Supply voltage	*V dd*	3.3V(single supply)
Input bandwidth	*fB*	20KHz
Input voltage amplitude (max)	*Ain*	1.65 V

A. *The 2nd Order CT Σ-Δ Modulator*

The 2nd order CT **Σ-Δ** feed-forward modulator is shown in Figure 8.

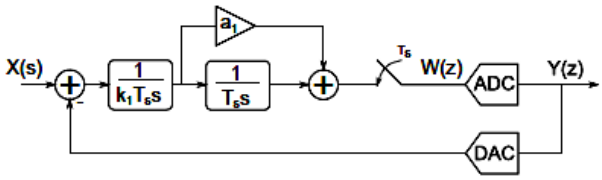

Figure 8: A 2nd order CT **Σ-Δ** feed-forward modulator.

The ADC is a 1-bit quantizer using the LVDS buffer (as a comparator) in the FPGA. The DAC is chosen to be a 1-bit DAC employing NRZ pulses. The DAC will only use one output pin on the FPGA. By using NRZ DAC, the coefficients $k1$ and $a1$ becomes 1 and 1.5, respectively.

B. *Realization of the 2nd order CT Σ-Δ modulator*

The realization of the modulator is shown in Figure 9. The loop-filter is a single amplifier section, derived from [24], this loop-filter only use one OP amplifier, which is better than two in a low-cost perspective.

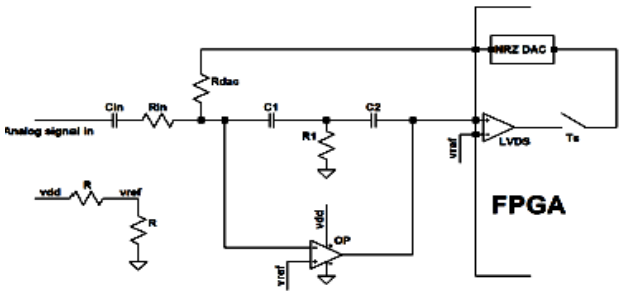

Figure 9: Realization of the 2*nd* order CT **Σ**-Δ modulator.

The reference voltage is mid-range, i.e. Vdd=2 = 1:65V and is generated by a voltage divider with two resistors. The transfer function from the DAC to the input of the LVDS buffer is:

$$H_\gamma(s) = -\frac{R_1(C_1+C_2)s+1}{R_{DAC}R_1C_1C_2s^2} = -\frac{a_1T_s s+1}{k_1T_s^2 s^2}$$

Where

$$R_1(C_1+C_2) = a_1T_s$$
$$R_{DAC}R_1C_1C_2 = k_1T_s^2$$

Table. 4 show the chosen component values. The chosen component values corresponds to $a1$ = 2:5 and $k1$ = 156.

TABLE IV
COMPONENT VALUES FOR THE LOOP FILTER IN THE SECOND ORDER Σ-Δ MODULATOR.

Component	Value
C1	100pF
C2	100pF
R1	1K
RDAC	100K
RIN	100K
R	4.7K
CIN	1μF

IV. Simulation Results

To observe the simulation results the PC generates a sine wave which is sent to an external sound card, the M-Audio Fast Track Pro. The sound card is then generating an analog signal of the sine wave which is sent to the DUT (Device under Test). The DUT is the converter under test, which is a PCB with the FPGA and external components. The result of the A/D-conversion, generated by the DUT, is then fed back to the sound card using S/PDIF with 24 bits resolution, which is then recorded by the PC. The collected data is analyzed in Matlab.

This section presents the simulation results for the two types of Σ-Δ converters. The simulation was done using Simulink / Matlab with the passive modulator and 2*nd* order CT **Σ**-Δ modulator. The filtering and decimation used in this simulation are "ideal", in order to characterize the **Σ**-Δ modulator only. Figure 10 shows an FFT plot of the output of the modulator. The input signal is 2 KHz and has an amplitude of 1V

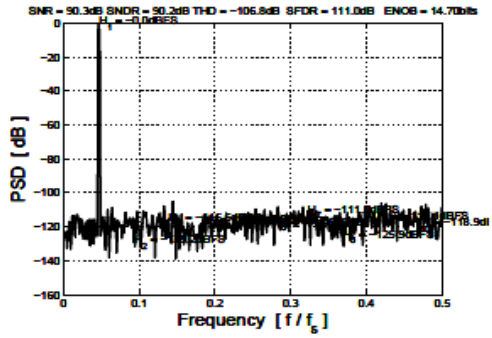

Figure 10: 1024 point FFT plot of the output of the passive **Σ**-Δ modulator.

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The Figure 11 shows the SNDR/SNR vs. input frequency and Figure. 12 show the SNDR/SNR vs. input amplitude of the output of the passive **Σ**-Δ modulator.

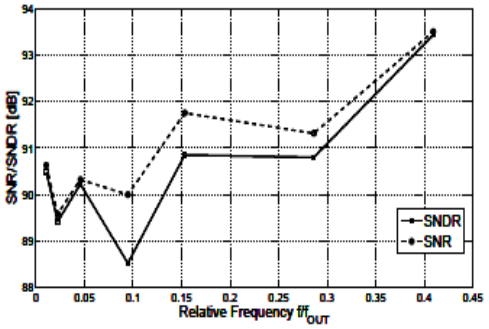

Figure 11: SNDR and SNR vs. Input Frequency. Using a 1V input signal.

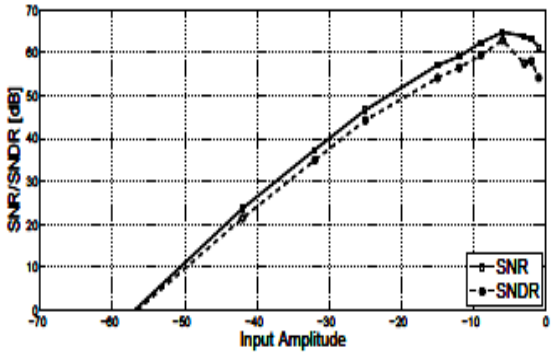

Figure 12: SNR and SNDR vs. input amplitude using a 7.3 KHz input signal.

The Figure.13 shows an FFT plot of the second order converter and Figure 14 shows SNR/SNDR vs. frequency of the output of the converter.

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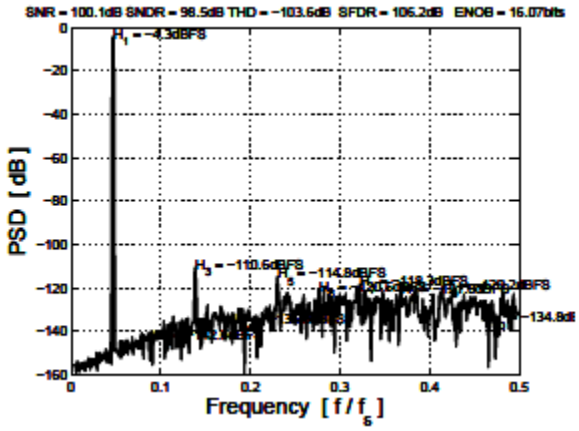

Figure 13: Simulation result of the second order **Σ**-Δ modulator using 1024 points FFT, 1V input amplitude (-4.3 dBFS).

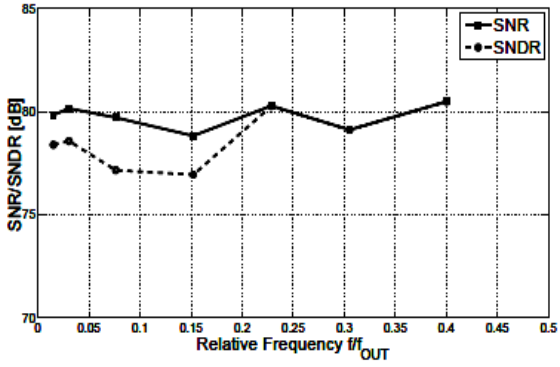

Figure 14: Simulation result of the second order **Σ**-Δ modulator, SNR/SNDR vs. Frequency.

Figure 15 shows the SNDR/SNR vs. input amplitude of the output of the **Σ**-Δ modulator.

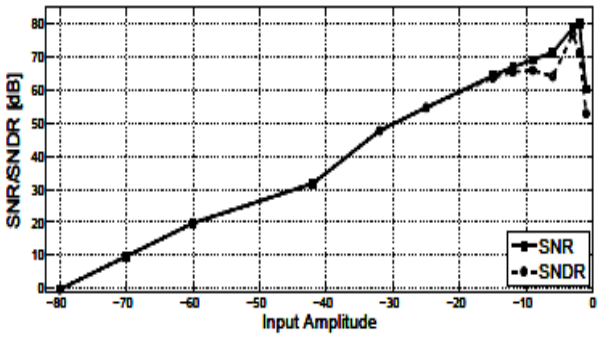

Figure 15: SNR and SNDR vs. input amplitude, using a 7.3 KHz input frequency.

CONCLUSION

The Table 5 shows a comparison between the passive **Σ**-Δ converter and the second order **Σ**-Δ converter and the converter that is used today in a product from Actiwave: PCM1807 from Texas Instruments. I have used the same test setup as indicated in section IV the PCM1807, except that it is powered from another power supply. Since the PCM1807 is a dual channel ADC, the resources are divided by two in order to compare it with my two solutions.

The prices of PCM1807 ($0.90) and LMV793 ($0.45) are taken from Texas Instruments website [5][3]. The prices for the passive components (resistors and capacitors) are set to $0.01. The prices don't include the decoupling capacitors needed. With proper design and careful PCB layout with the PCM1807, the theoretical SNDR is typical 93dB (ENOB _15.15) according to the datasheet of the PCM1807 [21]. But in order to compare the A/D converters, the same test setup is used (except for another power supply used for PCM1807).

According to Table 5, there can be conclusions:

1. The first order passive CT **Σ**-Δ is moderate in SNDR, but with low cost of external components and with relative large FPGA area. If there's a priority in low-cost the first order passive CT **Σ**-Δ is a good choice.
2. The second order CT **Σ**-Δ have the best SNDR, but with large FPGA area and highest cost per channel. With demands for good quality in SNDR the second order CT **Σ**-Δ is a good choice.

TABLE V
COMPARISON BETWEEN THE A/D CONVERTERS. SINCE THE PCM1807 IS A DUAL CHANNEL ADC, ITS RESOURCES ARE DIVIDED BY TWO.

Dynamic parameter	1st order passive CT Σ-Δ	2nd order CT Σ-Δ	Actiwave AB with T1PCM1807
SNR [dB]	63	80.3	77.9
SNDR [dB]	62.3	80.3	77.8
ENOB [bits]	10.06	13.04	12.63
Resources/channel FPGA			
I/O Pins	3	3	4/2
Slice regs	597	610	256/2
LUTs	408	426	146/2
Block RAMs	5	3	0/2
DSP	8	5	0/2
DCM/PLL	1	1	1/2
Resources/Channel Components			
Active components	0	1	1/2
Passive components	6	7	2/2
Total price [$]	0.06	0.53	0.46

3. The PCM1807 have good SNDR, small FPGA area and fairly high cost of external components. If there's demand for small FPGA area and good quality in SNDR an external ADC (such as the PCM1807) is a good choice.

There seems to be a tradeoff between quality (e.g. SNDR), FPGA area and cost. It is some difficulty to

compare the two converters presented in this paper with the PCM1807. For instance, PCM1807 need two voltages (3.3V and 5V) in order to function [7]. This adds up to the total price for the Actiwave AB solution, which is not listed in Table 5.

The two converters presented in this paper can easily be doubled in order to convert stereo audio (like the PCM1807). This doesn't necessary scale the resources of the FPGA and the total price by a factor of two. For instance, one can use LMV794 (which is two LMV793 in a single package) for the second order CT **Σ**-Δ converter in order to convert stereo audio. The price for LMV794 is $0.63 [4] which implies a total price of $0.71 for the second order CT **Σ**-Δ converter with dual channel. The corresponding total price for the PCM1807 (dual channel) is $0.92.

The two converters presented in this paper can be used for other purposes. For example, the passive **Σ**-Δ converter can easily be modified to be able to convert other analog signals, e.g. signals from sensors that perhaps only need 10 bits ENOB and is very low-cost.

The recommendation for Actiwave AB is not to use the passive CT **Σ**-Δ converter for audio applications. Since Actiwave AB is working with high precision audio, this is not an option. But the passive CT **Σ**-Δ converter can be used for other applications, e.g. convert analog signals from sensors.

To cut cost, Actiwave AB could use the second order **Σ**-Δ converter in a dual channel configuration (with LMV794) instead of the PCM1807. However, the LVM794 has to be tested and further investigation of the second order CT **Σ**-Δ converter is necessary in order to achieve 16 bits ENOB.

References

[1] Pervez M. Aziz, Henrik V. Sorensen, and Jan Van Der Spiegel. An Overview of Sigma-Delta Converters: How a 1-bit ADC achieves more than 16-bit resolution. IEEE Signal Processing Magazine, 13:61, 1996. Cited on pages 10 and 11.

[2] Feng Chen and Bosco Leung. A 0.25-mW Low-Pass Passive Sigma-Delta Modulator with Built-In Mixer for a 10-MHz IF Input. IEEE Journal of Solid- State Circuits, 32(6):774–782, 1997. Cited on pages 34 and 35.

[3] Texas Instruments. LMV793, July 9 2013. http://www.ti.com/product/lmv793. Cited on page 57.

[4] Texas Instruments. LMV794, July 9 2013. http://www.ti.com/product/lmv794. Cited on page 58.

[5] Texas Instruments. PCM1807, July 9 2013. http://www.ti.com/product/pcm1807. Cited on page 57.

[6] Lattice Semiconductor Corporation. Simple Sigma-Delta ADC, November 2010. RD1066. Cited on pages 2, 37, and 62.

[7] Texas Instruments. PCM1807: Single-Ended, Analog-Input 24-Bit, 96-kHz Stereo A/D Converter, September 2005. SLES147. Cited on pages 1, 57, and 58.

[8] Lars Wanhammar. Analog Filters Using MATLAB. Springer, 2009. ISBN 978-0-387-92766-4. Cited on pages 24, 48, and 61.

[9] Xilinx. Spartan-6 FPGA Data Sheet: DC and Switching Characteristics, v.3.0 edition, October 2011. DS162. Cited on pages 6 and 36.

[10] Axel Zimmermann, Endric Schubert, and Christian Grumbein. Integration of Analog-Digital and Digital-Analog Converters into FPGA-Based Microcontrollers. 2011. Cited on page 2

10.32377/cvrjst0612