Design And Implementation Of A Cyclic ADC For CMOS Image Sensors

O. Venkata Krishna[1], B. Janardhana Rao[2]
[1]CVR College of Engineering/EIE, Hyderabad, India
Email: venkatakrishna.odugu@gmail.com
[2]CVR College of Engineering, Hyderabad, India
Email: janardhan.bitra@gmail.com

***Abstract*— The constant strive for improvement of digital video capturing speeds together with power efficiency increase, has lead to tremendous research activities in the image sensor readout field during the past decade. The improvement of lithography and solid-state technologies provide the possibility of manufacturing higher resolution image sensors, as they provide possibilities for reduced power consumption and integration of complete on-chip cameras. With the increase of image sensors' resolution and frame rate, traditional serial readout schemes become more laborious to design and in many cases simply unachievable for certain required readout speeds. This transfer however imposes additional demands to parallel ADC designs, mainly related to achievable accuracy, area and power.**

In this paper a 12-bit Cyclic ADC (CADC) is designed and implemented in 180nm CMOS technology aimed for column-parallel readout implementation in CMOS image sensors. The multiple CADC sub-component architectures and few various Multiplying DAC (MDAC) structures have been re-examined and implemented. Three comparator architectures have been explored and a dynamic interpolative Sub-ADC is presented. Finally, some weak spots degrading the performance of the carried-out design have been analyzed. As an architectural improvement possibility two MDAC capacitor mismatch error reduction techniques have been presented.

***Index Terms*—ADC, DAC, Sensor, CMOS, Low power, Switched Capacitor, Comparator.**

I. INTRODUCTION

The target of this paper is to design an algorithmic, also commonly known as cyclic, ADC architecture for the purpose of its implementation in a column-parallel readout CMOS image sensor. With the increase of image sensor's resolution and frame rate, traditional serial readout schemes become more laborious to design and in many cases simply unachievable for certain required readout speeds.

A possible solution to this problem is the usage of multiple parallel working ADCs, in order to relax the speed requirements of the otherwise standalone data converter. This solution to the problem however, as in any technological problem has its advantages, challenges and disadvantages. One of the challenge points in column-parallel ADCs appear to be the tight silicon area and power consumption requirements. As various ADC architectures exist, among the compact ones strike to be the algorithmic (cyclic) ADC. The most relevant reasoning about the conduction of this study on cyclic ADCs is the low area requirements as well as the reasonably high resolutions and conversion rates achievable with this type of converters.

Historically the first trials of image sensor developments date back to 1969, when Willard Boyle and George Smith at Bell Labs invented the first charge-coupled device (CCD), which a few years later was implemented in the Hubble Space Telescope [2]. In the same decade range a non-charge-transfer imaging device, as we know it nowadays as CMOS image sensor, was introduced. Even though that both technologies are based on converting photons to electrical charges, CCD based image sensors gained higher velocity due to the fact that they provided much better imaging qualities with the existent semiconductor technology. In the later years, starting late 1980s, with the development of high precision lithography and silicon purification technologies, CMOS image sensors gained popularity, as they provide possibilities for reduced power consumption and integration of complete on-chip cameras. The most important pixel parameters of the image sensors required as input data for the ADC design, Output range, Integration (exposure) time, Reset time and Noise boundary.

The Table 1. lists the main imposed ADC requirements for this work. The provided specifications have been kept in mind during the design. The required sampling speed has been set to comply with a readout speed of 60 frames per second on a 1080p vertical resolution sensor utilizing digital correlated double sampling.

TABLE I
SPECIFICATIONS OF ADC

Parameter	Value	Unit
Resolution	12	bits
Sampling Rate	>130	KSps
Integral Non-Linearity	<10	LSB
Differential Non-Linearity	<0.5	LSB
Power Consumption	300	µW
Supply Voltage	3.3	V
Technology	180	nm
Area		µm

II. Design and Implementation of Cyclic ADC

A broad seek for simple architectures incorporating digital correlated double sampling (Digital CDS) and no need for the pixel's signal pre-conditioning was performed. A few attractive architectures in literature were found [5] ,[4] & [7], in a sense that all of them incorporated the fore-mentioned basic functionality, combined with simple choice of circuitry, namely single-ended MDAC designs. The reasons for the hunt after simplified circuits employing single-ended schematics, stood behind the main design limit, which is the narrow column pitch in high resolution image sensors 2 to 6 μm, demanding very low area designs. To achieve high frame rate and high resolution from a sensor, could practically only be achieved with the column-parallel readout architecture.

This section aims to give an overview of the proposed ADC. The block diagram of the cyclic converter shown on Figure 1. The converter utilizes an almost similar single-ended MDAC structure but, in this split of the sampling capacitor into two sub-capacitors allowing the generation of the mid-reference locally. The converter utilizes the popular 1.5 bit redundant signed digit conversion, thus allowing for relaxed comparator offset requirements by utilizing a digital error correction.

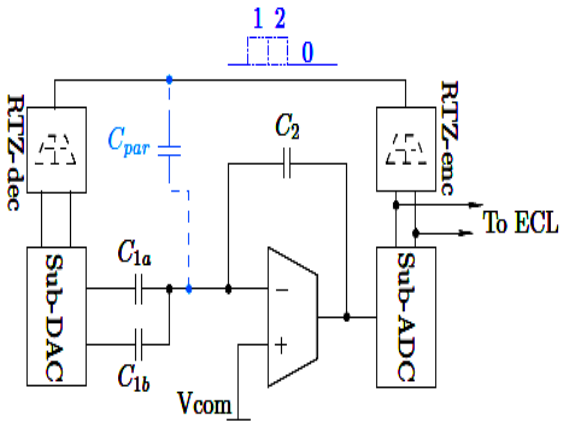

Figure 1. The Principal diagram of Cyclic ADC architecture.

One major disadvantage with respect to the circuit's performance of the proposed MDAC architecture is its single-ended nature. A differential structure would typically be more insensitive to common-mode noise and provide a more stable readout and parasitic insensitiveness. However due to the additional circuit complexity and two extra sampling capacitors as well as switches required, it appeared to tilt the scales towards a single-ended architecture. While in an isolated case a single-ended structure would give much worse performance results, in a mutual aid with Digital CDS as well as the RTZ coding technique, could potentially provide enough noise independence and accuracy to suit for a 12-bit column-parallel ADC.

A In-DAC mid-reference generation scheme

The in-DAC reference generation Figure 2. proposed by [5], practically utilizes the MDAC sampling capacitor as a capacitive divider during the feedback phase to generate the third mid-reference locally from the fed-in *VrefH* and *VrefL*.

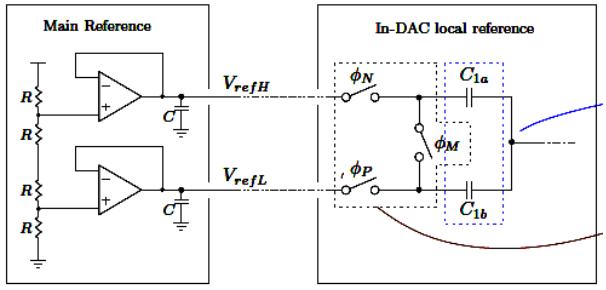

Figure 2. Local in-DAC mid-reference generation.

Apart from the obvious silicon area improvement advantage, by relaxing the requirements of the external voltage reference block or in other words removing one extra required reference voltage to be routed, this internal generation scheme allows for a more accurate mid-reference generation, regardless of the absolute values of the *VrefH* and *VrefL* references. Of course all these statements imply that such resulting converter linearity improvements with this scheme would be possible only by having highly matched sampling capacitors.

B RTZ coding scheme for parasitic sensitivity relaxation

While a fully differential configuration is less sensitive to parasitic coupling of the feedback signals from the sub-ADC, a single-ended structure can not boast with such an advantage. Theoretically the differential MDAC should be 4/6 times less sensitive to parasitic or to formulate it, the error voltage due to parasitic coupling to the summation node will be equal for a single-ended case to:

10.32377/cvrjst0604

$$V_{err} = \left(\frac{C_{par1}}{C_2} andD_0 + \frac{C_{par1}}{C_2} andD_1 \right) V_{data-line}$$

Although it might be possible to guard the data lines with an extra metal for wider-pitched columns, the authors proposed a return to zero (RTZ) encoding scheme for an effective reduction of the parasitic coupling to the charge summation node. The principal diagram of the ADC architecture on Figure 1. gives an outline of the RTZ coding scheme. The thermometer code from the Sub-ADC is encoded into a pulse width modulated signal, which is quickly transmitted before the very end of the feedback phase. In this way the effect of the parasitic couplings to the charge summation nodes is reduced practically to almost zero. The parasitic effect from these nodes will only be dependent on the transmission speed of the pulse-width encoded signal.

C The MDAC in details

This section aims to provide a detailed analysis of the re-examined MDAC implemented by [5] and comment on its advantages and disadvantages. As a start Figure 3. shows a principal schematic of the MDAC, built-up around an operational transconductance amplifier. An OTA is a common choice for applications with small capacitive loads, as the case of the MDAC is, due to a row of reasons, standing behind the circuit simplicity of an OTA, or mainly the lack of an output buffer stage in comparison with most OPs.

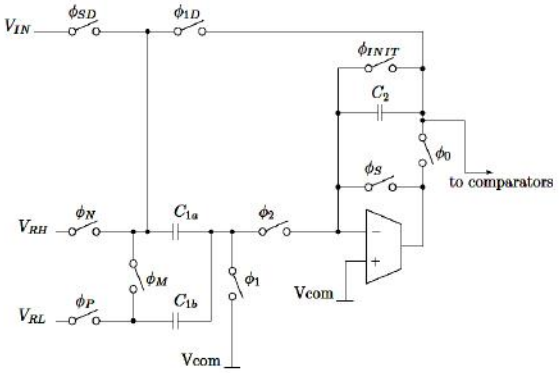

Figure 3. Principal schematic diagram of the MDAC.

The MDAC structure differs slightly from the "Modified Flip-Around" structure, apart from the split sampling capacitor allowing for internal mid-reference generation, the structure halves the accommodated OTA offset. This results in a global ADC offset, which should not be troublesome and in addition the DCDS technique should fully cancel-out such offset. To go through the functionality of the MDAC we can look at the separate sub-phases and perform a charge redistribution analysis. Figure 4. shows the 4 basic modes of operation of the MDAC.

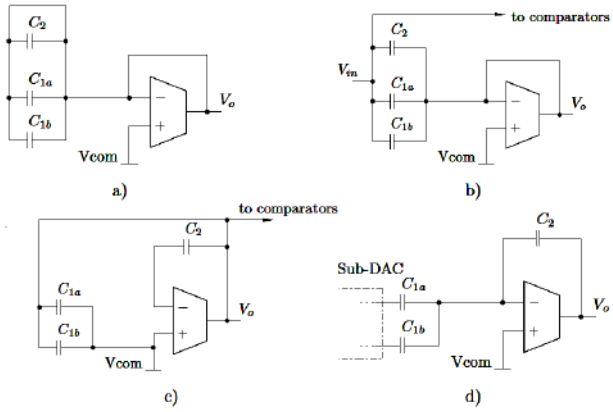

Figure 4. Detailed MDAC configurations for the four phases.

D Functional analysis

Before performing signal sampling, in order to make sure that there is no residual charge from previous conversions and make sure all conditions are the same for every CDS step, all capacitors are reset for a short period of time, Figure 4 a). After completion of this phase, signal sampling can start, Figure 4 b). This implies that the charge stored in the capacitors would be:

$$q_{1a}(t) = (V_{in} - V_{com} + V_{os})C_{1a}$$
$$q_{1b}(t) = (V_{in} - V_{com} + V_{os})C_{1b}$$
$$q_2(t) = (V_{in} - V_{com} + V_{os})C_2$$

During the next - feedback phase, Figure 4. c) the sampled signal is amplified by two. Here is the place to mention again that the accumulated offset during sampling will appear as a global ADC offset with half the magnitude of the OTA offset, as capacitor *C*2 had stored the offset in the previous phase and during the present phase is connected in the feedback loop, thus the amplifier would have added half the OTA offset. The fourth phase performs the analogue subtraction. Depending on the decisions taken during the feedback phase by the Sub-ADC, the top plates of *C*1*a* and *C*1*b* are connected to the reference voltages.

III. COMPARATOR IMPLEMENTATIONS

A Static latched comparator.

To begin with a simple static latched comparator is shown on Figure 5 as proposed by [3]. Transistors *M*1, *M*2, *M*3 and *M*4 are forming a differential amplifier, which controls the current flow through the latch composed of transistors *M*5 and *M*6 via the control transistors *M*7 and *M*8. The decision is taken when the reset transistors' *Vgs* is pulled down, thus releasing the latch from reset state, depending on the currents flowing through the differential pair, thus the two latch

branches, one of the transistors *M*5 or *M*6 switch on first and trigger the regeneration.

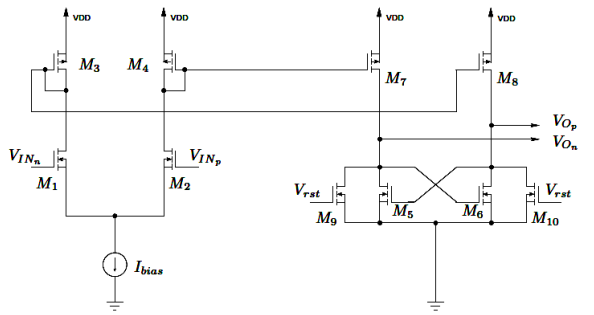

Figure 5. A principle schematic diagram of a simple static latched comparator.

The simple static implementation candidate shown on Figure 5 has some advantages and disadvantages as compared to dynamic comparator implementations. As the currents flowing through the latch transistors are well defined by the biasing current, the comparator's speed can be very easily controlled, however the connection between speed and static power consumption is very closely tight. As it is crucial to keep low power consumption in a column parallel ADC, this architecture does not allure a great interest due to its low efficiency. The architecture provides a somewhat more adequate kickback noise performance, in comparison with some dynamic implementations as we shall see further. The differential amplifier and the current mirroring transistors provide a very good isolation between the latch pair. These however may have a speed reduction effect due to the additional capacitive load overhead i.e. an additional pole added at the drains of the differential pair diode loads.

B Class AB comparator.

An architecture, very similar in a functional point of view to the first static candidate is shown on Figure 6.

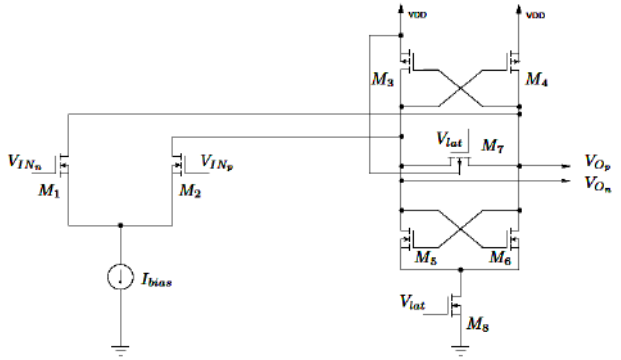

Figure 6. A semi-static often referred to as Class AB comparator.

In order to increase the comparator's speed the semi-static or often referred to as Class AB comparators, do not rely on keeping the latch in reset by holding the reset transistors on, as was the previous case with the static comparator in Figure 5. Instead to reduce the static current drawn by the latch a complementary latch pair is utilized (transistors *M*3, *M*4, *M*5 and *M*6) together with a switchoff transistor *M*8. Shortly, when *Vlat* is low, the only current path flows through the differential pair, transistor *M*7 is on, which keeps the upper latch (transistors *M*3 and *M*4) in reset. When *Vlat* is triggered high, *M*7 turns off, meaning that the upper latch's regeneration is triggered. At the very same moment *M*8 turns on and the bottom pair's drain currents start increasing depending on the upper latch's tilt. This implies that the output should be driven much faster, as there is no intentional current limitation. A major drawback of this architecture as also described by [5] appears to be the increased kickback noise at the inputs, since the differential pair's drains are capacitive coupled directly to the output nodes, which jump back and over from rail to rail. In addition, a hidden effect, decreasing comparator's accuracy, potentially introducing higher metastability issues is the reset transistor *M*7. When turned off, its residual channel charge will flow to both output branches, which may not be with equal impedance nor voltage level, therefore setting unequal starting conditions for the regeneration latch. This would imply that the Class AB stage would potentially have higher offset dependency, as if the regeneration latch transistors *M*5 and *M*6 are mismatched, the effect of charge injection from *M*7 will be amplified.

C A dynamic implementation

A major drawback in the static implementations described in the previous section is the poor power efficiency as well as relatively low speeds. A solution to the power efficiency problem appear to be the dynamic implementations. Figure 7. shows a dynamic comparator implementation using two inverter gates as a regeneration
latch.

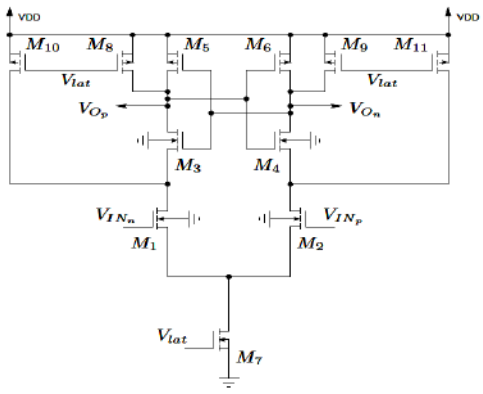

Figure 7. A dynamic comparator implementation.

It could be noted that transistor *M*7 when *Vlat* is kept low, completely turns off the whole circuit and only the leakage currents through *M*7 contribute to the

10.32377/cvrjst0604

total power consumption at this phase. Transistors *M*8, *M*9, *M*10 and *M*11 keep the inverters consisting of *M*3, *M*5, *M*4 and *M*6 reset and ensure equal starting conditions for both of them. When *Vlat* is triggered high, *M*7 starts conducting, the reset transistors *M*8, *M*9, *M*10 and *M*11 switch off and the regeneration process starts. When the inverters settle, there is no current flowing through the system, besides the DS leakage currents flowing though the inverters. The output voltage range of this dynamic implementation is however limited in the lower end by the DS drops over the differential pair transistors *M*1, *M*2 and the tail switch
*M*7, thus the architecture does not ensure full rail-rail output range. This implies that if full swing is required some level restoration circuits must be used, in its simplest example this could be an inverter stage. The kickback noise generated from this architecture seems to be comparable with the AB stage. The differential pair is closely coupled with the output nodes, only *M*3 and *M*4 provide insignificant insulation, as their *VD* is also expected to jump up-down. The dynamic implementation
besides the static offset from the differential pair, will also be susceptible to larger dynamic offset due to the charge injection (CI) and clock feed-through of the switches. The particular structure on Figure 7. would possibly have somewhat relaxed CI effect, as the reset transistors *M*8, *M*9, *M*10 and *M*11 would, to a large extent, cancel-out the charge influence on the inverters. *M*10 and *M*11 would inject charge on the source nodes of *M*3 and *M*4, while *M*8 and *M*9 would do on the drains of *M*5 and *M*6. This however is a very idealistic and difficult to define effect, as in reality there would be a clock skew and respectively turn-off time between all reset transistors, which makes the analysis difficult to follow.

D The Sub-AD comparator implementation

Due to its power efficiency the fore mentioned dynamic implementation was chosen as the basic building block of the Sub-AD module. In addition a voltage reference interpolation technique has been used to ensure higher reliability for the cost of a few additional elements and a small increase in power consumption.

As the dynamic implementation offers lowest power consumption and moderately high offset, which is acceptable, it appeared to be the most attractive architecture among the above-described. As an additional improvement possibility, implementing an interpolative Sub-AD was also possible with the chosen dynamic architecture, for the only cost of an additional latch stage as proposed by [23].

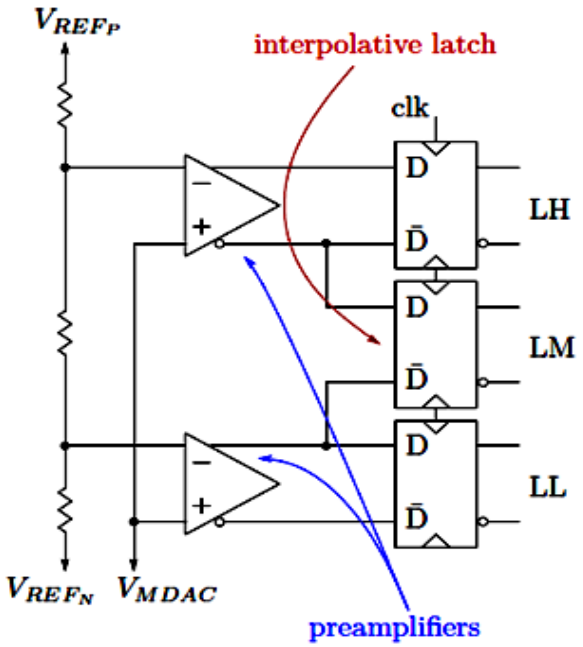

Figure 8. Sub Flash AD Comparator Interpolation Technique

To start with, the basic interpolation idea is clarified on Figure 8. The preamplifiers amplify the difference between the fed-in voltage from the MDAC and the generated sub-references, for further decision from the latches. We can clearly see that the two neighboring shoulders of the differential amplifiers could be used for generating an additional decision level for the cost of an extra latch. Figure 9. shows the outputs of two differential amplifiers hooked-up in a configuration as shown on Figure 8. with a swept input node close to the two reference voltage levels. Practically the interpolative latch, will be triggering on the mid-reference which should be equal to:

$$V_{REF_M ID} = \frac{V_{REF_H} + V_{REF_L}}{2}$$

The main drawbacks of this implementation stand behind the required balancing of the unequal loading of the differential pairs, as this may create a static design-inherited offset and also create a higher linearity requirement. The extra preamp loads also add additional poles and in general such interpolative structures are slower. In the case with the current application, requirements on the comparator's speed are somewhat relaxed and utilizing interpolation does not cause additional issues with respect to speed. The principle schematic on Figure 8. aims to present the interpolation technique in the voltage domain, this however in the case of the chosen fully dynamic comparator would be transferred into the current domain, as all the current flows through the differential pairs.

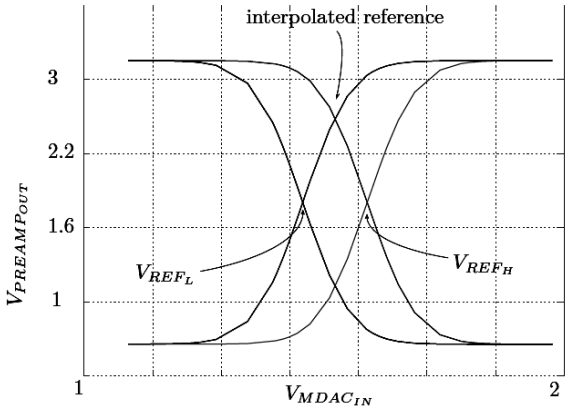

Figure 9. Mid-reference interpolation output voltages of two differential amplifier stages in a function of a linearly swept input voltage, hooked-up following the configuration on Figure 8.

To give a final summary of the designed dynamic comparator's performance for the Sub-AD module, Table 2. shows the main measured parameters. It should be noted that the comparator's design would most probably require modifications after parasitic extraction estimations and/or layout. A design of a comparator fulfilling the requirements in all corners, including parasitic sensitiveness prediction could be a very time-consuming task. As the scope of this thesis is to explore the proposed architecture and possibly improve it, full corner and parasitic optimizations are to be further explored.

TABLE II
SUMMARY OF THE MAIN MEASURED COMPARATOR PERFORMANCE PARAMETERS

Symbol	Parameter	Min	Typical	Max	Unit
ΔV_{os}	Input Offset Voltage Drift	-58	3	+61	mV
T_d	Response Time	-	118	-	ns
σ_n	Noise variance	-	0.48	-	mV
δ_{min}	Resolution	-	0.317	-	mV
V_{supp}	Supply Voltage	-	3.3	-	V
P_{dyn}	Dynamic Power	-	6	-	µW
P_{stat}	Static Power	-	0.224	-	µW

IV. SUB-AD CONTROL LOGIC

As the code provided by the comparators is thermometer-encoded and an RSD representation output is required, certain encoding logic had to be introduced. In addition the Sub-AD logic has the task to control the MDAC and determine the In-DAC switch states during the next feedback phase. In the previous subsection an interpolation technique for the comparators was introduced, thus effectively forming a 2 bit Sub-AD. As this extra half bit was introduced for reduction of an error probability, it is the Sub-AD logic that needs to convert the three thermometer encoded comparator levels to binary 1.5 bit RSD. Table 3. shows a truth-table of the implemented Sub-AD logic.

TABLE III
A TRUTH TABLE OF THE IMPLEMENTED SSB-AD LOGIC

vCODEIN<0:2>	BINOUT<0:1>	P_HP	P_HM	P_HN
000	00	1	1	0
001	01	1	0	1
011	01	1	0	1
111	10	0	1	1
100	00	1	1	0
010	01	1	0	1
110	10	0	1	1
101	00	1	1	0

As a reference, the hardware implementation of the encoding logic is shown on Figure 10.

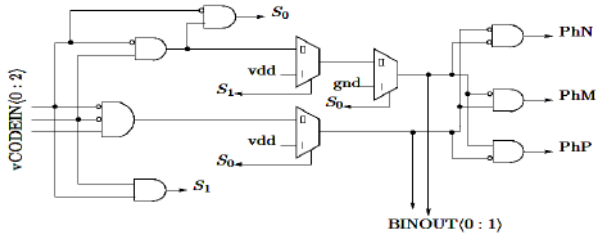

Figure 10: A principal logic diagram of the implemented Sub-AD encoding control logic.

V. RESULTS

In this section of the paper, The main ADC performance parameters concerning image sensors were introduced. In order to estimate the converter's performance from linearity point of view, transient noise simulations based on multiple samples per code were performed, following the IEEE 1241 standard [1]. Figure11. And figure 12. shows distribution histograms of the differential and integral non-linearity simulations.

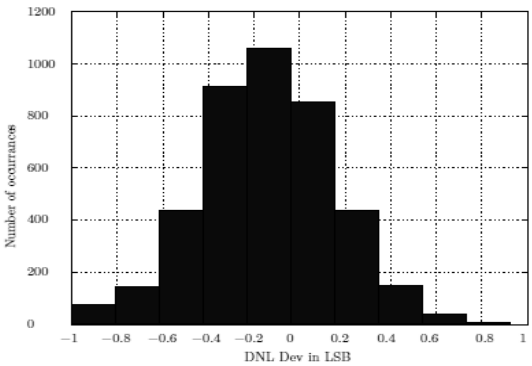

Figure 11. Differential Non-Linearity deviation distribution.

10.32377/cvrjst0604

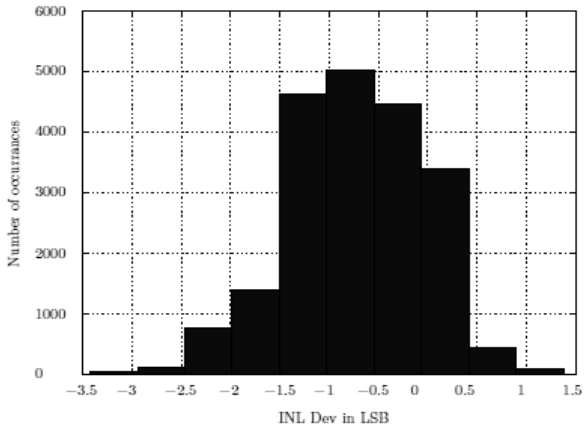

Figure 12. Integral Non-Linearity deviation distribution.

The random noise of an ADC is the excursive fluctuation of its converted digital code word, when an ideal noise-free signal is applied at its input. In the case with the current application, the random ADC noise would appear as a spatial image noise and is thus an important degradation index. The currently performed random noise tests were performed following the IEEE1241 Method 4.5.3.1 standard [1]. Practically following that standard the noise variance was estimated. Figure 13. shows a histogram of the acquired logic level differences from sample to sample. An evaluation script was developed using the IEEE1241 Method 4.5.3.1 and Method 4.5.3.2.

To provide an overview of the current state of the converter Table. 4 provides summarized results for the designed converter. These must be only taken as indicative results, as the current design state does not include device mismatch, external reference voltage and Sub-AD reference generation non-idealities.

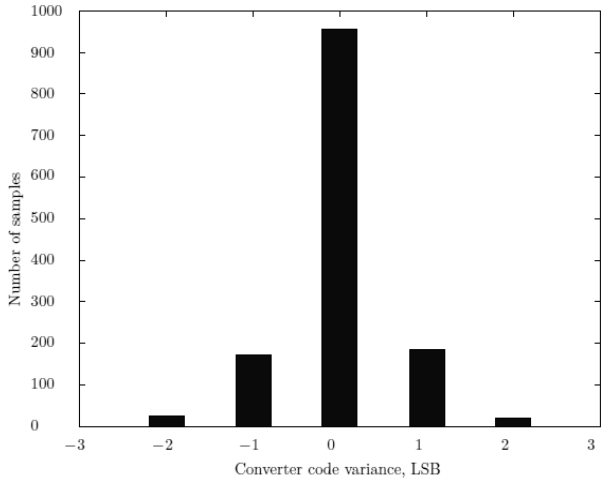

Figure 13: Simulated random noise variance, estimated by 1500 samples, worst case corner.

TABLE IV
SUMMARIZED PERFORMANCE RESULTS OF THE DESIGNED CONVERTER

Parameter	Value	Unit
Technology	180	nm
Resolution	12	bits
Sampling Rate	<150	Ksps
Input Voltage Range	1.35	V
Integral non- Linearity	+1.5/-3.5	LSB
Differential Non-Linearity	±0.8	LSB
Random Noise	367	µV
Power Supply	3.3	V
Power core	72	µW
Power cor+logic	193	µW
Energy per conversion Cycle	15.4	µJ
Reference Voltage H	2.35	V
Reference Voltage L	1.00	V

VI. CONCLUSION

For the Image sensors the single-ended MDAC architecture appeared to be of particular interest due to its design simplicity and was chosen as a re-exploration basis for the conducted design work.

An analysis on the architectural choice was performed and all basic ADC core component requirements were identified. A few MDAC OTA architectures have been listed and a choice, design and validation of a current mirror OTA with output cascodes had been conducted. The interpolative dynamic Sub-AD comparator module was developed, along with all digital control and feedback logic to the MDAC. Finally a few capacitor flipping mismatch reduction techniques had been proposed as possible ADC core improvement.

While all ADC sub-blocks have been implemented, wired-up and synchronized to achieve certain linearity and sampling speed performance measures. The Process corner simulations have been performed, however process variations and mismatch has not been taken into account.

The achieved results show that the major ADC speed limitation component is the MDAC's OTA. Following the converter's direct accuracy parameters as integral and differential linearity, the most critical influence components appear to be the MDAC's sampling and feedback capacitors. Capacitor mismatch reduction techniques appear to be of high relevance to the converter's linearity and further investigation on possible capacitor flipping techniques is left as a future task.

REFERENCES

[1] Ieee standard for terminology and test methods for analog-to-digital converters. IEEE Std 1241-2000, pages i–, 2001.

[2] W. S. Boyle and G. E. Smith. Charge coupled semiconductor devices, 1970.

[3] P.M. Figueiredo and J.C. Vital. Kickback noise reduction techniques for cmos latched comparators. Circuits and Systems II: Express Briefs, IEEE Transactions on, 53(7):541–545, 2006.

[4] Jin-Fu Lin, Soon-Jyh Chang, Chin-Fong Chiu, Hann-Huei Tsai, and Jiann- Jong Wang. Low-power and wide-bandwidth cyclic adc with capacitor and opamp reuse techniques for cmos image sensor application. Sensors Journal, IEEE, 9(12):2044–2054, 2009.

[5] Jong-Ho Park, S. Aoyama, T. Watanabe, K. Isobe, and S. Kawahito. A highspeed low-noise cmos image sensor with 13-b column-parallel single-ended cyclic adcs. Electron Devices, IEEE Transactions on, 56(11):2414 –2422, nov. 2009.

[6] Clemenz Lenard Portmann. Characterization and reduction of metastability errors in cmos interface circuits. Technical Report CSL-TR-95-671, ARPA, June 1995.

[7] Min-Woong Seo, Sung-Ho Suh, T. Iida, T. Takasawa, K. Isobe, T. Watanabe, S. Itoh, K. Yasutomi, and Shoji Kawahito. A low-noise high intrascene dynamic range cmos image sensor with a 13 to 19b variable-resolution columnparallel folding-integration/cyclic adc. Solid-State Circuits, IEEE Journal of, 47(1):272–283, 2012.

[8] F. Silveira, D. Flandre, and P. G A Jespers. A gm/id based methodology for the design of cmos analog circuits and its application to the synthesis of a silicon-on-insulator micropower ota. Solid-State Circuits, IEEE Journal of, 31(9):1314–1319, 1996.

[9] M.F. Snoeij, A.J.P. Theuwissen, K.A.A. Makinwa, and J.H. Huijsing. A cmos imager with column-level adc using dynamic column fixed-pattern noise reduction. Solid-State Circuits, IEEE Journal of, 41(12):3007 –3015, dec. 2006.

10.32377/cvrjst0604