Optimization and Effective analysis of Full Adder Circuit Design in 45nm Technology

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Abstract **— In this paper work, a new XOR logic gate and multiplexer logic has been proposed. Proposed design shows acceptable output logic levels with noise margin of 0.5V with 1.0V as input signals in 45nm technology. A full adder design for single bit has been implemented using proposed XOR gate, pass transistor logic multiplexer. The full adder designed with 12 transistors shows power dissipation of 7.74nW and maximum output delay 59.74nS. This circuit works with well reduced supply and simulations have been carried out for 0.8V, 1.0V & 1.2V supply voltage in the step of 0.2V. Simulations are performed by using CADENCE based on gpdk45 library CMOS technology. Simulation result provides the advantage of the newly designed adder circuit against the conventional adder circuits. Consumption of power for proposed full adder has been compared with earlier reported full adder circuits, this proposed design circuit gives better performance in terms of power consumption, speed and transistor count.**

Keywords **-- Exclusive-OR (XOR), CMOS, full adder design, low power and pass transistor, multiplexer.**

I. Introduction

Research efforts are bringing changes in the field of low power VLSI (very large-scale integration) systems, in today's world portable electronic devices like laptops, audio/video based multimedia and cellular communication devices increase as growth of technology. Nowadays, research efforts are optimizing the transistors density on chip, power dissipation of VLSI systems is also increasing further to influence reliability and run time failure problems. Packaging and cooling mechanism become costly and more complex due to the increasing consumption of power. Lowest power dissipation is one of the most important design criteria for integrated circuit (IC) design engineers at all levels of designing, along with delay and area considerations. The functionality of system will be considered at lowest supply voltage and logic swing. With this, There are three major source of power consumption which exist in CMOS VLSI circuits. They are (i) Power due to capacitor charging and discharging at a node is switching power, (ii) Power due to current flow of supply to ground with simultaneous functioning of PMOS and NMOS is short circuit power, (iii) Power due to leakage currents of device is static power consumption. In general VLSI design circuit power dissipation can be reduced by scaling supply voltage and capacitance further. As the supply voltage is reduced further, problems of poor noise margin, small voltage logic swings, and leakage current arise.

The fundamental most frequently used arithmetic operation in microprocessors, DSP processors, application specific integrated circuits (ASIC) and application specific integrated processor (ASIP) etc, is addition of two binary numbers. A single bit binary adder circuit is significantly basic building block in these VLSI circuits, which must be efficient.

Implementation of the full adder will affect the performance of entire VLSI system design. Recently different types of adder circuits have been designed using various logic function styles in previous literature. Standard CMOS logic has 28 transistor adder circuit using pull-up and pull-down networks which are having NMOS and PMOS transistors that are equal in number[1]. Transmission gate cmos adder (TGA) is based on transmission gate logic with 20 transistors [3]. The main disadvantage of TGA is that double number of transistors required compared to the pass transistor logic to implement same logic function. A transmission gate logic full adder (TFA) is based on transmission logic theory and uses 16 transistors [4]. A hybrid cmos logic style adder circuit with 22 transistors is reported [8]. A full adder using 22 transistors based on hybrid pass transistor logic (HPSC) is presented. Full adder for embedded and signal processing applications using 3-input XOR logic gate is reported [10]. A 16T full adder cell with XOR & XNOR logic using pass transistor and transmission gate logic is reported [11]. Logic function of a full adder is based on the following two equations with A, B, C_{in} which are the three 1-bit inputs and generate two outputs of 1-bit they are Sum and C_{out} as given below

$$Sum = (A \oplus B) \oplus C_{in}$$

$$C_{out} = A.B + C_{in}(A \oplus B)$$

Structural design approach of XOR gate for implementation of single bit full adder [12] is as shown in Fig.1.

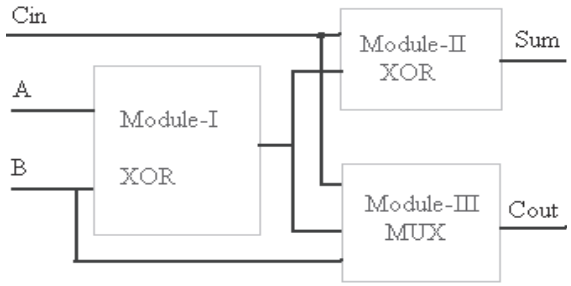

Fig.1: Structure of One Bit Full Adder Design

More number of full adder circuits have been implemented with XOR logic gates and performance of these XOR logic gate also affects the adder circuit including the performance. The XOR logic is the main

basic building block of full adder circuit. The XOR logic can be designed and implemented using AND, OR, & NOT basic logic circuits but shows in high redundancy. Optimized design of these basic building blocks of gate will definitely improve the performance of VLSI systems, as these basic gates are used as sub block in arithmetic circuits. XOR, AND, OR & NOT designs with reduced number of transistors having satisfactory performance levels are extremely useful for efficient implementation of the circuit designs such as adders, multipliers etc. 4T pass transistor logic based XOR gates with some limitation of driving capability are reported in [6]. Different types of designs for XOR/XNOR gates using 4T also presented [4]. Three inputs XOR logic gate design in place of two inputs XOR logic are reported in [13]. The XOR/XNOR design with 10 transistors based transmission logic gate is reported in [8]. The XOR/XNOR circuit with dual feedback is also reported in [9]. The logic circuit schematic level, an optimized and efficient circuit design is necessary where number of transistors can be reduced, with less power consumption and acceptable output voltage level swings. Here, in this paper a new XOR logic gate with three transistors has been proposed. A new single bit full adder with 12 transistors based on proposed XOR gate and pass transistor logic multiplexer has been presented.

II. Proposed Logic Circuits

A) XOR Logic

Proposed XOR logic circuit design with 3T has been shown in Fig. 2. Proposed XOR logic, the channel length of all three transistors has been taken as 0.45µm. Width of NMOS transistor (N1) has been taken as 0.50µm, Width of PMOS transistors (P1 & P2) has been taken as 0.50µm. In this proposed circuit when inputs *A*=*B*=0, the output is low because P1&P2 transistor are ON and N1 transistor is OFF, then low level logic is passed to the output. The input combinations *A*=0 and *B*=1, circuit shows high output as transistors P2&N1 is ON while transistor P1 is OFF. In another case when inputs *A*=1 and *B*=0, transistor P1 is ON and transistors P2&N1 are OFF, then the output node is at high logic. When the inputs are A=1 and B=1 transistor N1 is turns ON and transistors P1&P2 are OFF, then gives as the low logic level at output node but the resistance of transistor (N1) made high by reducing of its width, for acceptable output logic or voltage swing for input combinations (W/L) ratios have been modified. Widths of P1&P2 transistors has been made large to decrease the resistance and width of N1 transistor has been made to reduced for slow discharging.

Degradation of the voltage due to threshold drop can be modified by changing W/L ratio as high of transistor N1. The equation relates the gate channel length and width of MOS transistor with threshold voltage of the transistor.

$$V_T = V_{TO} + \gamma\left(\sqrt{V_{SB} + \phi_0}\right) - \alpha_1 \frac{t_{ox}}{L}\left(V_{SB} + \phi_0\right) - \alpha_v \frac{t_{ox}}{L} V_{ds} + \alpha_w \frac{t_{ox}}{W}\left(V_{SB} + \phi_0\right)$$

Where: V_{t0} -zero bias threshold voltage,
γ – Bulk threshold coefficient,
ϕ_0-- $2\phi_F$ and $\phi_F$is Fermi potential,
t_{ox} -Thickness of oxide,
α_l , α_v, & α_w – process dependent parameters
from the above equation, it is understand that by increasing the width(W) it is possible to reduce the voltage degradation. In the last combination A=B=1, the output node show low logic level as transistor N1 is ON, so that proposed circuit works as XOR gate as shown in Fig.2. Design of proposed 3T XOR logic gate operation has been obtained. Width of P3&N2 transistors has been taken as 240nm and 120nm respectively.

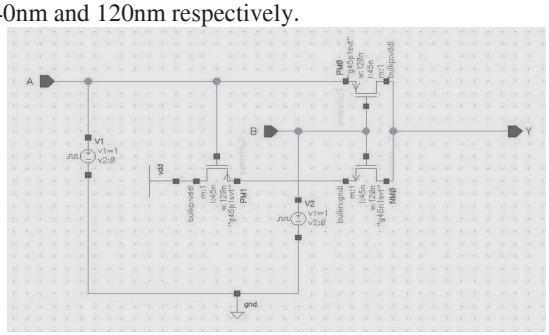

Fig.2. Schematic Circuit For XOR Logic With 3 Transistor

Here proposed logic function simulation results are obtained using spectre simulator in cadence tool at 45 nm technology. The transient analysis of 2-input XOR logic gate with inputs A, B and the output Y as shown in fig.3. The output of 3T XOR logic simulated using ADE-L at 45nm technology under the transient analysis of the period of 100nS and supply of 0.8V to 1.2V by steps of 0.2V.

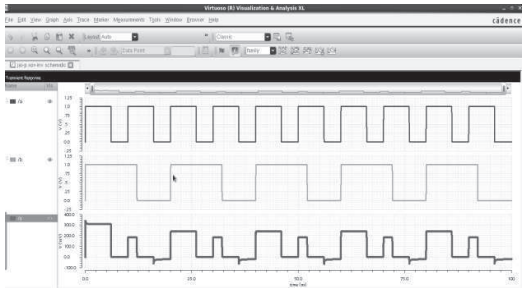

Fig.3. Simulated Output of XOR Logic With 3T

B. Two Input Multiplexer

Proposed logic function for 2-inputs mux design with two transistors is shown in Fig.4. In a multiplexer, channel lengths of two transistors have been taken as 0.45nm. Width (*W*n) of NMOS transistor (N1) has been taken 120nm. In proposed circuit when *S=0* output is selected as A because PMOS transistor is ON and input A is passed to output. When the selection input *S=1* circuit gives the output as B because NMOS transistor is ON and input B is passed to output. While output logic for certain input combinations the transistor W/L ratios have been modified to be acceptable level.

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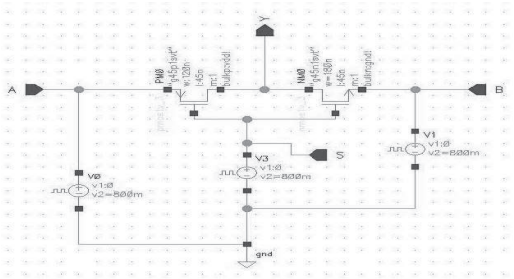

Fig.4. Schematic Circuit For 2-Input Multiplexer Logic With 2 Transistor

Here proposed logic function simulation results obtained using ADE-L spectre simulator in cadence tool at 45nm technology. The data analysis of the input and output such as A, B, S & Y shown in Fig.5. The output of 2T 2-input multiplexer logic is simulated at 45nm technology, under the transient analysis for the period of 100nS and power supply of 08V to 1.2V by steps of 0.2V.

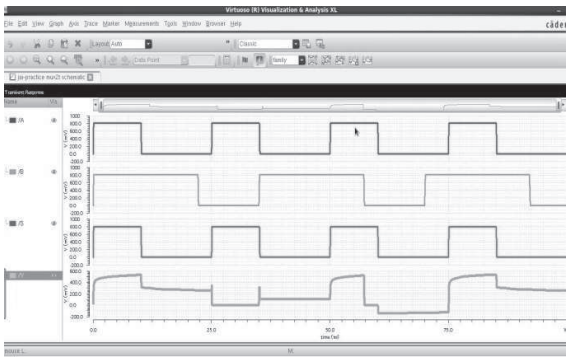

Fig.5. Simulated Output of 2-Input Multiplexer Logic With 2T

III. Implementation of Full Adder

Design of proposed single bit full adder circuit can be implemented by distinct combinations of XOR logic gates and multiplexer blocks. This proposed structure approach as shown in block diagram of Fig.1, we have used two XOR cells and three multiplexers to design the full adder as shown in Fig.6. Sum is generated by two XOR gates and C_{out} is generated by three multiplexer as given in Boolean equations. Based on 2T multiplexer with pass transistor logic to be used to generate C_{out} which is reduces the total number of transistor count of full adder to 12. Since the pass transistor logic is gives poor noise margin, in this current design XOR logic for sum is already generated for single bit full adder using proposed XOR cell and multiplexer cell using 12 transistors has been implemented as shown in Fig.2 and Fig.4. The multiplexer section value of width for NMOS and PMOS transistors have been taken as 100nm & 250nm respectively. Simulations is also carried out with varying different supply voltages from 0.8V to 1.2V by steps of 0.2V.

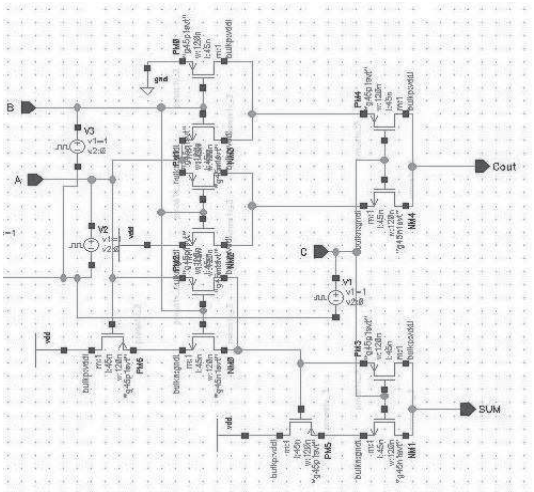

Fig.6. Schematic circuit for proposed full adder Logic with 12 Transistor

Here proposed logic simulation results obtained using spectre simulator in cadence ADE-L tool at 45nm technology as shown in Fig.7. The analysis of input-output such as A, B, C_{in} and S, C_{out} with this the output of 12T full adder logic is simulated at 45nm technology under the process of transient analysis for the period of 100nS and power supply of 0.8V to 1.2V by steps of 0.2V.

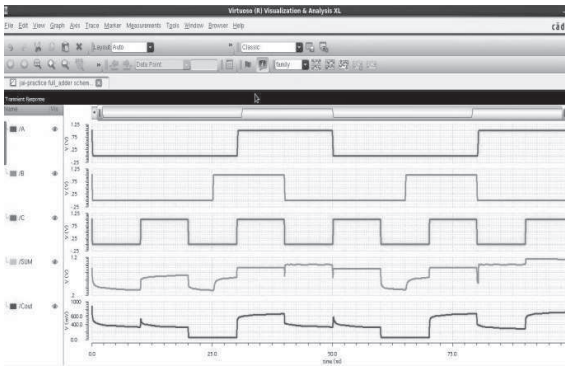

Fig.7. Simulated output of proposed full adder logic with 12T

IV. Simulation Results

Results are performed by SPECTRE in Virtuoso platform for Simulation, Cadence at 45nm CMOS process with the 0.8V and 1V and 1.2Vsupply voltage. After verifying the functionality, various performance parameters those are Power, Delay and Power Delay Product (PDP) of the proposed design are summarized in the Table.1 for different voltages at a fixed input rise and fall time.

TABLE.1

SIMULATED RESULTS AT 0.8V SUPPLY

Parameter	Supply - 0.8V	
	Conventional CMOS FA	Proposed FA
Dynamic Power(µW)	1.81	0.0437
Static Power(µW)	0.57	0.0235
Total Power(µW)	2.38	0.0672
Delay(nS)	59.75	40.31
PDP	108.14	1.761

TABLE.2
SIMULATED RESULTS AT 1V SUPPLY

Parameter	Supply - 1V	
	Conventional CMOS FA	Proposed FA
Dynamic Power(µW)	4.36	0.0232
Static Power(µW)	1.23	0.0542
Total Power(µW)	5.59	0.0774
Delay(nS)	59.75	40.29
PDP	260.51	0.934

TABLE.3
SIMULATED RESULTS AT 1.2V SUPPLY

Parameter	Supply-1.2V	
	Conventional CMOS FA	Proposed FA
Dynamic Power(µW)	3.74	0.0537
Static Power(µW)	8.51	0.0322
Total Power(µW)	12.25	0.0859
Delay(nS)	59.75	40.29
PDP	223.46	2.163

The 12T proposed full adder and Conventional CMOS full adder has been simulated at 45nm technology for calculation of different parameters at different supply voltages.

V. COMPARISION

Comparison between conventional CMOS and proposed CMOS full adder is shown in Tables. It represents that low power and high speed CMOS full adder is achieved best performance and shows less leakage and active power along with total power. The resulted less delay which enhances the speed of operation and gives less PDP (Power Delay Product). Full adder with 20fF capacitive load performance is given in tables, shows the best performance effect of various loads on power, delay and PDP at 0.8V, 1V and 1.2V as shown in below Fig.8 and Fig.9.

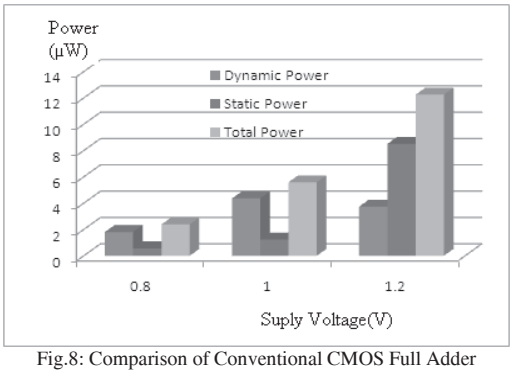

Fig.8: Comparison of Conventional CMOS Full Adder

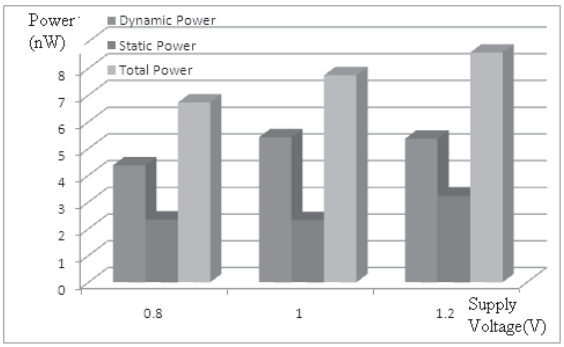

Fig.9: Comparison of Proposed Full Adder

VI. CONCLUSION

Design and simulation of optimized low power, delay and area of a single bit full adder design analysis is done under 45nm Technology. Various parameters at different scenario is calculated and compared with conventional full adder too. The simulation results signify that the parameters of full adder circuit is optimized, delay is reduced to 40.29ns and power dissipation is reduced to 7.74nW and leakage current is reduced to 2.32nA for 1.0V at 45nm Technology. Comparison and analysis show that the implementation of the single bit full adder circuit will be better for 1.0V than 1.2V supply voltage.

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