SoC Based SIFT Algorithm for Identification of the Quality Objects for Palletization Application

D.Renuka[1] and Dr B.K.Madhavi[2]
[1]SWEC/ ECE Department, Hyderabad, India
Email:renuka.do11@gmail.com
[2]SWEC/ ECE Department, Hyderabad, India
Email:bkmadhavi2009@gmail.com

Abstract: **In some of the manufacturing industries automation problems occur most commonly like quality control and palletization. This paper proposes a system level design for the identification of quality objects for palletization process to solve the automation problems. The quality of the object is identified by using SIFT (Scale Invariant Feature Transform) algorithm which is one of the image processing algorithms most popularly used for local feature detection. By using SIFT algorithm featurepoint extractions are performed for an input image. After featurepoint extraction, feature matching is performed by comparing the extracted featurepoints of the input image and original image featurepoints which are stored in database. The output comes after the feature matching will actuate the palletization process to differentiate the type of objects. The processing of an image using SIFT algorithm for palletization process is designed in MATLAB by using Xilinx System Generator and simulations are performed. Then the HDL code is generated for the whole design by using system generator. The generated HDL code is synthesized by Design vision compiler in Synopsys tool. To integrate the whole system design into SoC (System on Chip) using 90nm technology physical design is performed in Cadence Encounter tool. Due to this design the whole system obtains optimized area and power.**

Index Terms- **Palletization, SIFT, Featurepoints, Gaussian pyramid, DoG, Extrema detection, Xilinx System Generator.**

I. Introduction

In present days due to the advancements in digital technology, manufacturing industries are using the fully automation machines. In industries during the manufacturing of the products some of the automation problems will occur such as quality control and palletization process. These are the most recurring process in manufacturing industries [1]. Quality control is used to check the quality of the products after the completion of product manufacturing to differentiate the good products from the defective products. Palletization process is a process of stacking the products on a pallet which will come from production line in industries for distribution or storage purpose. Different type of palletizers are used in industries. They are mechanical palletizer and robotic palletizer. Mechanical palletizers are fast, inflexible and have larger product changeover downtime. Robotic palletizers are slower but flexible and have shorter product changeover downtime [2-3]. The quality control of the object is performed by using image processing algorithms in vision system which is most commonly used in robotic application for the object recognition. Traditionally some of the image processing algorithms like edge based, adaptive thresholding [4, 5] are used for object recognition but for complex objects these algorithms are difficult for object recognition. To solve this problem SIFT algorithm is used to detect the local feature points of an image, because SIFT can be able to detect the features even in invariant size, rotation, view and illumination [6]. Image processing algorithm can be implemented in Field Programmable Gate Array (FPGA) due to the recent developments in the FPGA hardware architecture. FPGAs have great processing speed and flexibility to process the image processing algorithms in real-time applications [1].SIFT algorithm performs high computations to detect the feature points of the image. So the SIFT is suitable to implement in FPGA because of its pipelined structure of architecture [7, 8]. But due to the increasing of low power and area consumption requirements in the present days of markets (VLSI systems) System on Chip (SoC) design is used instead of FPGAs, because of the advantage of low power consumption and reduced area for the typical design. SoC is an Integrated Circuit (IC) which will integrates the whole system design into a single chip.

In this paper, a system level design is implemented for the identification of object using SIFT algorithm. It will actuate the control flow of a palletization process and the proposed system is integrated into SoC to obtain optimized area and power.

This paper is organized as section II gives the brief description of SIFT algorithm. The block diagram and logical design for the proposed system is explained in section III. The implementation of the proposed system in SoC is described in section IV. In section V and VI results and conclusion are given.

II. Sift Algorithm

SIFT algorithm proposed by David Lowe [7] is an image processing algorithm which is used to detect the local feature descriptors of the faces or any object. SIFT is used in many robotic applications for object recognition and tracking the objects in computer vision system. SIFT has a great ability to detect the feature points of an object even in invariant conditions also such as different in size, rotation, intensity and view. SIFT algorithm is divided into three steps to detect the feature points of an image. They are Gaussian pyramid, Difference of Gaussian (DoG) pyramid and Extrema detection [9] as shown in Fig. 1.

doi:10.32377/cvrjst1111

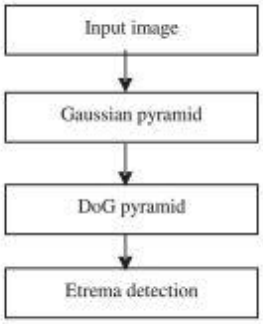

Figure. 1 Steps of SIFT algorithm

A. Gaussian pyramid:

The input image I(x, y) is multiplied with Gaussian kernel G(x, y, σ) by using Gaussian filter. It will generate the Gaussian image L(x, y, σ) [10] and is shown in (1)

(1)

(2)

By changing the value blur point of the image will be changed. A Gaussian pyramid consists of multiple octaves with multiple scales. Scale is nothing but a number of Gaussian blur images. One octave consists of stack of Gaussian blur images [9].

B. DoG (Difference of Gaussian):

Difference of Gaussian is constructed by subtracting two Gaussian images as shown in (3). An example is shown in Fig. 2 DoG constructed from Gaussian pyramid with four scales and one octave.

(3)

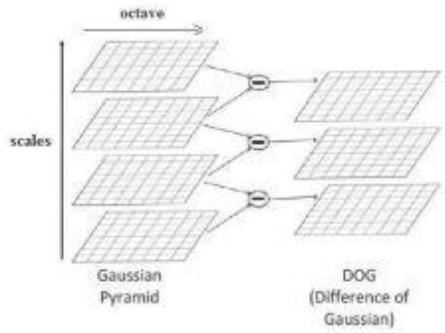

Figure. 2 Gaussian pyramid and DoG with 5 scales and 3 octaves

C. Extrema detection:

After the construction of DoG, local maxima and minima points are constructed by selecting a sample point from one DoG image and compared that point value with its neighbouring point and adjacent DoG image points value either maximum or minimum as shown in Fig. 3. Then from these maxima and minima points a stable point is taken as keypoint or featurepoint of an image by adding threshold value [10].

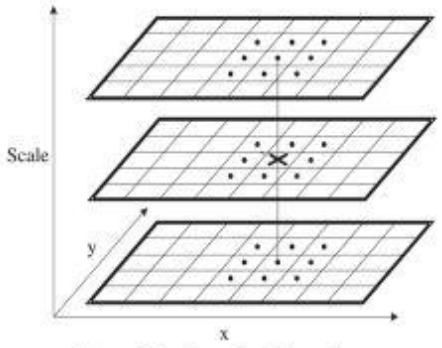

Figure. 3 Maxima and minima points

III. Logical Design For The Proposed System

Block diagram of the system is shown in Fig. 4 for the processing of the image by using SIFT algorithm to detect the feature points. It will actuate the control flow of a palletization process. The processing of the image by using SIFT algorithm is clearly explained in section II, and gives the output as feature points will separate the type of objects and detect the defective object for physical actuation of a palletization process.

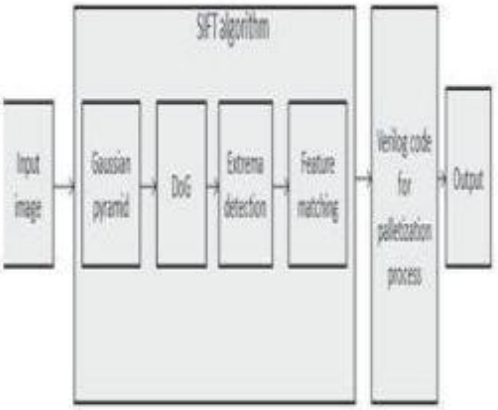

Figure. 4 Block diagram of the proposed system

For this block diagram, control flow chart is shown in Fig.5. In this design, three input images are taken as A, B and B defective. First the input image is preprocessed by converting into 300x300 pixels of grayscale image [11]. Then the image is processed by using SIFT algorithm to extract feature points of the image.

doi:10.32377/cvrjst1111

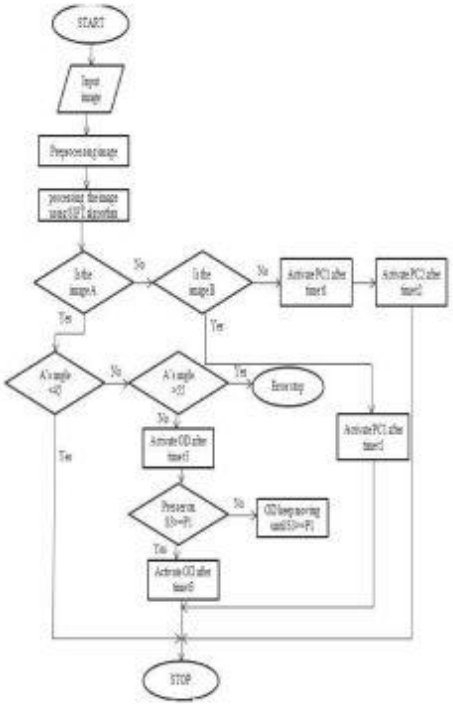

Figure. 5 Control flow chart of the proposed system

If the image comes after the processing using SIFT algorithm is type A with angle less than 45^0, then the process is stopped. If angle of image A is greater than 55^0 then the Orientation device (OD) will be activated which is a mechanical palletizer [1] used to set the inclination of the image until the pressure S1 is greater than or equal to P1. After that OD will be deactivated. If output comes from SIFT algorithm as image B, then the PC1 (pneumatic cylinder) will be activated .If output image is B defective, PC1 and PC2 will be activated.

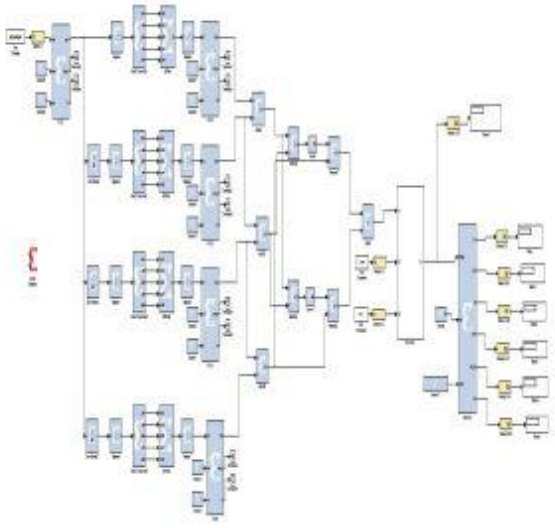

Figure 6: Whole system diagram in MATLAB using Xilinx System Generator

The whole control flow of the proposed system is designed first in MATLAB using Xilinx System Generator as shown in Fig. 6 and HDL code (Verilog code) is generated.

By using the Xilinx system generator blocks the control flow chart is designed in MATLAB for identification of quality of the objects for the palletization process. First the preprocessed image is stored in FIFO block to construct Gaussian blur image [11]. In this, we have constructed Gaussian pyramid with four scales is nothing but four Gaussian blur images and one octave. From the four Gaussian blur images three DoG images are constructed by using Addsub block to subtract the two successive Gaussian blur images. Then the maxima and minima points are constructed by comparing the three DoG images using Relational block and from the maxima and minima points featurepoints are extracted by using Logic OR block. Feature matching is performed by comparing the extracted feature points with the original featurepoints which are stored in From workspace block of SIMULINK block which is used to store the values of an image from MATLAB workspace. The output which comes after the feature matching is given as input to Black Box block (it is used to interface the HDL code and Xilinx system generator blocks).In this Black box Verilog code is given which is written manually for the control flow of a palletization process and simulation is performed for the system model. A System generator token is added to the whole system model which will serve as a control panel for controlling panel and simulation parameter. Then the HDL code is generated by the System generator token according to its specifications [12].

IV. Implementation Of The Proposed System In Soc

The generated Verilog code from the MATLAB is compiled in Xilinx to generate the RTL schematic as shown in Fig. 7

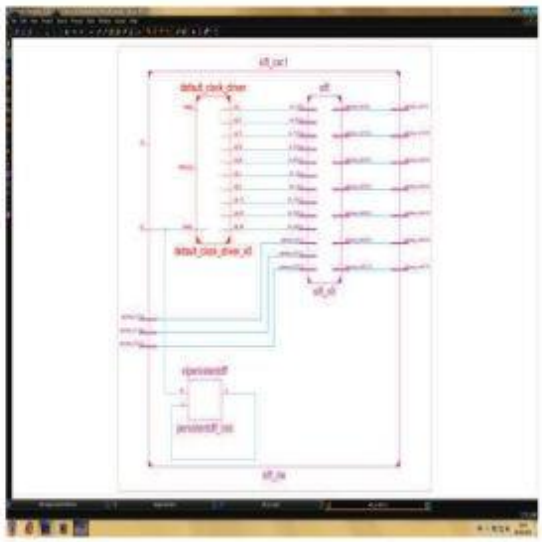

Figure. 7 RTL schematic

doi:10.32377/cvrjst1111

Then the Verilog code is synthesized by using Design vision compiler in Synopsys tool to generate RTL Netlist and to perform the area analysis, timing analysis and power analysis which is shown in section V. To integrate the whole system into SoC using 90nm technology, physical design is performed in Cadence Encounter tool. After the physical design, chip layout design and GDS (Graphical Data System) file will be generated. GDS file is used in chip fabrication for Real-Time application.

V. RESULTS

A. Simulation results in MATLAB:

The featurepoint extraction of input object A, B and defective B are shown in Fig. 8, 9 and 10 respectively performed by using SIFT algorithm in MATLAB using Xilinx system generator blocks.

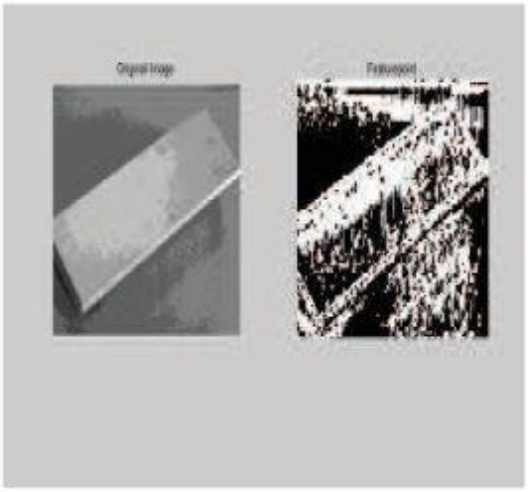

Figure. 8 Featurepoint extraction of image A

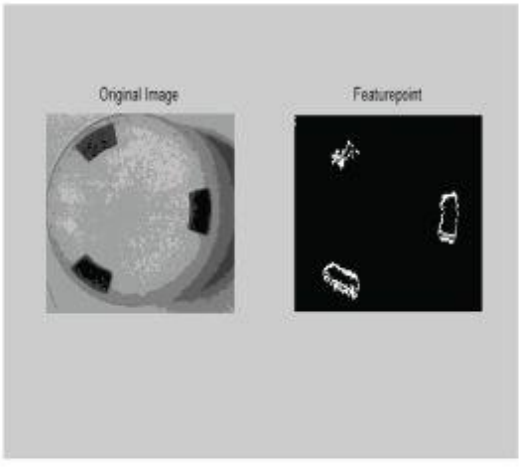

Figure. 9 Featurepoint Extraction of image B

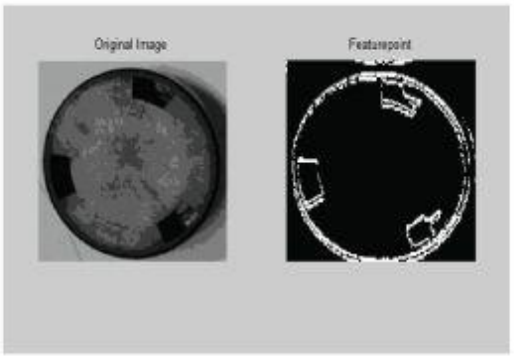

Figure. 10 Featurepoint extraction of image B defective

B. Simulation results in Xilinx:

After the whole system is designed in MATLAB, Verilog code is generated. Then the generated Verilog code is compiled and simulation results are observed in Xilinx software. For input image A with angle 50^0, the output obtained is OD=1 and stop=1 is shown in Fig. 11. For input image B, the output obtained is PC1=1 and stop=1 is shown in Fig. 12. For input image B defective, the output obtained is PC1=1, PC2=1 and stop=1 is shown in Fig. 13.

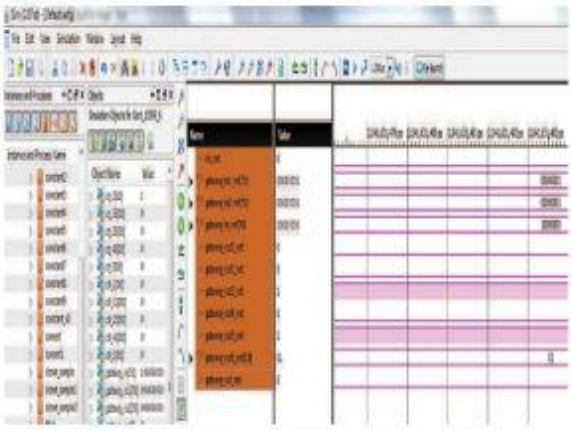

Figure. 11 Simulation result for image A with angle 50^0

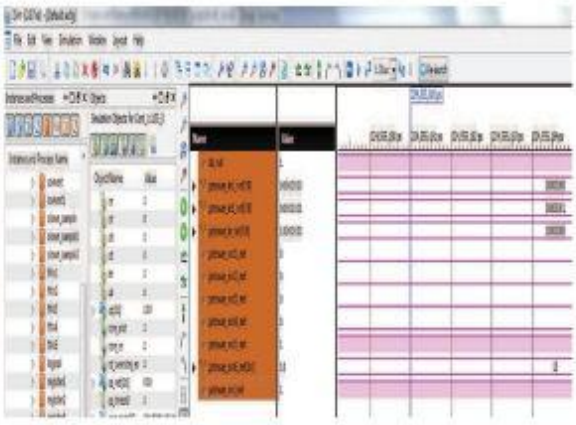

Figure. 12 Simulation result for image B

doi:10.32377/cvrjst1111

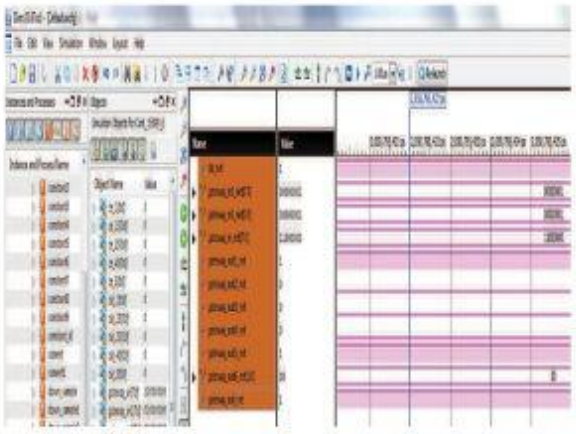

Figure. 13 Simulation result for image B defective

C. Synthesis results:

After the simulation of proposed system in Xilinx, Verilog code is synthesized in design vision compiler by using Synopsys tool to generate RTL Netlist. Area, power and timing analysis are performed. RTL Netlist generation is shown in Fig. 14 for the proposed system

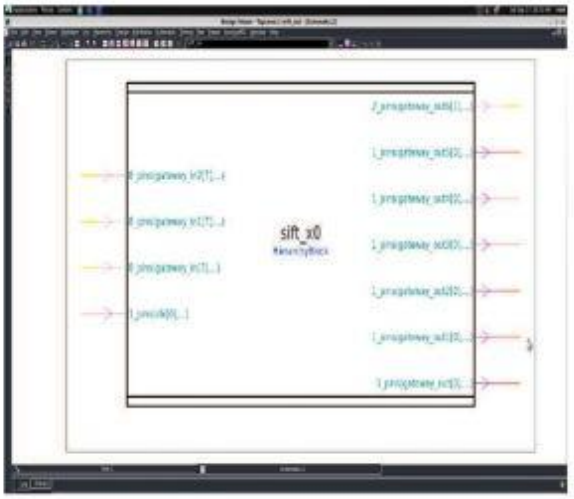

Figure. 14 RTL Netlist

Table I shows the area, timing and power report of the total system.

TABLE I.
AREA, TIMING AND POWER REPORT OF THE CHIP

Parameter	Chip Results
Area	34727 m^2
Timing	8ps(clock period)
Power	12mw

D. Physical design results:

To integrate the whole system design into SoC physical design is performed to generate chip layout. In Fig. 15 shows the generated chip layout for the whole system.

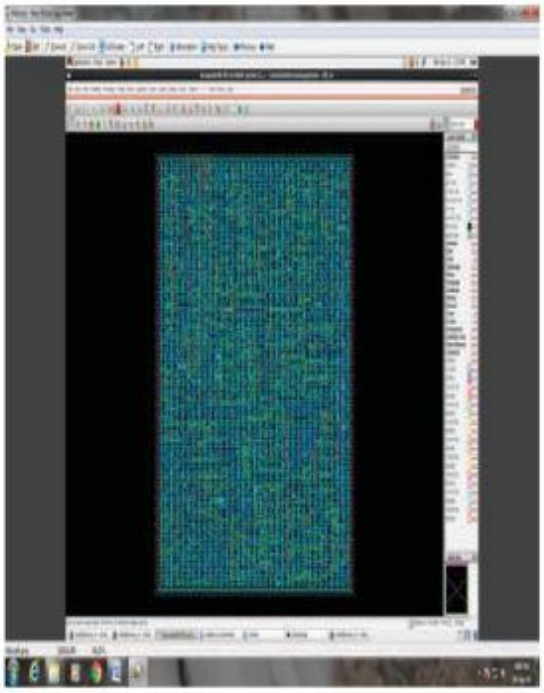

Figure. 15 Chip layout for the whole system design

VI. CONCLUSIONS

In this paper, the proposed system is designed in MATLAB using Xilinx System Generator for identification of quality of the objects for palletization process. Featurepoint extractions of the images are performed by taking 300x300 pixel size of input image and simulation results are performed in Xilinx. Then the whole system design is synthesized by Design vision compiler in Synopsys tool and RTL Netlist is generated. Physical design is performed for the proposed system to integrate into SoC in 90nm technology by using Cadence Encounter tool. Due to this proposed system the optimized area of 34727µm² and power of 12mw are obtained.

REFERENCES

[1] MS Salman, AA Ata, AM Ashir "FPGA Based Image Processing System for Quality Control and Palletization Applications", IEEE International conference on Autonomous Robot Systems and Competitions(ICARSC) May 14-15, Espinho, Portugal.

[2] P. Dzitac and A. M Mazid, "An Efficient Control Configuration Development for Systems," IEEE Conference on Robotics, Automation and Mechatronics, 2008, pp.140-145.

[3] Pavel Dzitac and Abdul Md Mazid "Improved Control Strategy for a Robotic Palletizer," Appiled Mechanics and Materials Vols. 278-280 (2013) pp.599-606.

doi:10.32377/cvrjst1111

[4] A. Sultana and M. Meenakshi, "Design and Development of FPGA based Adaptive Thresholder for Image Processing Applications", 2011 IEEE Relevant Advances in Intelligence 2011, pp.633-637.

[5] Z. Guo, W. Xu and Z. Chai, "Image Edge Detection Based on FPGA", IEEE Ninth International Symposium on Distributed Computing and Applications to Bussiness, Engineering and Science, Feb.10,2010,vol.5,pp.169-171.

[6] David G. Lowe, "Distinctive Image Features from Scale-invariant Keypoints", International Journal of Computer Vision, 60(2), 91-110(2004).

[7] Z.Wang, H. Xiao, W.He and F. Hen, "Real-time SIFT based Object Reorganization System", Proceedings of 2013 IEEE International Conference on Mechatronics and Automation, August 4-7, 2013, vol 5, 1361-1366.

[8] Gi-woong Shin, Jong-tae Sung, Young-Hyoung kim and Yong-hwan Lee, "Hardware Design of Feature Point Extraction using SIFT Algorithm", Advanced Science Technology Letters vol.48 (CIA 2014) ,pp 42-46.

[9] Hazma Bin Ijaz "A Hardware Architecture for Scale-space Extrema Detection", Master's Thesis at KTH School of ICT and Robert Bosch GmbH.

[10] Lindeberg T., "Feature Detection Automatic Scale Selection", International Journal of Computer Vision, 30, 79-116(1998).

[11] Tom Ganley "FPGA Co-Simulation of Gaussian Filter Algorithm", Michigan State University ECE 480 November 19, 2010.

[12] User guide "System Generator for DSP", UG640 (v11.4) December 2, 2009.

doi:10.32377/cvrjst1111