SoC Based Sigma Delta ADC Using ANFIS Algorithm for ECG Signal Processing Systems

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Abstract: **This paper presents a design of low power sigma delta ADC by using ANFIS algorithm which is applicable for high resolution ECG signal processing systems. The ECG signal analysis which is also known as a comprehensive analysis of the Heart, which helps for collecting the information of abnormal and normal conditions of the heart. The resolution of the ECG signal helps in the diagnosis of heart abnormalities. With the proposed design, the resolution of the ECG signal is improved and reduced power consumption levels of ADC. The ANFIS algorithm is used to decide the sampling clocks of ADC which changes the power consumption levels in the ECG system. The main advantage of this ANFIS algorithm is to take instantaneous decisions. This ANFIS system can also be called as an intelligent system which makes use of neural networks. The ECG signal data is used as an input data for implementing the whole system SoC (System-on-chip) design using 90nm technology. The SoC includes the integration of 14 bit sigma delta ADC, ANFIS system, multiplexer, down sampling and up sampling circuits. The algorithm is designed in MATLAB and the whole system is modelled using VERILOG language. The simulation results were shown in Xilinx system generator, the synthesis is performed in Synopsys Design vision. The physical design of the chip is carried out in Cadence Encounter tool. The complete system can operate at 400 MHZ frequency and the power consumption of the system can be given as 15mw. This high resolution low power system level design is used for health care monitoring applications.**

***Index Terms*--- ADC, ANFIS algorithm, SOC domain, ECG signal processing, power consumption.**

I. Introduction

The Electrocardiograph is a machine that performs electrocardiography and results in electrocardiogram. The electrocardiogram is a painless test, which records the electrical activity of the heart. For every heart beat an electrical signal is generated from the top of the heart to the bottom. These electrical signals were set to rhythm of heart beat.

The hierarchy level design of the ECG signal processing system consists of an Analog- to- Digital converter and digital signal processing system. A dynamic system clock source is given to both ADC and the DSP system. The primary components of DSP signal processing system includes instrumentation amplifiers and operational amplifiers. The ECG signal processing system with sigma-delta ADC is shown in the Fig 1.

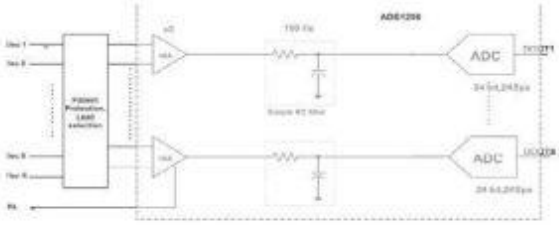

Figure. 1 Example of an ECG signals processing system with sigma delta ADC.

Delta sigma converter is a type of oversampling and noise shaping analog-to-digital converter. The main purpose of the ADC is to convert the analog ECG signal data into digital ECG data.

The pattern of an ECG signal with PQRST format can be given as shown in the below Fig 2.

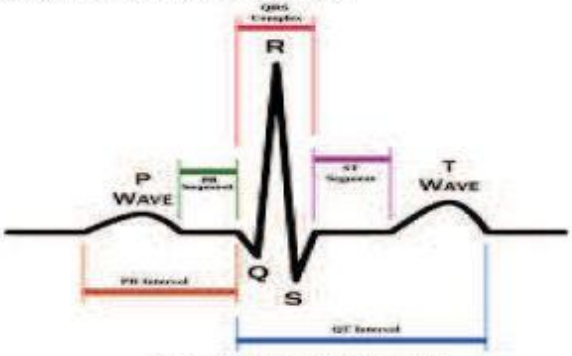

Figure. 2 Example of an ECG pattern.

The ECG data base can be obtained from the web based source called physionet[17] which is a free access source of signals.

This paper is organized as: Section II shows the brief explanation about analog –to-digital converter. Section III explains about the Adaptive Neuro Fuzzy Inference system algorithm and its architecture. Section IV gives the block diagram for experimental environment. Section V includes the methodology applied in the project and finally section VI includes the simulation results and chip layout for the proposed work.

II. Analog –To-Digital Converters

The **analog-to-digital converter** is a system that converts an analog signal into a digital signal. A digital-to-analog converter (DAC) performs the reverse operation.

The ADC can also be defined as the on-chip interface between digital domain and the real domain of analog signals.

The general process of converting an analog signal into digital signal consists of two steps .They are: 1) sampling 2) quantization. Consider the analog signal x (t) when performing the sampling process the analog signal is converted into sampled signal and then the sampled signal is quantized and finally the signal is converted into digital.

Different types of analog –to-digital converters are flash ADC, successive approximation ADC, pipe line ADC, and time interleaved ADC. The highest resolution ADC is Sigma –delta ADC [2] which is a cost efficient low power converter. The basic building blocks of ADC are comparators, amplifiers and integrators. The brief explanation about sigma –delta ADC can be given below:

A. Sigma-Delta Analog-To-Digital Converter

The sigma delta Analog to digital converter [2] is a 1-bit sampling system. This type of ADC can also be called as an oversampling ADC. Delta-sigma ADCs implement oversampling, decimation filtering, and quantization noise shaping to achieve high resolution and excellent anti aliasing filtering.

The block diagram of the ADC is as shown in Fig 3. The components of the ADC are summing amplifier, integrator, quantize (comparator), DAC, digital filter.

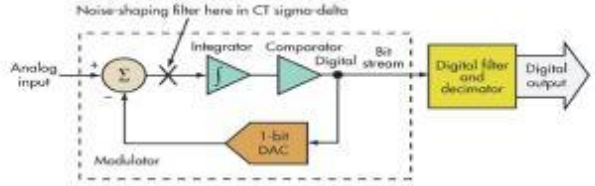

Figure. 3 Sigma-Delta Analog To Digital Converter.

The input analog signal and the output signal of 1-bit DAC are applied to the summing amplifier and the output analog signal is given to the integrator. In integrator, the noise shaping of the obtained signal is performed and the resultant signal is allowed to pass through the quantizer. The quantizer results only two levels for the obtained signal. The amplitude of the quantized signal can be "1" or "0". Hence the analog signal is finally converted into 1-bit digital signal and then again the feedback is given to the summing amplifier.

Finally, the obtained 1-bit digital stream of data is given to the digital low pass filter which results in the N-bit digital signal for the given input analog signal.

This is the working principle of sigma delta ADC which has a very important role in the functioning of an ECG signal processing system.

III. ANFIS Algorithm

The Adaptive Neuro Fuzzy Inference System is a type of network which is a combination of artificial neural network and fuzzy logic control [5],[13]. This network can also be called as hybrid intelligent network. The integration of both neural network and fuzzy control has a potential to capture the benefits of both, in a single frame. These networks may be linear or non linear, predictable or unpredictable. The neural network has the ability to recognize the patterns and adapt them with changing environment.

The important steps for developing a neuro fuzzy system are:

1) Fuzzification of the input parameters.
2) Computation of degree for linguistic terms.
3) Conjunction of fuzzy inferred parameters.
4) Defuzzification of the output.

The adaptive fuzzy inference system architecture[4],[6] with two inputs such as X, Y and the corresponding output F is given in Fig4.

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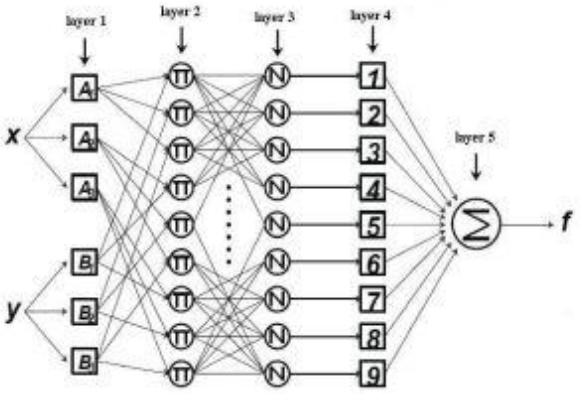

Figure. 4 ANFIS structure for two-input one output.

A two-input, one-output zero order ANFIS [4] with three Membership functions per input (nine fuzzy if-then rules) is shown in Fig. 4. It is composed of five layers. The square nodes in the first and fourth layer represent adaptive nodes, e.g. they depend on a set of parameters; the circle nodes are fixed.

The operations performed in each layer are shown below:
Layer 1: Every node in This, is adaptive with a node function. Each input node has linguistic variables which can be called as membership functions.

$$\mu_A(x_1) = \frac{1}{1 + \left| \frac{x_1 - c_i}{a_i} \right|^{2b}}$$

where x is the input node and a and c are the parameters of the membership function.

Layer 2: Firing Strength of Rule

- Use T-norm (min, product, fuzzy AND, ...)

$$O_{2,i} = w_i = \mu_{A_i}(x_1)\mu_{B_i}(x_2)$$

(for i=1,2)

Node output: *firing strength of rule*

Layer 2: each node in this layer calculates the firing strength of a rule .The output obtained from this layer is the strength obtained by performing rule matrix operations.

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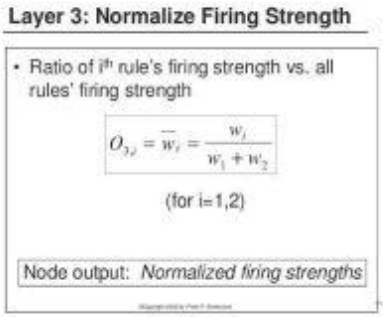
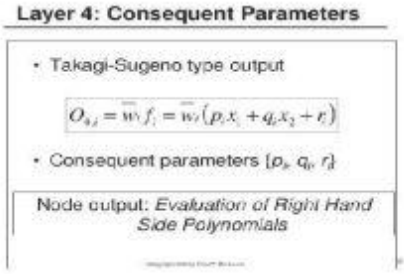
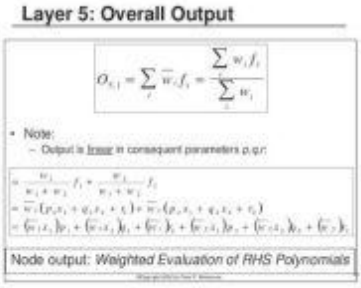


Layer 3: Every node in this layer calculates the ratio of rule firing strength to the sum of all the firing strengths of the rules. The outputs of this layer are the normalized firing strengths.



Layer 4: every node in this layer is multiplied with a node function, with a consequent parameter set.



Layer 5: This layer consists of only one node which calculates the final output of the Neuro fuzzy system.

Hence this is the working principle of adaptive neuro fuzzy inference system.

Some of the important considerations for determining the rules are as follows: For example, if '*g*' is Very Low and '*f*' is Very Low then the sampling clock is selected as HCLK or if '*g*' is Very High and '*f*' is Very High then the sampling clock is HCLK. The sampling clock of the ADC is selected as MCLK For example, if *g* is Medium and *f* is Medium then the sampling clock is MCLK. For example, if *g* is Low and *f* is Low then the sampling clock is LCLK. Table **I** tabulated the fuzzy adjustment rule table for the frequency of the sampling clock of the ADC. It maps the two input fuzzy sets to an output fuzzy set.

TABLE I
FUZZY ADJUSTMENT RULES FOR THE FREQUENCY OF THE SAMPLING CLOCK

f \ g	Verylow	low	medium	high	Very high
Verylow	HCLK	LCLK	LCLK	LCLK	HCLK
low	HCLK	LCLK	LCLK	LCLK	HCLK
medium	HCLK	MCLK	MCLK	MCLK	HCLK
high	HCLK	HCLK	HCLK	HCLK	HCLK
veryhigh	HCLK	HCLK	HCLK	HCLK	HCLK

The terms such as verylow, low, medium, high, veryhigh are called as linguistic variables for input parameters.

HCLK, MCLK, LCLK are the linguistic variables for the output of the ANFIS system. An example for different clocks is as shown in the Fig 5.

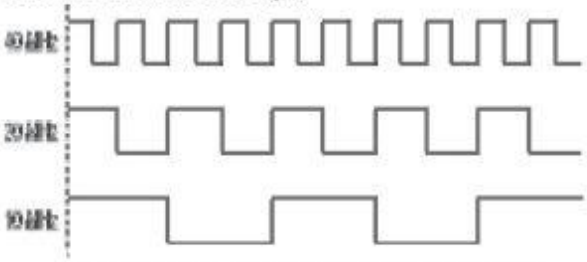


Figure. 5 Example showing the three different types of clocks

In this paper, an ECG signal data is taken as input data to implement the ANFIS algorithm[8]. The membership functions are developed to perform fuzzy rules to produce the best logic control for the proposed system. Consider 'f' & 'g' are the parameters of the ECG signal in which 'f' is the amplitude of the signal and parameter 'g' is the slope value of the input ECG signal. The expressions for the parameters can be given as:

F(n)=abs(p(n)) (1)

G(n)=abs(p(n)-p(n-1)) (2)

Where p(n) is the amplitude of the ECG signal.

The main concept of the proposed system is to select the base sampling rate in the normal regions and oversampling rate in abnormal regions of the body signals. The sampling rate is controlled by the fuzzy logic control technique. By this technique the quality of the waves can be efficiently improved.

IV. BLOCK DIAGRAM FOR EXPERIMENTAL ENVIRONMENT

The proposed ECG signal processing system in Fig.6 includes a sigma-delta ADC, ANFIS system, two down sampling circuits, interpolation filter, phase locked loop(PLL), Multiplexer. The details of each component in the system are described below:

1) Sigma –delta analog to digital converter: the ADC[3] can be realized by making use of various architectures depending upon the characteristics of the signals. The

proposed 14 bit sigma delta ADC [3] was implemented by using sigma adder, delta adder, digital-to-analog converter. It is used for converting the analog ECG signal into digital stream. This design is used for the proposed ECG signal proposed system because of its various characteristics such as various sampling rates can be used and it is a high resolution ADC.

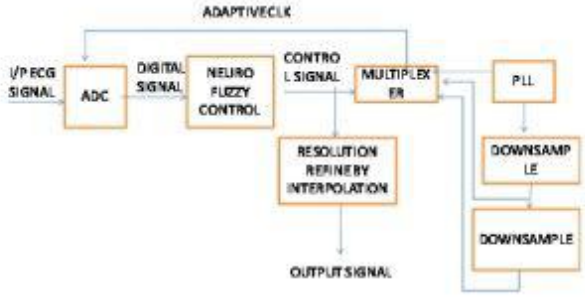


Figure. 6 Block diagram of the proposed system.

2) Adaptive Neuro Fuzzy Inference system: The adaptive neuro fuzzy controller[8] was implemented by making use of adders, multipliers, dividing blocks. It is used for deciding the sampling clock of ADC from the given different clocks. It performs the comparison for the body values from the ECG signal. Next, it obtains the variance between various amplitudes of the ECG signal and results in the two parameters such as 'f' & 'g' with this comparison. The final step is to decide the sampling clock for the proposed ADC. The sampling clock can be HCLK, LCLK, MCLK according to the given input pattern.

3) Down sampling circuits: The down sampling circuit consists of anti-aliasing filter and a decimation filter. In these circuits, first the HCLK signal which is generated from the PLL is allowed for filtering, by anti-aliasing filter and then it is sub sampled by a decimation factor. Then the HCLK signal is sampled to MCLK and then the MCLK is sampled to LCLK. By the design technique, three various frequencies of clock can be produced by using two down sampling circuits.

4) Multiplexer: The Multiplexer is a device that selects one of the inputs from the various inputs given depending upon the selection line. The control signal for the multiplexer can be given from the adaptive neuro fuzzy inference system and the inputs for the multiplexer are HCLK, MCLK, LCLK signals which are obtained from the clock generator and down sampling circuits. The output of the multiplexer is given as a sampling clock of ADC[2] which varies the power consumption levels of the device.

5) Interpolation filter: Interpolation[14] is a process of converting the sampled signal into highest sampling rate by adding the samples in particular intervals of time by using various design techniques. Here, the input for the interpolation filter is the control signal obtained from the adaptive neuro fuzzy inference system. By performing interpolation the signal can be converted into highest sampling rate signal by which the resolution of the converted ECG signal can be increased which is used for diagnosis of heart beat signals.

V. Methodology For The Proposed Design

The working flow of the proposed system in detail can be explained from the flow chart which is shown below in Fig.7

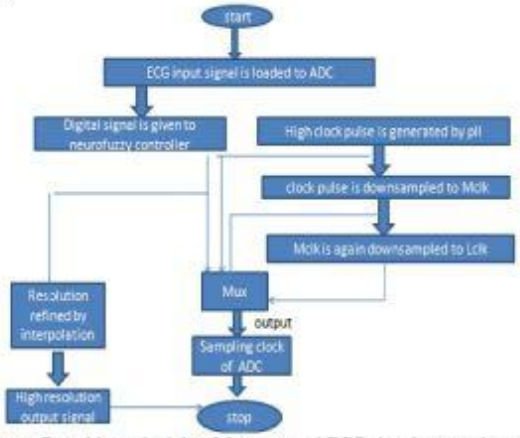


Figure. 7 working principle of the proposed ECG signal processing system

The chip includes the integration of Sigma-Delta ADC, ANFIS system, multiplexer, down sampling circuits, pulse generator, up sampling circuit, decimation filter and interpolation filter. The input ECG signal[8] is taken from physionet [5] which can be in the format of MIT-BIH Arrhythmia data in which each signal has 360 samples per second. The frequency of the general ECG signal is 360 Hz. This taken signal consists of each sample of length of 14-bits and is loaded in the MATLAB. From the workspace of MATLAB the ECG signal is given to the sigma delta ADC for converting the analog ECG signal to the digital signal.

The digital signal data is given as input for neuro fuzzy system such as ANFIS(adaptive neuro fuzzy inference system). Here, the obtained input from the ADC is allowed to obtain the membership functions required for performing the fuzzy rule matrix operations. The outputs obtained from the rule matrix are normalized and the normalized outputs were allowed for defuzzification. The final result obtained from the defuzzification layer of the system is the final output of the ANFIS system .The output of the ANFIS system can be HCLK or MCLK or LCLK which can be decided by the given digital input signal. This output signal is given as a selection line for the multiplexer.

The multiplexer is a 4X1 MUX which consists of four inputs and two selection lines and single output. The ANFIS system output is taken as a selection line for the multiplexer. The inputs for the multiplexer can be given from the down sampling circuits. HCLK can be given from clock generator, MCLK, LCLK signals which are derived from the down sampling circuits are given as inputs for the multiplexer. By performing the operation of multiplexer we can get a decision control signal depending on these clock signals .The output obtained from the multiplexer can be given as a sampling clock of sigma-delta ADC.

Depending on the sampling clock given to the ADC, the power consumed can be changed at different clock periods. The output obtained from the multiplexer can be allowed to undergo upsampling so that by adding the samples to the control signal the resolution can be improved and by

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performing the interpolation, finally resolution refined signal is obtained from the whole system.

Firstly, the proposed design is implemented by using the co simulation of MATLAB, Xilinx system generator[16]. The verilog code has been manually written for the ANFIS algorithm and it is interfaced with the other blocks such as downsampling circuits present in the system generator tool. Finally after interconnecting the ADC with ANFIS system the logical simulation is performed in MATLAB. By using the hardware description language verilog the design is simulated in Xilinx system generator and Design Vision compiler which belongs to SYNOPSYS tool was used for the synthesis of the design in VLSI circuit using 90nm technology. The placement and routing of the chip is performed in Cadence Encounter and a chip layout is generated for the proposed design. The photo of chip layout is illustrated in Fig 13.

Synthesis results show the area of the proposed signal processing system is 121613µm². Which was synthesized in 90nm technology The power consumption for the whole design can be obtained from the design vision. It consumes 15mW at 300 MHz operating frequency with 1.62V supply voltage .The specifications are listed in table III.

TABLE II
OUTPUT SAMPLING CLOCKS OF ADC AND POWER CONSUMPTION LEVELS

SAMPLING CLOCK	FREQUENCY	POWER
HCLK	400MHZ	5.4W
MCLK	285MHZ	3.08W
LCLK	222MHZ	1.4W

VI. SIMULATION RESULTS OF THE COMPLETE SYSTEM

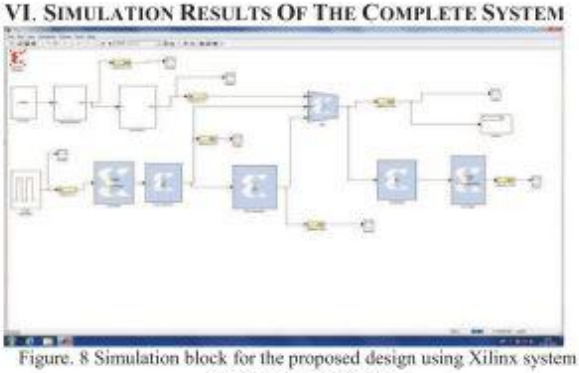

Figure. 8 Simulation block for the proposed design using Xilinx system generator & MATLAB

The input given to the system is an ECG signal data. The ECG signal data loaded in to the MATLAB can be shown in the below Fig 9.

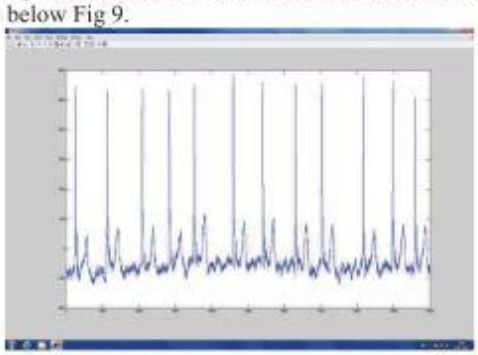

Figure. 9 Input ECG signal used for the simulation of the proposed system

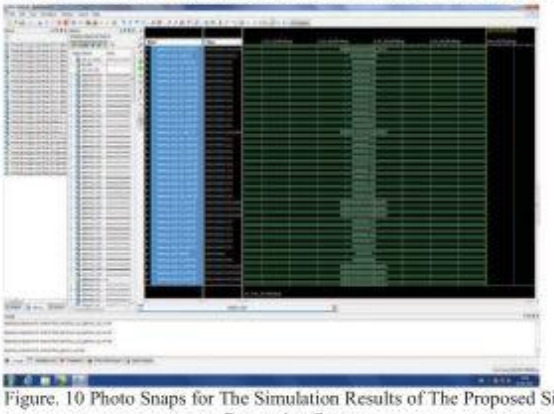

Figure. 10 Photo Snaps for The Simulation Results of The Proposed Signal Processing System

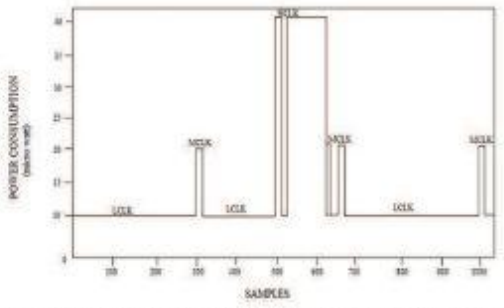

Figure. 11 Clock information and distribution of power consumption

VII. SYNTHESIS RESULTS

The synthesis of the proposed design is performed using Design Vision Compiler of Synopsys tool. The RTL netlist of the design is as shown in the Fig. 12.

Figure. 12 RTL Netlist for The Proposed Design

The specifications of the proposed design includes area, power, resolution, frequency, process are shown in the table listed below:

TABLE III
CHIP RESULTS OF THE PROPOSED SYSTEM LEVEL DESIGN

Specification	Chip Results
Process	UMC 90nm
Core Area	121613µm²
Power	15mw
Supply Voltage	1.62v
Operating Frequency	300mhz
Resolution	16 Bit

The chip layout for the proposed design is as shown in the Fig 13. This process is performed in Cadence Encounter tool.

By performing this physical design we can obtain the netlist, DEF(Design Exchange File) & GDS –II(Graphical Data System) file. With these files we can go for further steps such as fabrication of the chip for the proposed design. This can be used for real time applications.

VIII. Chip Layout For The Complete Design

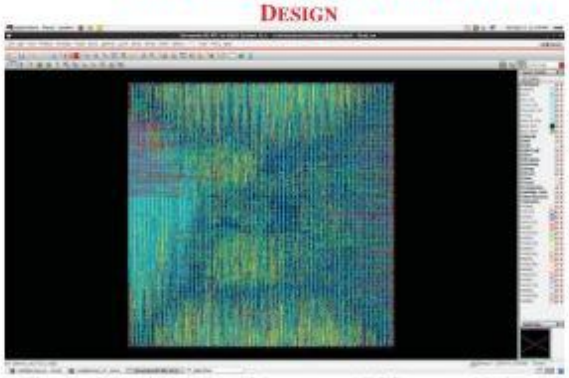

Figure. 13 Physical design of the proposed ECG system chip layout in Cadence Encounter

IX. Conclusions

In this project the system level design of the low power ECG signal processing system which includes the integration of sigma-delta ADC, ANFIS system, multiplexer, up sampling and down sampling circuits is implemented. The sampling clock of sigma delta ADC is selected by using the decision technique which is done by using intelligent algorithm called ANFIS algorithm which can also be called as an intelligent system. The design is modeled by taking the ECG signal features as the input parameters. As the ANFIS approach provides a general frame work for combination of NN and fuzzy logic, the efficiency of ANFIS for deciding the sampling clock of ADC can be concluded by observing the power consumption levels of ADC at different clock periods. The SoC implementation of the proposed design reduces the area, power consumed by the circuit. The results show that this work can not only improve the quality of the ECG signals but also improves the power consumption of the devices. The obtained chip area is about 121613μm^2 and the power consumed by the device is 15mW.the resolution of the ECG signal is increased by 0.14%. This is applicable for real time health care monitoring applications.

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