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Design of Inexact Speculative Adder for High Performance Applications

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Abstract: **The low power and less area are equally vital in the implementation of high speed adders. The response time as the key point is also considered and focused for the optimization and considered for real-time interfaces. The general block schematic of the ISA consists of a carry speculation (SPEC) block, an addition block (ADD) and an error compensation (COMP) block. The Inexact Speculative Adder (ISA) design therefore, improves speed, reduces power consumption, propagation delay and accuracy management due to a short speculative path and to an error compensation technique. This technique allows to precisely controlling errors. The simulation and synthesis is carried out using CADENCE tools in 90nm CMOS technology. The power consumption and area occupied by the design is presented.**

Index Terms: **Compensator, Adder, Carry propagation, Speculator, ISA, CMOS Technology, delay, short speculative path and compensates erroneous sum.**

I. Introduction

The optimized adders are mostly required for many digital processing applications [2]. In many computers and other kinds of processors adders are used in the ALU. These adders are the most commonly used blocks in multipliers, dividers and subtracters. Addition is one of the fundamental arithmetic operations. Adders decide the efficiency of the digital system. The optimized adder always gives accurate work

. The CLA adders basically operate by generating two signals (Propagate and generate signals) for each and every position of the binary digit. The basic principle of operation is based on whether the carry bit is propagated from an LSB or absent in the binary digit position. In many situations the propagate binary digit is sum output of half adder circuit and generate binary digit is the carry output of the half adder. The carry for each and every bit position are invoked after the propagate bit and generate bits are created. By combining multiple CLA adders, even larger adders can be created.

Applications are aimed on providing sensing and actuating operation where the primary component is the response time which needs optimization for real time application. Hence the design of this High speed adder which is very important mainly when it comes to speed play. The inexact speculative adder designed using CLA adder. The ISA adder circuit design is a new approach with improved speed, power and area in the deep sub micron, scaled technology version. This approach is applicable for error- tolerant applications to get statistical results.

In this paper, the idea of Inexact Speculative Adder with highly optimized hardware efficiency and precision techniques of compensation using error correction or error reduction technique is presented. A greater control over accuracy can be obtained and improved by the Inexact Speculative adder which employs a specific topology.

results. The area, power and propagation delay are important measuring factors of the adder. The powerful and highly optimized adders are required for the implementation of present multipliers and other digital systems.

There are various kinds of adders. The binary adders are half adder, full adder, ripple- carry adder, carry- save adder, carry-look ahead adder etc. Among these adders, ripple-carry adder, carry-save adder, Carry skip adder [3], Carry Look Ahead (CLA) adder supports multiple bits.

The block based addition may be designed using carry skip and carry select adders also. But, in these adders area is the penalty. In an adder circuit which focuses on carry save, it is more beneficial not to propagate the carry bit, in case the adder circuit needs to compute the sum of the numbers which contains three bits or more bits. Hence this adder provides a reduction in the number of bits. A better solution to this problem is to employ three bit adders at the input, which generates sum and carry as the output without waiting for the subsequent carry bit propagation. The sum and carry bits can be applied to the two inputs of the three bit carry save adder. Once the adding of the bits is complete for all the stages we may use CLA adder to super impose the final result of sum and carry bits.

To reduce the computation time and area, CLA adders were designed, implemented and are used for ISA in this

II. System Overview

In this section, the overview of the ISA is presented. The Inexact and approximate circuit design [1] is a better approach for enhancing the performance and saving in energy in low power VLSI design systems. The conventional topology of speculative adders improves performance and enables precise accuracy control.

As wireless devices become ubiquitous, the primary concern of digital systems is power efficiency. Grievously, obtaining low-power and Process-Voltage-Temperature robustness needs elaborate and contradictory design restrictions and reliability. Particularly, IC's are make-up to incessantly guarantee meticulous operation. In order to circumvent error results, they accomplish the majority of calculations earlier than the worst case acceptable delay or with a greater precision essential for typical operations. This culminate failing to make the best utilization of resources and leads to "over-engineered circuits.

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- Inexact and approximate circuit design is a very good approach to transfer this counterproductive quest for process of improving substantial rate in power and speed. The preliminary objection is to determine where and how to forbid an error or an approximation take place in the circuits without conciliate the functionality. With increscent quantity of data being processed, a broad range of applications could tolerate in erroneousness. Consider an example, in multimedia processing inadequate percentage of faults is not appreciable to humanoids, and in highly precision data processing algorithms such as data mining, recognition.

A new approach to design inexact circuits is to use speculation in order to improve power and speed such circuits can be used to implement energy efficient and high-performance DSPs and hardware accelerators. It also lowers integration cost along with higher speed or duty cycling.

A new speculative adder is proposed in this paper called ISA. This ISA gives advantages of energy efficient, error management and improves performance through an optimized speculative path. It also comprises the versatile dual-direction error compensation technique.

Speculative adders use the truth that a normal carry propagation adder will not reach the entire length of the adder, thereby making it more convenient to have an estimation of the in-between carry bit using a fixed number of antecedent stages. In this way the carry propagate chain can be divided into two or more short distance paths in the path of the adder there by providing more relaxation in the entire design process and reducing the undesirable glitching power and improving the Energy-Delay-Area Product beyond the normal bounds of the traditional adders.

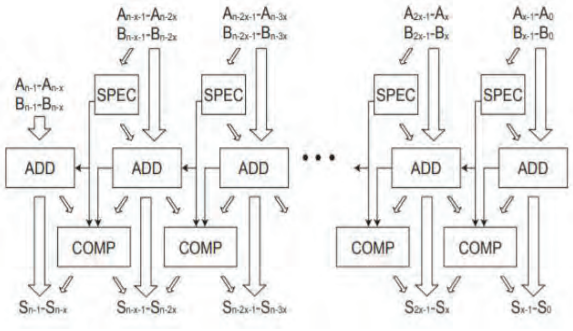

Figure 1. General block diagram of the Inexact Speculative Adder

Many speculative adders have been suggested in literature in order to lower error frequency or magnitude .The ETE2 adder consists of sub-adder blocks along with input carries speculated from carry-look-ahead blocks with same length. To increase accuracy many of the most significant carry-look-ahead adder blocks are chained in the ETA2M version. To lower the relative errors the ETA2B adder adds variable speculation signs and sub adder sum balancing multiplexer (MUX) blocks. N. Zhu et al. and Y. Kim et al. have proposed adders with improved accuracy by taking it into account two prior speculation blocks instead of one along with carry select or carry skip technique.

The existing speculative adders can be improved, in which the circuit hardware is not utilized efficiently. The overhead due to carry speculation is large and entirely lies in the critical path. The sum balancing blocks consist of parallel multiplexers also contribute to the critical path, have large fan-outs. This ISA architecture that I have proposed greatly improves hardware efficiency to lower the control errors.

III. Proposed VLSI Architecture of ISA

In this section, the block diagram of proposed VLSI architecture for ISA and modified internal blocks are discussed. The block diagram of n bit ISA is shown in the figure 2.

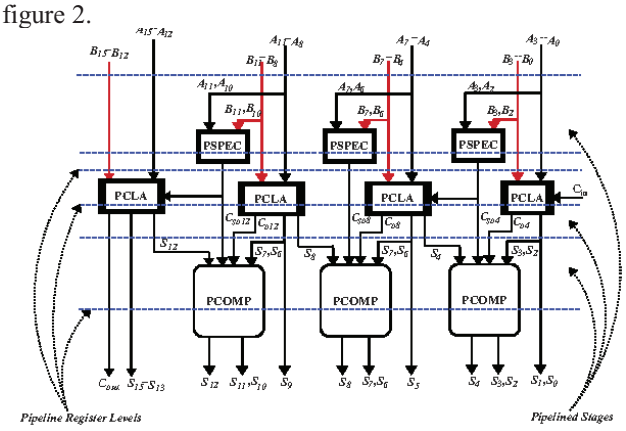

Figure 2. 4-bit VLSI architecture of ISA

The proposed architecture comprises of pipelining SPEC, pipelining CLA and pipelining COMP blocks. From the n number of inputs, 4 inputs are applied to each PCLA and PSPEC blocks simultaneously [6]. Here, the PCLA is used to enhance the speed of the operation. The analysis of an individual blocks are presented in the further sub sections.

A. Speculator and Adder Block:

The inputs for the addition, the operands are represented as A = {$A0$, $A1$, ...$An-1$} and B = {$B0$, $B1$, ...$Bn-1$}and carry input as Cin ; whereas, the carry and sum outputs are represented as S = {$S0$, $S1$, ...$Sn-1$}, and $Cout$ respectively. The figure 5 shows the implementation diagram of modified speculator, which is in the proposed architecture. The CLA adder is used internally to implement this speculate carry output of each of the four input blocks [7]. The speculation process carried out for r number of MSB bits of each and every block. The size of the r is selected as les than to the input block size x=4. Subsequently, each speculator block carry input is 0 or 1, which creates +ve and –ve errors respectively. Each speculator block carry out (Cso) is applied as input carry for the succeeding adder blocks as shown in the figure 1. Then, each four bit block never waits for the input carry of the preceding 4-bit adder block. Here, all the adder blocks are parallel or simultaneously perform the addition process on relieving input carry bits from the concerned speculator blocks

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[10]. The SPEC block produces a speculated internal carry from very short number of input bits. The ADD block computes a local sum from the carry speculated in the SPEC block. If the carry propagation spans the entire SPEC block, it cannot predict exactly the carry and a wrong guess could lead to a speculative error. The COMP block detects those incorrect speculations and compensates erroneous sum. Speculator block computes carry based on the equation shown below:

$$P_i = A_i \oplus B_i \quad (1)$$

$$G_i = A_i B_i \quad (2)$$

$$C_{i+1} = G_i + (P_i . C_i) \quad (3)$$

The P_i, G_i and C_i are necessary to compute the C_{i+1}^{th} bit. The C_{i+1}^{th} bit is located in the critical path of Inexact Speculative Adder and the delay produces very small as we need to calculate the carry bit only for small numbers of bits. Whereas the adder block performs the sum of inputs from 4 bit blocks at the input. CLA adder is based on the equation given below.

$$S_i = P_i \oplus C_i \quad (4)$$

The above work uses CLA in the suggested hardware since the amount of signal delay in the propagation process is less when compared to traditional methods. As the adder operation is done by making use of the speculated carry bits at the inputs, the sum which is calculated in parallel from each of the blocks of the adder does not resemble the expected output. The sum value correction and balancing is carried out by the compensator block. Adder and compensator blocks are the ones which consume maximum delay along the critical path of the architecture.

B. Compensator Block

The compensator circuit in the ISA adder circuit differentiates the carry output from each of the four binary digits hardware adder circuit with speculated carry bit using EX-OR gate. An error flag is produced from the EX-OR gate output which initiates any one of the compensation techniques: error correction and error reduction to get activated. If the output of EX-OR gate is LOW (logic 0) then the local sum is passed directly to the last output. In the same style, if the EX-OR gate output is '1', that means the error may be positive or negative. The positive error represents a speculation of '0' instead of '1'. Hence, it induces lower sum value too. Albeit a negative error indicates a speculation of '1' instead of '0' which induces higher sum too. Based on the direction of potential error (very high error is solved by a '-1' and very low error is solved by a '+1') an unsigned increment or decrement for the group of LSBs is carried out by compensator block. If the result gets overflowed this correction cannot be possible. Then, the compensator block balances the group of MSB bits of the preceding sub adder block in the reverse direction of the error. The following equation is used for the balancing process;

$$2^n > \{ 2^n + 2^{n-1} + 2^{n-2} + \ldots\ldots + 2^0 \} \quad (5)$$

Whenever a 2^n error is found in the sum bit then it could be redressed by producing LSB errors for the sum bit in the direction opposite. The error reduction of unity can be achieved by balancing all the LSB's in the reverse direction as given by:

$$\{ 2^n - 2^{n-1} - 2^{n-2} - \ldots\ldots .- 2^0 \} = 1 \quad (6)$$

Generally, the p numbers of bits are used for the correction and hence p numbers of LSBs for each 4 input adder block are passed to the compensation block. Then that block checks the overflow condition. The correct compensation technique which provides balancing will be selected. This process is carried out before getting the sum of all other bits from the adder block. For the optimum result, the p value is usually selected as unity. Neither the pre-computing of error correction nor the compensation choice lies in the critical path of the ISA adder is the significant feature of the proposed architecture. The EX-OR gate, MUX and De-MUX of compensator block are only involved in the critical path of the ISA.

The pipelining process of proposed architecture is explained using 16 bit ISA. Here the n=16 can be increased, and which will not affect the critical path because of x is always 4 only. Due to these 4-bits as constant, the adder, compensator and speculators are not changed. In the proposed 32-bit ISA architecture, all the conventional blocks are replaced with pipelining blocks, such as PSPEC, 4-bit PCLA and PCOMP blocks. The individual blocks are internally consists of 2 stage pipelining. The entire architecture is designed using pipelining blocks and corresponding levels of registers, which retains the critical path delay.

The schematics and test-benches of sub blocks have been presented in further sub sections. From the observation of those sub blocks, the critical path is expressed in (7) and it can be used to determine the maximum clock frequency of proposed ISA.

$$\delta_{crt\text{-}prop} = \delta_{clk\text{-}Q(ff)} + \delta_{xor} + 3\,\delta_{and} + \delta_s \quad (7)$$

Where, $\delta_{clk\text{-}Q(ff)}$ is clock to Q delay and $\delta_{clk\text{-}Q(ff)}$ setup time flip-flops respectivelly. Then the maximum clock frequency can be evaluated by ISA is given as,

$$F_{max} \leq 1/\{\delta_{crt\text{-}prop} - \delta_{skew}\} \quad (8)$$

Where, δ_{skew} represents the clock skew which may occur in such scenario.

C. Power and Area Analysis

In the VLSI system design, pipelining is the activity of diminishing the critical path at the trade off but increasing the cost of area and the hardware. The hardware is increased due to the insertion of the registers for the pipelining process. Because of the deep pipeline

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process the numbers of registers are more for the proposed structure than the conventional ISA. The proposed ISA structure [9] in to several stages by pipelining it is segregated. So, this architecture is more compatible for the clock gating which is used to reduce the power consumption in the VLSI structures. In the proposed design, the clock signal that is fed into every stage is gated.

The active blocks and ideal blocks are differentiated in this architecture and hence clock switching which significantly reduces the power consumption. The clock gating process is only valid for the beginning and ending of the overall process. For the addition, at the very starts the later pipeline stages are ideal stages. These stages can be pipelined. At the ending process of addition, starting or earlier stages are clock gated.

For example: pipeline stages five, four, three and two are ideal while the process is being carried out in the first stage when the addition begins. Similarly, first stage will be ideal while rest keeps processing data when addition is towards the completion. However, the clock gating cannot be applied for the middle of the addition process, because all the blocks are busy by involving in the computation of the addition process.

IV. Results

In this section, the implementation of 32- bit ISA and the corresponding internal blocks are presented and analyzed. The figure 3 represents the schematic of 32-bit ISA adder created using Virtuoso Schematic editor. The simulation of adder using proper testing inputs is carried out in the CADENCE tools.

The ADEL (Analog Design Environment) Editor is used to simulate the ISA adder schematic for the test bench shown in figure 4 and corresponding simulation results shown in figure 11 and figure 12.

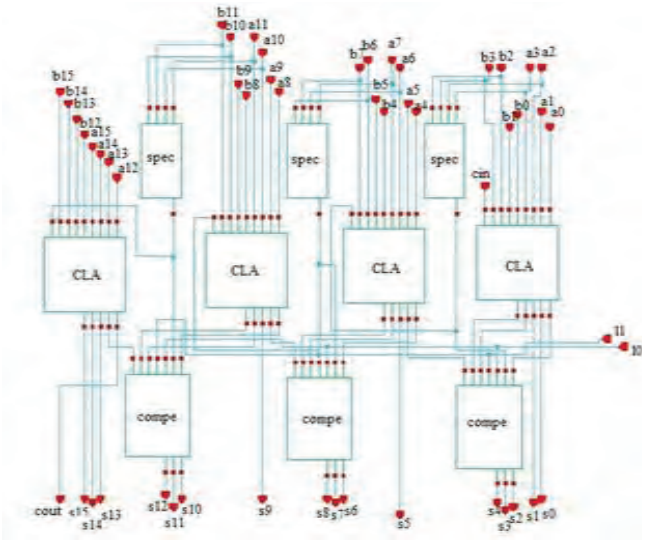

Figure 3. Schematic of 32- bit ISA in schematic editor

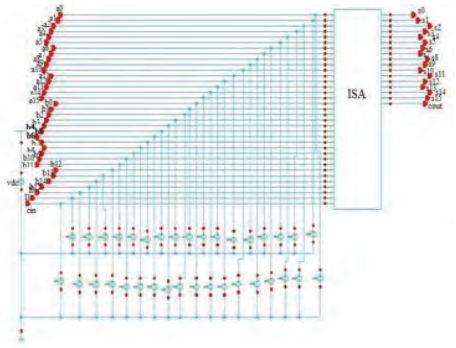

Figure. 4. Test bench of 32-bit ISA

The figure 5 represents the schematic of Speculator block which is used in the ISA. It consists of five AND gates and three OR gates. The schematic of Speculator block is implemented in the Virtuoso schematic editor and test bench for Speculator shown in figure 6.

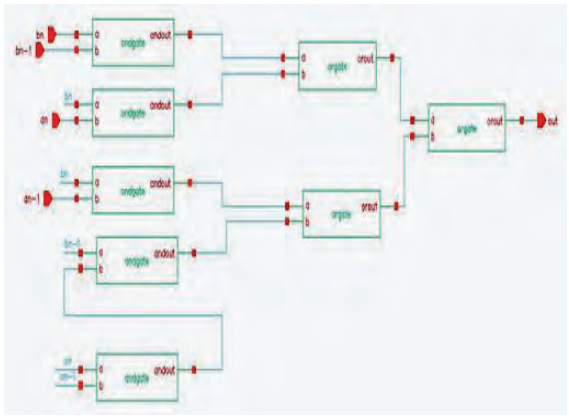

Figure 5. Schematic of speculator of ISA

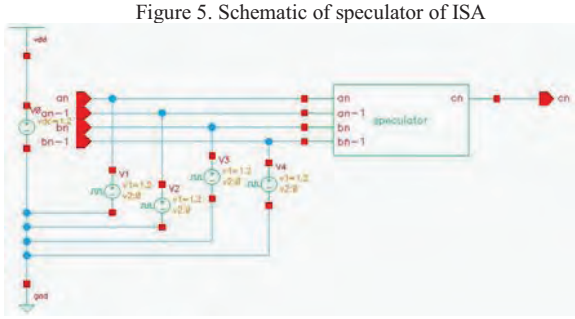

Figure 6. Test bench of speculator of ISA

The figure 7 represents the compensator block which is used in ISA adder. The compensator block designed with 9 AND gates, 3 OR gates, 3 NOT gates and 2 XOR gates. This block is implemented in Virtuoso Schematic Editor and simulated in ADEL using the Test bench shown in figure 8.

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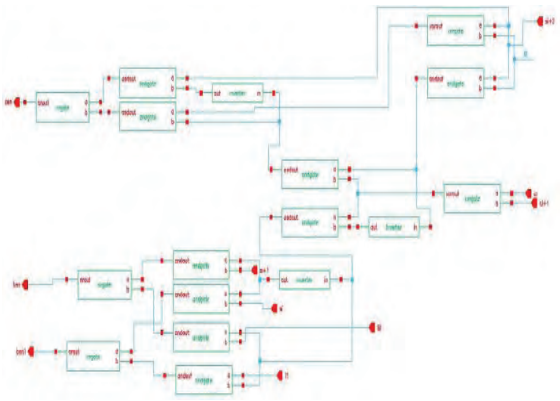

Figure 7. Schematic of Compensator of ISA

The power consumption and delay of the 32-bit ISA adder are shown in the table.1. The entire power for the 32-bit ISA is 36.94µW and the delay for the 32-bit ISA is estimated as 78.38ps.

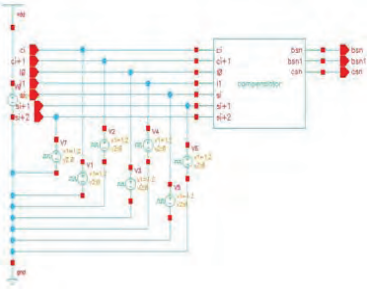

Figure 8. Test bench of Compensator.

The figure 9 represents the CLA circuit which is used in ISA adder design. The carry look adder designed with 23 AND gates, 10 OR gates and 8 XOR gates. This design is implemented in Virtuoso Schematic Editor. This block is simulated in ADEL using the Test bench shown in figure 10.

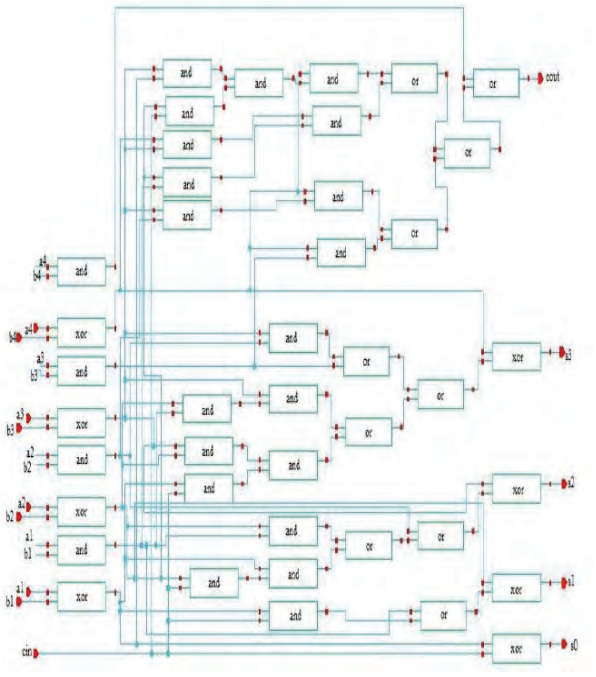

Figure 9. Schematic of Carry-look-ahead adder

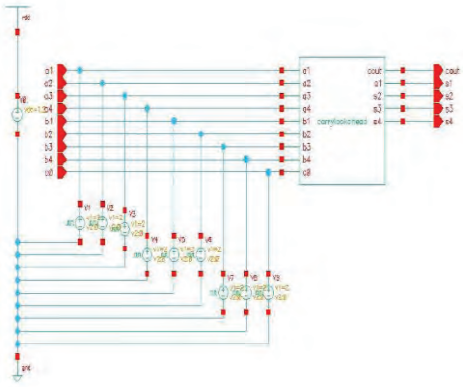

Figure 10. Test Bench of Carry-look-ahead adder

TABLE I.
POWER AND DELAY OF PROPOSED ISA

Parameter	Value
Power	36.94µW
Delay	78.38ps

The figure 11 and figure 12 represents the simulated output wave forms of the two different test inputs for the 32-bit ISA adder.

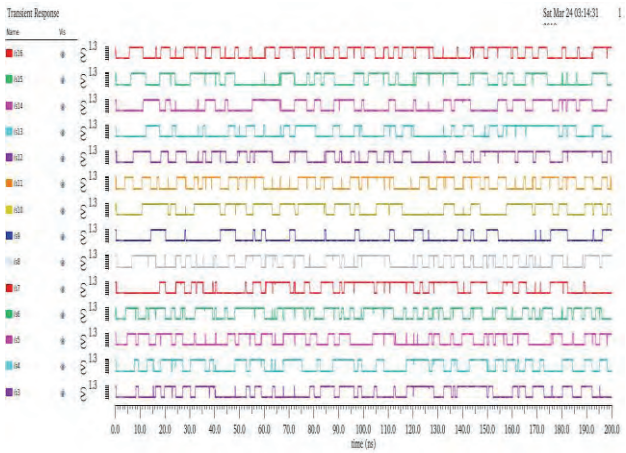

Figure 11. Simulated output waveforms of 32-bit ISA

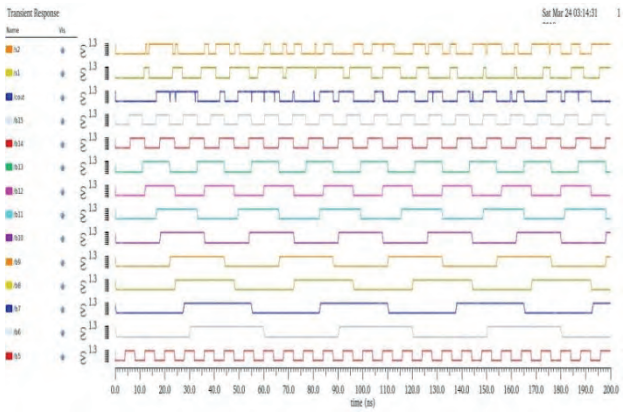

Figure 12. Simulated output waveforms of 32-bit ISA

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The power and delay values of 32 bit ISA adder are compared with the existing different types of 32 bit adders [5]. The delay and power are much improved. The comparison of various adders with ISA power and delay values are shown in the table II. The power is saving up to 43% and delay reduced to 40%.

TABLE II.
COMPARISON OF VARIOUS ADDERS WITH ISA

TYPE OF ADDERS	POWER	DELAY
ISA	36.94μW	78.38ps
Parallel Adder using 10T full adder	110μW	4.24ns
Carry look ahead adder	84.90μW	3.1ns

IV. CONCLUSIONS

A conventional architecture of Inexact Speculative Adder (ISA) with hopped-up performance and a versatile precision is presented. In this architecture a novel error correction and error reduction method is used. This process enhances the overall worst case accuracy. The overhead speculative hardware is removed from the critical path of the structure. The ISA architecture allows precise tuning of multiple error characteristics and enhances the interpretation to a large extent the design of inexact speculative adder produced lesser delay compared to the parallel adders designed. It has been proved that ISA, due its low delay contributes a higher speed of operation.

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