

Fault Tolerant Design using 5-Modular Redundancy Configuration with Different Voter Circuits

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Abstract: In the current situation, the reliability of a complex digital system is indigent owing to large amount of components, transistors, Integrated Circuits (ICs), etc. As a result the claim to design a good system with reliability is crucial. Such systems are frequently used in very critical applications such as bank transactions, defense communications, aerospace applications, etc. If these systems fail in the field, then the loss will be massive. The circuit designers carry on research to enhance the reliability of a system by adding redundancy like in hardware, software, information and time. The hardware redundancy is proposed to improve the reliability of the system. At present the Triple Modular Redundancy (TMR) is the most common technique used in the field of microelectronics to improve the reliability. This TMR system can tolerate one error for the correct output of the system. This paper primarily focuses on the 5MR scheme for the betterment of reliability which can tolerate two errors. The TMR in the 5MR system is implemented using FPGA Altera board with various voter circuits and ASIC implementation is carried out using ISCAS'85 and ISCAS'89 benchmark circuits. This paper analyze the 5MR system in detail using different majority computation circuits with TMR portion and convey the optimum circuit which will be suitable for low power, less area overhead and lesser delay.

Index Terms: Fault-tolerant, Majority voters, NMR, TMR, VLSI

I. INTRODUCTION

In the recent microelectronic circuit design scenario, the significance of reliability is to be addressed carefully, otherwise the system may fail due to the reduced supply voltages, higher operating frequencies, lower internal capacitances, and low noise margins. A self checking fault tolerant circuit was designed to improve the reliability in a nanoscale FPGA [1]. A self checking circuit for different voter circuits is designed for error detection. This investigates about the reduction of power, area and delay. Here five inputs are taken for the voter circuits and results are compared with respect to its performance [2]. Many researchers investigated the reliability improvement by considering the voter circuits. A high reliable low cost fault tolerant circuit was designed to gain the reliability in an efficient manner rather than conventional TMR system.

Moreover most of the TMR systems focused on the redundancy methodology [3].

To design a system to withstand more than one error, the N-modular redundancy (NMR) approach can be deployed in real time. Here N is any odd number which can withstand the error upto $(N-1)/2$ errors. For example, the 5MR system can tolerate two errors; the 7MR system can tolerate three errors and so on [4–6]. The noticeable shortcoming with this NMR system is area and power consumption overhead. This study focuses mainly on the hardware redundant logic techniques using 5MR approach with tolerance of two errors.

II. MATERIALS AND METHODS

The reliability of the system can be improved by implementing 5MR rather than TMR system at the rate of area and power consumption.

A. The existing 5-MR configuration

The 5MR system is shown in Figure 1. The inputs A, B, C, D and E are applied to the circuit and the output (V) is obtained as calculating the majority among the inputs [4]. This system works as follows:

- i) If $D = 0$ and $E = 0$, results in the majority output (V) as “ABC”.
- ii) If $D \neq E$, then the voter output becomes as the majority among the inputs A, B, and C. That is the voter output make use of the TMR configuration along with the inputs A, B, and C.
- iii) If $D = 1$ and $E = 1$, the majority output (V) becomes as “A+B+C”. This is apparent with reference to the given Fig. 1.

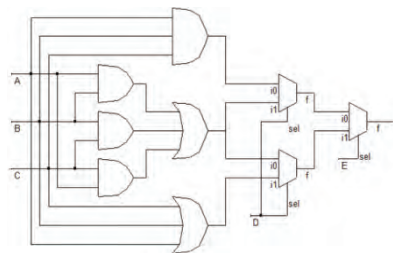


Figure 1. The 5MR system

The TMR subsystem which is available in the 5MR system can be built using different voters [7]. This is the motivation to construct different 5MR systems with various kind of voters and the simulation results with performance comparison are obtained with few industry standard benchmark circuits. The TMR subsystem used here is shown in Fig.2. Here, the TMR output is obtained as “AB+BC+CA” as a carry output of a full adder [8–9]. This subsystem can tolerate only one error.

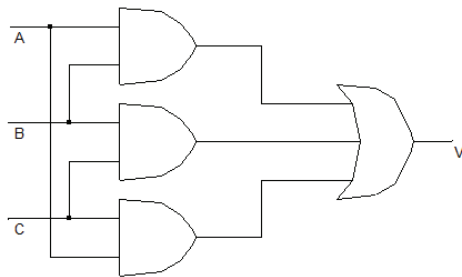


Figure 2. Conventional voter with TMR

B. A 5-MR system using different voters

The voting section, that belongs to TMR is involved in the 5MR is replaced with many voters for performance comparison. Some voters may contain less layout area at the cost of power; few others may dissipate low power consumption at the cost of area. This kind of analysis would help the engineers to choose the optimum design for the system with better power and area metrics.

C. Voter using NAND and NOR gates

In a CMOS VLSI design approach, the NAND and NOR gates play a most vital role due to the unique behavior as universal gates. They may dissipate less power and contains low layout area. The Fig. 3 contains the voter using NAND and NOR gates [8].

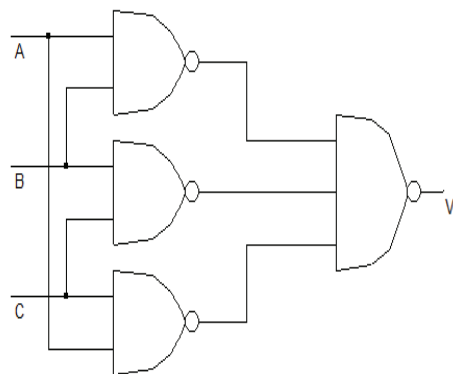


Figure 3(a) Voter circuits using NAND gates

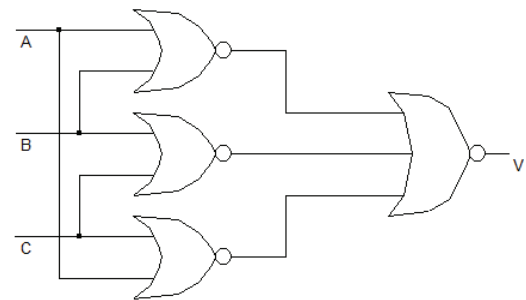


Figure 3(b). Voter circuits using NOR gates

D. Modified voter using carry look-ahead adder principle

The majority function can also being implemented as $\{(A \oplus B)C\} + \{AB\}$ using the concept of CLA (Carry Look-ahead Adder) circuit [8]. This circuit works as follows:

- i) If $A = B = 1$, then the majority output becomes 1.
- ii) If $A \neq B$, then the majority output follows the third input C.

The modified function $\{(A+B)C\} + \{AB\}$ also produce the majority among the three inputs. These circuits are shown in Fig. 4.

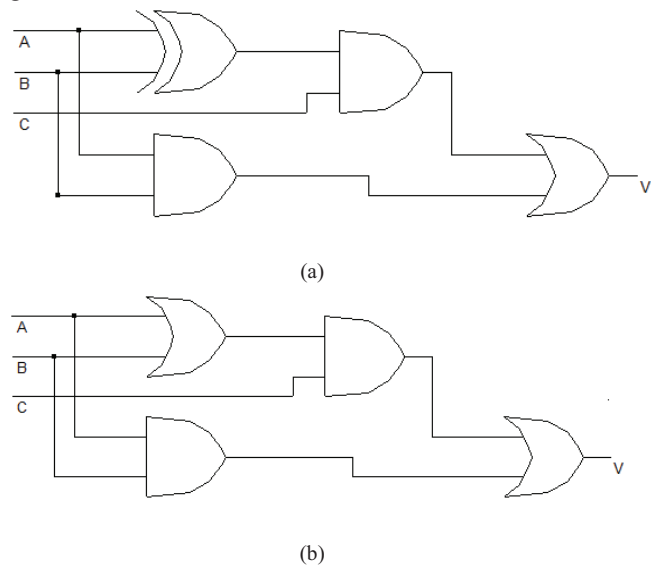


Figure 4. Voter circuits using CLA concept

E. Modified voter using Mux1 approach

The voter output here is calculated using a 2-to-1 multiplexer in which the input A act as a select signal; the inputs B and C are applied as data inputs to the multiplexer. This circuit is shown in Fig. 5 and works as follows:

- i) If $A = 0$, the majority function obtained as “BC”.
- ii) If $A = 1$, then the output V will be “B+C”.

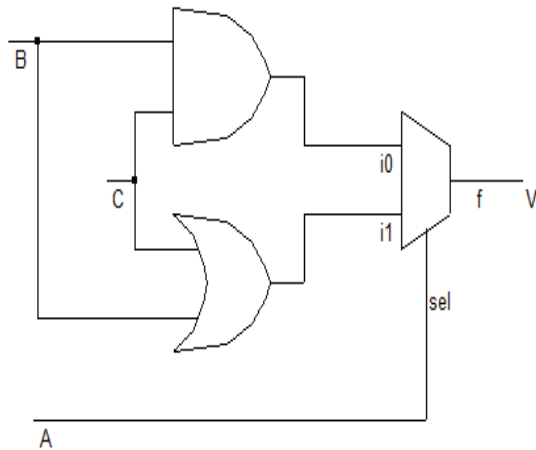


Figure 5. Voter circuit using Mux1 approach

F. Voter using Mux2 approach

The voter output is obtained using one 2-to-1 multiplexer and one XOR gate. This principle looks similar to the CLA subsystem discussed earlier but with modification in the schematic. The $\{B \oplus C\}$ signal act as a select signal to the multiplexer; the A and B inputs can act as data inputs to the multiplexer. This circuit is shown in Fig. 6 and works as follows:

- i) If $\{B \oplus C\} = 0$, the majority function becomes as B.
- ii) If $\{B \oplus C\} = 1$, then the voter output becomes as A.

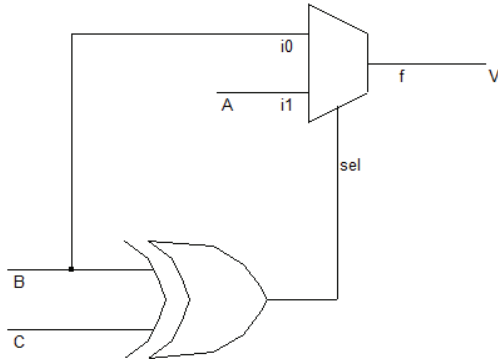


Figure 6. Voter circuit using Mux2 approach

G. The complete 5-MR system

The Fig. 7 shows the complete 5MR system in which the TMR portion is replaced with Mux2 approach. In this study, this TMR portion is replaced with the all above said various voter circuits to obtain the majority functions among the five inputs A, B, C, D, and E.

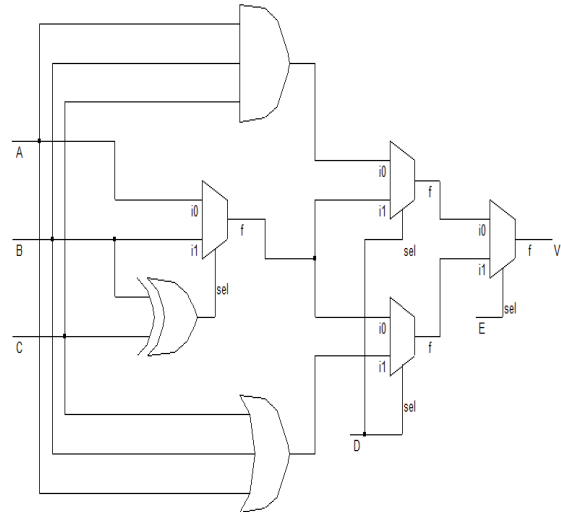


Figure 7. 5MR system using Mux2 approach as TMR

III. RESULTS AND DISCUSSION

The performance comparison of 5MR systems using difference voter circuits is done with few test circuits. The FPGA implementation was carried out with Quartus II 13.1 synthesis tool with Altera FPGA device EP4CE115F29C7.74X-series circuits like 4-bit magnitude comparator, 4-bit carry look-ahead generator and 4-bit adder are used as benchmark circuits. Table.I to Table.V depicted about this simulation. The Electronic Computer Aided Design (ECAD) tools like DSCH and Microwind are also used to test 5MR systems with ISCAS’85 combinational circuit (C17) and ISCAS’89 sequential circuit (S27) [12] with 120nm technology for ASIC implementation and Table.VI and VII showed this simulation. The Figure-Of-Merit (FOM) is computed as the inverse of the product of power, delay, and area (PDA) [4]. For a better design this FOM must be high. Tables I, II, III, IV, and V show the results of 5MR system with the test circuits like 8-bit Ripple Carry Adder (RCA), 4-bit RCA (74283), 8-bit magnitude comparator, 4-bit magnitude comparator (74L85) and a 4-bit carry look-ahead generator (74182) respectively. From the TableI, the Mux1 approach occupies only 94 Logic Elements (LEs), lower delay is obtained with NOR gates method as 17.710 ns, the Mux2 approach dissipates lower power dissipation as 133.91mW. It is apparent by referring other tables that the Mux1 and the Mux2 approaches are optimum as compared with the other style methods.

TABLE I.
SIMULATION RESULTS OF AN 8-BIT RCA USING 5MR WITH VARIOUS VOTERS

Metrics	Voter using different Majority function computations							
	K-map	Existing	NAND	NOR	$(a \oplus b)c+ab$	$(a+b)c+ab$	Mux1	Mux2
LEs	123	115	97	95	115	115	94	97
Delay (ns)	21.811	18.537	17.694	17.710	25.381	25.381	30.111	17.643
Power (mW)	139.38	133.92	140.42	140.42	154.61	154.61	137.54	133.91

TABLE II.
SIMULATION RESULTS OF A 4-BIT RCA USING 5MR WITH VARIOUS VOTERS

Metrics	Voter using different Majority function computations							
	K-map	Existing	NAND	NOR	$(a \oplus b)c+ab$	$(a+b)c+ab$	Mux1	Mux2
LEs	38	63	42	42	41	41	34	34
Delay (ns)	8.143	8.535	8.377	8.377	8.415	8.415	8.044	8.044
Power (mW)	132.27	139.96	139.94	139.09	142.98	144.35	131.31	131.30

TABLE III.
SIMULATION RESULTS OF AN 8-BIT COMPARATOR USING 5MR WITH VARIOUS VOTERS

Metrics	Voter using different Majority function computations							
	K-map	Existing	NAND	NOR	$(a \oplus b)c+ab$	$(a+b)c+ab$	Mux1	Mux2
LEs	109	113	115	111	108	109	107	107
Delay (ns)	22.395	15.807	17.309	18.338	16.893	18.972	20.711	17.862
Power (mW)	168.74	159.79	138.37	137.05	131.74	161.07	142.53	129.97

TABLE IV.
SIMULATION RESULTS OF A 4-BIT COMPARATOR USING 5MR WITH VARIOUS VOTERS

Metrics	Voter using different Majority function computations							
	K-map	Existing	NAND	NOR	$(a \oplus b)c+ab$	$(a+b)c+ab$	Mux1	Mux2
LEs	60	61	67	61	61	61	53	69
Delay (ns)	8.749	8.1	8.823	8.763	8.621	8.621	8.351	8.044
Power (mW)	133.04	133.27	130.09	134.66	134.77	134.60	137.95	130.01

TABLE V.
RESULTS OF A 4-BIT CARRY LOOK AHEAD GENERATOR USING 5MR WITH VARIOUS VOTERS

Metrics	Voter using different Majority function computations							
	K-map	Existing	NAND	NOR	$(a \oplus b)c+ab$	$(a+b)c+ab$	Mux1	Mux2
LEs	39	41	42	42	41	41	34	34
Delay (ns)	7.905	8.469	12.013	12.013	7.717	7.717	8.125	8.125
Power (mW)	143.46	142.71	140.81	140.95	131.55	130.66	131.58	131.58

TABLE VI.
SIMULATION RESULTS OF A C17 CIRCUIT USING 5MR WITH VARIOUS VOTERS

Metrics	Voter using different majority function computations					
	NAND	NOR	$(a \oplus b)c+ab$	$(a+b)c+ab$	Mux1	Mux2
Delay (ns)	0.870	0.870	0.930	1.170	0.870	0.870
Power (mW)	0.361	0.361	0.136	0.27	0.132	0.065
Area (μm^2)	1674.2	1674.2	3611.1	1300.8	4120.3	2004.9
FOM $\times 10^4$	19.0	19.0	21.89	24.07	21.13	88.17

TABLE VII.
SIMULATION RESULTS OF AN S27 CIRCUIT USING 5MR WITH VARIOUS VOTERS

Metrics	Voter using different majority function computations					
	NAND	NOR	$(a \oplus b)c+ab$	$(a+b)c+ab$	Mux1	Mux2
Delay (ns)	1.740	1.755	1.920	3.5	1.740	1.740
Power (mW)	0.379	0.379	1.673	1.761	1.688	0.16
Area (μm^2)	2375	2352.2	2364.4	2180.3	2468.2	2468.2
FOM $\times 10^4$	6.37	6.39	1.31	0.74	1.37	14.55

Simulation results with ISCAS'85 (C17) and ISCAS'89 (S27) benchmark circuits are obtained as in tables VI and VII respectively. One combinational circuit (C17) and one sequential circuit (S27) are taken as test benchmark circuits to compare the performance of different voters with 5mr system. The FOM and PDA are inversely proportional to each other, and the PDA is calculated as Figure-of-Merit (FOM). Since the optimum designs look for lower delay, less area, and low power consumption, the product term (PDA) will be a low value and hence the higher FOM. It is apparent that from tables, Mux2 approach produces better FOM as compared with the other methods.

IV. CONCLUSIONS

This study analyses the 5MR system in detail using different majority computation circuits in combination with TMR circuit and produced the optimum circuit which will be suitable for low power, less area overhead and lower delay. This kind of study helps engineers a lot in the current microelectronics trend of to choose the optimum circuits for the critical applications with more reliability. This work can be further extended to 7MR, 9MR and 11 MR circuits too with appropriate circuit intelligence.

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