High-efficiency Low-power Flash ADC for High-speed Transceivers

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***Abstract*-Modern communication systems require higher data rates which have increased the demand for the high speed transceivers. For a system to work efficiently, all blocks of that system should be fast.. This fact has led researchers to develop high speed analog to digital converters (ADCs) with low power consumption. Among all the ADCs, Flash ADC is the best choice for faster data conversion because of its parallel structure. This paper work describes the design of such a high speed and low power Flash ADC for the analog front end (AFE) of a transceiver. A high speed highly linear track and hold (T&H) circuit is needed in front of ADC which gives a stable signal at the input of ADC for accurate conversion. Averaging technique is employed in the preamplifier array of ADC to reduce the static offsets of preamplifiers. The averaging technique can be made more efficient by using the smaller number of amplifiers. This can be done by using the interpolation technique which reduces the number of amplifiers at the input of ADC.**

The Flash ADC is designed and implemented in 180 nm CMOS technology for the sampling rate of 1.6 G Samples/sec. The bootstrap T&H consumes power of 27.95 mW from a 1 V supply and achieves the signal to noise and distortion ratio (SNDR) of 37.38 dB for an input signal frequency of 195.3 MHz The ADC with ideal T&H and comparator consumes power of 78.2 mW and achieves 4.8 effective number of bits (ENOB).

***Index Terms*—ADC, low power, track& hold, comparator, high speed, transceivers.**

I. INTRODUCTION

For communication systems the need arises for higher data rate and high speed transceivers. To increase the data rates and handle wire losses, high speed analog to digital converters with multiple bits of resolution are needed at the receiver end. The development in analog and digital domain has grown dramatically over the years. As a result, the speed and efficiency of the digital circuits has increased to a great extent and also these circuits consume less power. In contrast to this, input output data rate of analog circuits is not as fast, because the outside world does not shrink along with the CMOS technology. Due to this technology difference we can see that the analog interfaces are the limiting factor in the whole system in terms of speed and power. The high speed Transceivers requires high bandwidth and high resolution ADCs. For high speed purposes, flash ADC is the best choice for fast data conversion. This paper work presents the design of such a high speed and low power flash ADC for the analog front end of the transceiver and concentrated on the design of track and hold circuit and preamplifier design.

The over view of the communication system shown in figure.1. This system mainly consists of a high speed transceivers and a channel through which data is transmitted and received. In high speed transceivers, the 8-level pulse amplitude modulation (PAM-8) modulation schemes are used for multi-gigabit transmission to reduce transmission time and for fast bit rate.

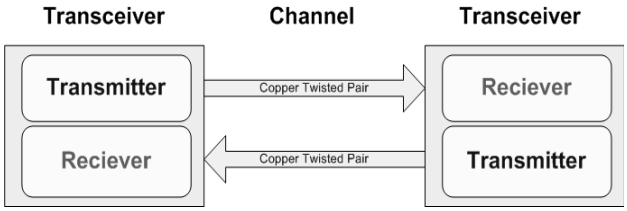

Figure 1: Block Diagram of Transceiver.

The transmitter sends the signal by using the pulse amplitude modulation (PAM) with the data rate of several Gb/s. In the Pulse Amplitude Modulation scheme, the information is encoded in the series of amplitude signal pulses. A PAM-8 is used in the above system which transmits three bits of information in each symbol time. This reduces the effective symbol rate of binary signaling by three and the required data rate can be transmitted with reduced channel bandwidth.

The channel is used in the above system is a Copper twisted pair cable, which is capable of reducing the noise interference and crosstalk between the differential pair of wires. These cables provide bandwidth up to 600 MHz and speeds of several giga hertz.

Next, the receiver consists of two main blocks, one is analog front end (AFE) and second is digital signal processor (DSP).The AFE receives the signal which is sent by the transmitter. The received signal is converted into an equivalent digital signal by ADC before sending to the digital signal processor (DSP) for processing. The AFE contains variable gain amplifier (VGA) and analog to digital converter (ADC) and other blocks. The block diagram of the AFE is shown in figure 2.

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A. Variable Gain Amplifier

In the AFE, the VGA amplifies or attenuates the input signal to produce signal amplitude which should match the full scale input range of the ADC. The variable gain amplifier (VGA) is used in many communication systems to improve the dynamic range (DR) of the overall system. There are two types of VGAs, a Digital variable gain amplifier (DVGA) and an Analog variable gain amplifier (VGA). 1. Digital variable gain amplifier (DVGA) uses binary weighted arrays of resistors and capacitors to control the gain. Application of DVGA is in cable TV system. 2.Analog variable gain amplifier (VGA) uses variable resistance to control the gain. They are used in ultra sound scanners and radars.

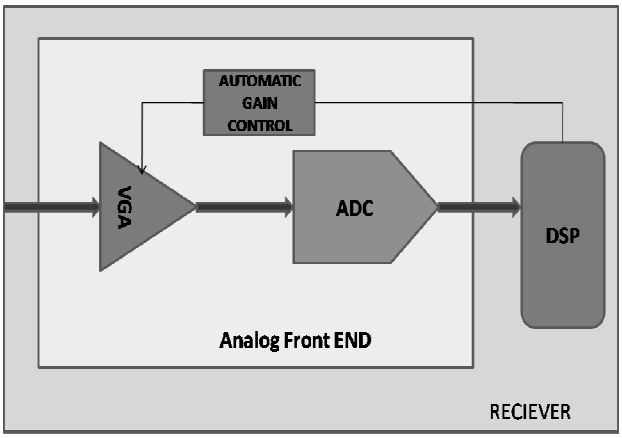

Figure 2: Block Diagram of Analog Front End.

B. Analog to Digital Converter

Analog to digital converter is used to convert an analog signal into a equivalent digital data. In the AFE, ADC takes the analog signal from VGA and converts it into digital form before sending it to the Digital Signal Processor for further processing. Mainly the Analog to digital conversion involves three steps: Sampling, Quantization and Coding. In the sampling process, the samples of the input signal are taken at discrete instants of time. Then the frequency corresponding to these samples is called the sampling rate of ADC. For accurate representation of signal, the sampling process should follow the Nyquist theorem i.e the sampling frequency should be at least twice the highest signal frequency .In quantization, the sampled signal is approximated to certain standard quantization levels depending on their amplitudes. In encoding process the quantized signal is converted into binary code.

C. Digital Signal Processor

The Digital Signal Processor (DSP) captures the digitized information from AFE through ADC and then manipulates it mathematically at a very high speed. In communication systems it is used for the Equalization, Non-linearity compensation, Decoding and Forward error correction. The other applications of DSP include audio and video compression, image processing, automatic gain control algorithms.

In this paper, the design of track and hold circuit and preamplifier for high speed and low power flash ADC for the analog front end of the transceiver system is placed.

II. FLASH ADC

Flash ADCs are suitable for applications where very high analog to digital conversion speed is required. But these Flash ADCs are limited to the resolution of six to eight bits because the number of comparators used in these ADCs double if the resolution is increased by one bit. Due to the large number of comparators, they ADC consume more power and are very costly for higher resolutions. The major applications of flash ADCs are in satellite communication, radar processing, data communications and real time oscilloscopes. In this thesis work, flash ADC is used for data communication applications.

The flash ADC can achieve better sampling rates as the only analog building block in flash ADC is comparator [21].The function of flash ADC is very simple, it compares the analog input signal with a number of reference voltages and produces the output. The parallel architecture of flash ADC allows conversion process in one clock cycle. So at the same conversion rate, flash ADC has low latency where latency is the number of clock cycles required by an ADC to convert the given input to an output. Thus, the flash ADC is extremely fast and gives the data conversion rates in several GHz. The only problem with the flash ADC is the power consumption which increase with the increase in number of bits, that's why this ADC limiting the number of bits to six to eight only. The block diagram of conventional flash ADC is shown in figure 3.

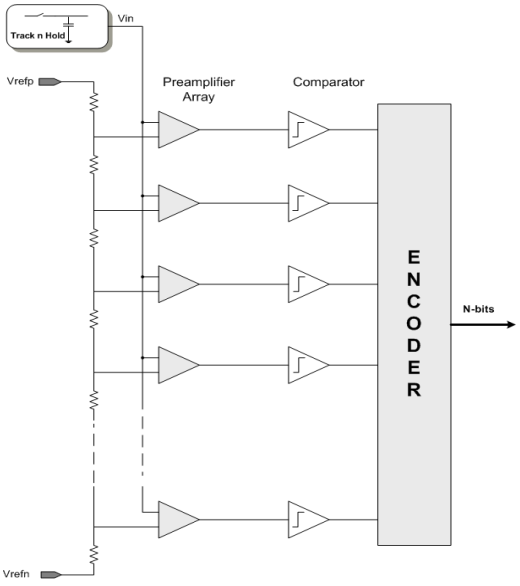

Figure 3: The block diagram of flash ADC

The signal coming from the track and hold is compared with a number of reference voltages which are generated by a reference circuit. If the input voltage is

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higher than the reference voltage, the comparator gives '1' at its output, and if the input voltage is lower as compared to the reference voltage, the comparator gives '0'. The code produced by comparator array is called thermometric code which is then converted to binary output by an encoder [10].

A. Track And Hold

The first circuit in the flash ADC is the T&H circuit is as shown in figure 4, It consists of a sampling switch and a hold capacitor. During the first half of the clock cycle, the circuit tracks the signal which is called the tracking mode and during the second half of clock cycle it holds this value in the hold capacitor for subsequent processing, and this is called the hold mode. The switch and the hold capacitor make a RC network, the time constant of which determines the BW that can be achieved through this network [16, 17].

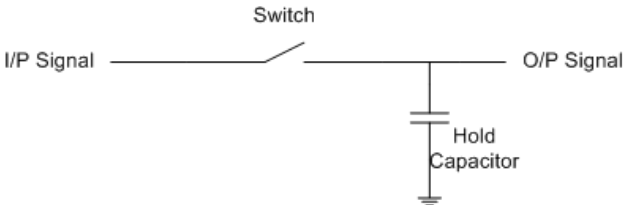

Figure 4: A basic track & hold circuit

Track and hold circuits are important building blocks of ADCs where they are used to improve the dynamic behavior and reduce the errors due to aperture jitter and clock skew [29]. This is because the T&H circuit is very small as compared to the whole ADC. The clock skew and jitter problems have effect only on the front end T&H circuit and the ADC have stable signals at their input. The overall performance of ADC depends highly on the performance of T&H circuit [6, 14].

The T&H circuits are classified into two types one is open loop and second is closed loop. In an open loop architecture, there is no feedback loop. The T&H circuit mainly consist of a sampling switch and a hold capacitor with input and output buffer. The purpose of buffers is to isolate the T&H circuit from the rest of circuit. The open loop T&H architectures are used where high BW and low power consumption is required. The accuracy of this open loop architecture is not so good due of the lack of feedback. At high speeds, the circuit produces instability.

In the closed loop architecture, a feedback loop is inserted between the output and the input. This feedback improves the accuracy of T&H circuit but reduces the speed. So this architecture is not suitable for the speeds in the range of GHz. Figure 5 shows the open loop and closed loop configuration of track and hold circuit.

B. Pre-amplifier

The function of pre-amplifiers in flash ADCs is to amplify the voltage difference between the input signal and the reference voltage. They are used at the input of comparators to suppress large dynamic offsets and reduce the meta-stability errors [2]. High gain of pre-amplifiers is needed to reduce bit error rate (BER) by reducing the offsets of comparators. The BW of Pas should also be high to improve the settling time and avoid distortions at high input signal frequencies. It is difficult to achieve high gain with high bandwidth in one stage so multiple stages of pre-amplifiers can be used to increase the gain [5, 8]. In addition to comparator large dynamic offsets, Pas also have their own static offsets. To reduce offsets of PAs, large transistor sizes can be used. These large transistor sizes increase the input capacitance of PAs which in turn increase the load for TnH circuit. Another efficient way of reducing the PA offset is to use averaging technique [13].

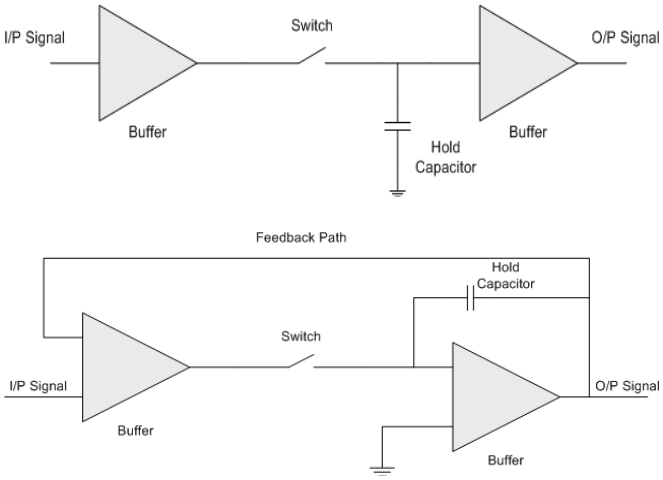

Figure 5: Open loop and Close Loop Track and Hold Circuits.

The averaging technique is used to reduce the offsets of PAs. In this technique, the outputs of PAs are interconnected through averaging resistor net work. By doing this, the errors contributed by individual PAs are averaged, and offsets are reduced. The reduction in offset depends on the ratio of averaging resistor and output impedance of PA. However, this technique causes problems at the edges of resistive network where the linearity is reduced because of boundary issues [9, 12, 13].

Averaging technique to reduce offset errors can be improved further if it is used with a reduced number of PAs [1]. To reduce the number of PAs at the first stage, interpolation is employed. In interpolation, intermediate voltage points are generated by replacing each resistor in the resistive network, with two resistors of half size. Multiple taps of interpolation are also possible [2, 13].Multiple stages of PAs can be used with averaging and interpolation to reduce the number of PAs significantly. For example, for six-bit flash ADC, if three stages of PAs are used with an interpolation factor of two, then the number of amplifiers needed at the first stage will be nine instead of 63. Another advantage of using interpolation is that the requirements for the track and hold circuit can be relieved as its output load is reduced because of the reduced number of PAs. Also, the size of PAs can be made bigger to reduce offsets further.

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C. Comparators

The comparators are the basic building blocks of flash converters and are used to convert the analog signal into digital form. A comparator in flash ADC acts as a one-bit quantizer. A N-bit flash ADC requires 2^N -1 comparators and for every additional bit, the number of required comparators becomes double which increase both power and area. Due to this fact flash ADCs are not suitable for high resolution. The outputs produced by comparators are not practical to be processed in the DSP, so an encoder is needed to produce binary output for further processing.

D. Encoder

The function of the encoder is to convert the thermometer code produced by comparator array into a N-bit binary code. Encoder can be implemented in different ways such as XOR encoder, ROM and fat tree encoder. The proposed encoder is a CMOS priority encoder. In this implementation, we have used pass transistor logic and dynamic circuitry not only to achieve high performance but also to minimize silicon real estate. we describe the circuitry of a CMOS priority encoder with no lookahead. Then extremely fast priority circuitry is added to this circuit, with a very small impact on the overall number of transistors, to produce an encoder that uses a priority lookahead scheme. The four bit priority encoder is shown in figure6.

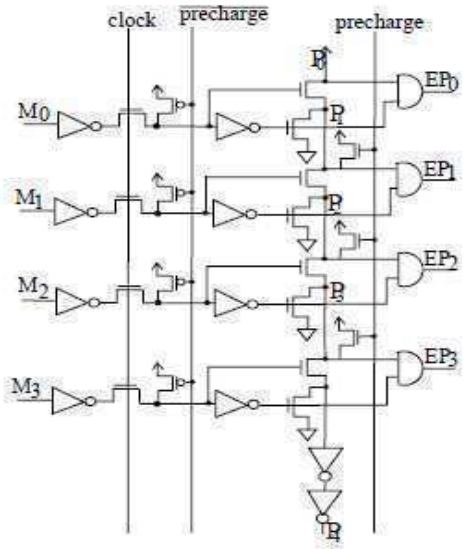

Figure 6: 4-bit priority encoder.

III. IMPLEMENTATION

In this section the blocks of the Flash ADC , mainly track and hold and preamplifiers are designed in the CMOS technology in the transistor level using 180nm technology.

A. Implementation Bootstrap Track and Hold

The open loop T&H provides high speed, but linearity of this architecture is not so good because there is no feed-back path. To overcome the linearity problems, a bootstrapped T&H circuit is employed in this paper which makes use of bootstrapped switch. Figure 7 shows the block diagram of such a bootstrap T&H circuit. One of the sources of non-linearity is a variation in on resistance Ron of sampling switch which is caused due to the non-constant gate to source voltage (Vgs) during the track mode. The Ron of sampling switch is given by ,

$$Ron = \frac{1}{\mu Cox(W/L)(Vgs - Vth)}$$

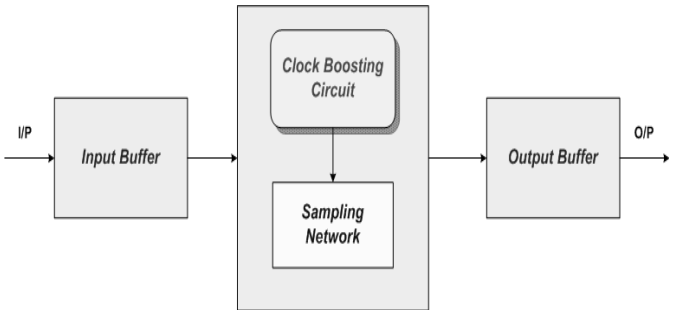

Figure 7: Block Diagram of Bootstrap Track & Hold Circuit.

The resistance of switch changes with the change in source voltage, which degrades the linearity of circuit. To avoid this, a bootstrap switch is used which keeps the Ron independent of source voltage by making the gate-source voltage of switch constant. Also, it is desired to have a small Ron for better linearity, this can be achieved by increasing the W /L ratio. The bandwidth is also reduced with small Ron. A bootstrapped switch is shown in figure 8.

The pseudo-differential architecture was chosen to design the T&H circuit. because it reduces the common mode (CM) hold pedestal and even order harmonics. In this way, it is possible to use hold capacitors of smaller sizes

There by increasing the speed of T&H circuit [18]. A pseudo differential architecture uses two separate but identical circuits which represent positive and negative part of the differential input signal [7].

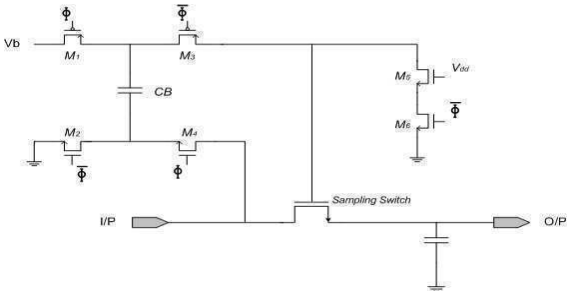

Figure 8: Bootstrap Switch.

The bootstrap T&H circuit used in this thesis is comprised of NMOS source follower (SF), a sampling network (SN) containing bootstrapped switch and a dummy switch, and finally a PMOS source follower. The description of individual blocks is given below.

B. NMOS Source Follower Buffer

Source followers (SF) are used in high speed T&H circuits as voltage buffers. A NMOS SF with resistor at source was used as an input buffer. The reason for using resistor at the source instead of current source was to get higher bandwidth. The gain of NMOS SF was limited because of using a smaller value of the source resistor to get high bandwidth. The non-linearity due to body effect was eliminated by connecting bulk of the transistor to its source. NMOS with triple well process was used to eliminate the body effect where it is possible to connect the source to bulk.

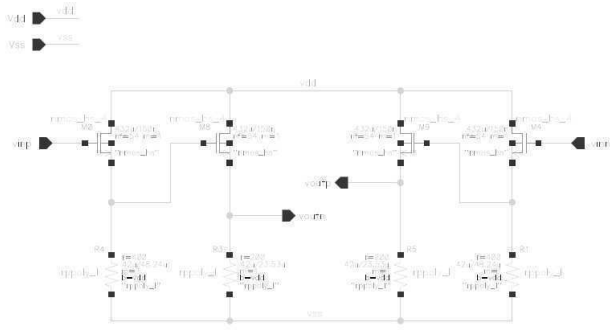

Figure 9: Transistor level implementation of NMOS Source Follower.

In this work, NMOS SF was used to drive the input capacitance of SN and isolate the TnH circuit from variable gain amplifier. A cascade of NMOS SF was used to shift the DC level of the input signal from 1.4 V to 450 mV. The level shift of signal could also be done in a single stage either by decreasing the size of transistors or by reducing the value of source resistor. In both cases, the gain of buffer reduced significantly. The level shifting was done to get the common mode voltage of 1.3 V at the output of track and hold circuit. The transistor level implementation of NMOS SF are given in figure 9.

C. Sampling Network

A NMOS transistor was used as a switch for its better speed as compared to the PMOS switch. A major drawback of the NMOS sampling switch is that it has strongly signal-dependent on-resistance [18]. A clock boosting circuit was employed for getting constant Vgs to reduce the variations in Ron. A dummy switch was added to reduce the non-linear effects due to charge injection and clock feed-through. The source and drain of dummy switch were shorted, and the gate of this switch was provided with the same clock boosting circuit as that of the sampling switch but in complemented form. The size of dummy transistor was chosen to be half the size of sampling switch, which is perfect for clock feed-through cancellation. The half size of dummy switch does not exactly match the charge from the sampling switch because of different operating regions of sampling switch while the Vds of dummy switch is constant as the drain and source terminals are shorted. It was therefore assumed that half of the channel charge from sampling switch is injected on both sides. The charge injected by the switch was absorbed by dummy switch thus preventing the error in the value of voltage on the hold capacitor. When the dummy switch turns off it also injects its charge on both sides. This is the reason why source and drain of dummy switch were shorted because in this way all the charge was injected to a low impedance, voltage driven source. Thus, the charge injection of dummy switch had no effect on the value of voltage on hold capacitor [11]. The transistor level implementation of bootstrap circuit are shown in figure 10.

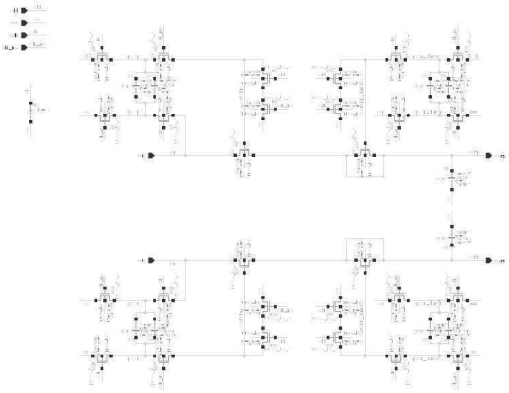

Figure 10: Transistor Level Implementation of Sampling Network.

The maximum input frequency of ADC is limited by the 3 dB frequency of sampling switch in TnH circuit. The 3 dB frequency of bootstrap switch and hold capacitor during the track mode is given by [18]:

$$f3dB = \frac{1}{2\pi\tau}$$

where

T is time constant and given by ד = Ron(CH + CP),

Ron is the on-resistance of sampling switch.CH and CP are the hold capacitance and parasitic capacitance respectively.

D. Output Buffer

The PMOS SF was used to drive the input capacitance of the amplifier array which act as a load for T&H circuit. To reduce the body effect, bulk of PMOS transistor was connected to the source so that the source bulk voltage remains constant. Due to reduced body effect, the linearity of PMOS source follower improved. The BW required for this buffer for its output to settle within half of the sampling period for 'n' bit accuracy, can be calculated by the equation given below :

$$BW > \frac{(n+1).ln(2).2.f_s}{2\pi},$$

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The figure 11. shows Transistor Level Implementation of PMOS Source Follower.The PMOS SF was simulated for the load capacitance of 250 fF and achieved the required bandwidth over all the corners. The gain of PMOS SF was less than unity because of which the output signal swing is smaller than the input signal swing as shown in the transient waveform.

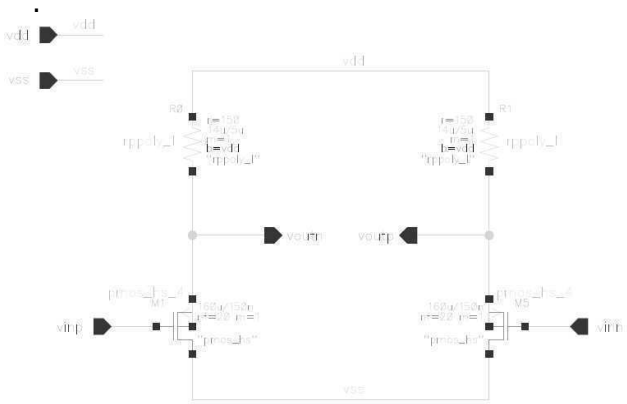

Figure 11: Transistor Level Implementation of PMOS Source Follower.

E .Design of Pre-amplifier

The PA consists of a simple differential pair which was used to amplify the output of differential difference amplifier. The amplification was need to have signal at the output of PA array be much larger than the input-referred comparator offset [13]. Three stages of PA were used for getting large amplification. The transistor level implementation of in figure 12.

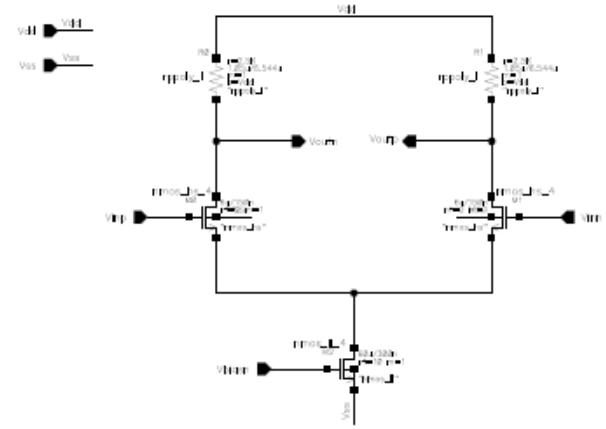

Figure 12: Transistor Level Implementation of Pre-Amplifier.

B. RESULTS

The NMOS source follower and track and hold circuit and PMOS source follower and pre-amplifier circuit blocks are simulated in 180nm CMOS technology using cadence tools and the transient responses are shown in figures 13,14,&15 respectively.

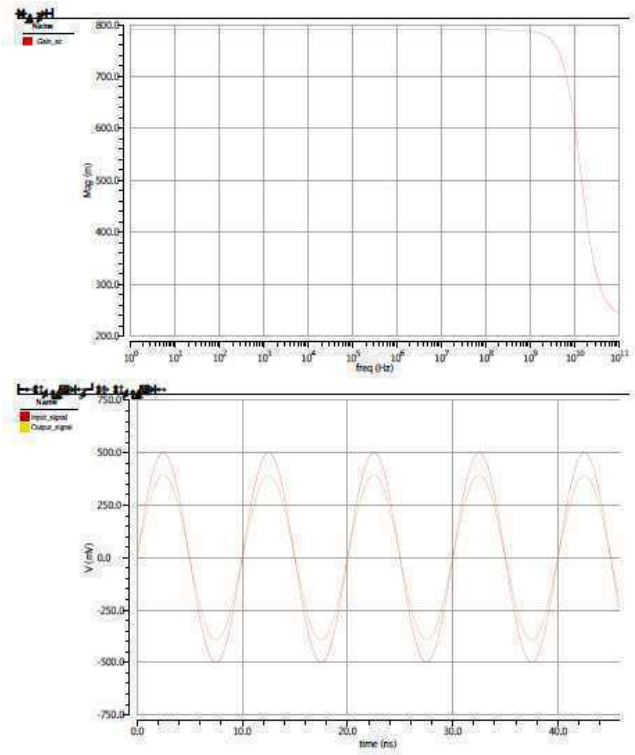

Figure 13: AC And Transient Response of NMOS Source Follower.

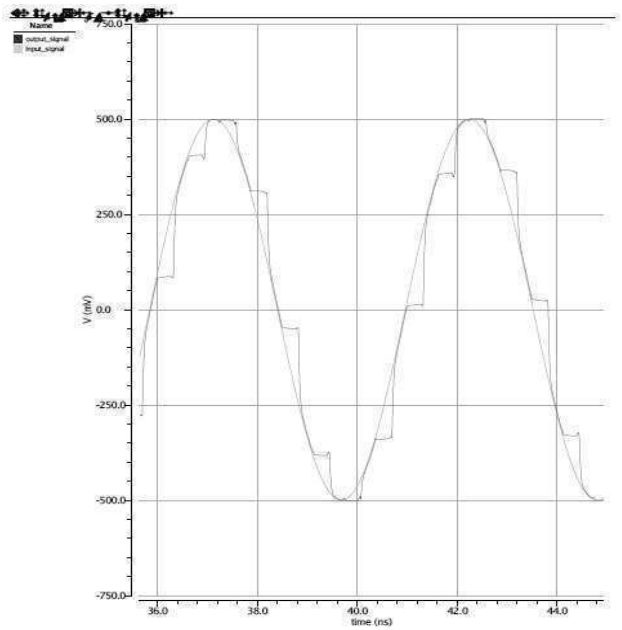

Figure 14: Transient Response of Track And Hold Operation.

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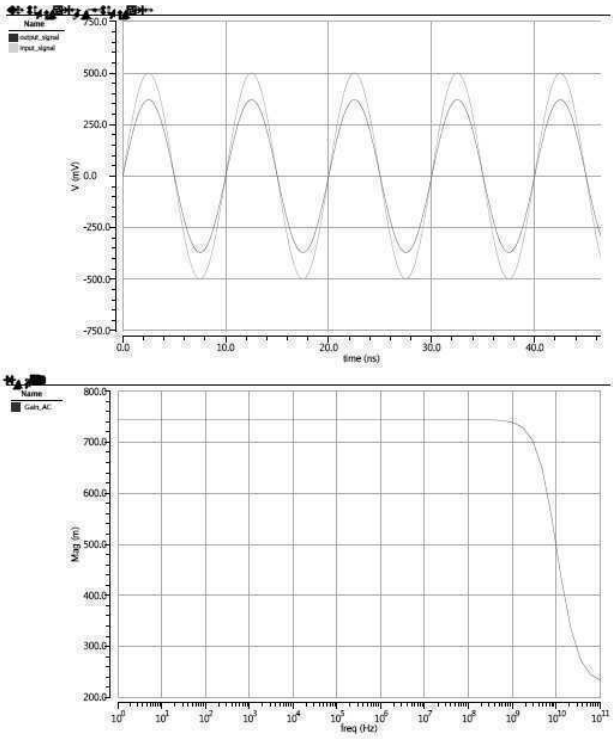

Figure 15: Transient And AC Response of PMOS Source Follower.

The simulation results show that the BW of 4.5 GHz was achieved for all the corners and SNDR of 37.38 dB was achieved. The SNDR could be improved further either by increasing the size of sampling switch or by increasing the hold capacitor value, but this also results in decrease of BW. The power consumed from bootstrap circuit was 27.95 mW, which is mainly because of large currents owing through NMOS SF. Table 1. shows the summary of results obtained from bootstrap TnH circuit with ideal clock. The results are shown for both corner and monte-carlo (MC) analysis. The Table 2. Shows the important parameters of track and hold circuit results.

TABLE 5.1
SIMULATION RESULTS FOR BOOTSTRAP TnH WITH IDEAL CLOCK.

Parameter	Minimum	Nominal	Maximum	StdDev.
BW Input Buffer (Hz)	4.55 G	7.3 G	10.73 G	7.8 M
BW Output Buffer (Hz)	6.83 G	8.87 G	12.23 G	12.86 M
BW SampleNetwork (Hz)	10.49 G	16.51 G	23.34 G	136.5 M
BW Track n Hold (Hz)	4.702 G	7.19 G	10.58 G	16.37 M
Tr.Gain InpBuf (Linear)	732.5 m	823.3 m	860.9 m	1.703 m
Tr.Gain OutBuf (Linear)	634 m	734.3 m	792.6 m	7.03 m
AC Gain InpBuf (Linear)	696 m	789.3 m	831.4 m	158 u
AC Gain OutBuf (Linear)	625.2 m	747.2 m	795 m	496.7 u
SNDR Sample Network (dB)	37.95 dB	60.12 dB	63.22 dB	226.7 m
SNDR PMOS SF (dB)	37.38 dB	55.53 dB	55.53 dB	206.6 m
Output Common Mode (V)	945 m	1.299	1.51	970.8 u
Power (W)	18.5 m	27.95 m	36.89 m	29.63 u

TABLE II
PARAMETERS OF TRACK AND HOLD CIRCUIT

Parameter	Bootstrap TnH
Bandwidth(Hz)	4.702 G
SNDR(dB)	37.38 dB
Power Consumption (W)	27.95m
Output Common Mode	1.3

The figure 16 and Table 3 shows the results of PA over corners and mismatches. Simulation results for PA shows that the gain greater than two was achieved over all the corners. The BW was simulated 1 dB low for the PA stage and minimum value obtained was 1.417 GHz with 25 fF load which is higher than the requirement. The offset for PA stage was high because of the small size of transistors. The transistor sizes for PA were kept smaller to avoid large load for preceding difference amplifier stage.

TABLE III
SIMULATION RESULTS FOR PRE-AMPLIFIER.

Parameter	Minimum	Nominal	Maximum	StdDev.
Bandwidth (Hz)	1.417 G	1.703 G	2.053 G	10.87 M
AC Gain (linear)	2.282	3.177	4.117	80.14 m
Tr. Gain (linear)	1.4	1.694	1.994	67.63 m
Input Offset (V)	0	0	0	9.894 m
Output Offset (V)	0	0	0	31.38 m
Output CM (V)	1.208	1.479	1.62	16.7 m
Power (W)	1.301 m	1.617 m	2.285 m	43.81 u

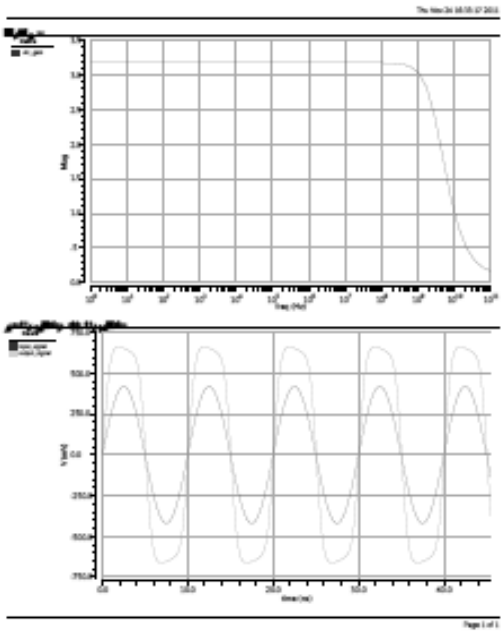

Figure 16: Transient And AC response of Pre-Amplifier.

Figure 17 shows the layout design of bootstrap Sampling Network. Antennas from digital library were included for layout to avoid the error which was occurring due to the

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small gate area of transistor. This happened because some transistors were connected directly to power and their gate area was very small as compared to the area covered by power rails. Again RC extraction was used to check for parasitic capacitances and resistance. The table 4 shows the comparison between schematic and layout of sampling network.

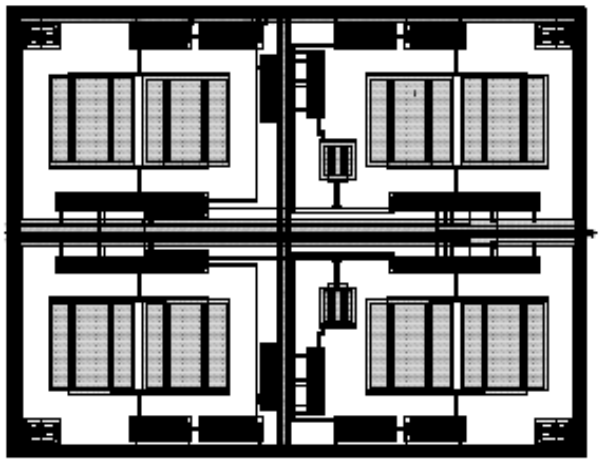

Figure 17: Layout of bootstrap sampling network.

TABLE IV
COMPARISON OF SCHEMATIC AND LAYOUT RESULTS FOR SAMPLING NETWORK.

Parameter	Schematic	Layout
Bandwidth (Hz)	17.47 G	10.71 G
SNDR (dB)	71.58 dB	57.45 dB
Power Consumption (W)	0	379.3 f
Output Common Mode (V)	428.3 m	399.1 m

CONCLUSIONS

A high speed flash ADC is presented for the AFE of receiver circuit. The flash architecture is chosen for its simplicity and fast data conversion rate. Track and hold circuit is implemented for improving the dynamic behaviour of the ADC. The bootstrapped architecture for T&H circuit a implemented in transistor level 180nm CMOS technology. The clock boosting circuit is used for bootstrap T&H circuit to reduce the non-linear effect caused by the Ron of switch and dummy switch is used to reduce clock feed-through and charge injection problem. Linearity of almost six bits is achieved from this circuit.

Preamplifiers are employed in front of comparators to reduce their large dynamic offsets. PAs also have offsets but smaller as compared to the large offsets of comparators. Averaging technique is presented to reduce the PA offset. To solve problems at the edges of amplifier array, a proper termination technique is also discussed. The effect of averaging is limited by the use of interpolation which is used to reduce the number of PAs in first stage in order to reduce load for the TnH circuit.

REFERENCES

[1] Peter C. S. Scholtens, Member, IEEE, and Maarten Vertregt, Member, IEEE, "*A 6-b 1.6-Gsample/s Flash ADC in 0.18-um CMOS Using Averaging Termination*," IEEE Journal of Solid-State Circuits, VOL. 37,NO. 12, DECEMBER 2002.

[2] Robert C. Taft, Senior Member, IEEE, Chris A. Menkus, Member,IEEE, Maria Rosaria Tursi, Member, IEEE, Ols Hidri, Member, IEEE,and Valerie Pons, "*A 1.8-V 1.6-GSample/s 8-b Self-Calibrating Folding ADC With 7.26 ENOB at Nyquist Frequency* ," IEEE Journal ofSolid-State Circuits, VOL. 39, NO. 12, DECEMBER 2004.

[3] Xicheng Jiang and Mau-Chung Frank Chang, Fellow, IEEE, "A *1-GHz Signal Bandwidth 6-bit CMOS ADC With Power-E_cient Averaging*," IEEE Journal of Solid-State Circuits, VOL. 40, NO. 2, FEBRUARY 2005.

[4] I.-H. Wang, J.-L. Lin and S.-I. Liu, "*5-bit, 10GSamples/s track-and-hold circuit with input feedthrough cancellation*," Electronics Letters 13th April 2006 Vol. 42 No. 8.

[5] Olli Viitala, Saska Lindfors and Kari Halonen Electronic Circuit Design Laboratory, Helsinki University of Technology, P.O.Box 3000, FIN-02015 TKK Finland , "*A 5-bit 1-GS/s Flash-ADC in 0.13-um CMOS Using Active Interpolation ,".*

[6] Hseyin Din, Student Member, IEEE, and Phillip E. Allen, Fellow, IEEE,"*A 1.2 GSample/s Double-Switching CMOS THA With -62 dB THD*," IEEE Journal of Solid-State Circuits, VOL. 44, NO. 3, MARCH 2009.

[7] Robert C. Taft, Senior Member, IEEE, Pier Andrea Francese, Member, IEEE, Maria Rosaria Tursi, Member, IEEE, Ols Hidri, Member, IEEE, Alan MacKenzie, Tobias Hhn, Philipp Schmitz, Heinz Werker, Member, IEEE, and Andrew Glenny, "*A 1.8 V 1.0 GS/s 10b Self-Calibrating Uni_ed-Folding-Interpolating ADC With 9.1 ENOB at Nyquist Frequency*," IEEE Journal of Solid-State Circuits, VOL. 44, NO. 12, DECEMBER 2009.

[8] Ying-Zu Lin, Cheng-Wu Lin, and Soon-Jyh Chang, "*A 5-bit 3.2-GS/s Flash ADC With a Digital O_set Calibration Scheme*," IEEE Transactions On Very Large Scale Integration (VLSI) Systems, VOL. 18, NO. 3, MARCH 2010.

[9] N. Stefanou, S.R. Sonkusale, "*Achieving Higher Dynamic Range in Flash A/D Converters*,".

[10] Mikael Gustavsson, J. Jacob Wikner and Nianxiong Nick Tan, "*CMOS Data Converters for Communications*," ISBN 0-306-47305-4.

[11] R. Jacob Baker, "*CMOS Circuit Design, Layout and Simulation, Third Edition*," ISBN 978-0-470-881323.

[12] Kevin Kattmann and Je_ Barrow, Analog Devices Computer Labs Division, Greensboro, NC, "*A Technique for Reducing Differential Non-Linearity Errors in Flash A/D Converters*," ISBN 0-07-118839-8.

[13] Pedro M. Figueiredo and Joao C. Vital, "*Offset Reduction Techniques in High Speed Analog to Digital Converters*," ISBN 978-1-4020-9715-7.

[14] Gang Chen, Yifei Luo, Allen Drake, Kuan Zhou Electrical and Computer Engineering University of New Hampshire Durham, New Hampshire , "*A 5-Bit 10GS/s 65nm Flash ADC with Feedthrough Cancellation Track-and-Hold Circuit,".*

[15] Wen-Lung Huang, Sing-Rong Li, and Yu-Wei Lin, "*A Low Power 6-b ADC with 800-Ms/s Conversion Rate*," Report for EECS598 ADC Final Project, Dec., 2002.

DOI:10.32377/cvrjst0511

[16] Mohammad Hekmat and Vikram Garg, "*Design and Analysis of a Source-Follower Track-and-Hold Circuit,"* EE315 (VLSI DATA CONVERSION CIRCUITS) Project Report JUNE 2006.

[17] Manoj Kumar and Ganesh Kumar, "*Optimization techniques for source follower based track and hold circuit for high speed wireless communication*," International Journal of VLSI design and Communication Systems (VLSICS) Vol.2, No.1, March 2011.

[18] Lei Wang, Junyan Ren, Wenjing Yin, Tingqian Chen and Jun Xu, "*A High-Speed High-Resolution Low-Distortion CMOS Bootstrapped Switch*," ASIC and System State Key Laboratory Fudan University Shanghai,China.

DOI:10.32377/cvrjst0511