Design and Implementation of Instrumentation Amplifier for EEG in 180nm CMOS technology

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***Abstract*— The EEG is Electro Encephalo Gram that which gives the electrical activity of the brain. Analysis of the electrical activity is very important to diagnose neurological problems. But, the problem generally involved is that the EEG signals have very low amplitude and these very low amplitude signals cannot drive displays for further analysis. So, we require to use amplifiers. Instrumentation amplifier is widely used for such applications because they give high gain. For designing the instrumentation amplifier, we have to first design the operational amplifier and this is further used to design the instrumentation amplifier. The 180nm CMOS technology has been used for the Implementation of this amplifier. It gives a hiah gain of 111 dB an low power dissipation of 16mW.**

***Index terms*—EEG, Instrumentation amplifier, Op-Amp, CMOs.**

I. INTRODUCTION

Measurement of brain signals is necessary to diagnose neurological disorders and other brain disorders. To diagnose, the brain signals are taken during sleep and other conditions of the patient. With the obtained results, the doctors conclude the disease and continue with the treatment. The Electrodes are placed on the scalp of the patient and these electrodes give an electrical output whose amplitude is in terms of micro volts. A protection circuit is used to avoid damage to the setup. These electrical signals are further amplified by an instrumentation amplifier and filtered and sent to a display device. The EEG is also vital for human machine interface that can be used for non-verbal communication. Electrodes are placed in specific locations of the scalp.

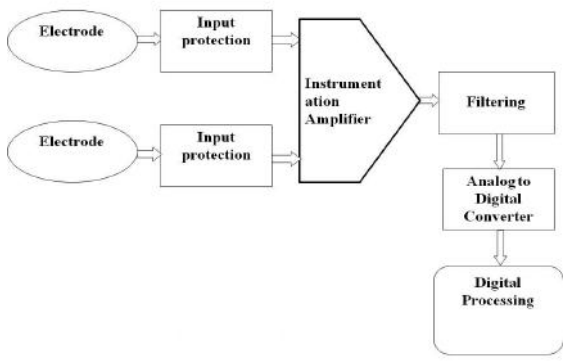

Figure.1: EEG signal chain.

When we look at the block diagram in Figure.1 , we understand the complete operation of the instrument. The electrodes collect the signal from the brain and given to amplifier and then filtered. The amplification occurs first because the brain waves have too low amplitude and frequency and it is very important for the signal to strengthen to separate artefacts and the EEG through filtering. There are many artefacts that cause distortions in the brain waves, they could be both technical and patient related. We can see even if a small part of the body is moved, even when they eye is moved, could be even due to sweating and even due to too much electrode jelly and low battery. We have filters like high pass, low pass, notch filters that allow only the brain waves. These filtered waves are then converted into digital signal and processed for further analysis.

From the above block diagram of an EEG it is evident that we require an amplifier for further analysis of the brain waves. It is also evident from the clinical applications of an EEG that measuring brain waves is vital to analyze the brain and conclude on diseases related to the brain. The instrumentation amplifier used has to be designed so as to meet the criteria of an EEG with following specifications.

Table 1. Specifications of Instrumenation Amplifier.

PARAMETER	VALUE
Input impedance	10Mohm
CMRR	>80dB at 50/60Hz
Noise	<2μV peak to peak
Bandwidth	0.1 to 95Hz, -3dB
Gain	3000
Impedance checking	Built in, 10Hz sine wave. Range 1kilohm to 50kilohms, 10%
Samples rate	200/400 samples/sec/channel, simultaneous sampling
Input signal range	2mV peak to peak full scale
DC input voltage range	±450mV max
Slew rate	10V/μs

II. DESIGN OF INSTRUMENTATION AMPLIFIERS

The instrumentation amplifier is similar to the differential amplifier that has input buffer amplifiers fitted to remove the need for extra circuitry required for impedance matching making these amplifiers useful for measurement and test equipment is shown in figure 2.

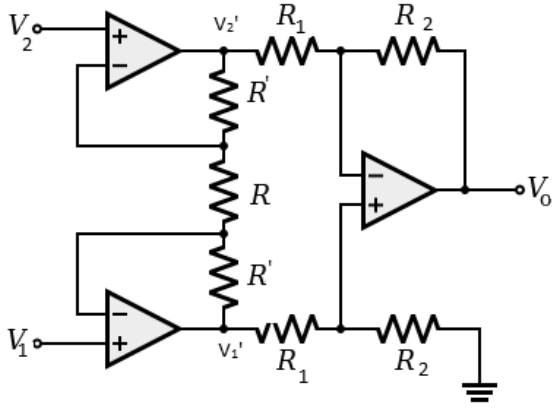

Figure 2: Instrumentation amplifier

The instrumentation amplifiers can be built with individual op-amps and precision resistors, but are also available in integrated circuit form from several manufacturers (including Texas Instruments, National Semiconductor, Analog Devices, Linear Technology and Maxim Integrated Products). An IC instrumentation amplifier typically contains closely matched laser-trimmed resistors, and therefore offers excellent common-mode rejection. Examples include AD8221, MAX4194, LT1167 and INA128.

Instrumentation amplifiers offer a unique combination of differential inputs, high input impedance, and excellent precision and noise specifications. Using both zero-drift and traditional topologies, Linear Technology's instrumentation amplifiers feature high precision, low drift and excellent PSRR and CMRR. Like all Linear Technology devices, our instrumentation amplifiers are unique in offering fully specified, tested and guaranteed performance for key parameters over the full operating temperature range, enabling high reliability designs.

Instrumentation amplifier is the front end component of every measuring instrument which improves the signal to noise ratio of the input electrical signal from the transducer. It uses the fact the noise is common to the both output terminals of a transducer across which the output is measured and sent to measuring instrument. Advantages of instrumentation amplifier High gain, the gain of the instrumentation amplifier can be varied by just varying resistors in input circuit without affecting the resistors in difference amplifier circuit, high CMMR, High input resistance.

To design an instrumentation amplifier an operational amplifier has to be designed first. We generally use a two stage operational amplifier since a single stage amplifier will have low gain. The proposed instrumentation amplifier was designed using 180nm CMOS technology. The technology provides six levels of metal (copper and aluminum) with Vth values of 0.48 V and -0.4 3 V for the NMOS and PMOS transistors, respectively. An extension to that technology provides optional passive devices for analog circuit design, including MIM (Metal-Insulator-Metal) and thick oxide MOS capacitors.

To understand the design of the instrumentation amplifier, we first consider a differential amplifier as shown in figure3.

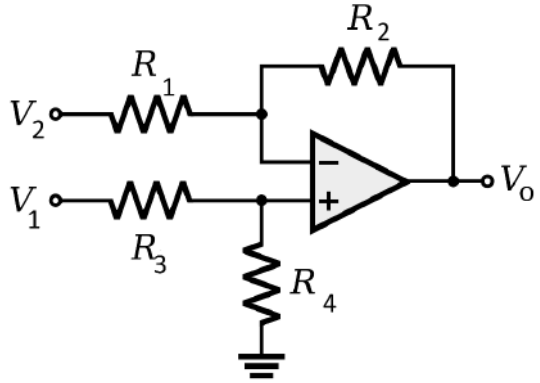

Figure 3: Differential amplifier

We use the super position principle and using that, when V_2 is applied alone:

$$V01 = -\frac{R2}{R1}.V2$$

When V_1 is applied alone:

$$V02 = \left(1+\frac{R2}{R1}\right).V' = \left(1+\frac{R2}{R1}\right).\left(\frac{R4}{R3+R4}\right).V1$$

Where,

$$V' = \frac{R4}{R3+R4}.V1$$

The output voltage V_o can be obtained as follows:

$$Vo = V01 + V02$$

$$Vo = -\frac{R2}{R1}.V2 + \left(1+\frac{R2}{R1}\right).\left(\frac{1}{1+\frac{R3}{R4}}\right).V1$$

Taking R2/R1 common, we get:

$$Vo = \frac{R2}{R1}.\left[-V2 + \left(\frac{R1}{R2}+1\right).\left(\frac{1}{1+\frac{R3}{R4}}\right).V1\right]$$

If R1/R2=R3/R4 then we have:

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$$Vo = \frac{R2}{R1}\left[-V2 + \left[\left(\frac{R1}{R2}+1\right).\left(\frac{1}{1+\frac{R1}{R2}}\right).V1\right]\right]$$

Simplifying,

$$Vo = \frac{R2}{R1}.[-V2 + V1]$$

Rearranging the terms,

$$Vo = \frac{R2}{R1}.[V1 - V2]$$

To avoid the problems of input impedance we add buffer circuits to the differential amplifier and it appears as shown in Figure 2. It represents a three op-amp instrumentation amplifier where the first two operational amplifiers act as input buffers and the third amplifier is responsible for the high gain [1].

Initially let us assume $V_1=V_2$ (common mode) then I=0, $V_2'=V_2$ and $V_1'=V_1$. If $V_1 \neq V_2$ then $V'_2-V'_1 > V_2-V_1$.

The differential amplifier output is given as:

$$Vo = \frac{R2}{R1}V2' + \left[\left(1+\frac{R2}{R1}\right).\left(\frac{R2}{R1+R2}\right).V1'\right]$$

Taking R_2/R_1 common in the above equation. We have:

$$Vo = \frac{R2}{R1}\left[-V2' + \left[\left(\frac{R1}{R2}+1\right).\left(\frac{1}{1+\frac{R1}{R2}}\right).V1'\right]\right]$$

$$Vo = \frac{R2}{R1}(V1' - V2')$$

From the circuit we get,

$$I = \frac{V1 - V2}{R}$$

Also,

$$V1' = IR' + V1$$

And,

$$V2' = -IR' + V2$$

Substituting the value of I in V'_1 and V'_2 we get:

$$V1' = \left(\frac{V1 - V2}{R}\right).R' + V1$$

$$V2' = -\left(\frac{V1 - V2}{R}\right).R' + V2$$

Using the above in the output voltage equation.
We obtain:

$$Vo = \frac{R2}{R1}.\left[\frac{V1 - V2}{R}.R' + V1 + \frac{V1 - V2}{R}.R' - V2\right]$$

Simplifying, we get:

$$Vo = \frac{R2}{R1}.\left[2.\frac{V1 - V2}{R}.R' + (V1 - V2)\right]$$

$$Vo = \frac{R2}{R1}.\left(1 + \frac{2.R'}{R}\right).(V1 - V2)$$

III. DESIGN OF AN OPERATIONAL AMPLIFIER

This section describes the design of operational amplifier which is basic block in the instrumentation amplifier. The figure.4 represents the transistor level diagram of two stage operational amplifier.

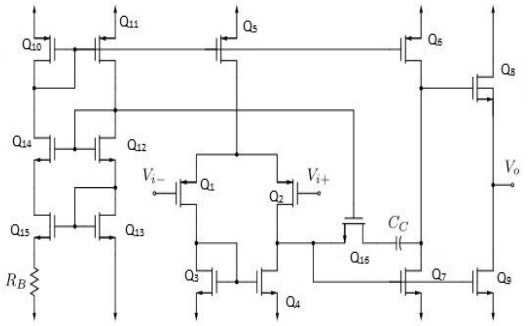

Figure.4: CMOS realization of a two-stage amplifier

A) Operational Amplifier Gain:

For low frequency applications, the overall gain is one of the most critical parameters. The gain of the first stage can be derived as follows:

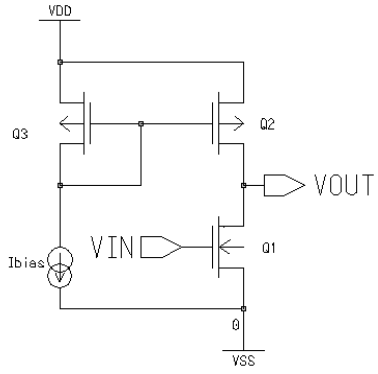

Figure.5: Common-source amplifier with a current mirror active load.

A small signal equivalent circuit for low frequency analysis for the common source amplifier is as follows:

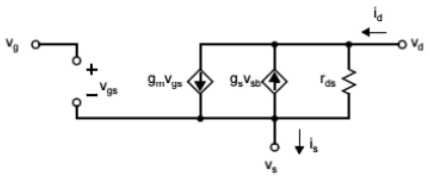

Figure.6: Small signal equivalent circuit for the common-source amplifier.

V_{in} and R_{in} are the Thevenin equivalent of the input source. It is assumed that the bias voltages are such that both the transistors are in active region. The output resistance, R_2, is made up of the parallel combination of the drain-to-source resistance of Q_1, that is, r_{ds1}, and the drain-to-source resistance of Q_2, that is r_{ds} [2].

Using small-signal analysis, we have $V_{gs1}=V_{in}$ an we have,

$$Av = \frac{Vout}{Vin} = -gm1.R2 = -r_{ds1} \| r_{ds2})$$

gm1 is given by,

$$gm = \frac{\partial Id}{\partial Vgs}$$

I_d in the active region is given by,

$$Id = \frac{\mu nCox}{2}\left(\frac{W}{L}\right)(Vgs - Vtn)$$

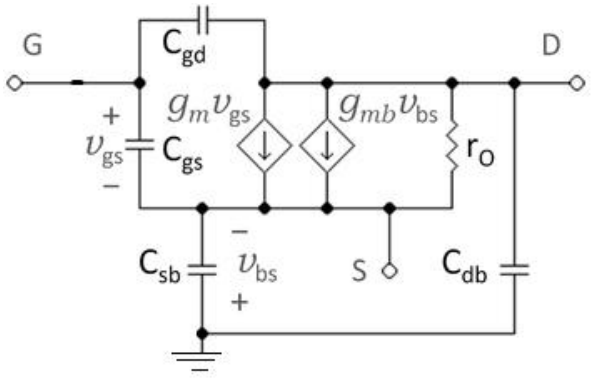

Figure 7: Small signal model for a MOS transistor in active region.

$$gm = \frac{\partial Id}{\partial Vgs} = \mu nCox\frac{W}{L}(Vgs - Vtn) = \mu nCox\frac{W}{L}Veff$$

Equivalently, we get:

$$gm = \mu nCox\frac{W}{L}Veff$$

Where, the effective gate-to-source voltage, Veff is defined as,

$$Veff = Vgs - Vtn$$

We now understand that the trans-conductance is directly proportional to Veff. It is desirable to express g_m in terms of I_D rather than Vgs, so we have:

$$Vgs = Vtn + \sqrt{\frac{2.Id}{\mu nCox(W/L)}}$$

From the above, we get:

$$Veff = Vgs - Vtn = \sqrt{\frac{2.Id}{\mu nCox(W/L)}}$$

Substituting Veff in gm and simplifying, we get:

$$gm = \sqrt{2.\mu n.Cox.\frac{W}{L}.Id}$$

Thus, the transistor trans-conductance is proportional to for a MOS transistor. Therefore, gm1 in gain of the first stage is given by,

$$gm1 = \sqrt{2.\mu n.Cox.\left(\frac{W}{L}\right).Id1} = \sqrt{2.\mu n.Cox.\left(\frac{W}{L}\right).\frac{Ibias}{2}}$$

Also, an approximation to the finite output impedance, r_{ds1}, of transistor Q1 is given by,

$$rds1 \approx \alpha\frac{Li}{Idi}\sqrt{Vdgi + Vti}$$

Where, α is a technology-dependent parameter of around 5 x 10^6.The second gain stage is simply a common-source gain stage with a p-channel active load Q6. Its gain is given as follows:

$$Av2 = -gm7(rds6||rds7)$$

The third stage is a common-drain buffer stage. This stage is often called a source follower, because the source voltage follows the gate voltage of Q8, except for a level shift. The gain of this source-follower is given by,

$$Av3 \approx \frac{gm8}{GL + gm8 + gds8 + gds9}$$

Where, G_L is the load conductance being driven by the buffer stage. When it is not possible to tie the substrate of Q8 to its source, as is the case when an n-well process is used, then the gain of the buffer stage is given by,

$$Av3 \approx \frac{gm8}{GL + gm8 + gs8 + gds8 + gds9}$$

Where, g_s is a body-effect conductance and is given by,

$$gs = \frac{gm.\gamma}{2.\sqrt{Vsb + 2\emptyset F}}$$

Voltage VSB is the source-to-substrate voltage and γ is the body-effect constant and 2□F is twice the difference between Fermi level in the bulk and the Fermi level of intrinsic silicon. Thus gs is around gm/5.

B) Frequency Response

The frequency response of the two-stage operational amplifier at frequencies where the compensation capacitor, C_C, has caused the magnitude of the gain to begin to decrease. There are some assumptions considered, first, all the capacitors are ignored except the compensation capacitor. Second, we assume that the transistor isn't

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present. This transistor operates as a resistor, which is included to achieve lead compensation and it has an effect only around the unity-gain frequency of the operational amplifier [3].

The second stage introduces a capacitive load on the first stage due to the compensation capacitor, C_C. using Miller's theorem, the equivalent capacitance C_{eq} at node V_1 is given by:

$$Ceq = Cc(1 + A2) \approx Cc.A2$$

The gain in the first stage can be found using the small-signal model, and it results in:

$$A1 = \frac{V1}{Vin} = -gm1.Zout1$$

Where,

$$Zout1 = rds2||rds4||\frac{1}{s.Ceq}$$

For mid-band frequencies, the impedance of Ceq dominates, and the above equation can be written as follows:

$$Zout1 \cong \frac{1}{s.Ceq} \cong \frac{1}{s.Cc.A2}$$

For the overall gain, we have:

$$Av(s) \cong \frac{Vout}{Vin} = A3.A2.A1 \cong A3.A2.\frac{gm1}{s.Cc.A2}$$

If we assume A3=1, then the overall gain simplifies to:

$$Av(s) = \frac{gm1}{s.Cc}$$

Using this equation the approximation of unity-gain frequency can be done. To find unity-gain frequency, ωta, we set, |Av (jωta)|=1. Thus we obtain the following relation:

$$\omega ta = \frac{gm1}{Cc}$$

C) Slew Rate

Slew rate is one of the important high frequency parameter of an operational amplifier. The slew rate is the maximum rate at which the output changes when input signals are large. When the operational amplifier is limited by its slew rate because a large input signal is present, all of the bias current of Q5 goes into either Q1 or Q2, depending on whether Vin is negative or positive. When Vin is a large positive voltage, the bias current, ID5, goes entirely through Q1 and also goes into current mirror pair, Q3, Q4. Thus, the current coming out of the compensation capacitor, CC, is simply equal to ID5 since Q2 is off. When Vin is a large negative voltage, the current mirror pair, Q3 and Q4 is shut off because Q1 is off, and now the bias current, ID5, goes directly into CC. in either case, the maximum current entering or leaving CC is simply the total bias current[4], ID5.

Slew rate is the maximum rate that V2 can change. Recalling that Vout≈V2, we have:

$$Slew\ rate = \frac{dVout}{dt} = \frac{ICc|max}{Cc} = \frac{Id5}{Cc}$$

Where, we used the charge equation q=CV, which leads to I=dq/dt=C(dV/dt). Since ID5=ID1, we can rewrite slew rate as follows:

$$Slew\ rate = \frac{2.Id1}{Cc}$$

Where ID1 is the original bias current of Q1 with no signals present. Also, using the unity-gain frequency equation, we get CC=gm1/ωta, substituting this in the above equation[5]. We get,

$$Slew\ rate = \frac{2.Id1.\omega ta}{gm1}$$

Recalling the value of g_{m1},

$$gm1 = \sqrt{2.\mu n.Cox.\left(\frac{W}{L}\right).Id1}$$

Using this in the slew rate equation we have:

$$Slew\ rate = \frac{2.Id1}{\sqrt{2.\mu p.Cox.(W/L).Id1}}.\omega ta = Veff.\omega ta$$

Where,

$$Veff = \sqrt{\frac{2.Id1}{\mu nCox(W/L)}}$$

D) Systematic Offset Voltage

When designing the two-stage operational amplifier, it is possible that the design will have an inherent (or systematic) input-offset voltage. To ensure that no systematic input-offset voltage exists, when the differential input voltage is zero (i.e., when Vin+=Vin-), the output voltage of the first stage, VGS7 , should be that which is required to make ID7 equal to its bias current, ID6.

VGS7 is given by,

$$Vgs7 = \sqrt{\frac{2.Id6}{\mu n.Cox.(W/L)7}} + Vtn$$

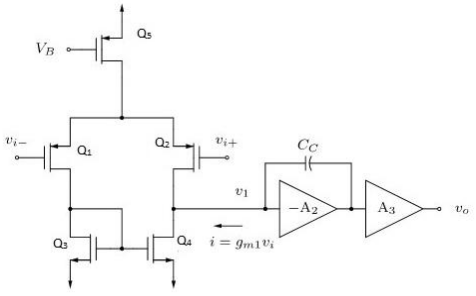

Figure.8: Input and gain stages of the two-stage op-amp.

When the differential input voltage is zero, the drain voltages of both Q3 and Q4 are equal by arguments of symmetry[6]. Therefore, the output voltage of the first stage, VGS7, is given by:

$$V_{GS7}=V_{DS3}=V_{GS4}$$

This value is the voltage necessary to cause ID7 to be equal to ID6. If this is not achieved, then the output of the second stage (with Q6, Q7) would clip at either the negative or positive rail since this stage has such a high gain[7]. However the gate-to-source voltage of Q4 is given as follows:

$$Vgs4 = \sqrt{\frac{2.Id4}{\mu n.Cox.(W/L)4}} + Vtn$$

Equating V_{GS7} and V_{GS4}, we get:

$$\sqrt{\frac{2.Id4}{\mu n.Cox.(W/L)4}} = \sqrt{\frac{2.Id6}{\mu n.Cox.(W/L)7}}$$

Simplifying, we have:

$$\frac{Id4}{(W/L)4} = \frac{Id6}{(W/L)7}$$

This equality, when the current density of Q_4 is equal to the current density of Q_7, guarantees that they both have the same effective gate-source voltages.
Since,

$$\frac{Id6}{Id4} = \frac{Id6}{Id5/2} = \frac{(W/L)6}{(W/L)5/2}$$

The necessary condition to ensure that no input-offset voltage is present it,

$$\frac{(W/L)7}{(W/L)4} = 2\frac{(W/L)6}{(W/L)5}$$

Using the above design equations, the width and length of the transistors have been found for the values assumed R_b=4.499KΩ and C_C=1.2pF.

Table .2: The W/L ratios of transistors in op-amp.

TRANSISTOR	WIDTH	LENGTH
Q_1	200µm	600nm
Q_2	200µm	600nm
Q_3	32µm	750nm
Q_4	32µm	750nm
Q_5	75µm	600nm
Q_6	312.52µm	600nm
Q_7	266.67µm	750nm
Q_{10}	11.66µm	1µm
Q_{11}	11.66µm	1µm
Q_{12}	3µm	1µm
Q_{13}	3µm	1µm
Q_{14}	3µm	1µm
Q_{15}	12µm	1µm
Q_{16}	18.905µm	700nm

IV. IMPLEMENTATION OF INSTRUMENTATION AMPLIFIER

An integrated chip shortly called as an IC can be designed in two ways. One is called Full-custom design and other the semi-custom design. The choice of particular design style depends on the factors which are required. Full costumed IC's consists of making the IC from the scratch. The basic building block of any chip is an interconnection of transistors and in full custom design each and every transistor is manually designed. This account for so much of time but advantage comes to be that circuit can be made for desired performance. Whereas in semi costumed IC's the design is mapped to pre fabricated gates whose technology is fixed [9].

The Figure.9 and Figure.10 represents the CMOS transistor level diagrams of two stage operational amplifier and instrumentation amplifier , respectively which are implemented in 180nm CMOS technology by CADENCE tools.

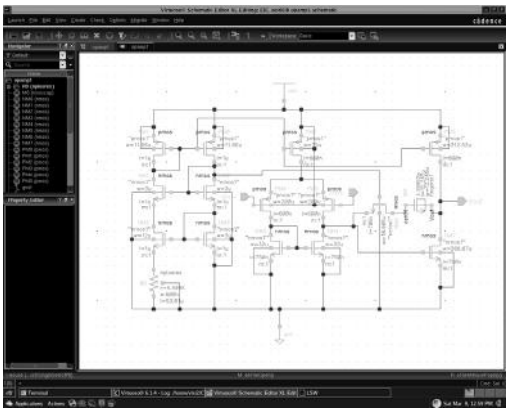

Figure.9: Schematic of operational amplifier

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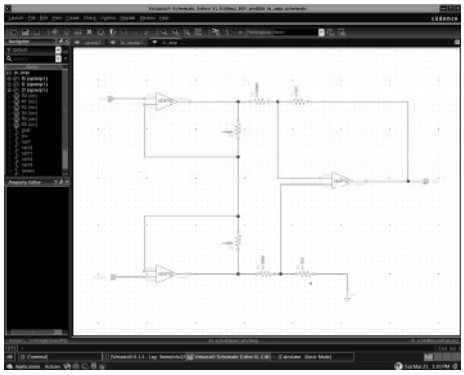

Figure.10: Schematic of instrumentation amplifier

V. SIMULATION RESULTS

In this section, the test bench set up for the instrumentation amplifier and simulation results are shown.

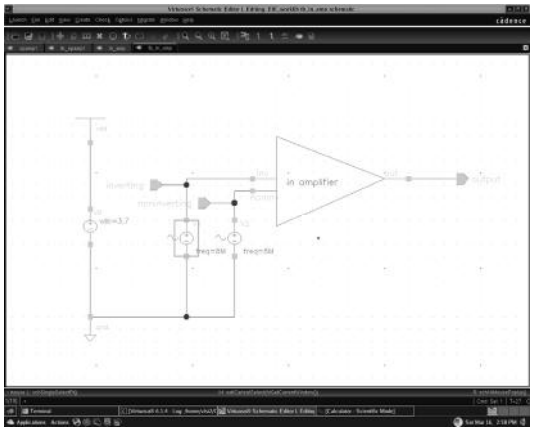

Figure.11: Test bench of instrumentation amplifier

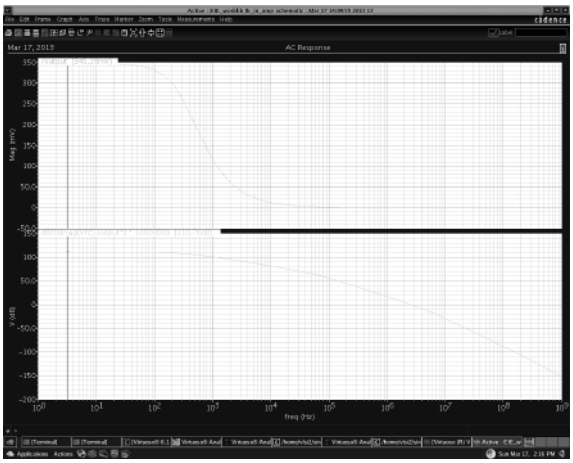

Figure.12: Simulation result of instrumentation amplifier

The above figure shows the gain of an instrumentation amplifier, which is around 111dB. The gain is obtained using AC analysis i.e. frequency response of the circuit. We also use the on screen calculator for the calculation of gain [8].The same instrumentation amplifier test bench is used to find the CMRR. A dc supply to this is 1.8V.

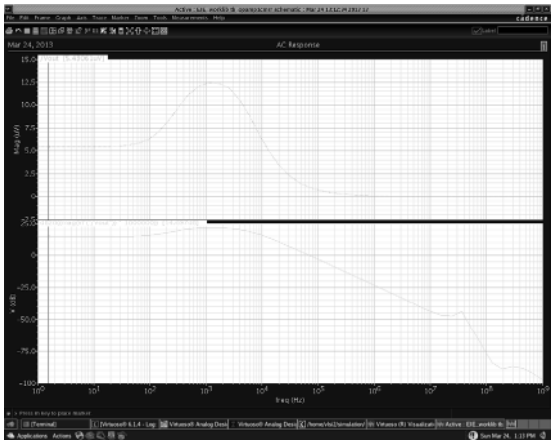

Figure13: CMRR response of an instrumentation amplifier.

The AC analysis is done for the circuit used earlier (test bench), the graph is obtained i.e. the frequency response and the CMRR is obtained by using the on screen calculator. The value of CMRR is around 15dB.

We know that offset is that voltage seen across the output terminals when no input is applied. So to find out the offset voltage, we give zero input and observe the output. The same has been implemented in a circuit form.

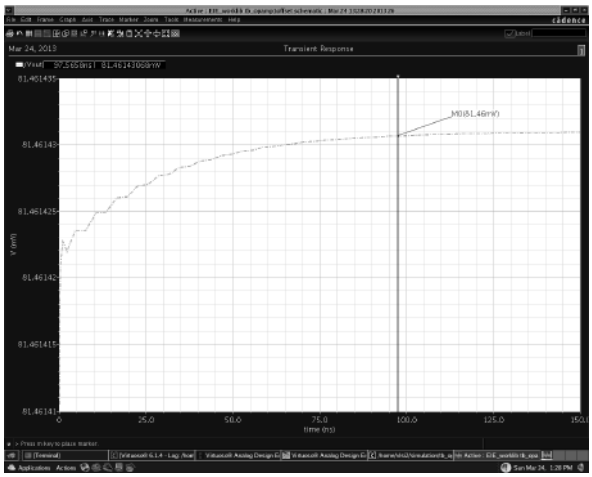

Figure.14: Offset voltage of an instrumentation amplifier

The response for the earlier circuit to find the offset voltage. We perform the transient analysis and find out the offset voltage. For the instrumentation amplifier it was found to be around 81.5mV, comparatively less than that of the operational amplifier.

To find PSRR we give both AC and dc supply to the entire test bench. One input of the instrumentation amplifier is supplied with dc voltage and the other is fed to the output pin.

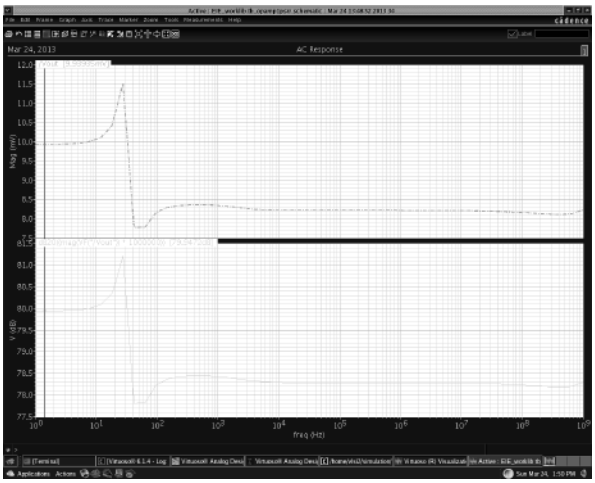

Figure.15: PSRR response of instrumentation amplifier

Using the PSRR test bench and performing the AC analysis i.e. finding the frequency response we obtain a plot. Using the onscreen calculator we can find out the ratio which was found to be around 80dB. The on screen calculator is used to find out the power dissipation and it is found to be around 5mW for the instrumentation amplifier.

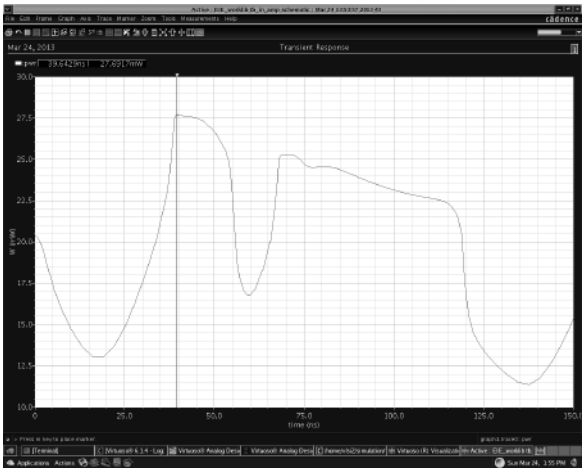

Figure.16: Power dissipation of an instrumentation amplifier

The following table represents the important parameters of Instrumentation amplifier and two stage operational amplifier, which are calculated from the simulation results.

Table.3: Calculated parameters

PARAMETER	OPERATIONAL AMPLIFIER	INSTRUMENTATION AMPLIFIER
Gain	82dB	111dB
CMRR	67dB	15dB
Offset	683.91mV	79.94mV
PSRR	79.99dB	79.94dB
Power dissipation	5.05mW	15.34mW

VI. CONCLUSIONS

The instrumentation amplifier successfully designed and achieving a gain of 110dB. A two stage operational amplifier has been used to implement the instrumentation amplifier. And the individual gain of the operational amplifier is 81dB. Since operational amplifier is the most basic amplifier used in signal conditioning circuits and this can be used for different applications. We have 180nm CMOS technology to implement it but, we can use further more advanced technologies like the 90nm or 45nm CMOS technology where the chip size is reduced thus power consumption is also reduced.

This instrumentation amplifier can be used for all the applications where the signals have very low amplitude. Usually, low amplitude signals are bio-signals and this instrumentation amplifier can be used to amplify bio-signals.

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