A Simple Power Balancing Algorithm to Improve the Source Utilization Factor for a Multilevel Inverter for Microgrid and Hybrid Electric Vehicle Applications

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Abstract **—With the promising growth of micro grids and HEVs, the final power quality delivered by an inverter and longevity of the input DC voltage sources has become a subject matter of concern. The conventional multilevel inverter topologies give AC voltages with higher Total Harmonic Distortion (THD) leading to a lower power quality. Also, the unequal usage of the input DC sources leads to a poor Power Source Utilization Factor (PSUF). This paper presents the 3 phase H-Bridge inverter topology with improved line to line power quality features. The proposition of improving Power Source Utilization Factor (PSUF) is achieved by incorporating a novel transposition technique. A comparative study is made to decide the wave shape and minimize the harmonics. The theoretical simulation results and the hardware results for the gate pulses are shown.**

Index terms— **H Bridge Inverter, THD, PSUF, battery balancing algorithm**

I. INTRODUCTION

Various inverters aim to achieve a closer approximation to AC sinusoidal wave by increasing the number of voltage levels. These levels are formed by the utilization of the DC voltage sources and selective sequencing of switches in cascaded mode which tap the source voltage in different proportions to give desired voltage levels at desired time.

There are a number of configurations of multilevel inverters [1] - [4] like voltage-source inverter topologies, including diode-clamped, flying capacitor, and cascaded H-bridge structures. Given the wide range of multilevel inverter topologies, the H-bridged topologies are superior to others as they realize those increased voltage levels for AC approximation levels with lesser hardware[5]-[6].

The paper deals with the inverter architecture, cascading and integrating it to 3 phase, power balancing algorithm and comparison of THDs and PSUFs for different cases has been discussed.

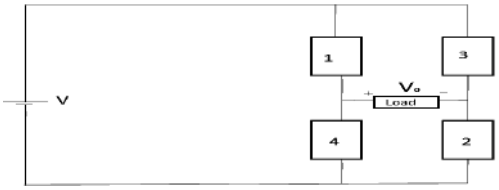

Figure 1. Module of H-Bridge Inverter

II. H - BRIDGE INVERTER

A. H-Bridge Inverters- Architecture

A H-bridge inverter consists of a DC voltage source, 4 switches arranged in a bridge configuration with load connected in between the two arms as shown in the Fig. 1. This is referred to as a module.

B. H Bridge Inverter Operation:

A H-Bridge inverter module powered by a DC voltage source of magnitude V has 3 attainable voltage levels (i.e. +V, 0, -V). These levels are realized using the switching sequence by triggering the gate terminals of the switches desired to be in conduction state. Further it can be observed from Table I. that, at any instant of time, only two switches are ON to give the required voltage level.

The complete voltage appears across the load with V_0 = +V when switches S1 and S2 are turned on. When the switches S3 and S4 are turned on, a total voltage V_0 = –V appears across the load because of the reversal in the current direction. No current passes through the load when all the switches are turned off and V_0= 0.

TABLE-I.

S1	S2	S3	S4	V_0
1	1	0	0	+V
0	0	1	1	-V
0	0	0	0	0

SWITCHING COMBINATIONS OF A SINGLE MODULE OF H BRIDGE INVERTER

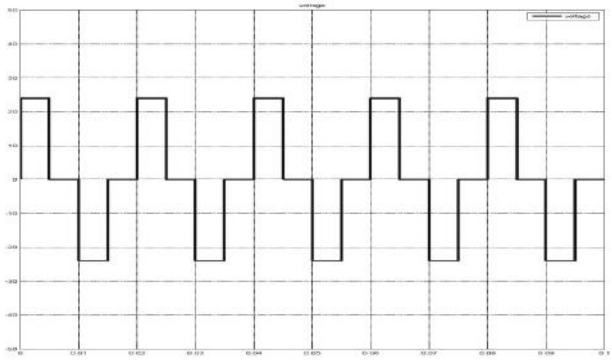

Figure 2. The output wave form of MATLAB simulated model of single module H Bridge inverter showing 3 different voltage levels (+V,0,-V).

III. CASCADING OF MODULES

A. Single Phase Cascaded H Bridge Inverter

Cascading is the series addition of a new module to an existing module. It increases the peak to peak voltage thereby creating new accessible voltage levels. The step increase in voltage level is equal to the magnitude of the voltage source in a single module of H-Bridge Inverter. As cited in [7] the number of accessible voltage levels is a function of the number of modules being cascaded

$$L = 2n + 1 \quad (1)$$

Where L = Number of different voltage levels
n = number of modules

Thus for three modules of cascading (as shown in Fig.3) each with a DC source of 'V' volts, the number of different voltage levels range from 3V to -3V covering a total of seven levels as shown in Fig. 4.

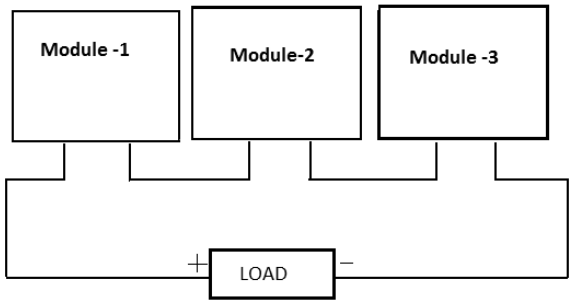

Figure 3. Single phase H Bridge inverter cascaded thrice

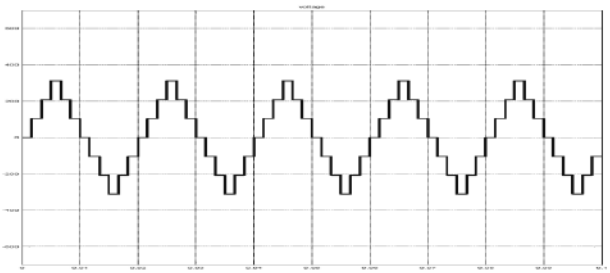

Figure 4. The output wave form of MATLAB simulated model of 3 module cascaded H bridge inverter showing 7 different voltage levels.

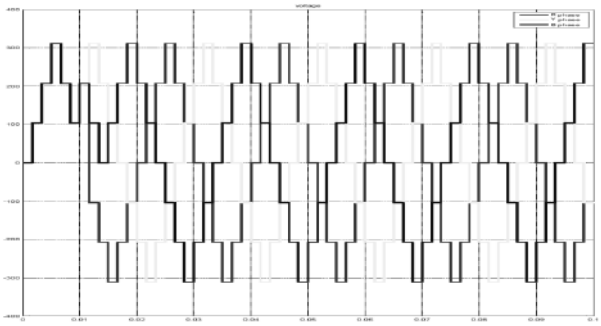

Figure 5. The output wave form of MATLAB simulated model of 3 phase (RYB) cascaded H bridge inverter showing 7 different voltage levels.

B. Three Phase Cascaded H-Bridge Inverter

The cascaded modules are integrated to three phase cascaded HBridge inverter and given to a three phase Delta connected load as it eliminates third order harmonics. The three phases are independant of each other and displaced by 120^0 as shown in the Fig 5.

IV. POWER BALANCING ALGORITHM

In case of conventional H Bridge inverters the power sources in 'n' level cascaded unit are not utilised equally. This leads to an unequal Power Source Utility Factor. To equalize the PSUF a specific power balancing algorithm has been proposed. For an 'n' cascaded module the number of cycles considered are 'n'. In these n cycles, the power being fed by the power source of each module is equalized using transposition technique which employs selective switching patterns fed to the gate terminals of switches as pulses.

Here comparative study is made between cases of wave-shape. Case – 1 is a wave-shape with two peak voltage levels and two zero voltage levels per cycle. Case – 2 corresponds to two peaks and zero zeros per cycle. Case – 3 deals with four peaks and zero zeros per cycle.

For example, consider a 3 phase 3 module multilevel H bridge inverter where the analysis is made for PSUF with and without transposition the PSU values for each cycle are analyzed as follows:

Consider three cycles of the output voltage waveforms as shown in Fig. 6 and Fig. 7 where the alphabet represent the module, positive sign represents the switching on of a switch and negative sign represents that the switch is off or acts as a bypass.

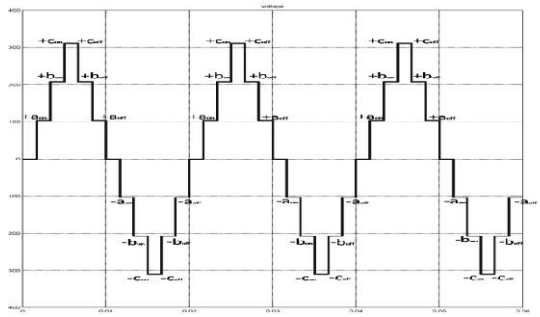

Figure 6. Output waveform of cascaded H-Bridge inverter of Case-1 without transposition.

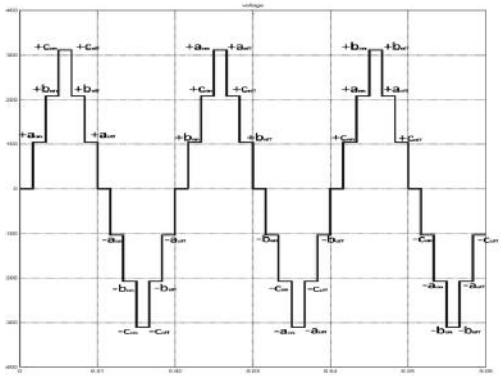

Figure 7. Output waveform of cascaded H-Bridge inverter of case-1 with transposition

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TABLE II

COMPARISON OF PSUF FOR CASE - 1

Without transposition					With transposition		
		MODULES			MODULES		
		1	2	3	1	2	3
CYCLES	C1	10/12	6/12	2/12	10/12	6/12	2/12
	C2	10/12	6/12	2/12	2/12	10/12	6/12
	C3	10/12	6/12	2/12	6/12	2/12	10/12
	PSUF	30/36 = 83.33 %	18/36 =50 %	6/36 = 16.67%	18/36 = 50%	18/36 = 50%	18/36 = 50%

The sequence for without transposition and with transposition is shown in the Fig. 6 and Fig. 7 respectively. The analysis is shown in the Table II. PSUF when not transposed is highest for the voltage source in Module 1 and lowest for the voltage source in Module 3. Whereas, when the switching pulses are transposed, the values of PSUF for all the modules are equal and hence power utility is balanced.

Similarly, other output wave forms and corresponding tables comparing the transposed and un-transposed PUSF for 2 peaks 0 zeros are Fig. 8 and Table III respectively, and for 4 peaks 0 zeros are Fig. 9 and Table IV respectively.

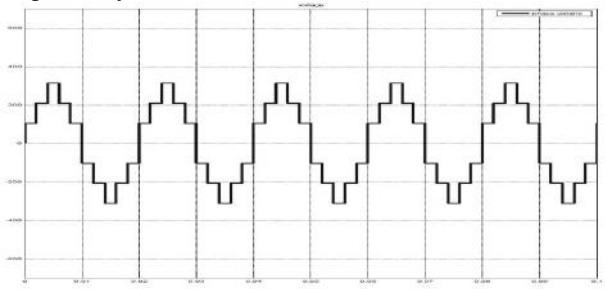
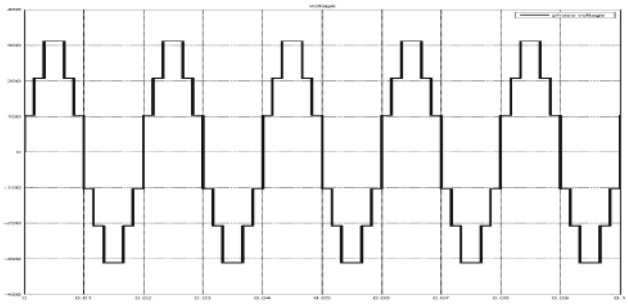


Figure 8(a) The wave form of Case -2

TABLE III

COMPARISON OF PSUF FOR CASE-2

Without transposition					With transposition		
		MODULES			MODULES		
		1	2	3	1	2	3
CYCLES	C1	10/10	4/10	2/10	10/10	4/10	2/10
	C2	10/10	4/10	2/10	2/10	10/10	4/10
	C3	10/10	4/10	2/10	4/10	2/10	10/10
	PSUF	30/30 = 100%	12/30 = 40%	6/30 = 20%	16/30 = 53.33 %	16/30 = 53.33 %	16/30 = 53.33 %



Figures 8(b) The wave form of CASE - 3

TABLE III

COMPARISON OF PSUF FOR CASE - 3

Without transposition					With transposition		
		MODULES			MODULES		
		1	2	3	1	2	3
CYCLES	C1	12/12	8/12	4/12	12/12	8/12	4/12
	C2	12/12	8/12	4/12	4/12	12/12	8/12
	C3	12/12	8/12	4/12	8/12	4/12	12/12
	PSUF	36/36 = 100%	18/36 =66.67 %	12/36 = 33.33%	24/36 = 66.67 %	24/36 = 66.67%	24/36 = 66.67 %

V. SIMULATION RESULTS AND HARDWARE

A.Simulation

As per the section 3.B a simulink model has been developed as shown in the Fig. 9

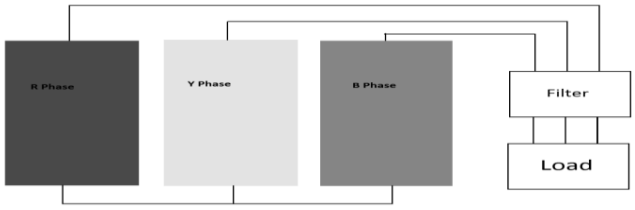


Figure 9 Block diagram of thre phase cascaded three module H Bridge inverter.

The line to line output voltage waveform is as shown in the Fig.10

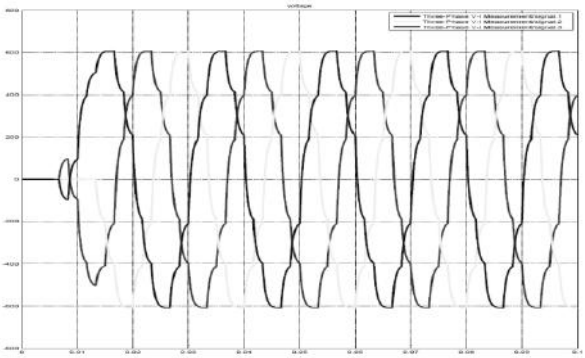


Figure 10. Line to line output voltage of three of thre phase cascaded three module H Bridge inverter.

The pulse for first switch of module 1 in phase A are developed for two cases i.e., with transposition and without transposition as shown in Fig.11 and 12 respectively.

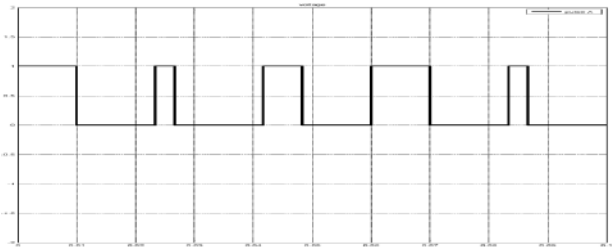


Figure 11. Gate pulse for transposed

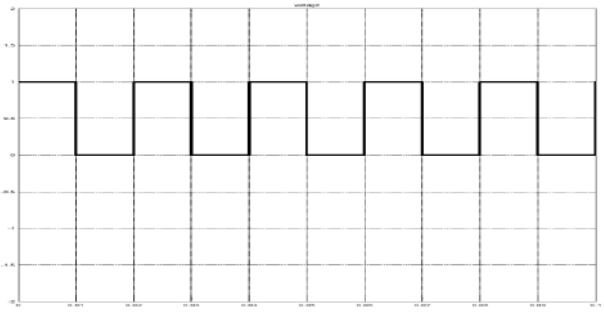


Figure 12. Gate pulse for un-transposed conventional

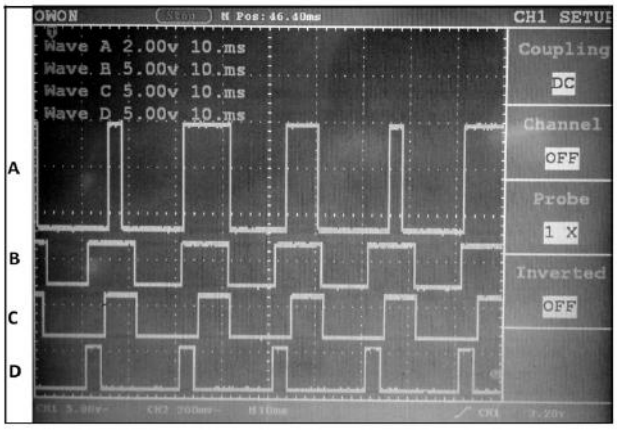


Figure 13. Transposed gate pulse (A) versus conventional gate pulses (B, C, D) generated and plotted on a CRO

The switch pattern generated by simulink has been interfaced to ATMEGA _ (Arduino UNO) so that the micro controller acts independently thereafter the pin output of the microcontroller produces the waveform as shown in the Fig. 13.

In waveform 'A' from b^{th} – $(b+0.02)^{th}$ (s) the source shall be ON for 16.67% of 0.02 seconds as shown in the fig. 13.D. In $(b+0.02)^{th}$ - $(b+0.04)^{th}$ second it conducts for 50% of time as shown in the Fig. 13. C. and in $(b+0.02)^{th}$ - $(b+0.04)^{th}$ second, it conducts for 83.3% of time as shown in the Fig. 13. B. where B, C, D are the pulses to switch 1 in modules 1, 2, 3 without transposition and 'b' is the integral multiple of 0.06 (i.e. b = 0.06*i) where 'i' is an integer.

VI. COMPARISION OF THD

The THD content in a wave is calculated after each waveform is simulated in MATLAB 2013. The theoretical calculations involved in THD computation are elucidated in [8]. A comparison of THDs of different cases gives the following results as shown in the Table IV

TABLE IV
COMPARISON OF THDs

CASE	THD
CASE – 1	5.09%
CASE – 2	7.1%
CASE - 3	4.97%

The figure to show the minimum THD obtained in Case-3 is shown in the Fig. 14

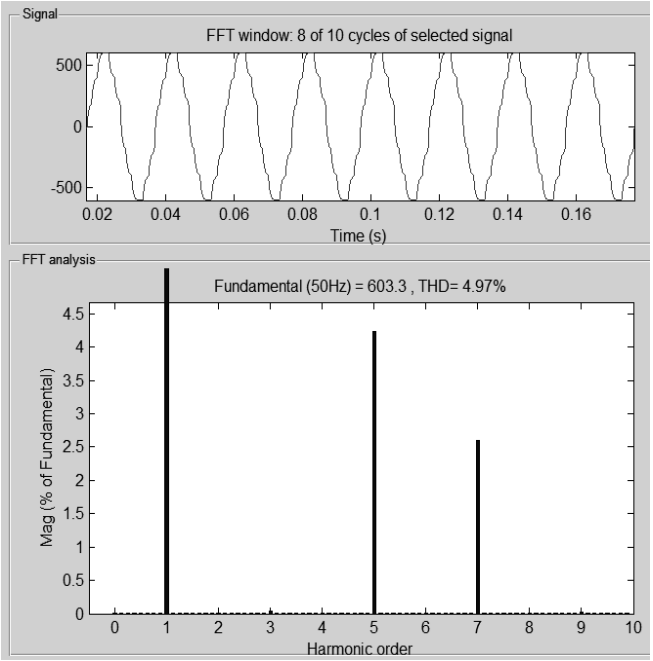


Figure. 14 THD of 4 peak 0 zero

VII CONCLUSIONS

The Total Harmonic Distortion of line-to-line voltage in a three phase H Bridge for different cases (1, 2 and 3) has been compared and found that cases 1 and 3 comply to the IEEE standards. The Power Source Utility factor in different modules of a cascaded unit has been improved significantly. This power source balancing has been realized by practically generating the pulses.

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