FPGA Implementation of MC-CDMA for High Security Applications

R.Ganesh[1] and Ch.Sandeep Reddy[2]
[1]CVR College of Engineering/ECE Department, Hyderabad, India
Email: rachaganesh@gmail.com
[2] CVR College of Engineering/ECE Departments, Hyderabad, India
Email: sandeepredy.ch@gmail.com

***Abstract*—The demand of wireless communications is increased in high speed, high security applications like missile communication, satellite communication etc. The communication with these features can be achieved by using different carrier modulation techniques like single carrier, multi carrier modulation etc. The multi carrier modulation with orthogonality of carriers provides high speed communication. This process is called Orthogonal Frequency Division Multiplexing (OFDM). The high speed and band width utilization can be achieved by using OFDM. The high security communication can be achieved by using coders and spreaders with different random generator sequences with the help of Spread Spectrum techniques. This can be done by using a method called Code Division Multiple Access (CDMA). The Multi Carrier CDMA is defined by adding the features of OFDM and CDMA and this is used for high speed and high secured communication system. The MC-CDMA uses convolution coder, viterbi decoder and spreader, de spreader etc to provide security.**

The MC-CDMA technique consists of a back to back connected transmitter and receiver with 8-point FFT/IFFT and QPSK modulation. This technique is designed by using Verilog HDL with Xilinx ISE Design suite 12.4 version tool. The design is implemented in Xilinx virtex-5 XUPV5LX110T FPGA board.

***Index Terms*—OFDM, CDMA, Orthogonality, Convolution Encoder, Viterbi Decoder.**

I. INTRODUCTION

The present communication systems components require high speed and high security in different application areas like missiles, satellites, mobile etc. The high speed or high security communication systems alone may creates some problems related to bandwidth inefficiency, spectrum utilization etc [1].To achieve better non functional performance parameters the high speed features of OFDM and security features of CDMA are combined to get a new technique called as Multi Carrier CDMA (MC-CDMA).

The MC-CDMA is one of the spectrum utilization techniques that are used for multiple access schemes. This technique gives best spectrum utilization, flexibility in terms of speed and security.

This paper explains the FPGA implementation of MC-CDMA for high security applications. This paper is organized such that the section 2 describes the introduction of basic wireless communication models for high speed, high security applications by using multi carrier techniques like OFDM, CDMA, and MC-CDMA, section 3 describes the results of MC-CDMA system by using Xilinx ISE tools, and section 4 describes the FPGA implementation of MC-CDMA by using Xilinx virtex5 FPGA. The conclusion is presented in section 5 followed by references.

II. OVERVIEW OF MC-CDMA

In wireless communication the data can be sent through the channel in two ways i.e. either single-carrier or multi-carrier. In single-carrier technique the available data stream is transferred sequentially, in this technique each modulated carrier occupies the entire bandwidth of the channel. But, in the multi-carrier technique the total bandwidth is divided into different sub frequencies so that each frequency can be used for one data input. This division of frequency gives better bandwidth spectrum utilization.

The single data input system uses one carrier signal with the total bandwidth allotted to this channel only. In multiple data input system the bandwidth is divided into N number of carrier signals for N inputs. The bandwidth utilization for single input and multiple input systems is shown in Figure1.

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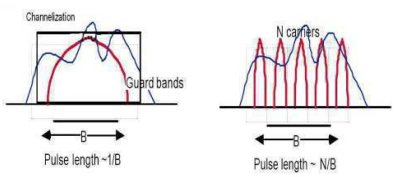

Figure.1: Difference between single-carrier and multi-carrier

Based on the application the multi-carrier technique is divided in to different types like CDMA (Code Division Multiple Access), OFDM (Orthogonal Frequency Division Multiplexing) and MC-CDMA (Multi-Carrier Code Division Multiple Access) etc. The CDMA can be implemented by using the spreading techniques, so it is used for high security applications. In OFDM the available spectrum is divided into N number of orthogonal sub carriers and this technique is used for high speed applications. The MC-CDMA technique is designed by adding the high speed features of OFDM and security features of CDMA [7]. The MC-CDMA uses frequency domain to spread the data, in this technique each sub carrier is having different spreading code. Another spreading technique called as MC-DS-CDMA spreads data in time domain, in this technique all sub carriers uses common spreading code. This concept of multiple spreading codes and single spreading codes for multi carrier design is shown in Figure2 (Fig2.a and Fig. 2.b).

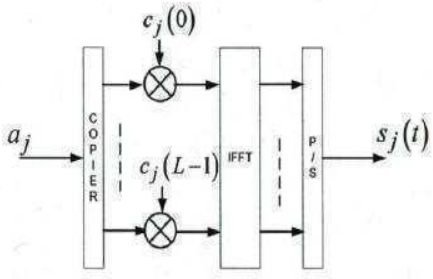

Figure. 2(a) MC-CDMA

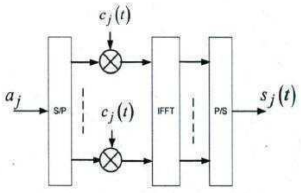

Figure. 2(b) MC-DS-CDMA

Figure 2: Classification of MC-CDMA

Advantages of MC-CDMA:

1. Higher data rates with better bandwidth utilization.
2. Best suitable for wireless systems with delay spread, Doppler spread.
3. Fading is reduced by using frequency diversity.
4. Limited energy loss due to the scattering of energy in all sub carriers.

Problems in MC-CDMA:

1. Peak-to-Mean Envelope Power Ratio (PMEPR) is high due to non linearity in amplification.
2. For high speed vehicles designs complex analysis is required because of carrier frequency offset sensitivity.
3. Sensitive to phase noise.
4. The frequency reusing factor is less compared to other techniques.

Block diagram of MC-CDMA:

The MC-CDMA communication system at base band level can be designed by using a transmitter and a receiver section . This design of transmitter and receiver consists of both security features using multi carriers with the help of encoders, decoders and speed features using OFDM with QPSK modulation/demodulation techniques. The transmitter section consists of convolution encoder, QPSK framer, IFFT etc. The receiver section consists of FFT, QPSK deframer, viterbi encoder etc. The block diagram of the MC-CDMA is shown in Figure3.

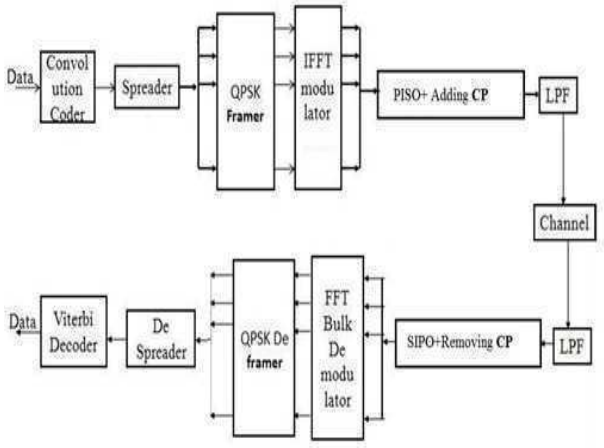

Figure 3: Block diagram of MC-CDMA

The individual blocks of MC-CDMA are explained below with respect to functionality.

Convolution Encoder:

The convolution encoder is used for security purpose, it will convert single bit input to two bit or multi bit output [12]. Convolution encoder is represented by (n, k, m) notation, where n is the number of output bits, k is the number of input bits and m is the constrained length. The rate of convolution encoder is defined as the ratio of number of input bits to number of output bits. It can be implemented by using FSM (Finite State Machine). The Figure 4 below illustrates a simple convolutional coder with k=1, n=2, g1 (n) = (1 0 1), g2 (n) = (1 1 1) and R=1/2. Where R is the code rate.

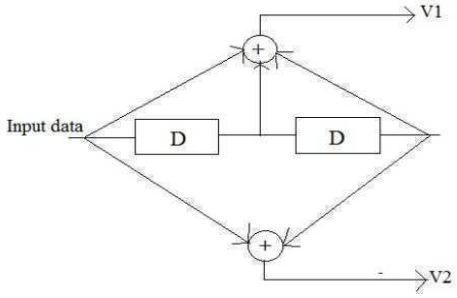

Figure 4: Convolution encoder

The state table for convolution encoder is shown in Table1indicating input, present state, next state and output values.

TABLE I
STATE TABLE OF CONVOLUTION ENCODER

Input (u)	Present state (S1,S0)	Next state (S1,S0)	Output (V1,V2)
0	00	00	00
1	00	10	11
0	01	00	11
1	01	10	00
0	10	01	10
1	10	11	01
0	11	01	01
1	11	11	10

The state diagram and the trellis diagram of ½ convolution encoder in Figure 4 are shown below Figure 5.a and 5.b.

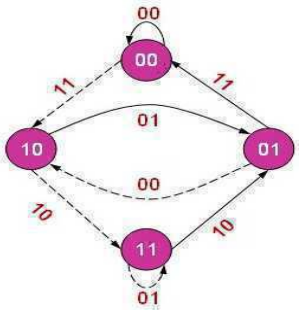

Figure. 5(a) state diagram

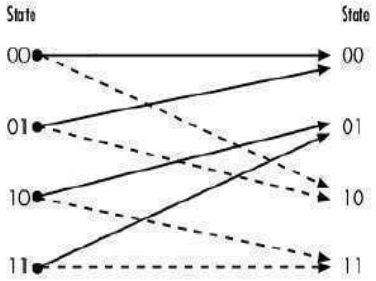

Figure. 5(b) Trellis diagram

Spreader:

The Spreader is also used for security purpose. This can be implemented by using Linear Feedback Shift Register (LFSR). The m-stage LFSR block diagram is shown in Figure 6.

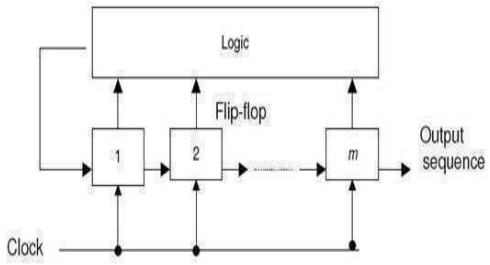

Figure 6: m-stage LFSR block diagram

The LFSR can be designed by using flip flops and some combinational logic circuit. The values in the flip flops are shifted by a single timing clock. The logic in the above diagram can be implemented by using the EXOR gates. The output of EXOR gate is feedback to the input of the LFSR.

QPSK Framer:

The Quadrature Phase Shift Keying (QPSK) is used to modulate the input data signal with the carrier by using four combinations of real and imaginary I and

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Q channels [8]. The selection of I and Q channels can be done by using the one of four possible carrier phase shifts (0, Π/2, Π, and 3Π/2). This mapping of I and Q channels to the input two bits in the form of constellation diagram is shown in Figure 7.

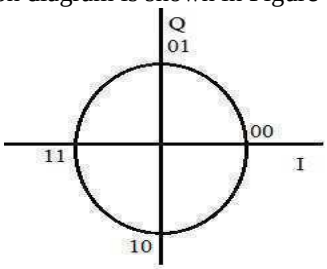

Figure7: QPSK Constellation diagram

IFFT (Inverse FFT) Modulator:

The IFFT is used in the transmitter section of MC-CDMA to minimize the complexity of the design. The IFFT is an algorithm that is useful for speeding up the computation and converts frequency domain to time domain [5].

The DFT of a sequence {x(n)} of length N by a complex valued sequence {X(K)}

$$X(K)=\sum_{n=0}^{N-1} x(n)e^{-\frac{j2\pi nk}{N}} \quad , \ 0\le k \le N-1.$$

Let W_N be the complex-valued phase factor, which is an N th root of unity expressed by

$$W_N = e^{-j2\pi/N}$$

Hence X(K) becomes

$$X(K)= \sum_{n=0}^{N-1} x(n)\, W_N^{nk} \quad , \ 0\le k \le N-1.$$

Similarly Inverse Discrete Fourier Transform (IDFT) become

$$x(n) = 1/N \sum_{k=0}^{N-1} X(K) W_N^{-nk} \quad , \ 0\le n \le N-1.$$

The butterfly diagram of 8-point IFFT is shown in Figure 8.

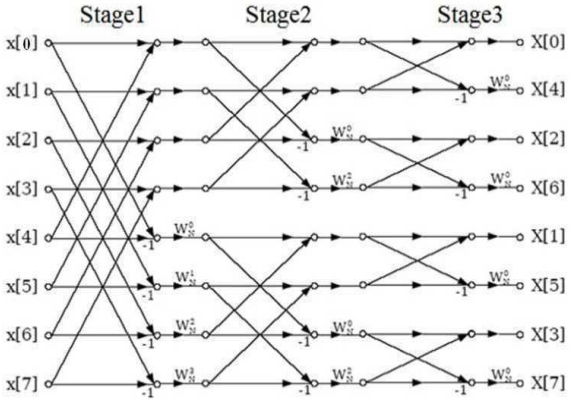

Figure 8: Butterfly diagram of 8-point IFFT

PISO (Parallel In Serial Out):

The parallel in serial out block accepts parallel data and produces serial data as output. The Inter Symbol Interference (ISI) problem of OFDM can be minimized by adding a guard time is inserted with duration longer than the multipath channel maximum delay. This ISI effect can be removed by extending this guard time cyclically in OFDM symbol. The cyclically extension of an OFDM symbol is shown in Figure 9.

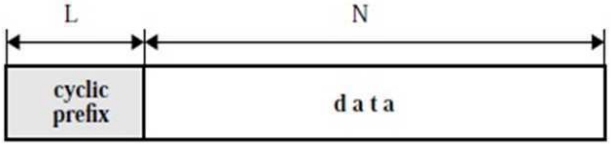

Figure 9: PISO with addition of CP

SIPO (Serial In Parallel Out):

The serial data can be converted into parallel data by using this block. Before applying the outputs of SIPO to FFT (Fast Fourier Transform) demodulator cyclic prefix can be removed.

FFT (Fast Fourier Transform) demodulator:

To reduce the complexity of MC-CDMA, Fast Fourier Transform (FFT) technique is used in receiver [6]. The FFT is used to convert from time domain to frequency domain.

The FFT is an algorithm that is useful for speeding up the computation. The 8-point FFT butterfly diagram is shown in Figure 10.

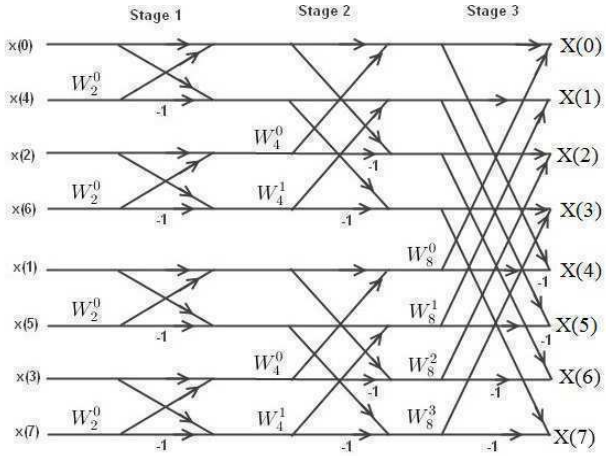

Figure 10: The 8-point Butterfly diagram of FFT

QPSK Deframer:

The parallel data bits are taken two bits together and converted from I, Q to the data bit pattern. The

parallel data is converted into serial data. This operation is exactly reverse to QPSK framer.

Despreader:

The serial data is again Exclusive-ORed with the PN pattern and resulting in original data bit pattern.

Viterbi Decoder:

The viterbi decoder is used to decode the output of the convolution encoder [11]. Block diagram of the viterbi decoder is shown in Figure11.

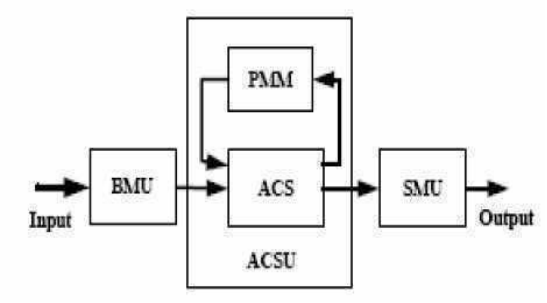

Figure 11: Block diagram of the viterbi decoder

The Viterbi decoder is designed by using Branch Metric Unit (BMU), Add Compare Select Unit (ACSU), and State Metric Unit (SMU) [13-15]. The branch metric computation block is used to count the number of differing bits in the received code symbol and expected code symbol. This is called as hamming distance. The ACSU makes a sum of branch metric and previously accumulated path metric, compare the path metric and select the smallest path metric and decision bits that are supplied to SMU. The SMU finds out the survivor path and decoding bits, SMU produces the decoded bits.

III. RESULTS OF MC-CDMA

The design of MC-CDMA is implemented on Xilinx ISE (Integrated Software Environment) tools; the design is simulated by using Isim simulator and synthesized by using XST (Xilinx Synthesis Tool).The design is prototyped on to XUPV5LX110T FGPA board using IMPACT configuration tool.

The simulation results of MC-CDMA transmitter and receiver are shown below figures 12 and 13.

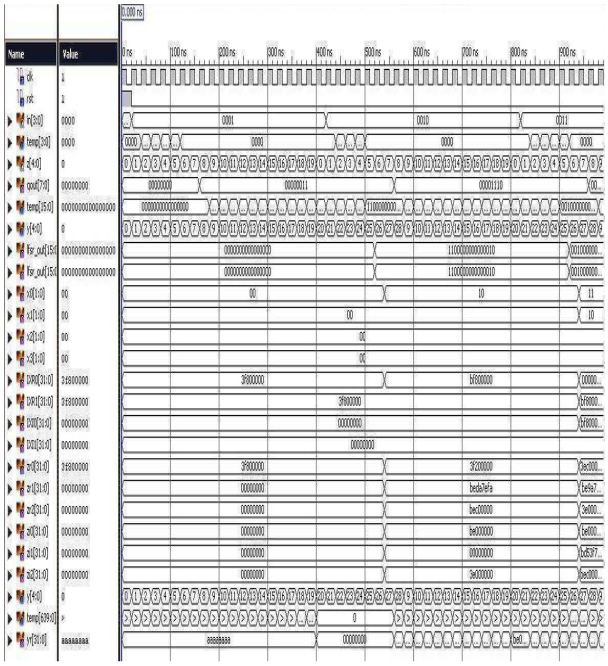

Figure 12: Simulation results of MC-CDMA transmitter

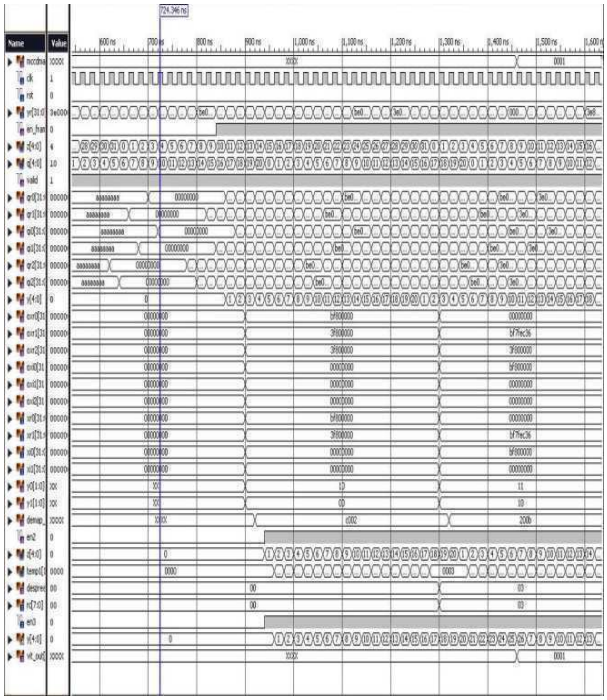

Figure 13: Simulation results of MC-CDMA receiver

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V. FPGA IMPLEMENTATION OF MC-CDMA

The design of MC-CDMA system is verified on Xilinx Virtex-5 FPGA by using Xilinx iMPACT tool. The output of MC-CDMA on virtex-5 FPGA is shown in Figure 14.

Figure 14: Output of MC-CDMA on Virtex-5 FPGA

V. CONCLUSION

The design of MC-CDMA system is implemented with 8-point IFFT/FFT, QPSK modulation, spreader, de spreader, convolution encoder and viterbi decoder is designed by using Xilinx ISE Design suite 12.4 version with Verilog HDL.

The design is simulated for functionality by using Xilinx ISE simulator tool. The synthesized MC-CDMA design has 1382 LUT slices, 2005 slice registers and 3 buffers. Timing analysis results show that the critical path is 2.329 ns, i.e. the maximum clock frequency is 429.369 MHz

The synthesized MC-CDMA design is implemented on XILINX Virtex-5 FPGA.

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