Design Procedure for Digital and Analog ICs using Cadence Tools

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***Abstract*—The present portable electronic devices like smart phones, Laptops etc. are capable of multi functional and multi domain application areas. These types of applications are possible due to the Integrated Circuit (IC) technology changes in terms of reduction in transistor size, supply voltage, time to market etc. These types of complex System on Chip (SoC) devices are designed by using Electronic Design Automation (EDA) tools to meet all nonfunctional IC design constraints. The selection of EDA tool is based on the type of IC design flow, design analysis, designer domain knowledge, nonfunctional optimization constraints etc. This paper gives an overview of Cadence company based VLSI EDA design tools and tool flow procedures for Digital and Analog ICs.**

***Index Terms*— VLSI, Cadence, EDA Tools, IC Design, System on Chip.**

I. Introduction

The present portable electronic devices can be designed by using hardware and software components. The hardware components are designed by using hardware IC design flows and software components are designed by using software design methods. The selection of hardware or software methodology is based on nonfunctional constraints like maximum operating frequency, area, power etc [3]. The hardware design can be done by using IC fabrication with the help of Very Large Scale Integrated Circuit (VLSI) design flows. The VLSI design flows are of different types based on the type of design entry and the type of final product.

The VLSI Design is divided into two major groups as programmable design and nonprogrammable designs. The types of VLSI design flows are shown in Fig 1.The programmable design uses programmable devices using programmable AND/OR arrays. These devices are of different types based on the type of programmable device. The major types of programmable devices are Programmable Logic Array (PLA), Programmable Array Logic (PAL), Complex Programmable Logic Device (CPLD) and Field Programmable Gate Array (FPGA). All the programmable devices are used to design prototyping devices for Digital Electronic ICs using digital logic or Hardware Description Language (HDL). The nonprogrammable designs can be designed using Application Specific Integrated Circuit (ASIC) methodology with either semicustom design or full custom design based on the type of design entry.

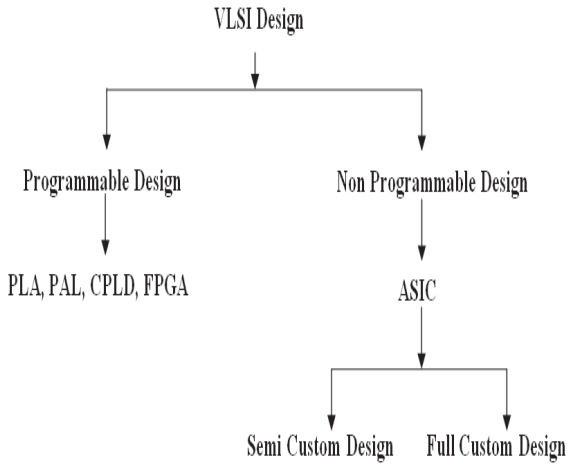

Fig.1: Types of VLSI Design flows

The semicustom design uses Hardware Description Language (HDL) entry for the design of Digital Electronic IC devices. The full custom design uses transistor level entry for the design of Digital, Analog and Mixed signal Electronic IC devices. The design functionality is verified by using simulation with the help of test benches.

The FPGA design is completed by using Xilinx, Altera, Atmel, Actel and other EDA companies by using vendor based FPGA prototyping tools and kits. The final digital design is downloaded onto FPGA kit using Joint Test Action Group (JTAG) cable. The non programmable designs can be done by using tools from product based companies like Cadence, Synopsys, and Mentor Graphics etc. All these nonprogrammable designs are targeted for IC technology library provided by IC manufacturing company.

This paper mainly concentrates on design flows and procedures of nonprogrammable IC designs using Cadence EDA tools. The introduction to Cadence tool flow for semicustom and full custom is explained in section II and the detailed semicustom design methodology procedure for simulation, synthesis, and implementation using cadence tools is explained in section III. The full custom design flow for transistor level entry using Cadence tools is explained in section IV, followed by conclusion and references.

II. IC Design Using Cadence Tools

The Integrated Circuit for nonprogrammable logic is designed by using either HDL design entry or transistor

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level design entry. The HDL design entry is used for semicustom design and transistor level design entry is used for full custom design. The complete IC design suite for semicustom and full custom designs using Cadence tools [1] is shown in Fig.2.

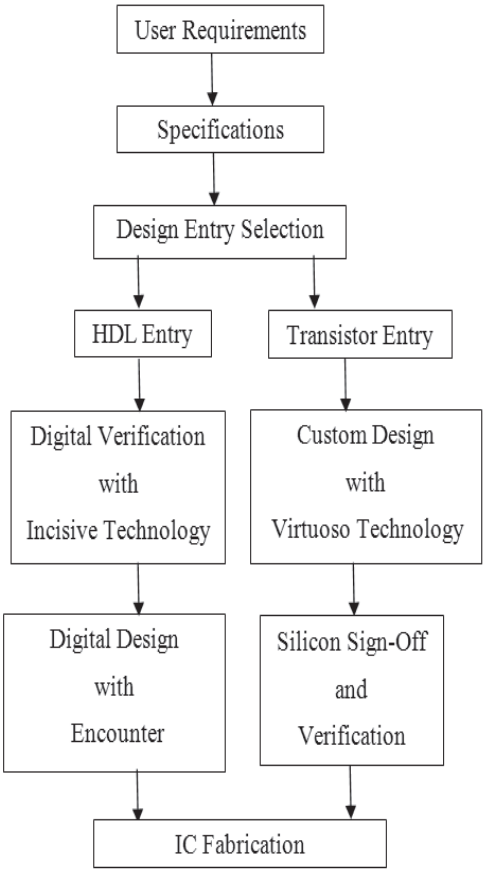

Fig.2: IC Design Flow using Cadence Tools

The IC design flow starts with the user requirements, and the designer extracts the specifications based on the feasibility, domain knowledge, time to market and other design parameters. The design entry for the IC fabrication flow is selected from the specifications as either HDL entry or transistor level entry. For Digital IC design, HDL or transistor entry is selected and for Analog IC design, transistor level entry is selected.

The Digital IC design using HDL is done using HDL design file and its functional simulation, verification using Cadence Incisive technology tools. After the verification, the digital design is synthesized and implemented using Cadence Encounter Digital Implementation platform tools targeting for the given IC manufacturing technology library. Then the final implemented file is given to manufacturing company for IC fabrication.

The Digital/Analog IC design using transistor level entry is done with Cadence Virtuoso technology tools with the help of schematic cell view, functional simulation, layouts etc. The timing performance of functional simulated design can be calculated with the help of parasitic extraction, timing analysis, physical verification etc. targeting given IC manufacturing library model files. This is done by using Cadence silicon sign off and verification tools. Finally, the functionally verified and implemented file is given to manufacturing company for IC fabrication.

III. Semicustom Design Using Cadence Tools

The semicustom design is used for HDL design entry based Digital design circuits. The Digital designs like all gates, multiplexers/demultiplexers, decoders/encoders, latches/flip-flops, shift registers, counters etc. can be designed using Cadence semicustom design suite. The semicustom design flow using cadence tools is shown in Fig.3.

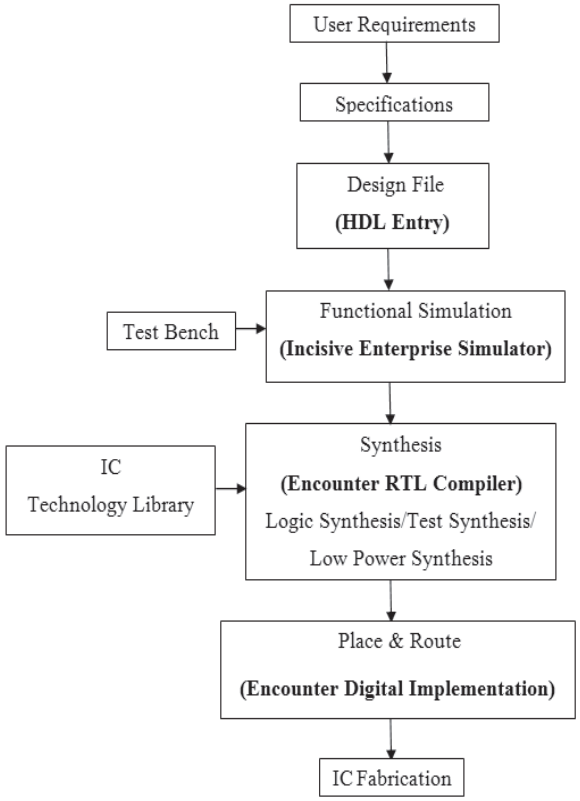

Fig.3: Semicustom Design Flow using Cadence Tools

The Semicustom design flow starts with user requirements and ends with IC fabrication. The specifications are extracted from user requirements and uses HDL design entry. The design flow consists of three major steps i.e. functional simulation using Cadence Incisive Enterprise Simulator, synthesis using Encounter RTL Compiler and place & route using Cadence Encounter Digital Implementation (EDI) tool.

A. Incisive Enterprise Simulator (IES)

The functionality of digital design is verified using Cadence Incisive Enterprise Simulator. The simulation is done for VHDL, Verilog HDL, SystemC and System Verilog design entries. The design flow for simulation using IES tool with sub tools is shown in Fig.4. The basic

simulation for any design entry consists of three steps i.e. compile, elaborate and simulate. For all the above steps two design environment variable files called cds.lib and hdl.var are required. The cds.lib defines the design libraries and concerned logical library names with physical library location. The hdl.var defines variables that affect the behavior of tools and utilities.

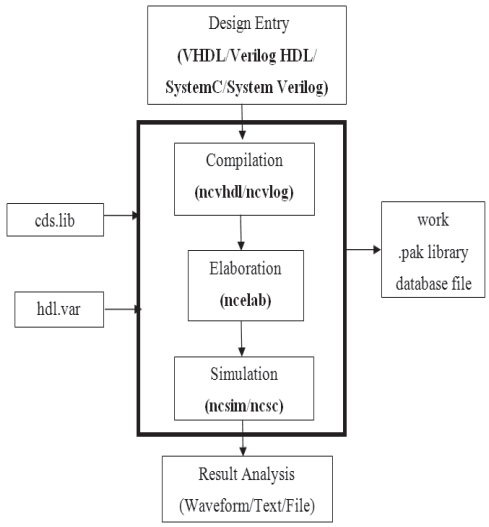

Fig.4: Simulation using IES tool

The commands for simulation process of Verilog HDL are shown below.

Compilation:

ncvlog –mess path_of_verlog_design_file/file.v

ncvlog –mess path_of_verlog_testbench/test_file.v

Elaboration:

ncelab –mess –access rwc testbench_module_name

Simulation:

ncsim –gui testbench_module_name

The database for compile, elaborate and simulate will be stored in a work directory in .pak format. The simulation results are analyzed with the help of graphical waveform or text form or file format.

B. Encounter RTL Compiler

The functionally verified design is given as input to the Cadence Encounter RTL Compiler synthesis tool and targeted for the IC manufacturing technology library. The synthesis RTL compiler can be generic synthesis (technology independent) or mapped synthesis (technology dependent) or incremental synthesis. Based on the type of analysis and optimization goal, the synthesis can be logical synthesis, low power synthesis, test synthesis. Some of the required input files and generated output files are shown in Fig.5 [2].

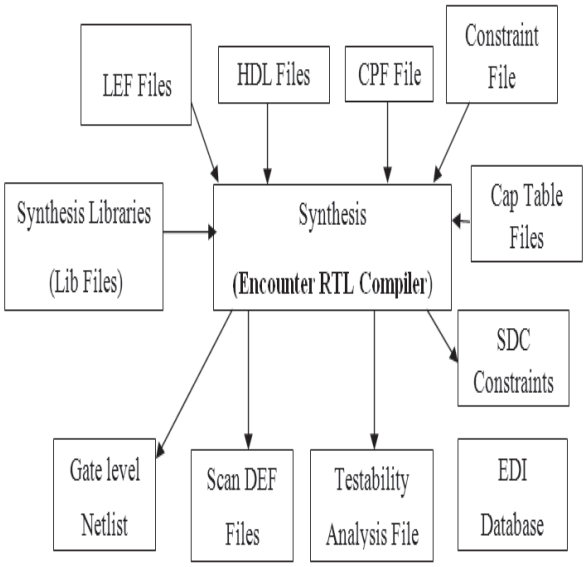

Fig.5: Input/output files for RTL Compiler

In RTL Compiler any type of synthesis will be done using Tool Command Language (TCL) based script file.

The basic flow of script file for synthesis is shown below.

Script:

1. *Set the error/warning information level*
2. *Set paths for HDL files, Library files, Script files*
3. *Load the logic library files, I/O library files*
4. *Load Library Exchange Format(LEF) files*
5. *Load capacitance tables*
6. *Read all HDL files*
7. *Elaborate top level HDL design*
8. *Apply and read constraints*
9. *Set synthesis to generic/mapped/incremental*
10. *Generate Netlist, SDC file, EDI database, area, power, speed and other reports.*

C. Encounter Digital Implementation(EDI)

The synthesized Netlist along with EDI database of Encounter RTL compiler tool is given as input to EDI environment for implementation. The simple design flow for EDI is shown in Fig.6 [3].

The EDI design flow starts with design import of synthesized net list output with library files and I/O pads information. The net list is loaded with sufficient floor planning, power planning to meet area, speed and power constraints. The design is placed according to the power routing, cell routing, and clock tree synthesis to avoid geometry and connectivity violations.

Some additional steps may be added to this design flow based on the optimization goal and digital domain. The implemented designs after placement and routing, without any violations will be sent to the IC manufacturing foundry for fabrication.

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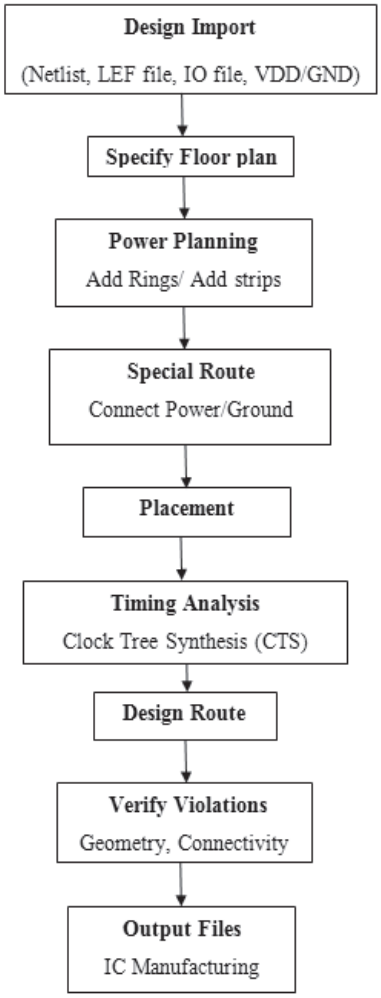

Fig.6: Simple Design flow for implementation

IV. Full Custom Design Using Cadence Tools

The full custom design flow is used for design of Digital and Analog ICs using transistor level design entry. The full custom design is used for design and analysis of Digital designs like all gates, multiplexers, demultiplexers, decoders, encoders, latches, flip-flops, counters etc. The same design flow is used for Analog designs like amplifiers, comparators, current mirrors, oscillators, op-amps etc to calculate nonfunctional and optimization performance parameter calculations. The full custom design flow using Cadence tools is shown in Fig 7 [1].

The full custom design flow is used for both Digital and Analog ICs targeting for the technology library provided by IC foundry. All the ICs are designed using MOS transistors, VDD, GND, voltage sources etc. These basic elements are connected according to the type of logic family to meet nonfunctional constraints. The logic family can be CMOS logic, Pseudo NMOS, Clocked CMOS logic etc.

The technology library information is available in the form of model files described by using SPICE language. All the SPICE models are available for different Process, Voltage and Temperature (PVT) parameters. The simulation can be done for different types of analysis and it is selected based on the type of the circuit and type of inputs. The different types of analysis are ac, dc, transient, frequency etc. The selection of the analysis is based on the time variant input, time invariant input and other types of input voltage or current sources. The voltage sources are like dc, ac, pulse, sine etc.

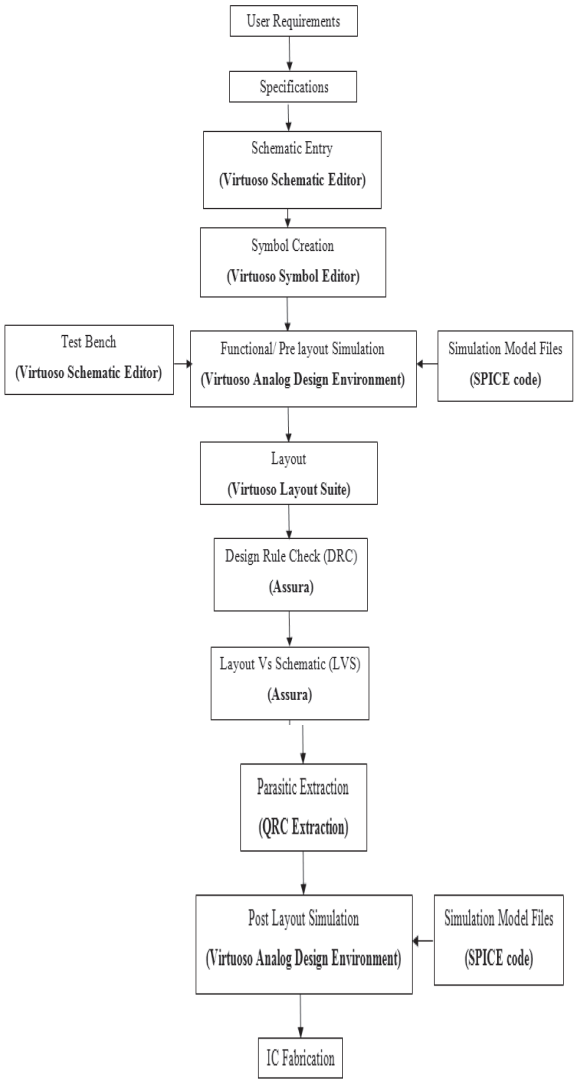

Fig.7. Full Custom Design Flow using Cadence Tools

The fabrication of the functionally verified design is done by drawing a layout according to the design rules and performing matching between layout and schematic. The timing delays are extracted from parasitic extraction of layout and its functionality is verified by using post layout simulation.

This design procedure is valid for both Digital IC fabrication and Analog IC fabrications. The Digital ICs functionality can be verified by using transient analysis. The dc analysis is used to calculate the operating point.

The Analog ICs performance can be verified by using transient analysis, frequency analysis and sensitivity

analysis etc. The tool driven calculator is used to calculate different performance metrics of Analog ICs like slew rate, gain, gain bandwidth, frequency of operation etc.

The post layout simulated design with no DRC, LVS violations is sent to fabrication house for IC fabrication. The Cadence tools can also be used for mixed signal IC design with the help of HDL entry and schematic entry options to meet the present day System on Chip (SoC) requirements.

V .Conclusions

The EDA tools are used to design System on Chip (SoC) applications with the help of Digital ICs, Analog ICs and Mixed signal ICs. In this paper the design procedures for Digital ICs simulation, synthesis and implementation using Cadence tools are discussed. The design procedure for Analog ICs fabrication using full custom design flow with Cadence tools is also discussed

References

1. Cadence training brochure 2014-15.
2. “Using Encounter RTL Compiler” Product Version 14.1, April 2014.
3. “EDI System Menu Reference” Product Version 14.10, April 2014.

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