High Performance Operational Amplifier for Pipelined Analog to Digital Converters

A.Anitha,
CVR College of Engineering/ECE, Hyderabad, India
Email: anitha90@yahoo.com

***Abstract*—As electronics and telecommunication worlds are moving fast towards digitalization and there is an ever increasing demand on speed and accuracy of the processed data, the need for high speed and high resolution ADCs has grown dramatically over recent years. Pipelined ADC is the architecture of choice in high speed and medium resolution applications. Op-Amps are basic building blocks of a wide range of analog and mixed signal systems. In this paper a Op-Amp is designed using 90nm CMOS technology, the small voltage difference can be around tens of millivolts is amplified by this Op-Amp. As new generations of CMOS technology tend to have shorter transistor channel length and scaled down supply voltage, the design of Op-Amps stays a challenge for designers.**

The main focus in this work is the Op-Amp design to meet the requirements needed for the 12-bit pipelined ADC. The Op-Amp provides enough closed-loop bandwidth to accommodate a high speed ADC (around 300MSPS) with very low gain error to match the accuracy of the 12-bit resolution ADC. The amplifier is placed in a pipelined ADC with 2.5 bit-per-stage (bps) architecture to check for its functionality. The Effective Number of Bits (ENOB) stays higher than 11 bit and the SNR is verified to be higher than 72 dB for sampling frequencies up to 320 MHz.

***Index Terms*—ADC, Op-amp, CMOS, Low supply, bandwidth. Pipelined, Gain Boosting, CMFB, Flash, MDAC.**

I. INTRODUCTION

Analog to digital converters are the most important building blocks in lots of applications. For these applications the digitalization and speed and accuracy of the processed data and high resolution is required.The ADC applications fall into four market categories 1) data acquisition, 2) precision industrial measurement, 3) voice band and audio and 4) high speed. For high speed and medium resolution applications the Pipelined ADC architecture is the best choice. Examples of these applications are instrumentation, communications and consumer electronics.

The choice between different architectures can be made based on the speed, resolution, area and power consumption requirements in the target application. Knowing the specification, one can choose between different architectures to achieve the needed performance. Among available ADC architectures, flash, folding, sub-ranging and pipelined ADCs are fast enough to be considered as a high speed ADC. Pipelined ADC is built from several low resolution converters in a pipeline. The number of stages and the number of bits resolved by each stage along with redundancy bit(s) should be determined wisely considering power, speed and resolution of the ADC and accuracy requirements on sub converters. Most of the time, in high speed ADCs lower resolution per stage is chosen to have lower inter-stage gain and settling time which results in higher conversion rate. Low resolution per stage also relaxes the requirement on accuracy of voltage references in Sub ADC and comparators. Drawbacks of having lower bits resolved in stages are higher number of stages that are needed and more noise and gain and offset errors from latter stages brought back to the input due to lower inter-stage gain and will lower the total ADC's accuracy.

Usually in high resolution ADCs, more bits are resolved in each stage. Higher resolution per stage gives the benefit of having higher inter-stage gain which will reduce the later stages' noise contribution to the overall noise of the ADC. However, this increases the power dissipation of the ADC and also the area required for the ADC. The noise and other errors of subsequent stages are reduced by former stages' squared gain. Adding more bits to be resolved in early stages, especially stage1, will relaxes the requirements on following stages' accuracy and noise requirements and will allow scaling to be applied to them. This technique helps with area and power limitations. Stages can also have redundancy bit that can be shared between neighbouring stages by overlapping. This technique leaves room for error correction (does not produces 111) and adds ½ LSB offset to prevent saturation of coming stages due to comparison errors occurred in present stage. This offset helps to keep the residue signal within the 0-Vref range of the ADC. Another advantage of this technique is the reduced inter-stage gain for higher number of resolved bits. For example in a 2.5 b stage with 3 raw bits and 2 resolved bits (one redundant bit) from total bits of the ADC, stage gain will be instead of . Reduced gain will relax the requirements on the OpAmp employed in the MDAC. Redundant bit can be added to any sub ADC with different resolution.

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II. PIPELINED ADC'S ARCHITECTURE

A 12-bit pipelined ADC incorporating 2.5 b stages is shown in Figure 1. The ADC incorporates 6 stages; each one (except for stage 6) consists of a sample and hold, DAC, subtraction and amplification circuitry (all of which known as multiplying DAC or MDAC) and a low resolution but high speed flash ADC. Stage 6 is a 3-bit flash ADC. In Figure 2 one stage of pipelined ADC is represented.

Inside each stage input voltage is converted to 3 raw bits by the high speed flash ADC and then reconstructed back to analogue by the DAC. The reconstructed signal is subtracted from original sampled signal and the difference is multiplied by the amplification factor, producing the residue signal. The residue signal is applied to the next stage to be processed and the current stage starts sampling the incoming signal and processing on the sampled and held data. The pipelining operation produces latency to the digital data production but after that there will be one conversion per clock cycle. As a result of this concurrency conversion rate of the ADC is independent of the number of stages.

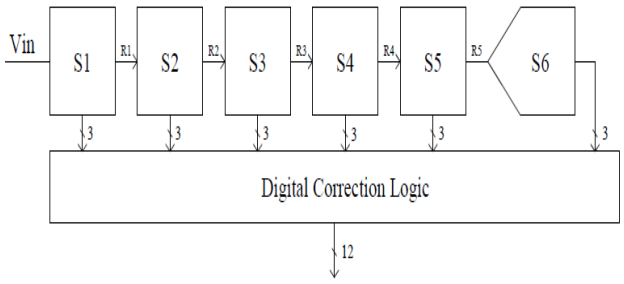

Figure 1: 12-bit Pipelined ADC

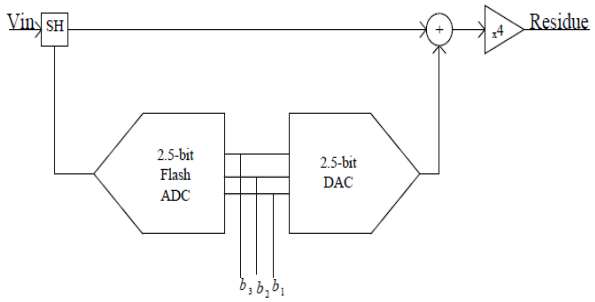

Figure 2. one stage of pipelined ADC

A. *Flash Sub-ADC*

The pipelined ADC has fully differential architecture. Fully differential architecture allows more dynamic range and reduces even harmonics' effect on nonlinearity. One out of six segment of the sub-ADC is presented in Figure 3.10].

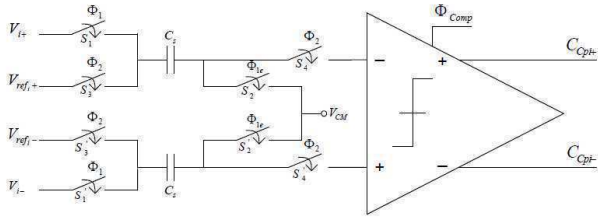

Figure 3. One Segment of Comparing Circuitry in Sub-ADC

Comparators clock is delayed version of clock2. In comparator's circuit pre-amplification is used to amplify small differences between input and reference voltage to increase the accuracy of the comparator. The pre-amp circuit needs time to settle and the delay allows the output to reach its final value to be used in comparison.

B. *Thermometer Decoder*

The thermometer decoder can be implemented using lots of techniques, for example by using pass-transistors, multiplexing, etc. In this design thermometer codes are used as address bits of an OR-based ROM. Figure 2-7 shows a 3-to-2 bit thermometer to binary decoder (Figure 1-2-b), using the ROM implementation. The address decoder circuit is OR-based designed as well. All address and data lines in the address decoder and ROM are connected to through PMOS devices which are always on. Whenever a line in the ROM should be chosen, all transistors in that line should be turned on which means the address line should be kept high. For an address line to be high, all transistors that are connected to it should be off. For example, if $C_2C_1C_0$ is 000 ($V_{in} \leq V_{ref1}$) then Add1 is V_{dd} and the transistors in the first line turn on, bringing data lines to 00 which is the binary output expected $V_{in} \leq V_{ref1.}$

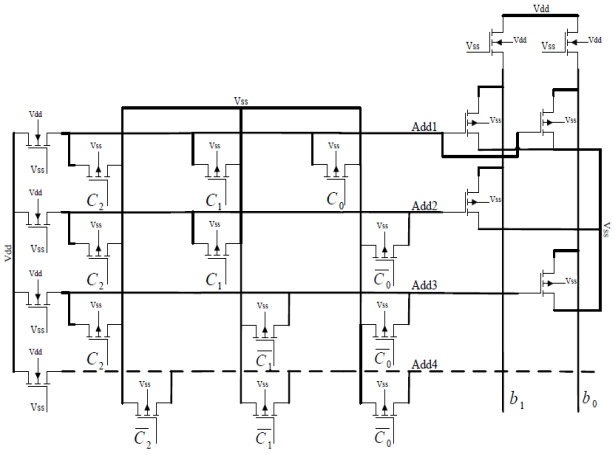

Figure 4. Thermometer to Binary Decoder Implemented by OR-Based ROM

In picture above, the last address line (dashed line) is not needed to be implemented, as it does not drive any transistor in the ROM. It has been kept in the picture for the sake of more accuracy. The actual design is fully differential 6-to-3 bit decoder (2.5bit/s implementation).

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C. Comparator

Comparators are made of two basic building blocks, a preamplifier and a latch. The comparator is used to resolve small input signal and produce a digital 0 or 1 output. Therefore, the amplifier does not have a linearity requirement. It should amplify the small input signal enough to make the latch change its state if necessary. The basic concept of a comparator is shown in Figure 5.

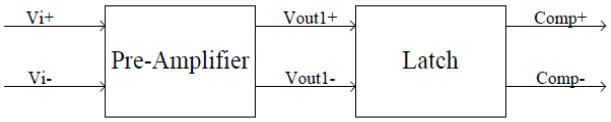

Figure 5. Basic Concept of a Comparator

The comparator operates in two phase, reset and evaluation (latching). In reset phase, the latch is pre-charged to V_{dd} to reduce the power dissipation in this phase. In evaluation phase, the amplified input signal causes the latch to change its state in either direction and by the aid of positive feedback the output signal will clip to one of the supply sources, producing the digital outputs.

D. MDAC

An MDAC performs sampling, digital to analogue conversion, subtraction and amplification. The circuit shown in Figure 2-12 is responsible for sampling, subtraction and amplification in an MDAC: Amplifier's clock is a delayed version of comparator's clock. This delay is needed for thermometer decoder and DAC to complete the conversions from thermometer codes to binary codes and from digital codes to analogue signal.

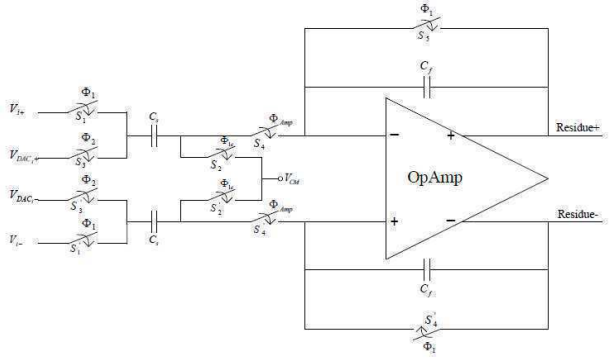

Figure 6. Sampling and Multiplication Part of The MDAC Circuit

E. Bootstrapping

High linearity requirement of the 12-bit ADC necessitates linear operation of the switches in the sub-ADC and MDAC structure. For a switch to work with high linearity, it should work with constant overdrive voltage. To serve this purpose some of the switches are bootstrapped, especially front end switches whose overdrive voltage suffers from the changes of input voltage. The bootstrap circuit, designed in [10] and adapted for low-voltage 65nm CMOS technology, is depicted in Figure7.

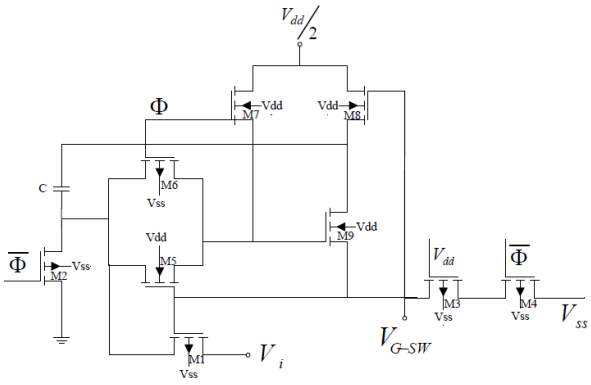

Figure7. Bootstrap Circuit

Bootstrapping also helps with switches conducting constant high voltages. It can provide a high enough overdrive voltage for those switches.

F. Clocking Scheme

Clock phases needed within the stage are depicted in Figure 8.Clock1 is used to sample the input data by the sampling network in flash sub-ADC and MDAC simultaneously. Pulse width of this clock is almost ¼ of the sampling period. Clock1e is similar to clock1 in regards to period and 25% pulse width, but it turns off before clock1 to cancel charge injection problem from sampling switches. Allocating less time to sampling allows the circuit to spend more time on amplifying which gives amplifier more time to settle, increasing maximum sampling frequency.

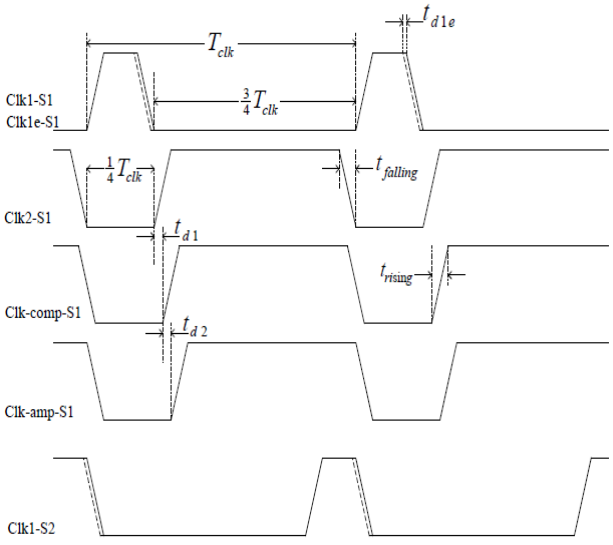

Figure 8. Stage Clock Phases

Clock2 is used for introducing reference voltages to the sampling network to be compared to sampled data (in

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sub-ADC) or subtracted from it (in MDAC). The pulse width of clock2 is almost ¾ of sampling period. As explained before, in sub-ADC and MDAC sections, the comparators' clock and amplifier's are delayed version of clock2. All clocks' pulse width is lowered by rising and falling time to obtain non-overlapping clocks.

Sampling in each stage (except for stage1) starts at the last 25% of the amplification clock of preceding stage. This way, as the OpAmp amplifies the residue signal and resides within the accepted error (½ LSB) of its final value, the sampling capacitance of succeeding stage is charged with the residue signal to reach the final value simultaneously. Using this scheme, conventional sampling period can be reduced by 25%.

G. Digital Correction and Time Alignment

The bits from each stage are not resolved at the same time. As a result the output bits from 6 different stages that correspond to the same input sample are ready at different point in 28 time and should be time aligned and then digitally corrected. In order to align the bits related to the same sample shift registers are used.

III. DESIGNE OF OPAMP

In this work, a two-stage gain boosted amplifier is designed to achieve high DC-gain and output swing. The price to be paid is high power consumption which is not avoidable when a high performance amplifier is needed. An OpAmp to be employed in a 12-bit pipelined ADC is designed and its performance metrics are shown.

A. OpAmp Requirements

For an OpAmp-based design of a high resolution and high speed pipelined ADC, there are high requirements for the OpAmp design to be satisfied. These two definition "high resolution" and "high speed" for an ADC adds a great deal of challenge on the OpAmp design to achieve the required performance regarding DC-gain, Bandwidth, noise, stability, speed and swing. All of which should be achieved under critical conditions of decreased supply voltages and intrinsic gain of today's CMOS technology. The down sized transistors of new coming technologies also have higher leakage and lower output resistance. They are faster switches as a result of the reduced parasitic capacitances (due to reduced transistor dimensions). Because of the higher number of transistors in smaller area, heat production is another problem of scaling in new technologies which will cause slower operation and reduced reliability and lifetime of the transistors. These transistors are also more prone to process variation. All of these characteristics of new scaled down technologies add more error to the OpAmp's transfer function, making it harder to satisfy the stringent requirements on the OpAmp.

OpAmps are the basic building block of an ADC which determine the speed and accuracy of the ADC. They introduce gain error and nonlinearity which should be minimized in design process or compensated for by digital correction circuitry. They are also the most power hungry part of the ADC and dissipate almost 60-80% of the total power. There are a few techniques to reduce OpAmps power consumption [18], like using class AB amplifiers which only consumes dynamic current, OpAmp sharing and OpAmp current reuse.

As discussed earlier, the OpAmp is used in the 2.5 b MDAC structure of the pipelined ADC. The OpAmp is placed in a negative feedback with amplification factor of 4. Now it is time to see what the requirement specification for this OpAmp is. Here we discuss DC-gain, Gain-Bandwidth (GBW), Slew-Rate (SR) and Noise. In the Table 1, the needed requirements on the OpAmp to be used in the pipelined ADC are summarized.

TABLE I.
SUMMARY OF OP AMP's REQUIREMENTS

Performance Metrics	Required Values
f_u	2.12 GHz
Slew Rate	5.27Kv/µs
Dc-gain	67 dB
SNR	71dB

B. Proposed OpAmp Architecture

The proposed OpAmp is a two-stage, fully differential, Cascode current mirror topology modified for low-voltage operation. It is an extended version of OpAmp used [19]. In Figure 9.the architecture of the amplifier is shown: The OpAmp is a two-stage amplifier to achieve high gain and voltage swing. It is also uses gain boosted cascode devices. Input devices are chosen to be PMOSFETs because of their lower flicker noise and more flexibility about the input CM level. Second stage incorporates NMOS devices for their higher intrinsic gain. Second stage is a simple CS stage to allow more output swing. 2pF load capacitor is considered to simulate next stage's input capacitance. The compensation scheme used here is Miller Compensation.

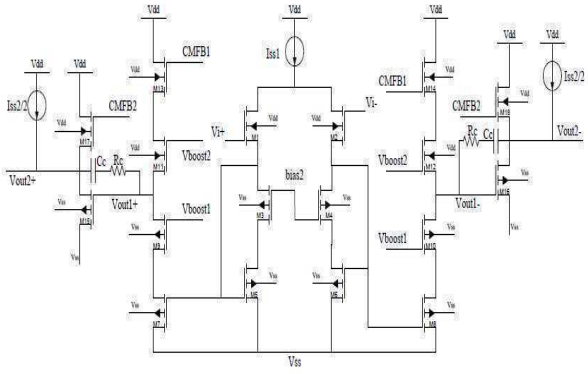

Figure 9. OpAmp Architecture

C. Common-Mode Feedback (CMFB)

Both stages CM levels are regulated by common-mode feedbacks. Figure 10 represents CMFB circuit:

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Differential outputs of each stage are sensed by a differential pair and compared to a voltage reference. In case of any differentiation, the CMFB brings back the output CM mode level to its equilibrium.

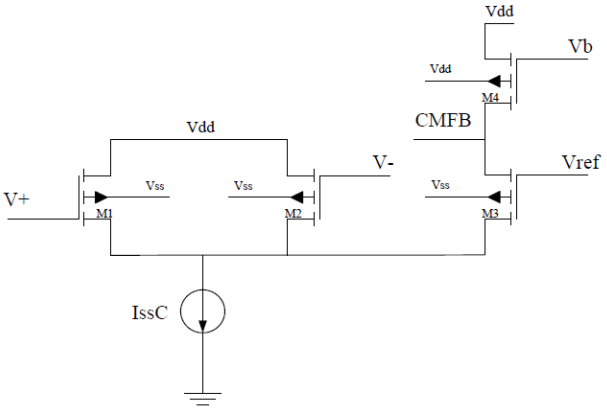

Figure 10. CMFB Circuit

D. Boosting Amplifiers

Boosting amplifiers are folded-cascode OpAmps. The folded-cascode OpAmps have high voltage swing and moderate gains. They also allow more input CM mode range. The 4 stacked transistors of first stage and the boosting amplifiers placed in the main amplifiers circuit are shown in Figure 11.

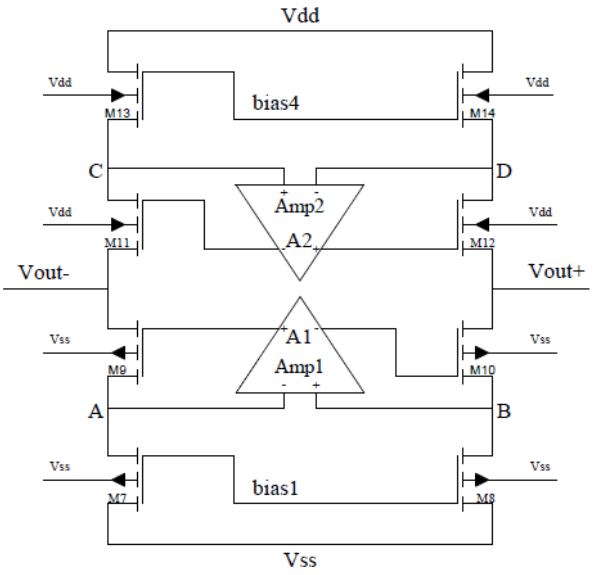

Figure11: Boosting Amplifiers Placed in The First Stage's Output Branch

Amp1 senses voltages of points A and B, regulates the cascode devices' (M9-M10) gate-source voltages and amplifies the total gain by A1. Amp1 has PMOS input devices to deal with low voltage CM levels in A and B. Amp2 incorporates NMOS input devices due to same reasoning. The architecture of boosting amplifier number two is shown in figure12.

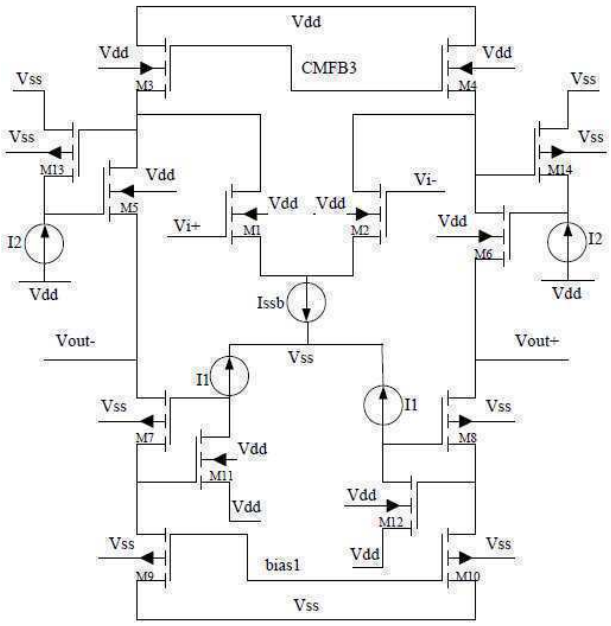

Figure 12: Boosting Amplifier

Boosting amplifiers are gain boosted as well. The technique is called Nested-boosting [14]. Sometimes the second boosting amplifier is simple, like this case, but it also can be scaled version of main boosting amplifier if more gain is needed. One should be cautious when putting boosting amplifiers into the circuit as they introduce internal loops that can be unstable.

To check for stability around internal loops, probes (to break the loop during simulation) and stability simulation can be used. In Figure 13, Figure 14, Figure 15 and Figure 16 gain and phase plots of both boosting amplifiers are shown and Table 2 and Table 3 contains simulated parameters for boosting amplifiers.

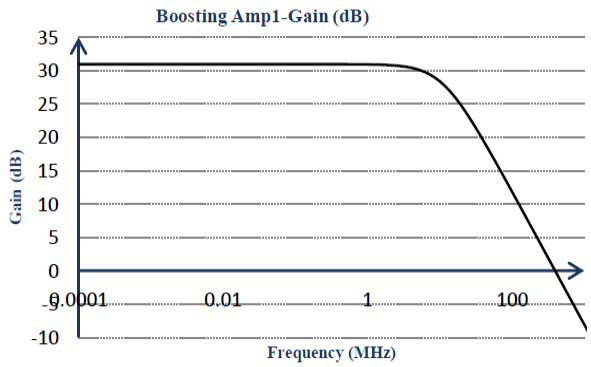

Figure 13: Boosting Amp1 Gain Plot

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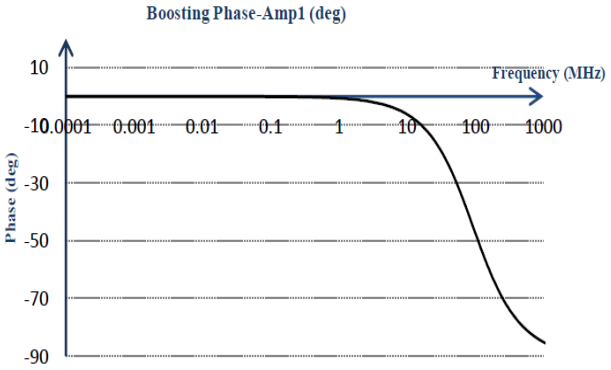

Figure 14: Boosting Amp1 Phase Plot

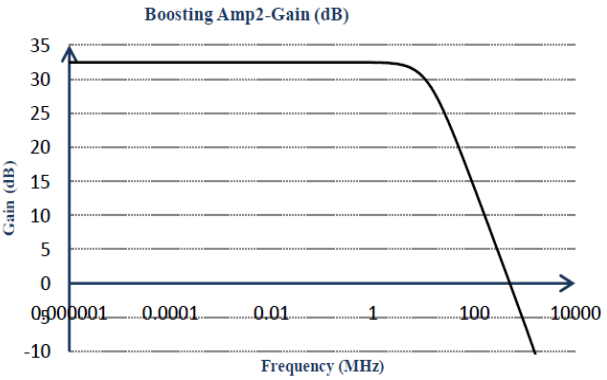

Figure 15: Boosting Amp2 Gain Plot

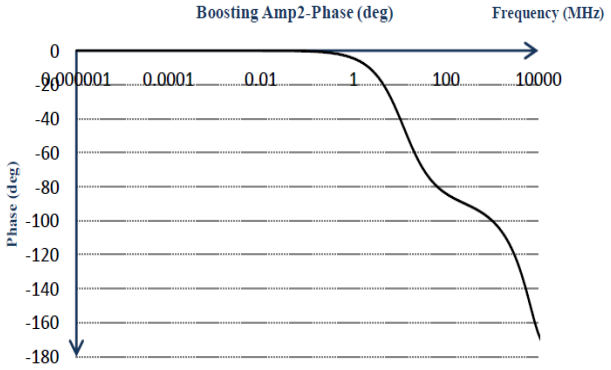

Figure 16: Boosting Amp1 Phase Plot

TABLE II
BOOSTING AMPLIFIERr NO.1 RESULTS.

Performance Metrics	Simulated Value
f_u	393.4 MHz
BW_{3dB}	11.45 MHz
$DC-gain$	30.98 dB
PM	89.93 deg
$i_{V_{dd}}$	11.44 mA

TABLE III
BOOSTING AMPLIFIER NO.2 RESULTS.

Performance Metrics	Simulated Value
f_u	512.9 MHz
BW_{3dB}	12 MHz
$DC-gain$	32.48 dB
PM	94.25 deg
$i_{V_{dd}}$	15.5 mA

IV. RESULTS

The OpAmp is placed in the test bench illustrated in Figure 17 to be simulated and its parameters are calculated. Sampling capacitor is 4 times of feedback capacitor to provide gain of 4 for the MDAC (C_s/C_f=1). The noise voltage at the output of amplifier falls below 0.2LSB by Choosing C_s larger than 100fF for 10-bit ADC and 2pF for 12-bit ADC. C_l is chosen 2pF to simulate the load effect of next stage.

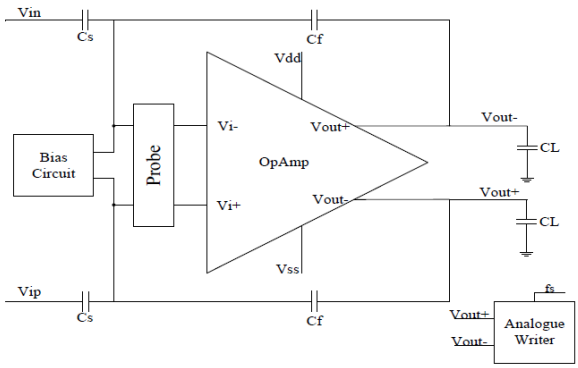

Figure 17. OpAmp Test Bench

The probe module shown in the figure17 is placed in the feedback to break the loop when using the stability simulator (stb Analysis in Analog Design Environment) in Cadence. The stability simulator calculates loop-gain and loop-phase and is used to determine stability of the circuit around the loop.

The analog writer module is responsible for sampling the output data and dumping the sampled data into a text file. The text file can be read by Matlab and used for OpAmp's performance determination.

The OpAmp reaches 72dB DC-gain and the gain stays constant when the output swing increases up to the point that the output voltage clips. In Figure 18 and Figure 19 the open-loop gain and phase of the designed OpAmp is shown. Other performance metrics of the amplifier are simulated and summarized in Table 4:

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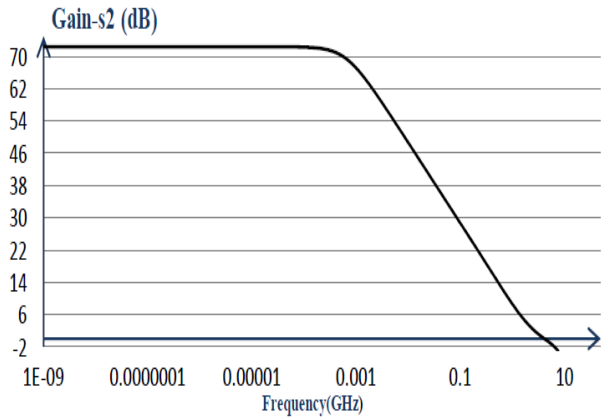

Figure 18. Open-Loop Gain Plot of 2-stage, Gain Boosted OpAmp

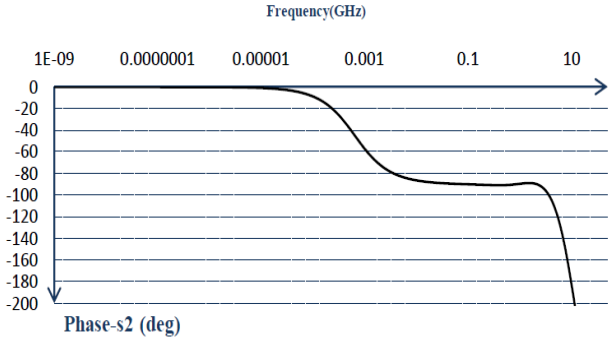

Figure 19: Open-Loop Phase Plot of 2-stage, Gain Boosted OpAmp

TABLE 4-4
OPAMP SIMULATED PERFORMANCE METRICS

Performance Metrics	*Simulated Value*
f_u	*4.077 GHz*
BW_{3dB}	*640.4 KHz*
DC – gain	*72.35 dB*
PM	*76.01 deg*
$i_{V_{dd}}$	*123.3 mA*
SNR(for fs up to 320 MHz)	*>100dB*
Slew Rate	*22.5kv/µs*

Settling behaviour of the OpAmp, for being used in 12-bit or 10-bit pipelined ADC and placed in the 2.5 bps MDAC (amplification factor of 4) is verified. The simulation is done applying low frequency (1MHz) pulse waves with different amplitudes to the input and recording the settling time of the amplifier, when the OpAmp settles to half of the corresponding LSB.

Table 5: Settling Time of The OpAmp for Being Placed in 12-bit ADC LSB for 10-bit ADC with maximum 1.4v input voltage (differential peak to peak voltage) is 1.37mv and settling between the 683.6µv (half LSB) error from final value is evaluated. Table 6: Settling Time of The OpAmp for Being Placed in 10-bit ADC.

TABLE V
SETTLING TIME OF THE OPAMP FOR 12-BIT ADC

$V_{in-pp-Diff}(mv)$	$V_{out-pp-Diff}(mv)$	$T_{settling}(ns)$	$f_{s-max}(MHz)$
200	800	2.243	356.66
240	960	2.92	273.97
280	1120	3.27	244.65
320	1280	3.56	224.71
360	1440	3.86	207.25

TABLE VI
SETTLING TIME OF THE OPAMP FOR 10-BIT ADC

$V_{in-pp-Diff}(mv)$	$V_{out-pp-Diff}(mv)$	$T_{settling}(ns)$	$f_{s-max}(MHz)$
200	800	2	400
240	960	2.25	355.55
280	1120	2.57	311.28
320	1280	2.79	286.74
360	1440	2.84	281.7

CONCLUSIONS

In this work, an OpAmp with very high gain-bandwidth, high linearity and Signal-to-Noise ratio has been designed. The performance of the OpAmp is verified using Cadence simulation and Matlab and they satisfy the requirements on the amplifier of a 2.5bps MDAC in a 12-bit pipelined ADC. The amplifier is placed in a pipelined ADC which is also designed in transistor level. The main focus in this work was the OpAmp design to meet the high requirements needed for 2.5 bps MDAC and provide an inter-stage gain of 4 in the ADC. The OpAmp should provide a high closed-loop bandwidth to accommodate a high speed ADC with very low gain error to match the high resolution definition.

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