A Low Power, Leakage Reduction, High Speed 8-Bit Ripple Carry TSPC Adder using MTCMOS Dynamic Logic

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Abstract- **In Every IC design adder is basic building block to perform arithmetic operations. This paper presents new TSPC (True Single Phase Clock) adder for 8-bit operations using MTCMOS dynamic logic. The proposed design comprises of 18-transistors instead of 21-transistors used in existing design. The design also has advantage of power trade-off where it consumes only 384.5pW with reduced leakage power from 96 to 99% in sleep mode of circuit operation. MTCMOS Dynamic technology includes both HVT(High V_{TH}) and LVT(Low V_{TH}) Cells. HVT Cells are used as power switch and LVT Cells are used for actual logic operation to increase speed performance of the circuit. Conventional CMOS logic has more static power dissipation. In this paper MTCMOS dynamic logic is introduced to eliminate static power dissipation. The proposed design is implemented using 45 nm technology with supply voltage(V_{DD}) of 1V.**

Index Terms-**TSPC, CMOS, MTCMOS, Power, Sleep mode**

I. INTRODUCTION

Adder is a very essential component in digital computing systems such as DSP processors ,FPGAs, Floating-point processors. In Microprocessors, adder has special role as it is used for address generation for data access as well as it used as functional blocks to design Multipliers. In recent trends VLSI design technology has scaled down from micron, deep sub-micron to nanometer technology [1]. Power supply is an important factor of interest in research area where the scaling down key lies based on minimizing the threshold voltage of MOS-transistor. CMOS technology[2] is being used for less power dissipation,but, it has a limitation of static power dissipation and more leakage power due to single threshold voltage (V_{TH}) transistors. There are many technologies that have more than one threshold voltages(V_{TH}), like dual-VTCMOS, MTCMOS, VTCMOS and etc. Among which MTCMOS logic is most useful approach for less power consumption and less leakage power.

The TSPC (True Single Phase Clock) adder has only single phase clock for easy clock distribution throughout the logic and avoids clock skew problem effectively. The circuit will be evaluated when clock signal is high and tristated when clock signal is low. This paper presents simulation results for single bit full adder as shown in section IV and the proposed design has conclusion in section V.

II. MTCMOS DYNAMIC LOGIC

Multi threshold voltage CMOS (MTCMOS)[3] logic is to improve speed performance and less power consumption. Leakage reduction is also very important key parameter by using MTCMOS logic. With the help of this technology the portable systems like Laptop, Mobile phones etc have more battery life and backup time.
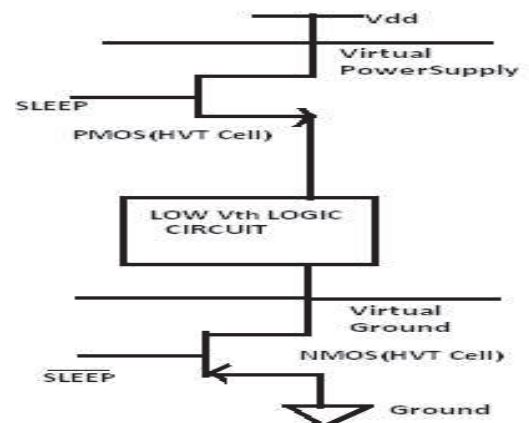

Fig 2.1 General MTCMOS Dynamic logic

In general a transistor has less threshold voltage (V_{TH}) will switch faster, a transistor has more threshold voltage(V_{TH}) will reduce static power dissipation.

The MTCMOS logic is composed of both transistors which have low threshold voltage(LVT cell) and high threshold voltage(HVT Cell). Fig 2.1 shows basic MTCMOS Logic in which HVT cells are used as power supply switches and LVT cells are used as actual logic operation to better speed performance. MTCMOS logic will work in two modes one being *active mode* in which

HVT cells (Sleep transistors) are switched to ON for logic evaluation. Second mode is *standby mode (idle mode) where* HVT cells (Sleep transistor) are switched to OFF state for reducing leakage power.

In general, MTCMOS logic has high V_{TH} PMOS transistors connected between Power supply (V_{DD}) and low V_{TH} logic,and high V_{TH} NMOS transistor is connected between low V_{TH} logic and ground. In this paper only high V_{TH} NMOS transistor is used as shown in Fig 2.2 for better performance and avoids bounce noise at ground.
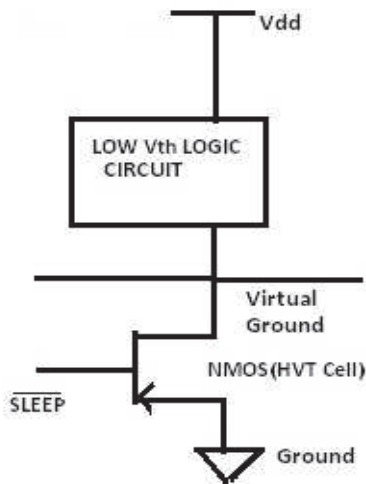

Fig 2.2 Single Sleep transistor MTCMOS Dynamic logic

III. PROPOSED SYSTEM

The proposed design has 18-transistors for one bit TSPC full adder shown in Fig 3.1.The existing design has 21 transistor with low performance [4], this design has decreased silicon area from 15 to 20 % with high speed performance and less power consumption. It has dynamic operation with the help of single clock signal. The output will be considered when the clock signal is high, and output is floated when the clock signal is low.
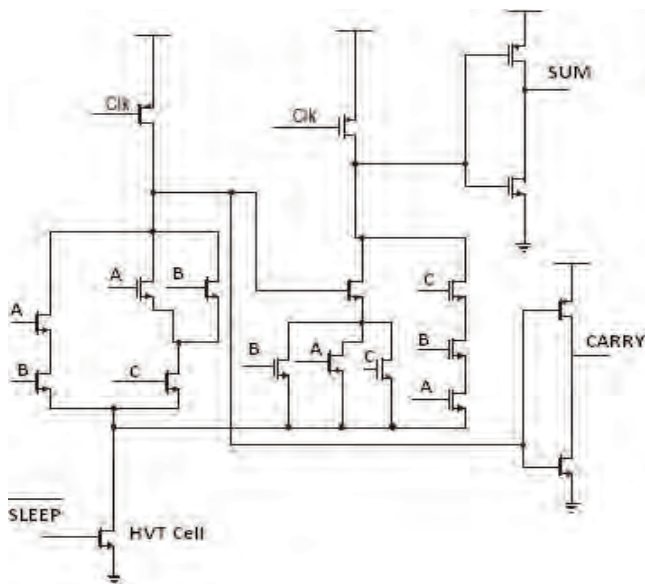

Fig 3.1 A Single bit TSPC adder with 18 transistors (Proposed)

The design logic built with low threshold voltage transistors (LVT) which has faster switching with no penalty of power consumption, and additional HVT cell is used for power switch i.e, if circuit is in idle mode the power switch will be OFF to save the power and to reduce the noise. The basic full adder logic has three inputs and two outputs shown in Fig 3.2
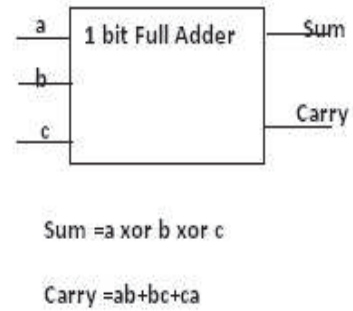

Sum =a xor b xor c

Carry =ab+bc+ca

Fig 3.2 One bit Full Adder block diagram

Ripple Carry Adder: Eight-bit ripple carry adder [5] is group of eight 1 bit full adders in which carry output of one full adder is one of the input for next full adder as shown in Fig 3.4. The design can be further used in hierarchical form to implement 16-bit, 32-bit adders. The 1-bit full adders are arranged in a manner from left to right where S_0 is LSB bit and S_7 is MSB bit. The carry is propagated through each adder, where the first full adder carry input is assumed as logic '0'.
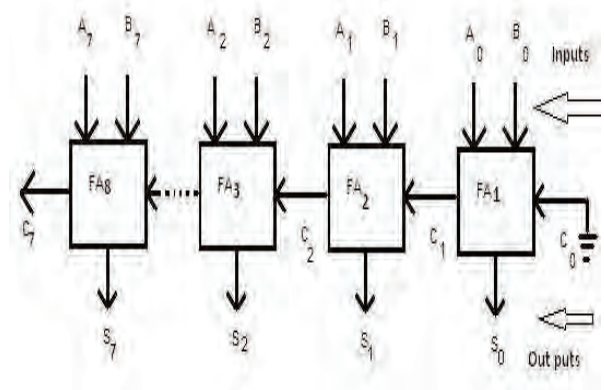

Fig 3.3 8 bit Ripple carry Adder block

IV. RESULTS

The 8-bit Ripple carry TSPC adder is designed and simulated using Cadence Virtuoso Schematic editor XL in 45 nanometer technology with supply voltage of 1V. The 1-bit TSPC full adder schematic diagram shown in Fig 4.1 is simulated using Cadence Analog Design Environment (ADE_L) [6].

A 4-bit adder is constructed from the four 1-bit full adders, and further a 8-bit full adder is constructed from two 4-bit full adders. First 1-bit full adder is simulated for different input combinations is shown in Fig 4.2. Consequently, design is verified for 4-bit, 8-bit full adders. The 8-bit adder block diagram is shown in Fig 4.3.
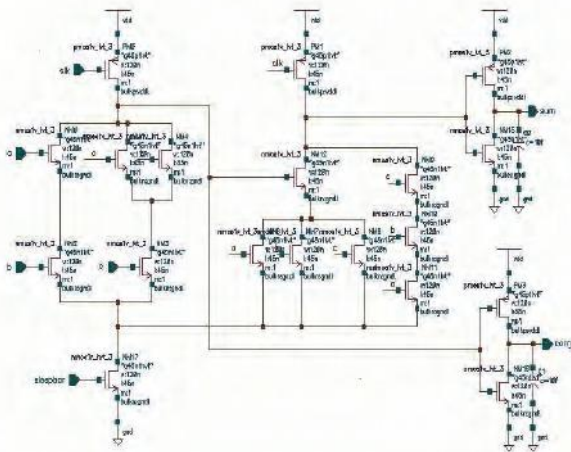
Fig 4.1 Single bit full adder schematic circuit

Fig 4.2 Single bit full adder simulation (input-output)

A 8-bit Schematic TSPC full adder is shown below, the design has two 4-bit adders and a carry. Carry is propagated from one 4-bit adder to another 4-bit adder.

Fig 4.3 Eight bit adder TSPC schematic using two 4 bit adders

The analysis for power dissipation, Leakage power and delay are performed. The Table-1 shows the delay statistics and comparision between CMOS and MTCMOS technology for TSPC adder[6]. TSPC adder Power and

Leakage power are tabulated in Table-2 for comparision of CMOS and MTCMOS technology.

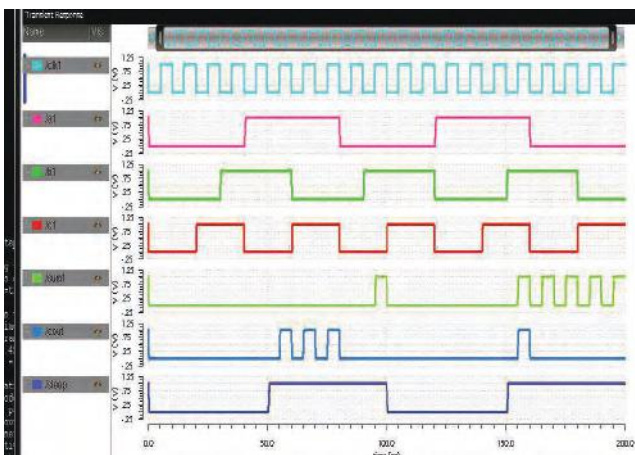
Fig 4.4 Leakage power comparison for CMOS and MTCMOS logic

Fig 4.5 Power delay product comparison for CMOS and MTCMOS logic
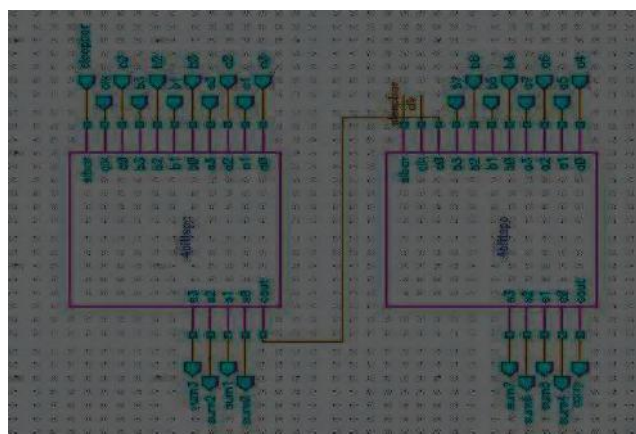
The Fig 4.4 and Fig 4.5 shows the graphs for Leakage power and Power delay product respectively, with comparison of Static CMOS and MTCMOS technology for TSPC adder, it shows good improvements in MTCMOS TSPC Adders.

Table-1
Comparison of Delay in CMOS and MTCMOS technology for TSPC adder

ADDER	Delay(pS)
CMOS-TSPC Adder	1430(existed)
MTCMOS-TSPC Adder	23.1(Proposed)

Table-2
Comparison of Power and Leakage power in CMOS and MTCMOS technology for TSPC Adder

ADDER	Average Power Dissipation (nW)	Leakage Power (pW)
CMOS-TSPC	1230(existed)	1452 (existed)
MTCMOS-TSPC	603.5(Proposed)	384.5(Proposed)

V. CONCLUSIONS

The 8-bit Ripple carry TSPC adder is designed by using MTCMOS logic and is simulated successfully using 45nm technology. The power dissipation, leakage power and delay are evaluated and compared. The proposed design shows more leakage power reduction. The leakage power is reduced by 96% to 99% in standby mode as

compared to the existing design[4]. The average power dissipation is also minimized. The active mode power dissipation 603.5nW(very less compared to existing design) is achieved with the help of single sleep transistor MTCMOS technology.

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