Design of Fast Locking ADPLL via FFC Technique using VHDL-AMS

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***Abstract*—In this paper ADPLL is designed via feed forward compensation technique and implemented using VHDL mixed signal Modeling technique in CADENCE. The use of mixed signal is that it can simulate SPICE codes, VHDL codes, Verilog codes and Verilog –A codes at a time using both SPICE simulator and Incisive Unified Simulator. The ADPLL consists of PFD, P2D, FDLPF, MD, LC and DCO blocks.The PFD block was designed using transistors. The FDLPF, LC and DCO blocks were designed using VHDL. The MD and P2D blocks were designed both by using VHDL and transistors. The implemented ADPLL achieves a fast frequency locking via the proposed feed-forward compensation algorithm, reduces power consumption and wide tunable frequency range.The designed ADPLL is very much suitable for SOC applications.**

***Index Terms*—All Digital Phase Locked Loop, Phase Locked Loop, Analog and Mixed Signal, System on chip**

I. INTRODUCTION

The PLL is a very important and common part of high performance microprocessors. These are widely used in clock generators for SOC microprocessors. In general, a PLL is made to work as an analog building block, but it is difficult to integrate an analog PLL on a digital chip. Therefore, the implementation of the loop filter and oscillator circuits in PLLs became popular.This type of PLL is called as All-Digital Phase Lock Loop [1].

Analog PLLs are more unsteady to noise and process variations. Digital PLLs allow a faster clock time. In high performance microprocessors, clock generation is achieved from digital PLLS[2].

ADPLL is a phase lock loop implemented in simple digital circuitry. It operates on finite precision digital words.The general ADPLL consists of four blocks. They are Loop fliter, Phase detector, Numerically controlled oscillator and Free running phase blcok as shown in the Figure 1.

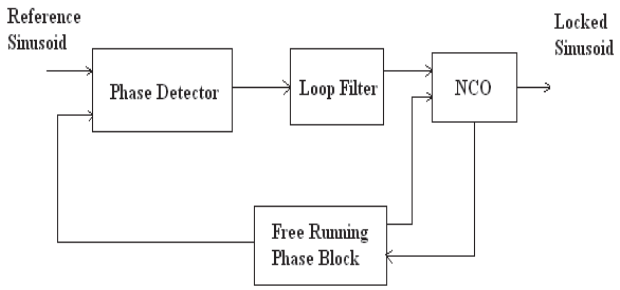

Figure 1. General ADPLL

The phase detector gives data about the difference in-phase and its two input signals. Digital multiplier creates a DC signal using reference signal. The created DC signal is proportional to the phase difference and a series of higher frequency components. The high-frequency terms which are created through multiplier are stored in the phase detector. The loop filter filters the stored data of the phase detector. The loop filter is usually a first or second order infinite impulse response (IIR) low-pass filter. The output of filter is passed through numerically controlled oscillator (NCO). The function of NCO is to adjust phase and frequency, by reducing the phase error to zero. This condition is called as phase lock. The frequency of the reference signal is within a defined distance from the free-running or open loop frequency of the NCO, known as pull-in range[2]. Frequency deviation between the two signals before they unlock is defined as hold range. Pull-in time is defined as the time taken to lock the loop. These parameters can be controlled by modifying the loop bandwidth of the ADPLL, but it cannot achieve good response only with these blocks. So, a new technique called feed forward compensation technique is implemented.

To improve the dynamic response of ADPLL Feed forward compensation is used successfully in many control systems. In PLL system design, the channel-switching event is disturbance from the point of view of controlled system. Since the disturbance is known, it is used to improve system performance.The block diagram of feed forward compensation is technique shown in the Figure 2.

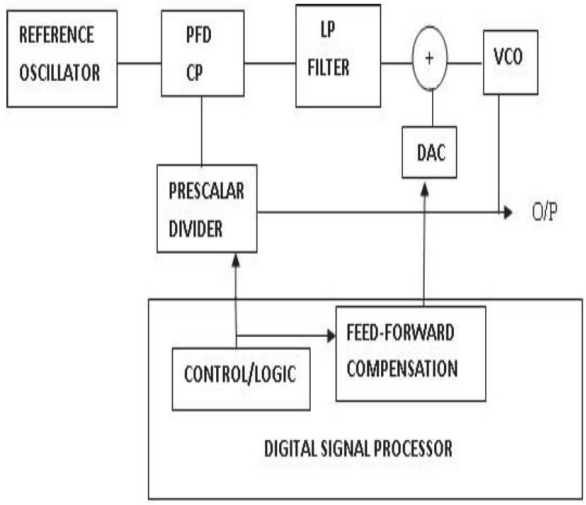

Figure 2. Feed Forward Compensation Technique

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In different divider ratio, dynamic response is made by the constant loop gain. This is done by multiplying the original loop gain with the known divider ratio.This data is used directly to adjust the VCO control voltage. The channel selection command from the DSP chip determines the divider ratio N. The desired VCO control signal is determined by a feed-forward controller. The converted VCO control signal from the analog domain is added to the feedback control signal.

In addition to the feed-forward control signal, feedback is necessary for feedback loop because of its unreliability result of VCO modelling error, DSP algorithm errors, DAC error, etc. The feedback loop is also used for reduction of close-in VCO phase noise, since the loop has a narrow bandwidth.

In this method, feed-forward controller decides the VCO control signal through the major component. The dynamic behaviour of the whole system has a comparatively small effect than the feedback loop. Change of loop gain by change of divider ratio will not affect the switching speed.

II. ARCHITECTURE OF EXISTING ADPLL

The architecture of existing All-Digital Phase Lock Loop by using FFC technique is shown in Figure 3. It consists of a phase/ frequency detector (PFD), a Modified Divider (MD), a Loop Control (LC), a ring type Digital Control Oscillator (DCO), a First-order Digital Loop Filter (FFDLPF), and a Phase to Digital converter (P2D). Here the existing ADPLL DCO has five clocks whose phases are different. The five clocks are named as CLK [0], CLK [1], CLK [2], CLK [3] and CLK [4]. CLK [1], CLK [2], CLK [3] and CLK [4] are written as for short CLK [4:1].

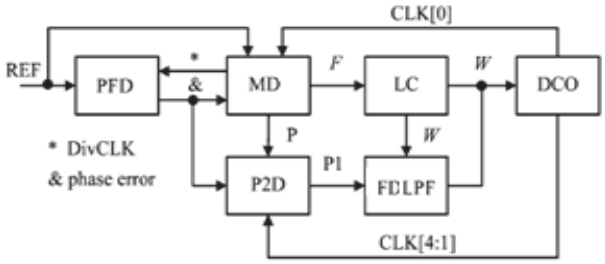

Figure 3. Architecture of Existing ADPLL with FFC

The designed blocks are connected in both feed forward and feed backward directions for the frequency acquisition mode and phase acquisition modes respectively. Here the reference clock is given by the user and the other clocks generated by the ring type DCO. Later these clocks are joined on the MD block to get the phase error and fed into the P2D to digitize the phase error. Here in existing ADPLL except LC all blocks are designed using transistors. Each block explanation is given below.

A. Design of PFD

The Phase frequency detector plays a significant role in PLL because it detects a difference in phase and frequency between the reference and feedback signal. The PFD output depends on both the inputs of phase and frequency. The design uses two flip-flops with reset features along with one AND gate, one OR gate and one Exclusive-OR gate.

The two D-inputs of flip-flops are connected to VDD. The two clock inputs of flip-flops are connected to Reference clock and Divide clock respectively. The output of flip-flops are Up and Down signals respectively. If the reference signal falls first, then up signal goes to high-level and down signal goes to low-level and if divide signal falls first, then down signal goes to high-level and up signal goes to low-level. If both the signals are at high-levels, then the two signals reset to low-levels of a feedback reset signal.

In the feedback loop output of AND gate is given to one of the OR gate input. The other input of the OR gate is, named as reset_div, and if it is, set of high-level, then the two D flip-flops in the PFD resets. The up and down signals are connected to a Xor gate to get the phase error signal as the output.The schematic design of PFD is shown in the Figure 4. Here the designed D-Flip-flops use transmission gates.

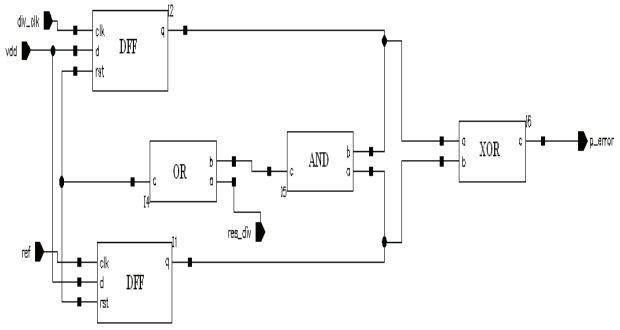

Figure 4. Schematic of PFD

B. Design of MD

It is the modified form of asynchronous frequency divider. Generally DIV used to generate the divider clock at high frequencies using DCO clock. In the modified DIV along with divider extra three modules were added. They are saveF module, Reset_syn module and T2D module.

The function of saveF module is to store the data according to the reference signals. It has two reference signals. One reference signal saves the value of the counter in the divider block and the other reference signal is used to store the counter value in the register block. Both the signals use raising condition. This module has a D-Flipflop and a register.

The function of the Reset_syn module is to readjust signals, to control operation of the divider. When the reset signal is at low-level, then the divider counts by the rising-edge of the clock and when it is at a low-level then the counter gets reset for the next counting operation and leaves the time for LC to tune DCO. This module consists of D Flip-flops, AND gate and OR gate.

The function of T2D module is to convert the phase eror to digital formats. It consists of a D Flip-Flop, two Registers and two adders. Here the sensed phase error by

the PFD is re-sampled on the falling edge of the clock and the value is stored in the registers during the rising edge of the signal phases because of the adoption of the feed-forward compensation algorithm. The schematic design of the MD is shown in the Figure 5. Here all the designed blocks use transistors.

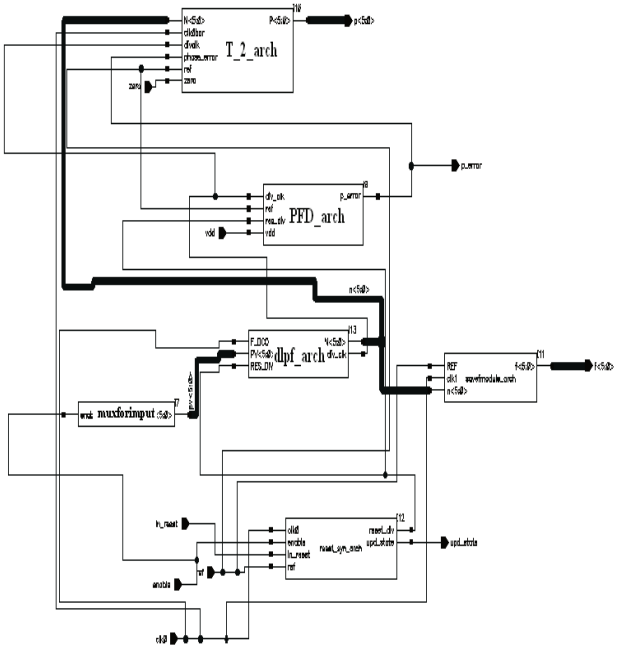

Figure 5. Schematic of Modified DIV

C. Design of LC

Loop Control is a digital processing section and when the ADPLL is initialized it performs two operations. First, the LC calculates Kf parameter coming from MD and second it generates W locked signal. The generated W locked signal is given to FDLPF and DCO.This block consists of four adders, one multiplier and one divider.

Two reference cycles are needed to obtain the parameter Kf, from the algortihm. The values of F1 and W1 are obtained from the first reference clock. The values of F2 and W2 are obtained from the 38 reference cycle. By division operation, Kf value is calculated. The dividend is ΔW=W1–W2 and the divisor is ΔF=F1–F2. The LC predicts the code W from the obtained Kf. The divider is used to divide A and B values that mean ΔW divided by ΔF [1]. Here VHDL codes are written for all the blocks. The symbol generation of LC using VHDL is shown in the Figure 6.

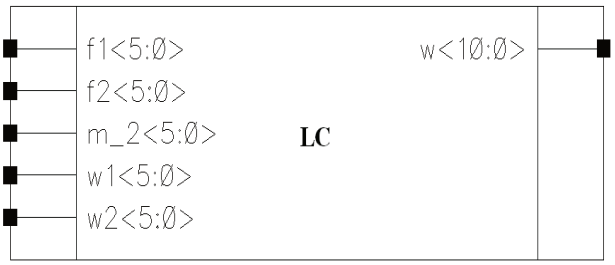

Figure 6: Symbol generation of LC

D. Design of DCO

The Digital controlled oscillator consists of both digital-to-analog converter and a Voltage controlled oscillator. The DAC changes input to the voltage Vc based on the input code. The changed voltage Vc controls the frequency of the voltage controlled oscillator. The DCO design includes a delay cell and voltage controlled cell for the conversion and controlling of frequency. The designed delay cell consists of two inverters and a modified NOR cell. The output of the delay cell will be at low-level when the input run signal turns to high-level during off state of the PLL. Due to this condition the power reduces. The voltage Vc controls the frequency of the VCO, when the signal run is at low-level. If the voltage Vc increases the delay time, then delay cell time decreases and the frequency of the VCO increases. The schematic design of the DCO cell is shown in Figure 7. Here all the blocks are designed using transistors.

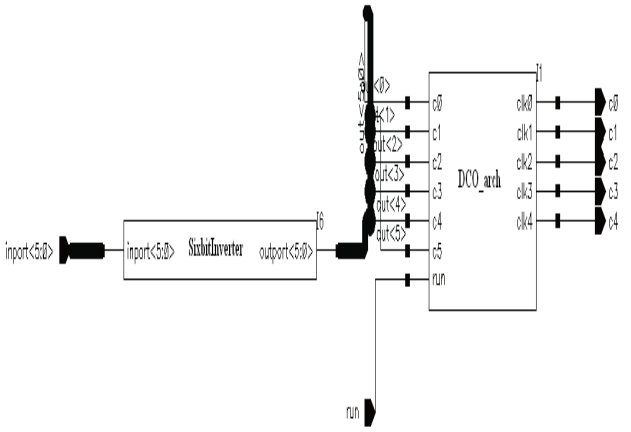

Figure 7. Schematic of DCO

E. Design of FDLPF

This is a First order digital loop filter and consists of two parameters. It consists of two adders, one multiplexer and one inverse block. It gets a W locked signal from LC and phase error signal p1 from P2D as the inputs. When the select signal of the multiplexer is set to high-level, then the code predicted by the LC is inserted into the integral path. The output of the FDLPF block is fed to the input of the DCO. The schematic design of FDLPF is shown in Figure 8. Here all the designed blocks use transistors.

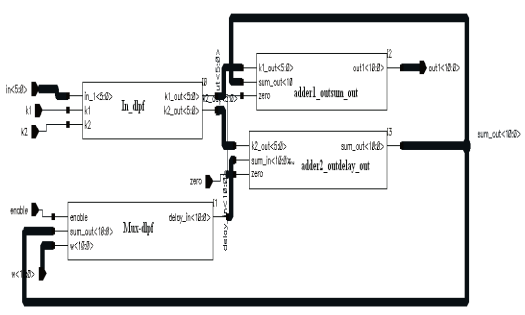

Figure 8. Schematic of FDLPF

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F. Design of P2D

The P2D is used to reduce the quantization error of the MD. This is possible only by adding the four DCO clocks through counter process. The design consists of four 2-bit counters, four comparators, one multiplier and two adders. The detected phase error of MD is connected to the P2D for its observation.

The generated clocks from DCO are connected to four clocks for triggering the counter. The two lowest LSB's of the counter are compared by four comparators which are connected to the output of the counter. Compared result is then multiplied by 5 and added to the sum of the comparison results and then forwarded to the FDLPF. The schematic design of P2D is shown in the Figure 9. Transistors are used for designing entire blocks.

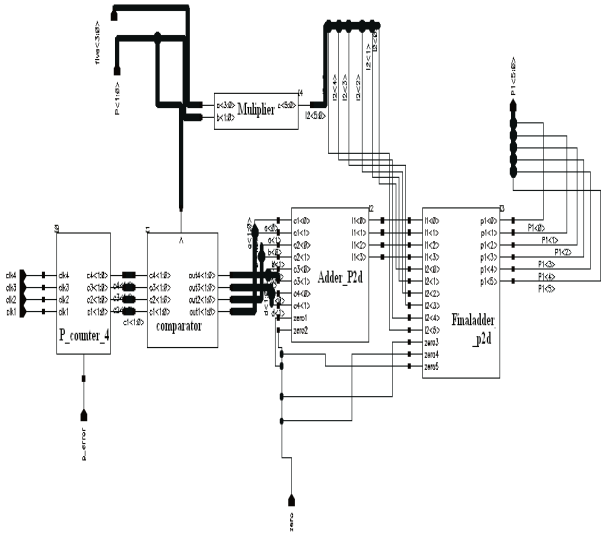

Figure 9. Schematic of P2D

III PROPOSED ADPLL

In Proposed ADPLL, both transistors and VHDL are used for designing MD and P2D blocks.VHDL is only used for designing FDLPF and DCO blocks. The PDF design is also included inside the MD block. The schematic of the proposed ADPLL design is shown in the Figure 10.

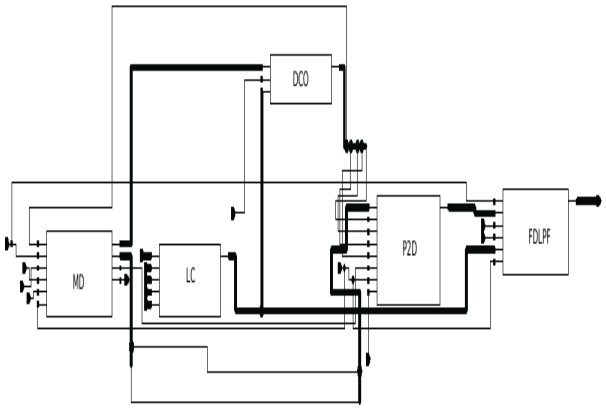

Figure 10.Schematic of proposed ADPLL

A. Design of MD

The MD designed here consists of T2D module, PFD module, SaveF module, Reset_syn module, Divider module and a multiplexer for input divider. Here VHDL codes were used for designing T2D module, Divder module and multiplexer for input divider modules. Flip-flops and registers are used for designing PFD and SaveF module which in turn uses CMOS transistors. The symbol generation of MD using VHDL and transistors is shown in the Figure 11.

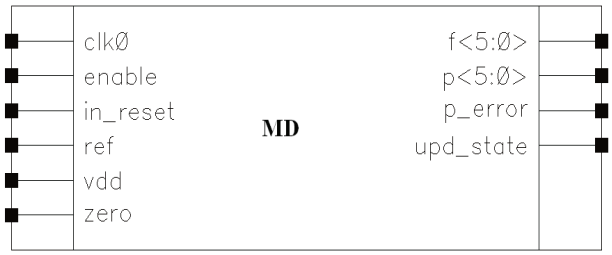

Figure 11. Symbol generation of MD

B. Design of P2D

The P2D designed here consists of one multiplier, four bit-counter, four bit-comparator and two types of adders. Here VHDL is used for designing multiplier, four bit-counter and four bit-comparator. The two types of adders were designed using half-adder, full-adder and flip-flops which are intern designed using gates. The symbol generation of P2D using VHDL and transistors is shown in the Figure 12.

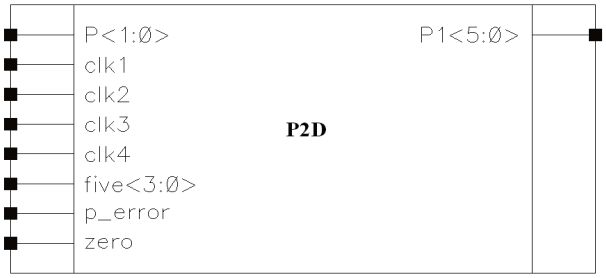

Figure 12. Symbol generation of P2D

C. Design of FDLPF

The FDLPF designed here consists of two types of adders, one multiplexer and one inverse block. Here one adder generates the sum and the other one used to generate output delay. Here all the blocks are designed using VHDL. The symbol generation of FDLPF using VHDL is shown in Figure 13.

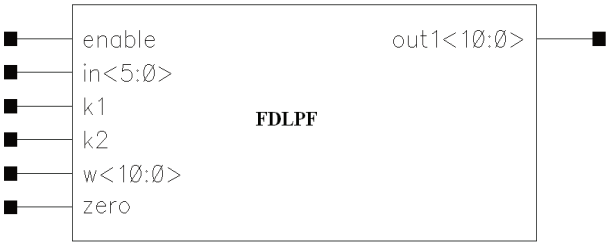

Figure 13. Symbol generation of FDLPF

D. Design of DCO

The DCO designed here consists of a delay cell and voltage controlled cell. Here designed block uses VHDL. The symbol generation of DCO using VHDL is shown in the Figure 14.

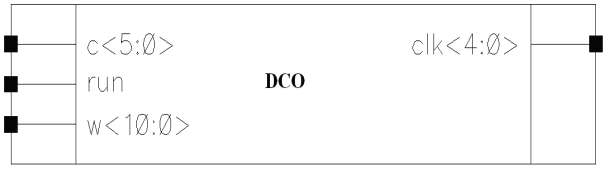

Figure 14. Symbol generation of DCO

IV. RESULTS

The entire designed ADPLL block uses are Cadence Virtuoso Schematic XL Editor and Cadence VHDL AMS Editor. The designed schematics use gpdk90nm technology. The spectre SPICE simulator using Cadence Analog Design Environment L-Editor is used for simulating the designed schematics. The Cadence Incisive Unified Simulator is used for simulating VHDL designs. The Cadence AMS Simulator is used for simulating entire ADPLL blocks. The simulation result of ADPLL shown in Figure 15.

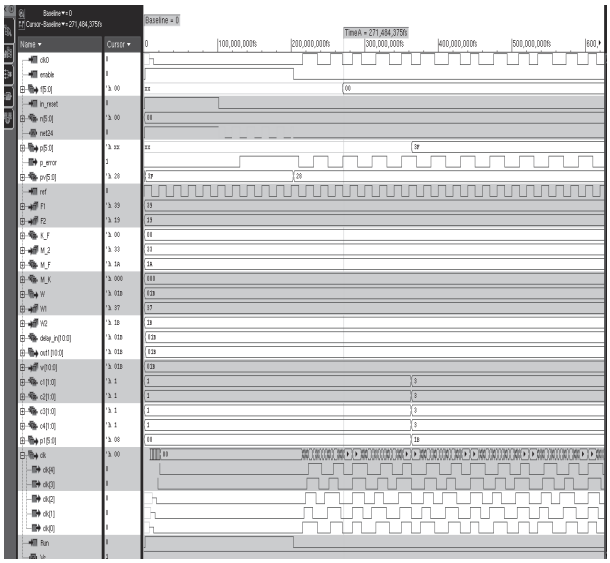

Figure 15. Simulation Result of ADPLL

Performance comparasions between existing and proposed ADPLL is shown in the Table I.

TABLE I

PERFORMANCE COMPARASIONS

Performance Parameter	Existing System	Proposed System
Process	0.18um	90nm
Power	11.394mw	962.75uw
Locking Time	3 cycles	2 cycles
Max.Frequency	416MHZ	625MHZ
Min.Frequency	4MHZ	10MHZ

V. CONCLUSIONS

In this paper proposed fast locking ADPLL uses VHDL-AMS. By using a feed forward compensation algorithm fast locking is achieved. The gpdk90nm technology is used to implement the design. The ADPLL frequency range is 10MHZ-625MHZ. The waveform results show that the ADPLL can complete frequency locking in 2 reference cycles, when locking to 271MHZ with 962.75uw power consumption. But in the existing system, the locking is achieved nearly after 3 cycles. So, the proposed ADPLL with feed forward compensation technique has more advantages than the existing methods. In LC block modifying with Digital Proportional integral controller (PI) locking time is reduced and used in low power application. Thus the fast and effective locking time is achieved based upon simulation.

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