Design of Sub-Threshold Source Coupled Logic Families for Low Power Applications

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***Abstract*--In this paper Standard cell libraries of Sub threshold Source Coupled Logic (STSCL) are developed in 90nm and 45nm technology using cadence virtuoso at 1V power supply. These gates are further used to design digital subsystems like Arithmetic logic unit (ALU) which work at low supply voltages and consume less power with promising performance.**

***Index terms*-- Sub threshold Source Coupled logic, MOS current mode logic, Binary Decision Diagrams.**

I. INTRODUCTION

For mixed signal application, MOS Current mode logic (MCML) or Sub-threshold Source coupled logic (STSCL) have become popular since past decade for high speed and high performance applications. They are a good alternatives for conventional CMOS technologies. Sub-Threshold Source Coupled logic (STSCL) is a good match for low power chips and systems which are used for both technical and business needs like hand held devices [1].

STSCL circuits have reduced switching noise and voltage swing due to its differential nature and immunity to common mode noise and low power dissipation at high frequencies when compared to CMOS STSCL circuits are used in different applications where ultra low power is required because all the transistors in the circuit are operated in sub threshold region and the circuits can operate at very low voltages with constant bias current down to 20p A which is much lesser than CMOS gates.

Reduction of power dissipation may increase the delay of each gate making power dissipation, logic swing and speed being tradeoffs in the design. This paper provides a novel logic families of STSCL which work on differential logic principle with equal and opposite complementary signal outputs with improved noise reduction, less sensitivity to power supply and more freedom for designing the logic gates. Because of these varied advantages STSCL gates have been implemented in many applications like Oscillators, Adders, Multipliers, ADCs, PLL, Microprocessors etc.

II. SUB-THRESHOLD SOURCE COUPLED LOGIC

A. Overview

Any STSCL logic circuit has three main elements: constant current source, source coupled NMOS pairs (pull down network) and the resistive load as shown in figure 1. The logic operation is done in current domain where NMOS switching network is the heart of the circuit which acts as differential pair and decides the logic operation of the gates depending on the arrangement of the these NMOS transistors [2] .It means that here a constant bias current is directed between two output branches which is converted to the output voltage by load resistors.

The speed of switching between differential pair NMOS transistors is very high and is proportional to the bias current of the circuit. In STSCL the load resistors are replaced by PMOS load with the bulk and drain connected as they give high resistance for less tail bias current (bias current) and also occupy less area [3]. This helps STSCL to work in sub threshold region.

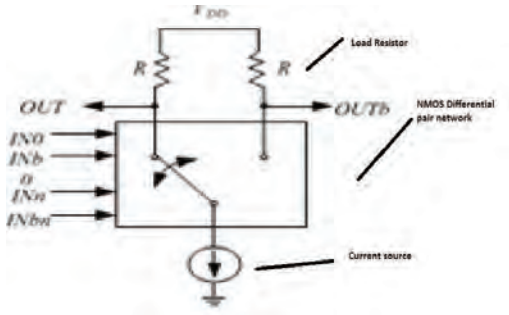

Figure 1 : General topology of STSCL circuit

Thus the output voltage swing V_{swing} of STSCL is decided by the tail bias current I_{SS} and the resistive load R_L.

$$V_{swing} = R_L \times I_{SS}$$

Good voltage swing and tail bias current more than junction leakage current are enough to implement good STSCL circuits with higher load resistances in order of MΩ. The power dissipation of STSCL circuits are constant and does not depend on the clock frequency, it is given by [4]

Power dissipation = V_{DD}. × I_{SS}

The output time constant is given by

$\tau_{SCL} = R_L \times C_L = V_{SW} / I_{SS} \times C_L$

where C_L is total output capacitance.

The power delay product is given by

$PDP_{SCL} = \ln(2) \times V_{DD} \times V_{SW} \times I_{SS} \times C_L$

Thus from above equations it is understood that the delay in the STSCL circuits depends on ISS and not on VDD which is not possible in CMOS topologies, hence the delay can be controlled without influencing PDP. Because of this STSCL can be designed with wide range of bias currents for different speeds and even very low power supplies. STSCL logic gates can work with very low tail bias currents from 10 p A to 100 pA and the power dissipation of these circuits can be reduced to 1fJ/gate which makes STSCL circuits very useful for low voltage-low power applications.

B. Binary Decision Diagrams and STSCL gates

The simple STSCL gate is the inverter/buffer which consists of differential NMOS pair whose sources are connected and given to current source I_{SS} called as tail bias current. The inputs of the STSCL circuit is given to A and its complement $\bar{A}$ applied to NMOS Transistors MN1 and MN2 as shown in figure 2

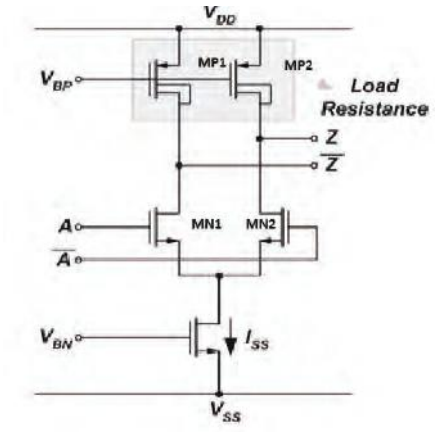

Figure 2 STSCL inverter/buffer

The PMOS transistors MP1 and MP2 act as active loads .The lower and higher digital logic levels are V_{OH}= V_{DD} and V_{OL}=V_{DD}- I_{SS} .R_L .So the logic voltage swing is

$\Delta V = V_{OH} - V_{OL} = I_{SS} . R_D$

After the design of the inverter/buffer circuit, next the basic logic gates like AND/NAND, OR/ NOR XOR/XNOR gates and DFF can be designed by developing a library of cells using the binary decision diagrams (BDD). STSCL logic gates cannot be designed like CMOS logic because STSCL consists of complementary inputs and the output logic level is determined by the switching of the current. BDD use graph algorithms for easy manipulation and have one to one correspondence with STSCL logic networks [5]

In the STSCL circuit, each differential pair represents a node, each interconnection represents an edge and the output nodes represent '0' and '1' leaf nodes of BDD. Thus BDD is directed graph which uses some notations like the result of logic function is shown by the leaf nodes and internal nodes represent one variable, each edge (0 or 1) shows a value assigned to the variable for that particular node from where it is beginning. The graph is a replica of the truth table of the logic gate by going through the path defined by the edges with the weights assigned to their associated variables in that line of the truth table.

For example in the BDD of AND gate as shown in figure 3 and Table 2, consider the combination of A=1 and B=0 the path in BDD results in logic '1'. Like this all the combinations in the truth table are drawn in the graph. The BDD and truth tables of OR gate and XOR gate is shown in figures 4 and 5 below.

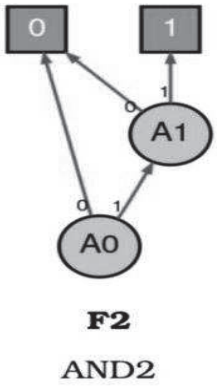

Figure 3 BDD of AND gate

TABLE 1
TRUTH TABLE OF AND GATE

A	B	out
0	0	0
0	1	0
1	0	0
1	1	1

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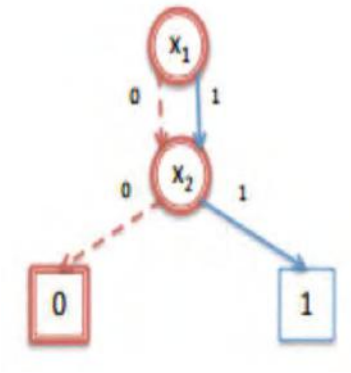

Figure 4 BDD of OR gate

TABLE 2
TRUTH TABLE OF OR GATE

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

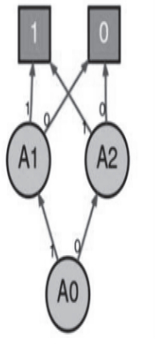

Figure 5 BDD of XOR

TABLE 3
TRUTH TABLE OF XOR GATE

Inputs		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

III. Implementation And Results

A Circuit Implementation

In this section, different standard cell libraries are designed using STSCL logic to estimate the effectiveness of the proposed STSCL logic [6]. All these logic gates shown in figure 6 are simulated in cadence virtuoso 90nm and 45nm technology and their delay and Power consumption is measured.

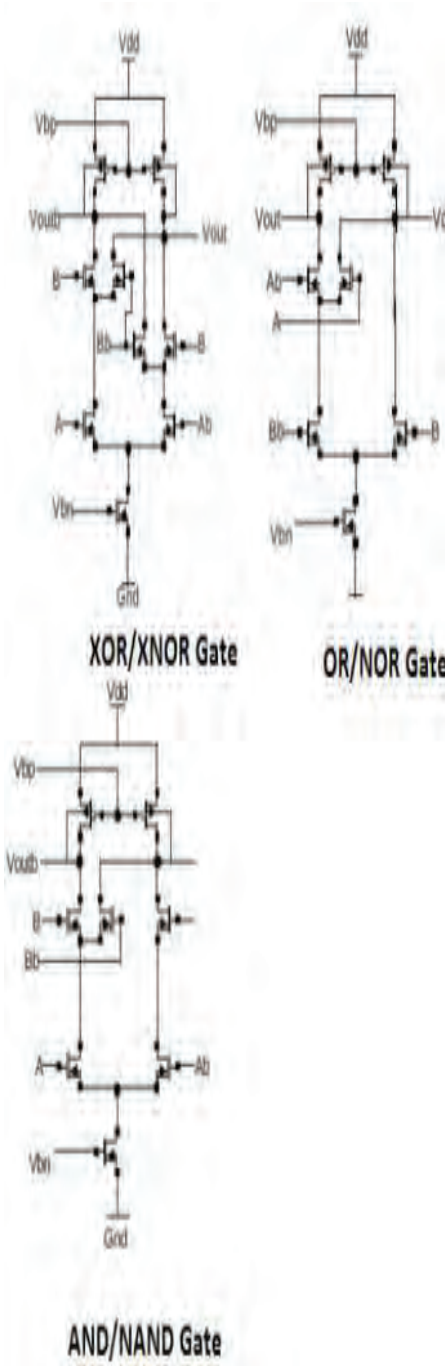

Figure 6 STSCL based XOR/XNOR, OR/NOR, AND/NAND gates

Digital subsystem like 1 bit Arithmetic and logic unit is designed using 8×1 MUX .Full adder and full sub tractor circuits which are designed using STSCL logic and verified as shown in figure 7. For 1 bit ALU conventional

structures are used and the supply voltage for STSCL 45nm CMOS technology for 1 bit ALU design is 1V.

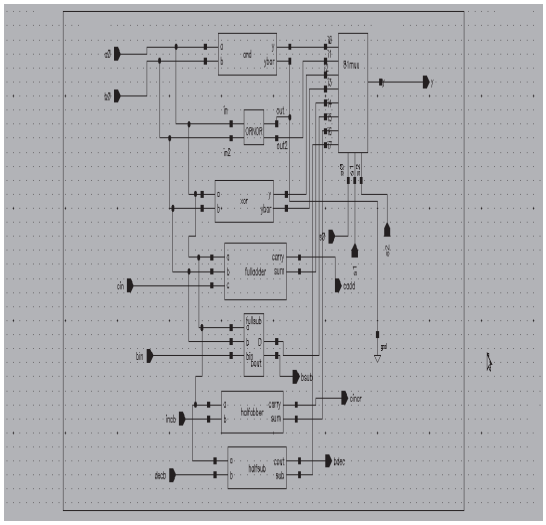

Figure 7 Schematic of 1 Bit ALU

B Results

The simulation results of all STSCL logic gates is given in the figures 8,9,10 below. The simulation results of 1 Bit ALU is given in the figure 11 shown below.

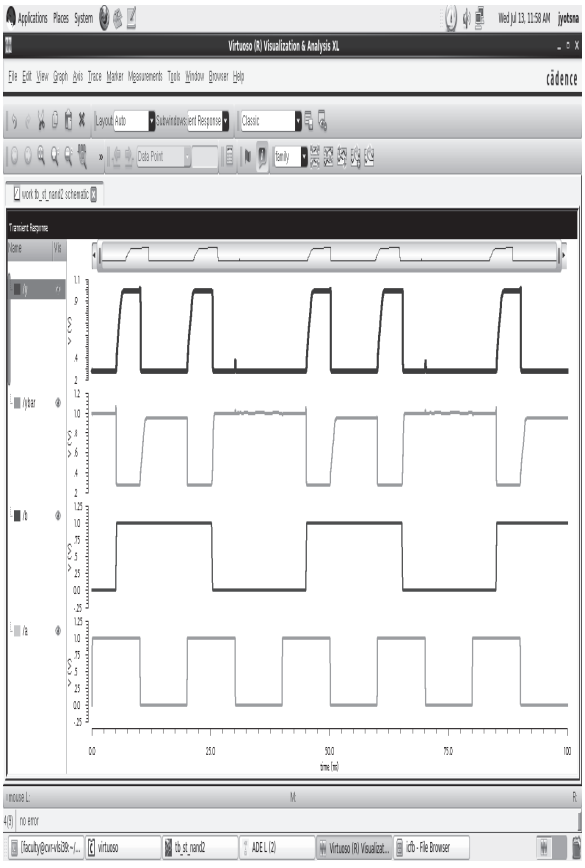

Figure 8 Output of NAND/AND Gate

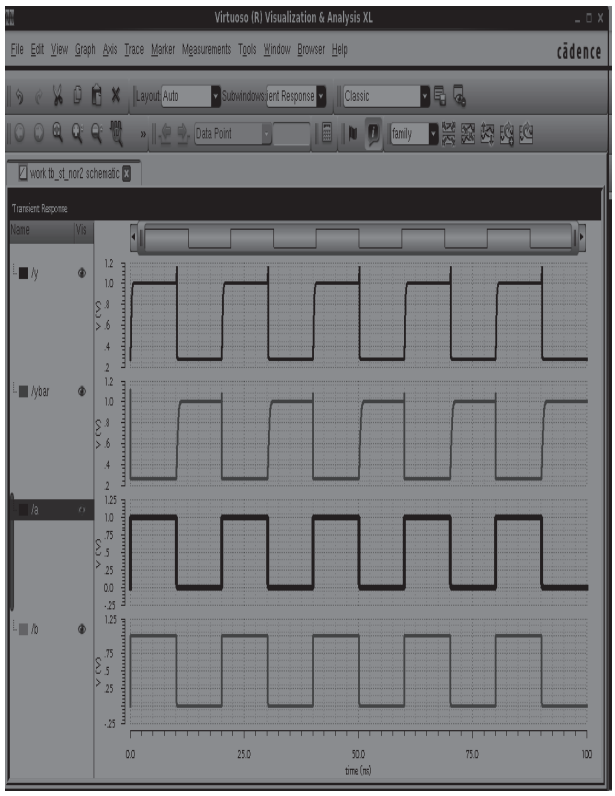

Figure 9 Output of OR/NOR gate

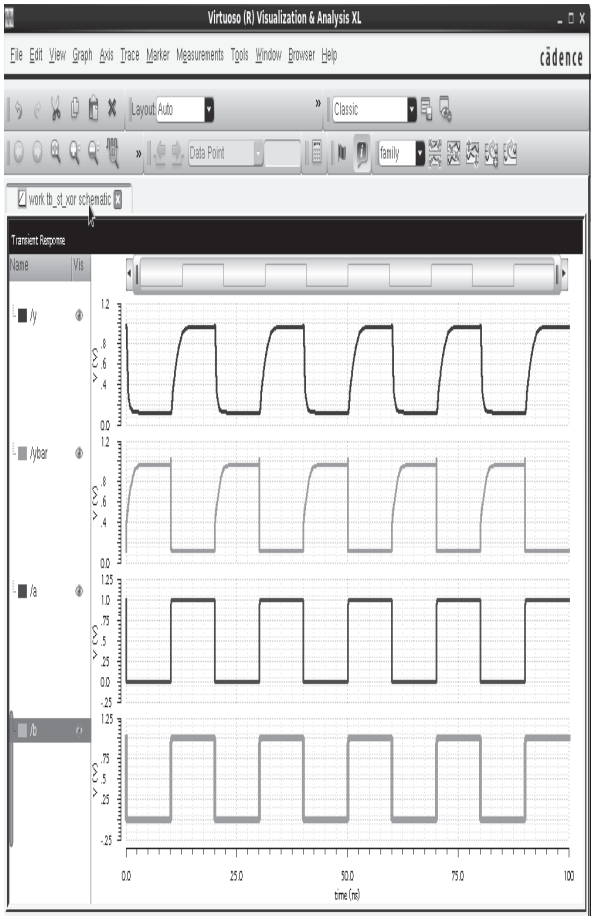

Figure 10 Output of XOR/XNOR Gate

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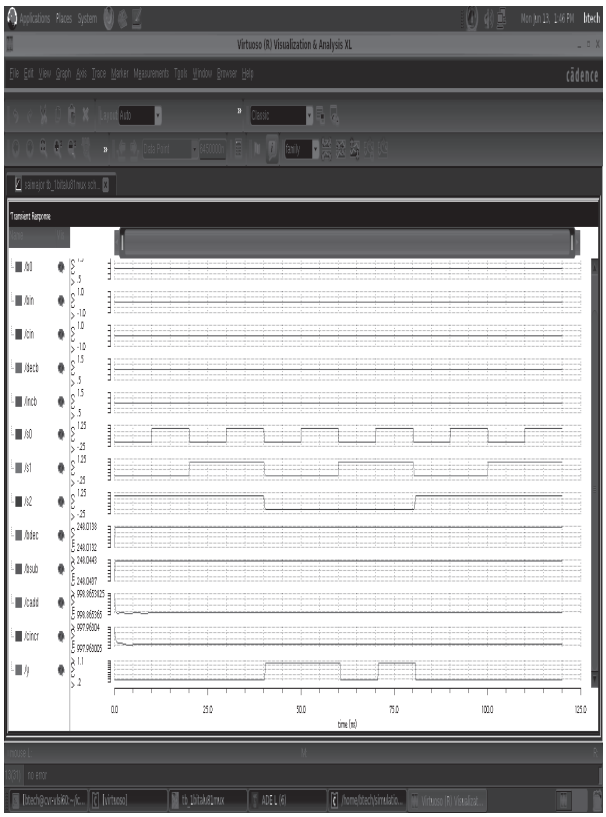

Figure 11 Output of 1 Bit ALU

The power and delay calculations of STSCL logic gates in. 90nm and 45nm technology is compared below in Table 3

TABLE 3

POWER AND DELAY OF BASIC STSCL GATES

Basic Gates	Power and Delay in 45nm		Power and Delay in 90nm	
	Power(W)	Delay(sec)	Power(W)	Delay(sec)
Inverter	7.28E-6	25.32E-12	912.4E-6	1.379E-12
OR	18.76E-6	19 .88E-9	11.1E-6	49.96E-9
AND	22.96E-6	10,04E-9	13.19E-6	30.24E-9
XOR	9.17E-3	20.28E-9	21.9E-6	25.21E-9
NOR	18.76E-6	10.1E-9	11.1E-6	40.0 E-9
N AND	22.9E-6	28.33E-12	27.57E-9	22.57E-9
XNOR	9.17E-3	1 5.24E-9	21.9E-6	126.72E-12

IV. CONCLUSIONS

In this paper a new method of implementing ultra low power STSCL circuits is proposed. Library of STSCL standard cells in 90nm and 45nm CMOS technology is presented and compared. These libraries are used to redesign the existing CMOS digital blocks. This approach benefits from small size PMOS load devices and implements the circuits in nA range. However the area occupied by STSCL circuits is slightly higher because of the differential logic of the circuit. Thus STSCL is a promising alternative to standard CMOS logic for high performance and low power applications.

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