Low-Power Successive Approximation ADC with 0.5 V Supply for Medical Implantable Devices

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Abstract- **In this paper the design and implementation of very low-power Analog to Digital converter, which is used in medical implantable devices like pacemakers et al. The ADC uses a successive approximation architecture and operates with a low supply voltage is 0.5 V. A suitable dynamic two-stage comparator is selected due to its energy efficiency and capability of working in low supply voltages. This ultra-low power 10-bit ADC is Implemented in a 90nm Complimentary Metal-Oxide semiconductor (CMOS) technology, this ADC consumes 12nW at supply voltage of 0.5V and sampling frequency of 1kS/s with figure of merit 0.14pJ/Conversion. It has a signal-to-noise-and-distortion (SINAD) ratio of 60.29dB and effective-number-of-bits (ENOB) of 9.72 bits.**

Index terms— **Pacemaker, Analog-to-digital conversion, CMOS, low power, low voltage, two stage dynamic latched comparator, binary search algorithm for successive approximation.**

I. INTRODUCTION

Successive approximation analog-to-digital converters have recently become very attractive in low-power moderate-resolution/ moderate-speed applications such as implantable bio-medical devices or wireless sensor nodes due to their minimal active analog circuit requirements and low power consumption. As an integral part of the medical implantable devices like the Pacemaker, a moderate resolution) with low power dissipation Analog-to-Digital Converter is required[1].The converter should also operate from a low power supply to drive its integration with low-power digital circuitry. In this paper, we present an analog-to-digital converter (ADC) that satisfies requirements of Pacemakers. The Architecture of a Successive Approximation ADC is shown in Figure.1, It consists of a sample-and-hold (S/H) circuit, a Comparator, a Successive Approximation Register (SAR), and a digital-to- analog converter (DAC). The operation of the Successive Approximation-ADC starts with the sampling phase, the analog input signal is sampled by the S/H circuit and this sample is given to comparator. During the conversion phase, the SAR and control logic perform a binary search algorithm, which constructs the binary word. This binary word is fed through the DAC; then DAC produced value is an equivalent analog value which is exactly half of the DAC reference value. This is compared with the sampled analog input signal by the comparator. The comparator gives either VDD or Zero, if $V_H > V_A$ or $V_H < V_A$ respectively. The same procedure is repeated for generating the reference voltage and it is compared with the sampled value and finally set the input Digital data for Successive Approximation Register in N clock cycles. For entire conversion of ADC N+1 clock cycles are required.

This paper proposes a new 10-bit ADC fabricated in the 90nm CMOS technology. Section II explains about the proposed SAR individual blocks. Various analyses about switching power and Implementation results are presented in section III. Finally, section VI draws our conclusions.

II. ARCHITECTURE DESIGN

The architecture of Successive approximation Analogto-Digital converter is shown in Figure 2. It mainly consists of Sample & hold circuit, Comparator, digital to analog converter and successive approximation register.

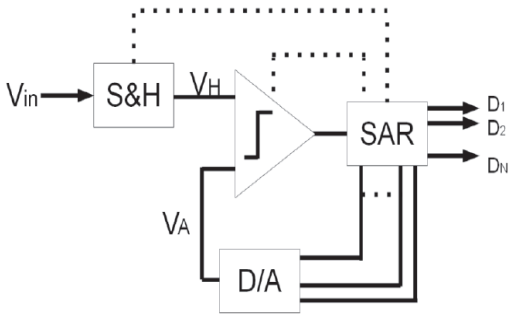

Figure 1. The Architecture of A Successive Approximation ADC.

A. *Sampling Network Design*

The Sampler takes the varying input Analog signal and converts it to a fixed voltage or current or electrical charge. The signal is sampled at Nyquist rate i.e. a frequency rate more than double the maximum

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frequency of the input analog signal. The Sampled signal has to be held constant while conversion is taking place in A/D Converter. This requires that an ADC should be preceded by a Sample & Hold circuit.

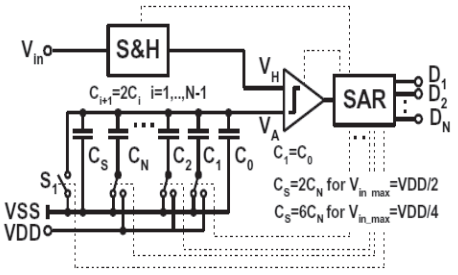

Figure 2. Overall Architecture of the ADC .

For Sample & Hold circuit, the important two basic elements needed in a sampling circuit are the switch and a memory element. The switch allows the S/H circuit to be configured into one of its two operating modes: one is Sample mode and other one is Hold mode. In CMOS technology, the MOS transistor is used as switch. For the storage purpose either voltage sampling or current sampling methods can be used. The voltage sampling method employs capacitors; the current sampling method employs inductors. However, in Integrated Circuit technology, the fabrication of capacitors is easier than fabrication of inductors. The reason for which all S/H circuits are done with voltage sampling only.

Next, the operation of the MOS transistor as a switch and its important limitations are discussed. When a voltage large enough is applied to the gate terminal of the MOS transistor, then the formation of the channel between its source and drain terminals allows the transistor to transmit any signal through that channel. The removal of a voltage at the gate follows the same operation principle of an ideal switch. When the transistor is turned "on" a signal path is present. If the transistor is turned off the channel vanishes and no signal path exists.

One of the main differences between an ideal switch and a transistor is that when the transistor is "on", a small on-resistance (i.e.0.5 - 2 kΩ) is present where as in ideal switch zero resistance is present, in the signal path between the drain and source terminals. Similarly, in the "off" state there is a resistance large enough to prevent signals from passing between the drain and source terminals.

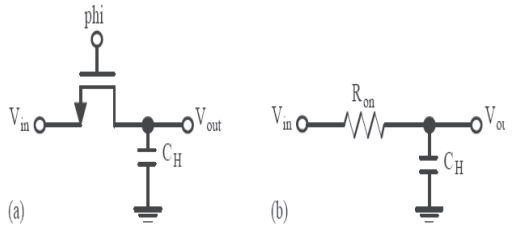

Figure. 3 (a) MOS-based S/H circuit (b) equivalent circuit during sampling phase.

Figure.3. (a) and (b), respectively, shows the basic sampling circuit using an MOS switch and its equivalent circuit during Sampling mode. When operated in the *triode* or linear region, the on-resistance of a NMOS transistor can be approximated as

$$\varepsilon_{settling} = e^{-t/R_{on}C_S} < \frac{1}{2^{N+1}} \quad \textbf{(1)}$$

B. Comparator Design

Latch only comparators are clocked comparators. They operate based on amplification and positive feedback. Figure.4 shows the Dynamic Latched Comparator circuit.

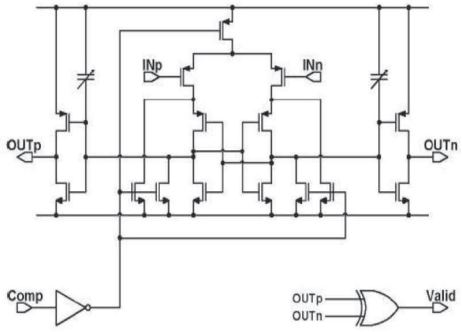

Figure 4. Dynamic-Latched Comparator circuit.

The figure 5. shows the operation of the comparator circuit. There are two operation phases, reset phase and regeneration or evaluation phase. In the reset phase, the output nodes are charged to supply voltage or discharged to the ground depending on the architecture of comparator. During the reset phase, the comparator tracks the input, and then in the regeneration phase the positive feedback produces a digital value at the comparator output. One of the advantages of dynamic-latched comparators is their power efficiency since they only consume power in the regeneration phase and there is no static power consumption in the reset phase.

Dynamic latched architecture is the most power efficient comparator. However, it introduces large input referred offset which makes it unappealing for high resolution ADCs. This effect can be reduced by increasing the width of input transistors in the differential pair. Employing offset cancelation techniques in the comparator implementation is also an effective approach to mitigate this problem. Furthermore, the offset voltage can be reduced by using a pre-amplifier which is previously described as a latched comparator with preamplifier. However, in all the mentioned methods, offset reduction is achieved at the cost of more power consumption. Latched comparators are fast and are suited to be used in high speed ADCs. In order to derive the

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delay equation, the latched comparator can be modeled as a single pole comparator with positive feedback. The delay time of this comparator is calculated as below [3].

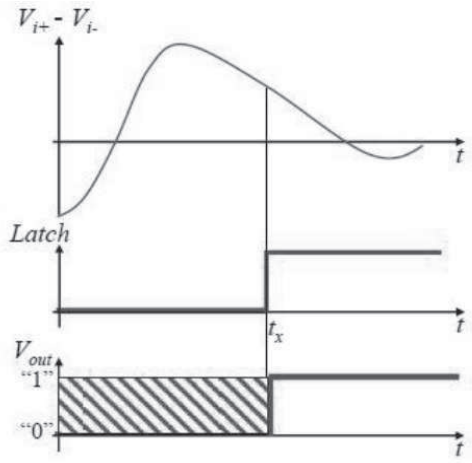

Figure 5. Latched Comparator Operation

C. Design of Digital-to-Analog Converter.

The digital to analog converter (DAC) converts the digital word at the output of SAR logic to an analog value. Then in the comparator, this value is compared to the input signal. In the capacitive DAC with inherent Sample and hold, the sampling operation is performed by DAC. This type of DAC is called charge redistribution DAC. Nowadays, charge redistribution DACs are commonly used. They consume less power and induce less mismatch errors compared to the resistive-based DAC. Charge redistribution DAC has fast conversion time. Moreover, they are fabricated easily [4], [5].

In this paper a 10-bit charge-redistribution DAC with the Binary weighted Capacitor (BWC) array was implemented in 90nm CMOS technology. Figure 6. shows the block diagram of the 10-bit DAC. There are three phases of the operation to perform a conversion: First, in the sampling phase switch S1 connects the top plats of all capacitors to the VCM and the bottom plates are connected to VIN. Thus, the input voltage is sampled on the capacitor array. During the hold phase, S1 is opened and the rest of switches connect the bottom plates to the ground therefore a charge of –VIN + VCM is stored in the capacitor array.

In the redistribution phase, the digital code determines the status of the switches and the actual conversion is performed in this phase. In the beginning of the conversion, D9 is high so the MSB capacitor is connected to V_{REF}. At this step the output voltage of the DAC is equal to $-V_{IN} + V_{CM} + 0.5V_{REF}$ and is compared to V_{CM}. Based on the comparator result, D_9 remains connected to V_{REF} if the comparator output is one, or change the connection to ground when the result of the comparator is zero. Thus, the MSB is defined. Next, D_8 is connected to V_{REF}. Depending on the value of D_9, Vout-DAC is $-VIN + V_{CM} + 0.5D_9.V_{REF} + 0.25V_{REF}$ and is compared to V_{CM}.

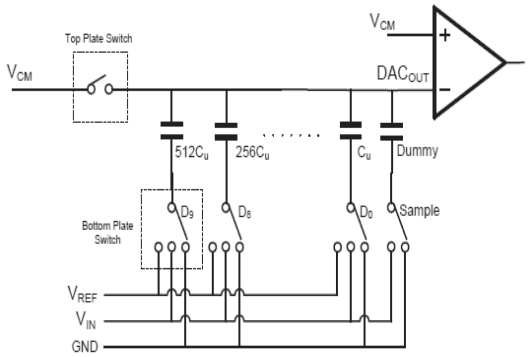

Figure 6.The schematic view of DAC

The linearity of ADC is restricted by the linearity of the DAC, which is caused by the capacitor mismatch. Therefore, choosing an appropriate value for the unit capacitance is vital. Reducing the unit capacitance value improves the linearity but deteriorates the noise performance at the same time due to thermal noise. The minimum required value of the unit capacitor is limited by several factors, including KT/C thermal noise, capacitor matching and the value of the parasitic capacitances [6]. A unit capacitance of 20fF is chosen in this design. The values of the other capacitors in the capacitor array are defined based on the unit capacitance.

The diagram of the bottom plate switches are presented In figure.7(a) NMOS switches can properly pass a zero while PMOS switches can pass a strong one. On the other hand, CMOS transmission gate combined both features of the NMOS and PMOS switch and is capable of properly passing both zero and one. It also benefits from low on-resistance [13]. In this design, VREF is set to VDD; therefore the PMOS switch is used for VREF. NMOS switch is employed to ground the bottom plate. Since Vin varies from 0 to 1, CMOS TG is chosen for Vin. Figure 7.2 (a) shows the block diagram of the bottom plate switches [7].

The leakage current contribution of the top plate switch is significant in this low speed design since most of the time this switch is off and it only turns on during the sampling phase. The leakage-current in the top plate switch adversely affects the linearity of the DAC and consequently the linearity of ADC [8]. In order to alleviate this problem, a stack of two PMOS switches are used in series form, this switch is depicted in Figure (b).

D. Successive approximation register

The successive approximation register (SAR) is realized in static CMOS logic. The circuit also generates the clock signals for the comparator and the sample-and

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hold circuit. All clock signals are derived from an externally provided master clock.

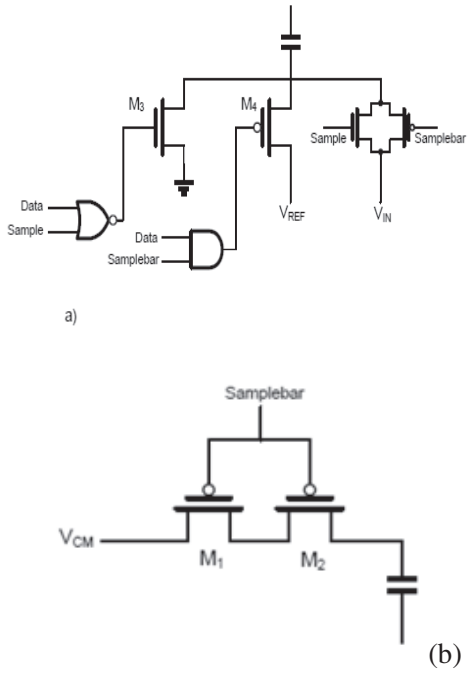

Figure 7.Schematic views of a) bottom plate switch and b) top plate switch.

Successive approximation register ADC implements the binary search algorithm using SAR digital control logic. In general, there are two fundamentally different approaches to designing the SAR logic. The first one is proposed by Anderson consists of a ring counter and a shift register. At least 2N Flip-flops are employed in this kind of SAR [9]. The other, which is proposed by Rossi, contains N flip flops and some combinational logic [10].

The SAR control logic determines the value of bits sequentially based on the result of the comparator. Each conversion takes 12 clock cycles. In the first clock cycle, SAR is in the reset mode and all the remaining outputs are zero. In the next ten clock cycles, data is converted and each bit is determined sequentially. The last cycle is for storing the results of the complete conversion.

The SAR architecture shown in Figure 8. is presented in [9], and is commonly used in SAR ADCs due to its straightforward design technique. This control logic encompasses a ring counter and a code register. The ring counter is in fact a shift register. For each conversion, in clock cycle 0, the EOC signal is high and all Flip Flops outputs reset to zero, and for the rest of cycles EOC is low. In the next clock cycle, the most significant Flip Flop is set to one which corresponds to MSB of the digital word to DAC. Then the counter shifts '1' through the Flip-Flops from MSB to LSB.

In each clock cycle, one of the outputs in the ring counter sets a Flip-Flop in the code register. The output of this Flip-Flop, which is set by the ring counter is used as the clock signal for the previous Flip Flop. At rising edge of the clock, this Flip-Flop loads the result from the comparator. This type of SAR logic requires 12 clock cycles to convert each sample.

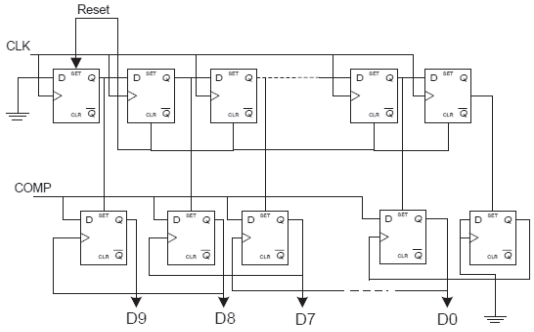

Figure 8. The SAR block diagram

The Flip-Flops which are employed in this structure are set-reset D-FFs. For the low power purpose, transmission gate based Flip Flops are used [11]. Minimum size transistors with double length are chosen for improving the power performance. In order to decrease the leakage power even more while simultaneously maintaining the speed, high threshold voltage transistors are used in the non- critical paths and low-VT transistors in the critical path. Thus, this dual threshold approach provides high performance Flip-Flops [12].

III. Simulation Results

The Low power 10-bit ADC is fabricated in a 90nm *n-well* CMOS process technology with single poly, four metal layers and a MIMCAP (Metal-Insulator-Metal) capacitor option. The threshold voltages are 0.43V for the n-MOS and -0.38V for the p-MOS device. Simulation results for the low supply voltage as well as high temperature are presented to evaluate their influence on power consumption.

The ADC is simulated with VDD= VREF = 1,VCM = 0.5V, and sampling frequency of 1kS/s. The input signal is an full swing sinusoidal with fin= 450Hz. The simulation results under 27ºC and 80ºC temperatures are presented in the Table 1.

The total power consumption of the implemented SAR ADC, including the clock power is almost 12.4nW. The distribution of power consumption between different blocks of ADC is shown in figure 9.

As shown in the Figure 9, DAC consumes the largest amount of power among other blocks which is 84%. As discussed above, the unit capacitance in the DAC is chosen to be 20fF. After DAC, SAR control logic with 12%, clock power and comparator both with 2% consumes the largest amount of power respectively.

A. Dynamic Performance Evaluation

The dynamic performance is evaluated by calculating the SFDR, SINAD, and ENOB of ADC. For this purpose, a full swing sinusoidal wave with fin = 30.273438 Hz which is based on coherent sampling is applied to the input of ADC. The simulation is performed to achieve 1024 samples with sampling frequency of 1kS/s. Then, Fast Fourier Transform of the stored output data is executed in MATLAB and by performing some post processing of the SFDR, SINAD, and ENOB are measured.

Table I.
Power consumption of different blocks of ADC

Block	Power Consumption at 27ºC (nW)	Power Consumption at 80ºC (nW)
DAC	10.4	11.1
SAR	1.54	2.028
Comparator	0.26	0.620
Clock Power	0.208	0.224
Total	12.408	13.97

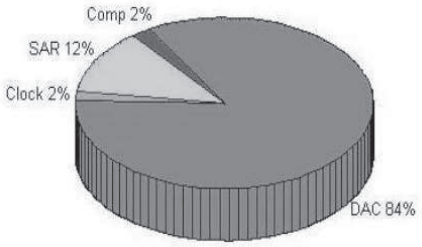

Figure 9. The Power distribution of ADC

The FFT of 10-bit ADC output is shown in Figure10. The simulation results predict that the ADC have SINAD=60.29, SFDR=79.89, and achieves 9.72 of ENOB which are reasonable for schematic level simulation. Energy per conversion-step can be calculated using the FOM definition of ADC which is given by Equation (2) [16].

$$FOM = \frac{P}{2^{ENOB} \cdot F_S} \text{ (fJ/conversion-step)} \quad (2)$$

Table II Summarize the performance parameters of the designed SAR ADC.

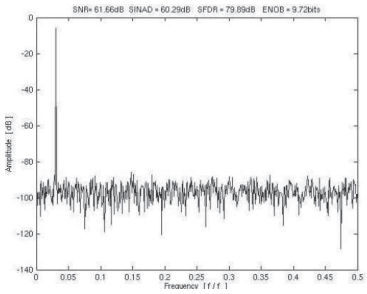

Figure 10. FFT of the ADC output for Fin=30.273438Hz

Table II.
Performance summarize for ADC

Items	Result	Unit
Technology	90nm	-
Supply Voltage	0.5	V
Resolution	10	bits
Sampling Frequency	1	KS/s
Power Consumption	6.8	nW
Conversion Time	167	ns
SINAD	60.29	dB
SFDR	79.89	dB
FOM	14.7	pJ/Conversion

CONCLUSION

This paper presented implementation of a 10-bit SAR ADC operating at 1kS/s and the supply voltage of 0.5 V in 90nm CMOS technology. The power consumption of 12.4nW is achieved. The ADC used a charge-redistribution DAC, a dynamic two-stage comparator, and a SAR control logic containing a sequencer and a ring counter. The ADC exhibited good performance and achieves a FOM of 14.7fJ/conversion-step with ENOB of 9.72 bit.

The SAR logic is implemented as a conventional SAR logic with a sequencer and a ring counter, consumes the lowest power of 1.2nW at 1kS/s. Thus the power consumption of SAR control logic is significantly reduced and consumes only 12% of the total power.

The Design of the comparator is a crucial part of ADC design. In this work, comparator performance metrics is studied and the two-stage dynamic comparator is designed. Dynamic comparators consume lower power compared to the other approaches. Therefore, the Architectures of dynamic comparators are implemented and compared regarding power consumption, speed, and accuracy.

This Very Low power ADC with moderate resolution and low sampling frequency is suited for biomedical applications such as Pacemakers. These results make SAR ADC is the suitable choice for biomedical application. It consumes low power due to its simple structure.

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