FPGA Implementation of OFDM Transceiver

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Abstract—**The OFDM is a multi-carrier modulation scheme in which the available carrier bandwidth can be divided into N number of orthogonal carrier frequencies and the data can be shared by these multiple carriers. This paper describes the design and implementation of OFDM transceiver using single FPGA board. The design methodology used is the 8-point IFFT/FFT with radix-2 with QPSK modulation scheme. The design unit consists of a back to back connected OFDM transmitter and receiver with QPSK framer, IFFT, PISO, SIPO, FFT and QPSK de framer etc. All these blocks are designed and simulated using Xilinx ISE 12.4 design suite. Finally the transceiver is implemented on Xilinx Virtex 5 LX110T FPGA with a data rate of 8, 16, 32 Mbit.**

Index Terms— **OFDM, FFT, IFFT, FPGA, QPSK**

I. INTRODUCTION

The growth of the wireless communication has produced a strong demand for advance wireless communication. Orthogonal Frequency Division Multiplexing (OFDM) is a state of the art modulation technique for high speed wireless communication with resistant to fading. The OFDM is a special form of Multi carrier Modulation which was originally used in high frequency radio. An efficient way to implement OFDM by means of Discrete Fourier Transform (DFT).The computational complexity would be reduced by a Fast Fourier Transform (FFT).Recent advances in VLSI Technology have enabled cheap and fast implementation of FFT's and IFFT's.

The data transmission over a wireless communication channel can be done by using a carrier signal with the help of modulation. The transmission can be done by using either a single carrier modulation or multi carrier modulation. In a single carrier modulation scheme each data symbol is transmitted sequentially on a single carrier i.e. signaling interval equal to data symbol duration [4]. The problem with single carrier modulation is the modulated carrier is occupies the entire available bandwidth. This problem can be solved by using multi carrier modulation. In a multi carrier modulation scheme N sequential data symbols are transmitted simultaneously on N multiple carriers i.e. signaling interval equal to N time's data symbol duration [4]. Here the available band width is divided into N number of sub carriers; hence it is bandwidth efficient compared to single carrier modulation.

The Orthogonal Frequency Division Multiplexing (OFDM) is one of the multi carrier modulation techniques for data transmission. In OFDM all the sub carriers are orthogonal to each other. The concept of conventional multi carrier and orthogonal multi carrier techniques are shown in Fig.1 (a) and Fig.1 (b) [5].

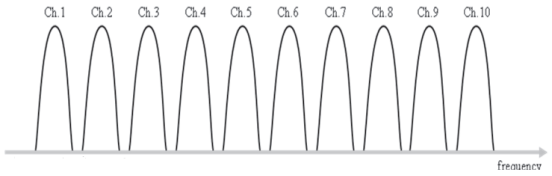

Figure. 1(a) Conventional Multi carrier technique

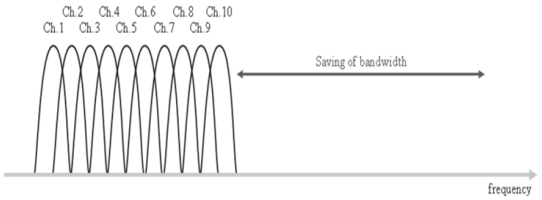

Figure. 1(b) Orthogonal Multi carrier technique

The Fig.2 shows block diagram of OFDM transmission system. The design consists of OFDM transmitter and receiver with different sub blocks. The OFDM transmitter accepts the serial data and this data is grouped in to n-bits and applied to IFFT through a bulk modulator like QPSK. The IFFT converts frequency domain signals into time domain signals and these signals are transmitted to receiver through parallel in serial out shift register with I (real) and Q (imaginary) channel data. At the receiver the received time domain data symbols are grouped with serial in parallel out and converted into frequency domain by using FFT with QPSK demodulation. The parallel frequency domain data is recovered in serial order using parallel in serial out shifter.

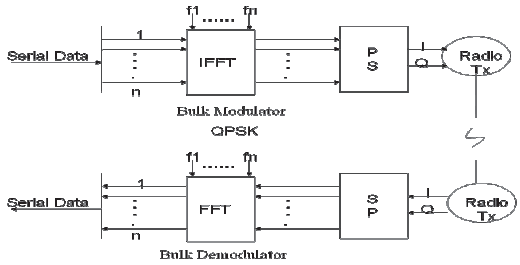

Figure.2 Block diagram of OFDM transmission system.

The objective of this paper is to develop the single FPGA based OFDM transceiver using bulk modulator and demodulator for high speed data transmission on

wireless media. The modulation is with QPSK and 8 sub carriers are used.

The 8-point IFFT/FFT is designed by using the fast implementation of IDFT/DFT equations using butterfly diagrams. The equation for DFT is given by [3].

$$X(k) = \sum_{n=0}^{N-1} x(n)\, W_N^{nk}$$

Where X(k) indicates the DFT of x(n) sequence and W_N^{nk} is the twiddle factor of the transform. The equation for IDFT is given by [3].

$$x(n) = 1/N \sum_{k=0}^{N-1} X(k)\, W_N^{-nk}$$

Where the x(n) is the inverse DFT of X(k), here n=8 and k=8.

The FPGA implementation of OFDM test set up with synthesis is explained in section II and Simulation results of each block is explained in section III. The FPGA implementation results are explained in section IV then conclusion in section V and references.

II. The FPGA Implementation of OFDM Test Setup

The FPGA implementation of OFDM needs a test setup. To provide the test set up the Fig.1 can be modified by removing two radios channels and directly connect the I/Q output values of transmitter to 1/Q input values of receiver. This setup will provide a back to back connected OFDM transmitter and receiver namely OFDM transceiver. This OFDM transceiver FPGA implementation test setup is shown in the Fig.3. The design is tested for 8, 16, 32 Mbit by using proper selection of input switches of FPGA.

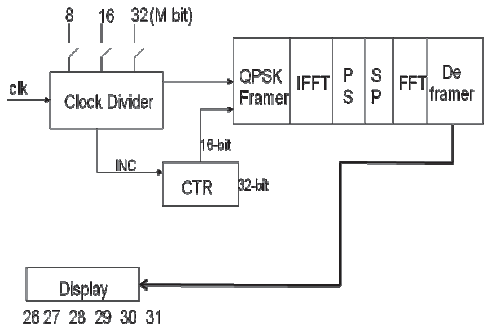

Figure.3 FPGA Implementation of OFDM transceiver test setup

The FPGA implementation of OFDM transceiver can be designed by using following blocks.

A. Counter

The serial I/P data to the OFDM transmitter can be applied by using a 16-bit counter. The 16-bit data is applied to QPSK framer.

B. QPSK framer

The QPSK framer accepts 16-bit data and converts every two bits data in to real and imaginary of constellation mapping as shown in Table 1. This QPSK framer block produces eight real and eight imaginary data values.

TABLE I
QPSK mapping

Input data	Output
00	1+j0
01	0+j1
10	-1+j0
11	0+j(-1)

C. IFFT

The eight complex pair outputs of QPSK framer is connected to the IFFT and the conversion from frequency domain to time domain can be done by using IEEE 754 floating point arithmetic operations on data and twiddle factors.

D. PS and SP (*Parallel in Serial out and Serial in Parallel out*)

The eight complex pair time domain IFFT output data (i.e. OFDM frame) is applied to PS and the output is taken serially and transmitted directly to the receiver first stage i.e. SP. The SP accepts serial input data from PS one after another and generates eight complex pair data as output (i.e. OFDM frame).

E.FFT

The eight complex pair outputs of SP (i.e. OFDM frame) is connected to the FFT and the conversion from time domain to frequency domain can be done by using IEEE 754 floating point arithmetic.

F. De framer

The De framer accepts eight complex pair data values and converts each pair of data in to two bit digital data according to de framer logic and produces 16-bit digital data as the output. This received 16-bit data should be same as the transmitted input data which is the output of 16- bit counter.

G. Clock Divider

The FPGA implementation of OFDM requires a clock signal frequency. The OFDM design frequency can be generated by converting the FPGA on-board clock frequency (i.e. 33Mhz) into different required frequencies by using the below formula.

$$\text{Required frequency} = \text{On-board frequency}/2^n$$

Where 'n' indicates the bit position in counter of frequency divider. Here the OFDM transceiver is running with three different frequencies of 0.5 MHz, 1 MHz and

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2 MHz by using proper selection of input switches available on FPGA board.

H. Display

The eight Most Significant output bits of the OFDM transceiver is connected to the eight LED indicators of Xilinx Virtex-5 LX110T FPGA board.

III. Simulation Results

The total OFDM transceiver blocks are designed and simulated and implemented by using Xilinx ISE 12.4 design suite with the sub tools listed in Table 2.

TABLE 2
List of Tools under Xilinx ISE design suite

Design Action	Name of the Tool
Design Entry	HDL Editor (Verilog)
Synthesis	Xilinx Synthesis Tool(XST)
Simulator	ISim Simulator
Implementation	FPGA Editor, Plan Ahead
Device Configuration	iMPACT

The OFDM transceiver has back to back connected transmitter and receiver blocks. The QPSK framer, IFFT and PS blocks forms OFDM transmitter.

The OFDM transceiver is designed by using Verilog Hardware Description Language. The design is synthesized for generating the net list from the given specifications for the target FPGA board. The output of synthesis i.e. RTL schematic view of OFDM transceiver is shown in Fig.4.

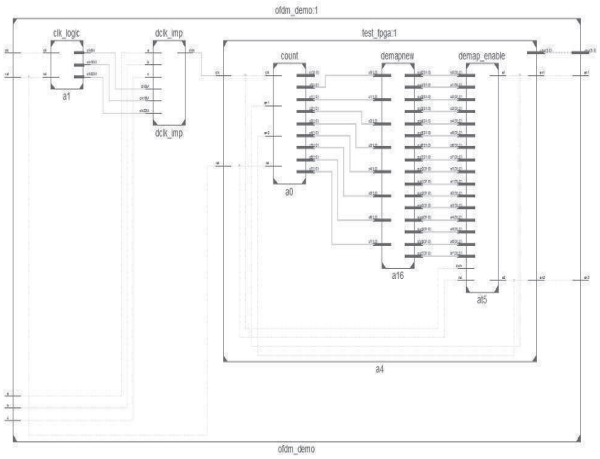

Figure.4 RTL Schematic of OFDM transceiver

The simulation results of all these blocks are shown in below figures. The Fig.5 shows the simulation results of OFDM transceiver data input counter.

The Fig.6 shows the simulation results of QPSK framer by accepting 16-bit input data from counter. This block generates eight real and eight imaginary modulated time domain signals.

The Fig.7 shows the simulation results of IFFT of QPSK framer output and generates eight real and eight imaginary frequency domain signals.

The IFFT output is connected to parallel in serial out shift register of transmitter. Since the design is back to back connected transceiver the parallel in serial out shift register output is directly connected to the first stage of receiver i.e. serial in parallel out shift register.

The SP, FFT and deframer forms OFDM receiver. The SP output is applied to FFT. The Fig.8 shows the simulation results of FFT. The FFT block generates eight real and eight imaginary frequency domain signals.

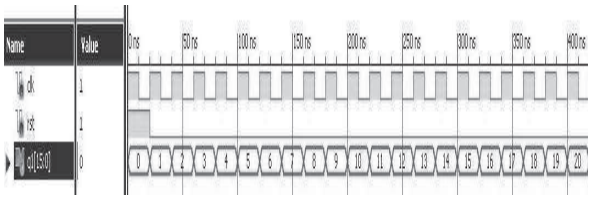

Figure.5 Counter simulation results

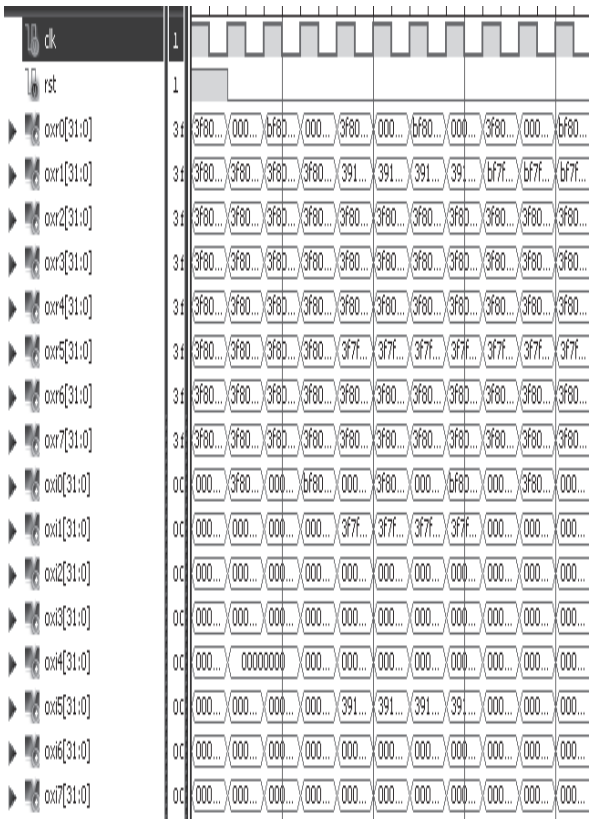

Figure.6 QPSK framer simulation

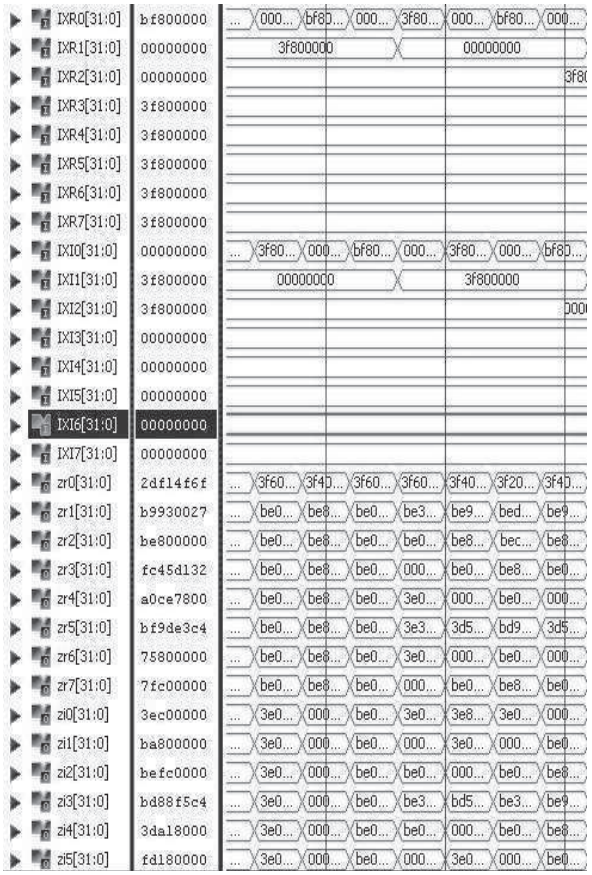

Figure.7 IFFT simulation results

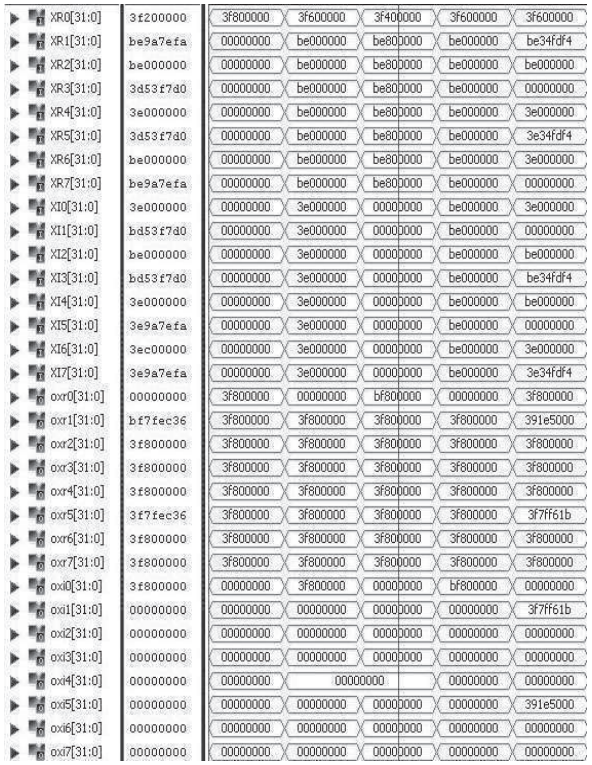

Figure.8 FFT simulation results

The FFT output is demodulated by using QPSK with the help of demapping logic by using deframer. The simulation result of deframer logic is shown in Fig.9. The simulation results guarantees that the functionality of OFDM transceiver is correct and the design can be used for FPGA prototyping for real time functional checking.

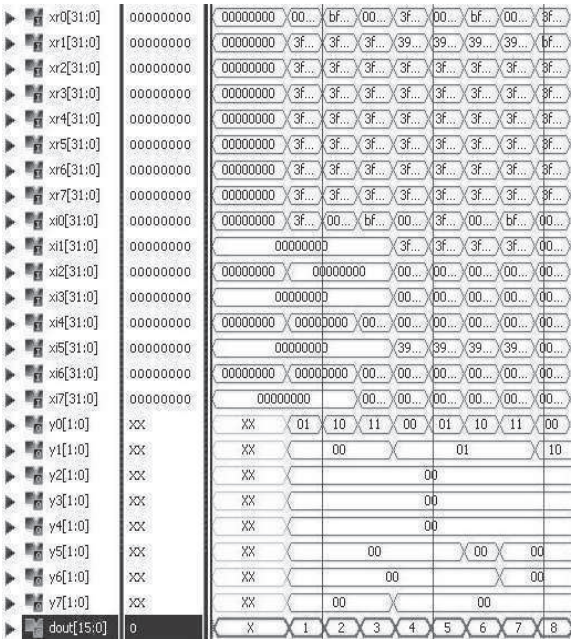

Figure.9 Defframer simulation results

IV. FPGA IMPLEMENTATION OF OFDM TRANSCEIVER

After the functional verification of the OFDM transceiver this design is used for implementation by using Xilinx Virtex 5 XC5VLX110T.The FPGA implementation of OFDM transceiver result is shown in Fig.10.

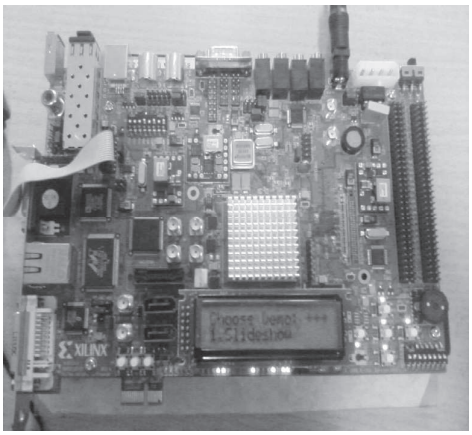

Figure.10 FPGA Implementation of OFDM Transceiver

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CONCLUSIONS

The main focus of this work is to design 8-point IFFT/FFT based back to back connected OFDM transceiver using single FPGA. In this work the design, simulation and implementation of OFDM transceiver using Xilinx ISE Design suite for Virtex 5 FPGA is completed. The design functionality is verified for 8, 16, and 32 Mbit data rates.

The design can be extended by isolating OFDM transmitter and receiver using two FPGA boards.

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