An efficient sense amplifier design for STT-RAM in 45nm hybrid CMOS process

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***Abstract*— in this paper different sense amplifier (SA) circuits for Spin Torque Transfer – Random Access Memory (STT-RAM) have been designed. Their performance is evaluated in 45nm hybrid-CMOS process. The goal is to design an efficient sense amplifier with lower power consumption, better read cycle stability and to reduce the access time. Analysis and design have been done for two circuit's i.e. conventional self-reference sensing (CSRS) scheme and non-destructive self-reference sensing (NDSR) scheme. The results show that CSRS provides good sense margin by trading power and performance. NDSR on the other hand improves the access time, reduces power consumption but with a reduced sense margin.**

***Index Terms* — STT-RAM, hybrid CMOS process, Magnetic Tunnel Junction (MTJ), conventional self-reference sensing, Non-destructive self-reference sensing,**

I. INTRODUCTION

STT-RAM is an emerging non-volatile memory technology. It has the characteristics of fast speed, low power consumption and good scalability. STT-RAM technology is based on spin-polarized current induced magnetic tunnel junction (MTJ). The theory of spin transfer torque was first proposed by Berger [1] and Sloncewski [2]. Further research was carried out by Stiles and Zangwill [3]. Those studies showed that a spin polarized current can reverse the magnetization of a ferromagnetic layer by the so called spin-transfer effect. This mechanism occurs in a sandwich structure of two ferromagnetic layers separated by a barrier layer made of MgO. This structure is called the Magnetic Tunnel Junction (MTJ). S. Yuasa et al.[4] and Parkin et al. [5] showed that very large Tunnel Magneto Resistance (TMR) ratios up to 200% at room temperature could be obtained with MgO Magnetic Tunnel Junction (MTJ).

Sense amplifiers are needed in memory cells to sense the bit line voltages and read the logic state stored in the memory cell. The sense amplifier should perform reliably during the read cycle and also be resistant to noise. This is called read stability. In order for the sense amplifier to function properly, it must accurately read the stored values in the memory cells. In this paper effort has been done to design an efficient sense amplifier for STT-RAM cells.

A. STRUCTURE OF A STT-RAM CELL.

The main element of the STT-RAM is the MTJ cell. Figure 1 shows the MTJ structure consisting of two ferromagnetic layers
separated by MgO barrier layer.

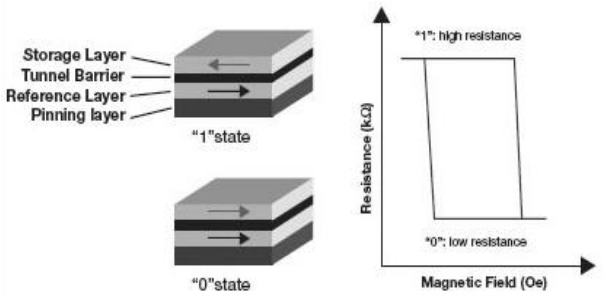

Figure 1. MTJ structure representing antiparallel ('1' state) and parallel ('0' state) [Alexander Driskill et al, Grandis corporation]

The resistance of the MTJ is determined by the relative magnetization directions of the two ferromagnetic layers. When the magnetization directions of the layers are parallel, the MTJ is in low resistance (R_p) state (representing a bit 0), whereas if the layers are antiparallel, the MTJ is said to be in high resistance (R_{ap}) state (representing a bit 1). Data storage is realized by switching the MTJ between high and low resistance states [6]. The ratio of the resistances R_p and R_{ap} is called the tunnel magneto resistance (TMR) and defined as:

$$TMR = \frac{Rap - Rp}{Rp}$$

The basic structure uses an MTJ as the storage element and an N-channel MOSFET (1T-1MTJ) as the selection device [7]. The circuit and cross section of the structure is shown in figure 2. In the STT-RAM cell the source of the NMOS transistor is connected to the source line (SL). The free layer of the MTJ is connected to the bit line (BL) while the other pinned layer to the drain of NMOS. The word line (WL) is connected to the gate.

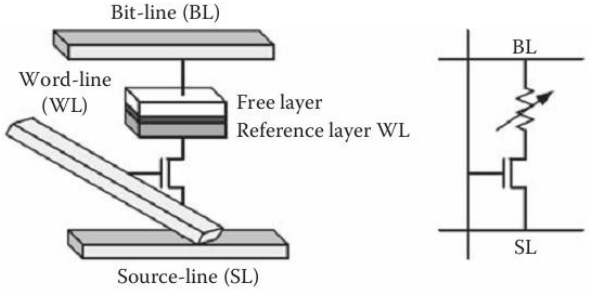

Figure 2. 1T-1MTJ STT-RAM (a) cross section and (b) circuit diagram.

B. READ AND WRITE MECHANISM OF STT-RAM CELL.

The switching of the states in MTJ is obtained by altering the direction of current through it. When a logic '0' is to be written the current flows from BL to SL, whereas when writing '1' the current flows in opposite direction i.e. from SL to BL. When the MTJ terminal is biased to $V_{dd,}$ the cell access transistor operates in the linear region and does not limit the current through the MTJ. Therefore a resistor is connected to limit the current through it. In the reverse bias case, the access transistor operates in a diode connected manner and thus the threshold drop across the access device limits the voltage drop across the MTJ. This voltage drop places an upper limit on the switching current that can be applied to the cell.

The data read operation is slightly different from that of conventional memory cell. The STT-RAM requires a reference voltage to compare the output generated by the sense amplifier. Generally the reference voltage is chosen as the voltage drop across the resistance $(R_p + R_{ap}) / 2$ where R_a and R_{ap} are the resistances of MTJ in parallel and anti-parallel states respectively. The read operation consists of making the word line as high, this selects the access transistor. By applying a read voltage to the selected memory cell, the generated current on the bit line can now be compared to the reference signal in the sense amplifier.

II. SENSE AMPLIFIER DESIGN

There are two main categories of sense amplifiers. Differential sense amplifiers, also known as voltage mode sense amplifiers, and non-differential amplifiers also known as current mode amplifiers [8]. Voltage sense amplifiers include both static and dynamic designs. Static designs are latch based and read the difference between the bit-lines once and hold that output. Dynamic amplifiers on the other hand constantly evaluate the difference between the bit-lines and adjust their output accordingly [9].

A good sense amplifier has to accurately read the logic states stored in the memory cell. Due to process variations, decision failure is a severe issue in STT-RAM design. Consequently, many sensing schemes have been proposed to alleviate this problem. In this paper two sensing schemes, i.e. conventional self-reference scheme and non-destructive self-reference scheme has been designed and evaluated in 45nm hybrid-CMOS process using cadence tools.

A. CONVENTIONAL COMMON READ-OUT SENSING SCHEME

The conventional common read-out mechanism is shown in figure 3. By applying a read voltage (current) to the selected memory cell, the generated current (voltage) on the bit-line can be compared to a reference signal in the sense amplifier. If the generated current (voltage) is higher than the reference, the data storage device (i.e. MTJ) in the memory cell is in the low (high) resistance state. The reference signal is normally generated by applying the same read voltage (current) on a dummy cell, whose resistance is ideally $(R_p + R_{ap})/2$.

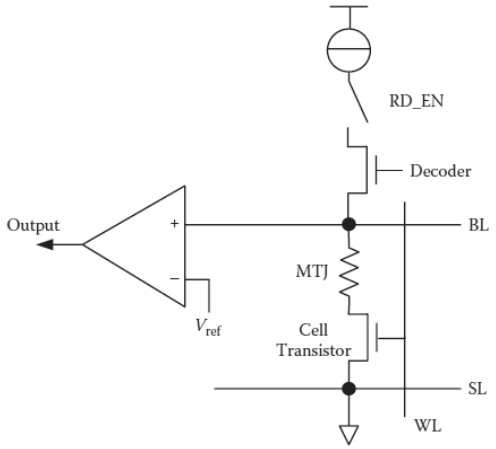

Figure 3. Conventional common read-out sensing.

However this scheme is intolerable to process variation. Due to process variation decision failure can occur in STT-RAM cells. For accurate reading of the logic state and to avoid decision failure, the reference voltage should satisfy the equation:

$$Vbl\,(L) = Ir.\left(Rl + Rtr(L)\right) < Vref < Vbl(H) = Ir.\left(Rh + Rtr(H)\right)$$

Where *V*bl (L) and *V*bl (H) respectively stand for the bit-line voltages *V*bl when the MTJ is in the low and high resistance states. R_{tr} represents the transistor resistance. R_l and R_h are the resistances in the low and high state respectively. I_r is the read current. Equation 2.1 indicates that sensing voltage in a high (low) resistance state of STT-RAM must be higher (lower) than the reference voltage.

B. CONVENTIONAL SELF-REFERENCE SENSING SCHEME(CSRS)

The motivation for a conventional self-reference sensing scheme (CSRS) is to directly compare the bit-line voltage generated by the original data stored in an MTJ with the bit-line voltage generated by reference data in the same MTJ [10]. Since the generated reference signal is from the same memory bit, the MTJ resistance variation is excluded from the sensing operation. Figure 4 shows the CSRS scheme. The read procedure is as follows: (1) Read the original data by applying a reference read current (I_{r1}) to generate bit-line voltage V_{bl1}. (2) Write '0' into the same MTJ (3) Read '0' by applying another read current (I_{r2}) that generates voltage V_{bl2}. (Here I_{r2} is slightly greater than I_{r1}) (4) Write back the original data back to the memory cell. If the current ratio $\alpha = I_{r1}/I_{r2}$ can be adjusted, then the impact of process variation can be minimized. However, the CSRS has the limitation that two write operations are required which introduces long latency (delay) and additional power consumption.

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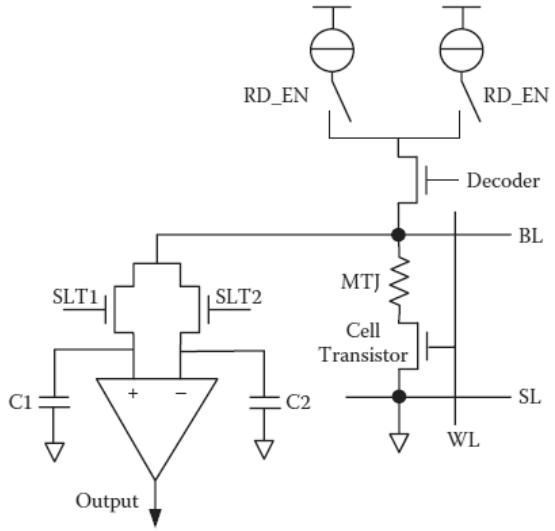

Figure 4. Conventional self-reference sensing scheme.

C. NON-DESTRUCTIVE SELF-REFERENCE SENSING SCHEME (NDSR)

NDSR is based on the unique characteristics of MgO based MTJs [11]. The MTJ has the characteristics of asymmetric static R-V curve which means that current roll-off slope of the high resistance state is much steeper than that of the low resistance state. NDSR has only two read steps without overwriting the original value in the STT-RAM cell. Figure 5 shows the scheme for NDSR.

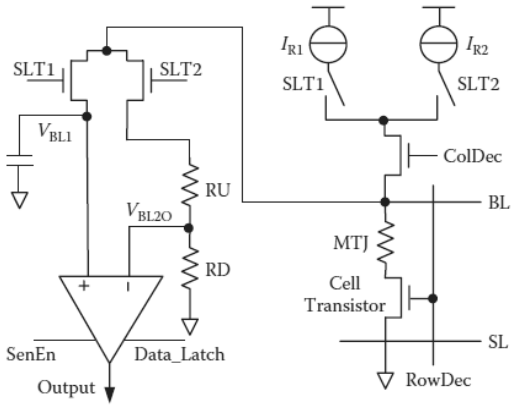

Figure 5. Non-destructive self-reference sensing.

The read procedure is as follows: (1) First apply a read current (I_{r1}) to generate bit-line voltage V_{bl1}, which is stored in capacitor C1. (2) Another read current I_{r2} ($I_{r2}>I_{r1}$) is applied and generates the bit-line voltage V_{bl2}. The V_{bl2o} is the voltage produced by a voltage divider with a voltage ratio $\beta = V_{bl2o} / V_{bl2}$. Proper selection of beta and read current α is necessary for better read stability and to reduce the latency in the access time of the memory cell.

III. DESIGN AND SIMULATION

The sense amplifier for a STT-RAM storage cell has been designed in 45nm CMOS process. Both CSRS and NDSR circuits have been simulated using cadence tools and their performance has been evaluated. The circuit schematic for CSRS and NDSR sensing scheme are shown in figure 6 and 7 respectively.

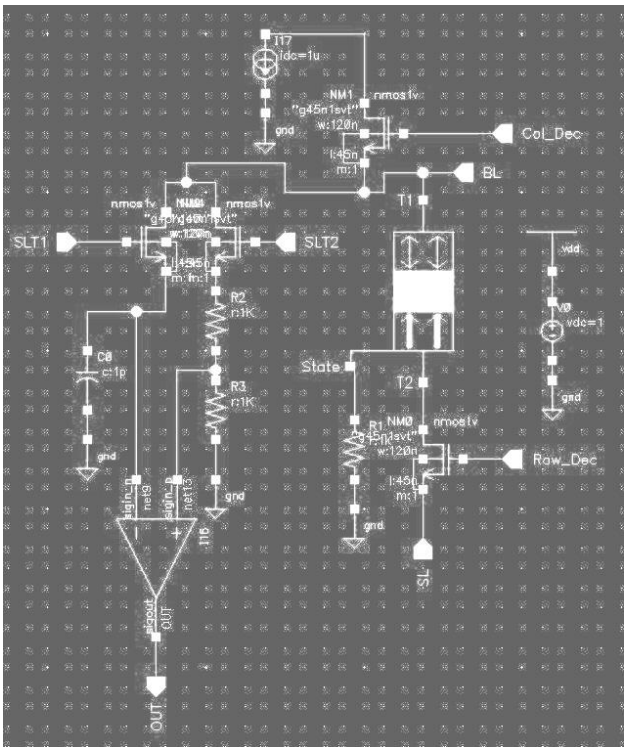

Figure 6. Conventional self-reference circuit.

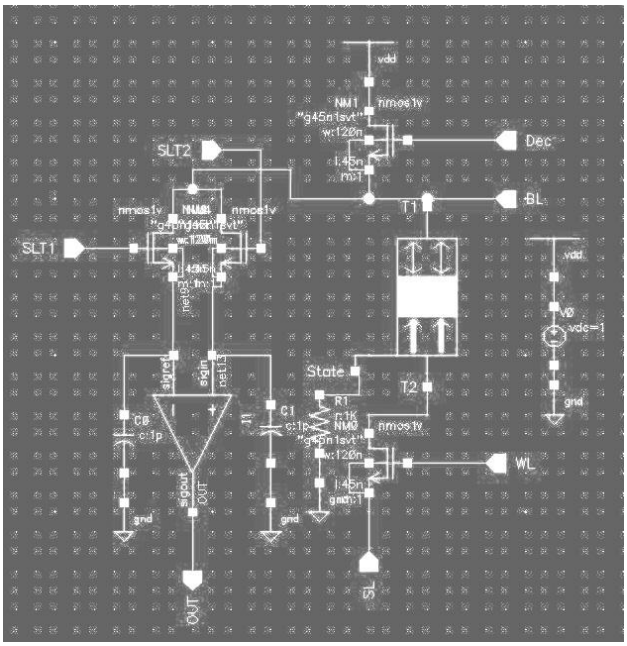

Figure 7. Non-destructive self-reference circuit.

Proper choice of read and reference current were chosen to read accurately the data stored in the MTJ in both the low and high states. The outputs generated are shown in figure 8 and 9 respectively for CSRS and NDSR circuits.

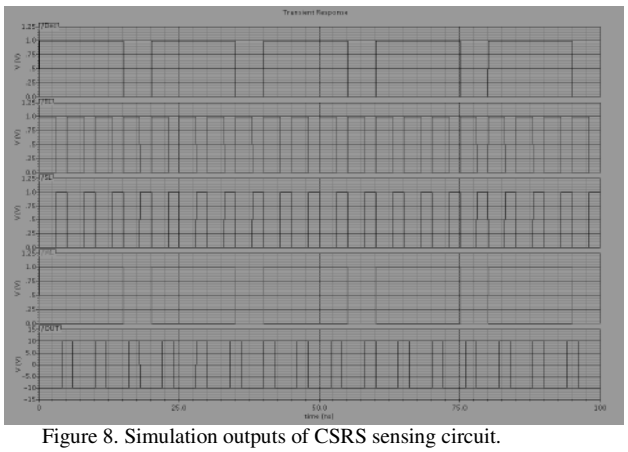

Figure 8. Simulation outputs of CSRS sensing circuit.

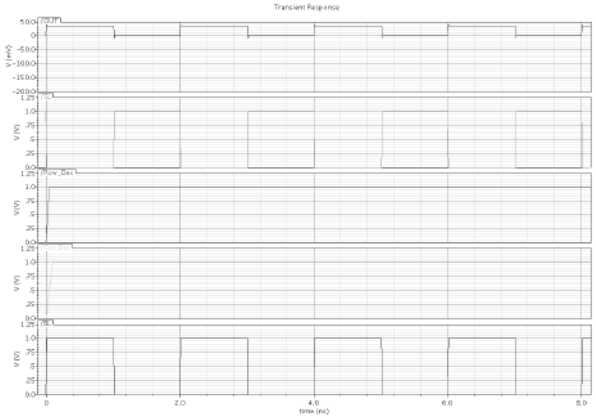

Figure 9. Simulation outputs of NDSR sensing circuit.

A comparison of the two schemes in terms of latency and power consumption is shown in Table 1.

TABLE I
LATENCY AND ENERGY COMPARISON OF CSRS AND NDSR SENSING CIRCUITS.

Designs	Read '1'	Read '0'	Latency
CSRS	20.2 pJ	20.0 pJ	40 ns
NDSR	2.16 pJ	1.12 pJ	15ns

CONCLUSIONS

This paper presented the sense amplifier design for STT-RAM cells in 45nm CMOS process. Two types of sensing circuits, conventional self-reference sensing and Non-destructive self-reference sensing circuits were designed and evaluated for their performance.

The results show that CSRS has much high power consumption. This is because it has two write steps - erase and write back original data. Comparatively NDSR has less power consumption since it has only two read steps. The latency in CSRS is also slightly higher than

that of NDSR because capacitor charging requires a finite amount of time.

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