Multilevel Inverters Fed PMSM Drive using Carrier Based Space Vector Pulse Width Modulation

G. Sree Lakshmi¹, Dr. S. Kamakshaiah² and Dr. G. Tulasi Ram Das³ 1 CVR College of Engineering, Department of EEE, Ibrahimpatan, R.R.District, A.P., India Email: s_sreelakshmi@yahoo.com ² JNT University, Department of EEE, Hyderabad, AP, India. Email: skamakshaiah@yahoo.com ³ Vice Chancellor, JNT University, Kakinada, A.P., India Email:das_tulasi@gmail.com

Abstract--- **Space Vector Pulse Width Modulation (SVPWM), one of the advanced computation based PWM techniques, has many advantages over conventional carrier-based PWM methodologies. This paper presents a systematic approach and simplified algorithm of space vector pulse width modulation (SVPWM) for a two-level & three level three-phase inverter, which can operate in under modulation and over modulation modes. This method is called as Carrier Based Space Vector Pulse Width Modulation (CBSVPWM) which is based on description of controllable redundant parameters in the modulating signals. The CBSVPWM methods can be described in a unified mathematical formulation, and obtain the same outputs similarly as of corresponding SVPWM. The simulation and analysis of CBSVPWM to the two and three level inverters fed to Permanent Magnet Synchronous Motor drives and their differences and advantages are also presented.**

Index Terms- **Multilevel Inverters, Space Vector Pulse Width Modulation (SVPWM), Carrier Based Space Vector Pulse Width Modulation (CBSVPWM), Permanent Magnet Synchronous Motor (PMSM).**

I. INTRODUCTION

The smaller voltage steps created by a multilevel converter lead to the production of higher power quality waveforms and also reduce the *dv*/*dt* stresses on the load, especially in AC motors, and reduce the electromagnetic compatibility problems [1]. Permanent magnet synchronous motors (PMSM) are widely used in high-performance drives such as industrial robots and machine tools for their advantages high power density, hightorque, and free maintenance and so on. In recent years, the magnetic and thermal capabilities of the PM have been considerably increased by employing the high-coercive PM materials [2]. In last few years permanent magnet synchronous motor (PMSM), consequently is acquired in more

and more far-ranging application, because of its properties such as small volume, light weight, high efficiency, small inertia, rotor without heat problem, etc. [3].

A variable voltage can be obtained by varying the input DC voltage and maintaining the gain of the inverter constant. On the other hand if the DC input voltage is fixed and it is not controllable, a variable output voltage can be obtained by varying the gain of the inverter, which is normally accomplished by PWM/SVPWM control with in the inverter. The output voltage waveform of a practical inverters are non sinusoidal and contains certain harmonics. For high power applications low distorted sinusoidal waveforms are required. It is possible to achieve high-voltage low-distortion ac waveforms by increasing the number of dc levels that are available in the inverter. Thus the concept of Multilevel Inverters is introduced. Multilevel inverters are an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms [4]. Using enough levels the multi level inverter generates approximately a sinusoidal voltage waveform with very low harmonic distortion. There are three types of multilevel inverters as NPC multilevel inverters, cascade multilevel inverter and dc capacitor clamped multilevel inverter. The most common configuration of multilevel inverters is the neutral point clamped voltage source inverter structure (VSI-NPC) which is widely used in medium voltage drives for rolling mills, marine, and traction applications.

To control multilevel converters, the pulse width modulation (PWM) strategies are the most effective, especially the space vector pulse width modulation (SVPWM) one, which has equally divided zero voltage vectors describing a lower total harmonic distortion (THD). By and large, the emphasis has been placed on space vector PWM (SVPWM) methods. SVPWM offers great flexibility to optimize switching waveforms and is suited for digital implementation [5]. However, due to constant sampling rate used in SVPWM and the complications associated with this method when we go to n-level, the equivalent carrier-based techniques have been developed.

 Carrier-based space vector modulation (CBSVM) is appropriate for inverters with more than five levels, where the computational overhead for conventional SVPWM is exceeding due to many output states. Wenxi Yao proposed carrierbased space vector modulation technique [8], which are harmonically equivalent, with the best spectral performance being achieved when the nearest three space vector states are selected with the middle two vectors centered in each half carrier switching interval. This strategy is known as carrier based space vector modulation (CBSVM).

 The speed or torque of a Permanent Magnet Synchronous Motor can be controlled by various modulation strategies for inverter. In this paper control of PMSM in open loop system using the best modulation strategy known as CBSVM technique is simulated for two and three level inverters and shown that Permanent Magnet Synchronous Motor performance is improved. The three level performance of PMSM is improved when compared to the two level inverter using CBSVM technique. The performance of the PMSM can be further improved.

II. MULTILEVEL INVERTERS

The demand for high voltage inverter drives and for power transmission has been rising in the recent years. For such applications, standard PWM voltage source inverters with only two switches per phase place requirements on the blocking voltage of the switches that cannot be met with a single device. Currently, to overcome this challenge we are using multilevel converters. Multilevel inverter technology has emerged recently has a very important alternative in the area of high-power medium-voltage energy control.

Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. Commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. Figure 1.[6] shows a schematic diagram of one phase leg of inverters with different number of levels.

The action of the power semiconductors is represented by an ideal switch with several positions. A two-level inverter generates an output voltage with two values (levels) with respect to the negative terminal of the capacitor while the threelevel inverter generates three voltages, and so on.

The term multilevel starts with the three-level inverter. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. However, a high number of levels increases the control complexity and introduces voltage imbalance problems.

III. CARRIER-BASED SVPWM

Carrier based SVPWM allow fast and efficient implementation of SVPWM without sector determination. The technique is based on the duty ratio profiles that SVPWM exhibits. By comparing the duty ratio profile with a higher frequency triangular carrier the pulses can be generated, based on the same arguments as the sinusoidal pulse width modulation [8].

The power circuit of a three-phase voltagesource inverter (VSI) is shown in Figure 2., V_a , V_b , and V_c are the three output voltages applied to the star-connected motor windings, and where V_{dc} is the continuous inverter input voltage. This is a twolevel inverter consisting of six power transistors S1 through S6, which are controlled by switching signals.

When an upper transistor is switched on, the corresponding lower transistor is switched off. There are eight different combinations (000), (100), (110), (010), (011), (001), (101), and (111). The first and last states do not cause a current to flow to the motor, and hence, the line-to-line voltages are zero. The other six states can produce voltages to be applied to the motor terminals. If the inverter operation starts by state (100) to be state 1, it is possible to compute the voltage space vectors for all inverter states which are shown in the complex space vector plane in Fig.3 [3]. The six active voltage space vectors are of equal magnitude (2/3) V_{dc} and mutually phase displaced by 60° , as shown in Figure 3.

Note that the switching states of each arm should be combined with each other to compose the required three-phase output voltage. Because each pole voltage has only two levels according to the related switching state, the time duration in which the different voltages are maintained is definitely related to the voltage modulation task. Therefore, the modulation task can be greatly simplified by considering the relation between the time duration and the output voltage[9]. We now focus on the effective voltage that makes an actual power flow between inverter and load. Fig.4 shows the switching states of sector 1 at different times during two sampling intervals. T_S denotes the sampling time and T_{eff} denotes the time duration in which the different voltage is maintained. Teff is called the "effective time". For the purpose of explanation, an imaginary time value will be introduced as follows:

$$
Txs = \frac{Ts}{Vdc} Vxs * (x=a,b,c)
$$

 V_{as} ^{*}, V_{bs} ^{*} and V_{cs} ^{*} are the A-phase, B -phase, and C-phase reference voltages, respectively. This switching time could be negative in the case where negative phase voltage is commanded. Therefore, this time is called the "imaginary switching time".

Now, the effective time can be defined as the time duration between the minimum and the maximum value of three imaginary times, as given by

$$
\begin{array}{c}\n\text{There } T_{\text{eff}} = T_{\text{max}} - T_{\text{min}} \\
\text{Where } T_{\text{min}} = \min(T_{\text{as}}, T_{\text{bs}}, T_{\text{cs}}) \\
T_{\text{max}} = \max(T_{\text{as}}, T_{\text{bs}}, T_{\text{cs}})\n\end{array}
$$

When the actual gating signals for power devices are generated in the PWM algorithm, there is one degree of freedom by which the effective time can be relocated anywhere within the sampling interval.

Therefore, a time-shifting operation will be applied to the imaginary switching times to generate the actual gating times (T_{ga}, T_{gb}, T_{gc}) for each inverter arm, as shown in Fig. 4. This task is accomplished by adding the same value to the imaginary times as follows:

$$
\begin{array}{c}\nT_{ga} = T_{as} + T_{offset} \\
T_{gb} = T_{bs} + T_{offset} \\
T_{gc} = T_{cs} + T_{offset}\n\end{array}
$$

Where T_{offset} is the 'offset time'.

This gating time determination task is only performed for the sampling interval in which all of the switching states of each arm go to 0 from 1. This interval is called the "OFF sequence". In the other sequence, it is called the "ON sequence." In order to generate a symmetrical switching pulse pattern within two sampling intervals, the actual switching time will be replaced by the subtraction value, with sampling time as follows:

$$
\substack{T_{ga}=T_{s}-T_{ga} \\ T_{gb}=T_{s}-T_{gb} \\ T_{gc}=T_{s}-T_{gc}}
$$

IV. MODELLING OF PMSM

The stators of the PMSM and the wound rotor synchronous motor (SM) are similar and there is no difference between the back EMF produced by a permanent magnet and that back EMF produced by an excited coil. Hence the mathematical model of a PMSM is similar to that of the wound rotor SM [11], [12].

The stator *d*, *q* equations of the PMSM in the rotor reference frame are:

$$
\nu_q = r i_q + P \omega_r \lambda_d + p \lambda_q
$$

$$
\nu_d = r i_d - P \omega_r \lambda_q + p \lambda_d
$$

Where

$$
\lambda_q \ = \! L_q \; i_q
$$

$$
\lambda_d = L_d \, i_d + \lambda_m
$$

Where *P* is the pole pairs, *p* is the *d/dt* operator, v_q and v_d are the *q*, *d* axis voltages, i_q and i_d are the q , *d* axis stator currents, L_q and L_d are the q , *d* axis inductances, λ_q and λ_d are the *q*, *d* axis stator flux linkages, while r and ω_r are the stator resistance and rotor speed, respectively. λ_m is the flux linkage due to the rotor magnets linking the stator.

The electromechanical torque developed by the motor is:

$$
T_{em} = \frac{3}{2} P(\lambda_d i_q - \lambda_q i_d)
$$

By substituting the values of λ_q and λ_d in the above equation

$$
T_{_{em}} = \frac{3}{2} P(\lambda_{m} i_{q} + (L_{d} - L_{q}) i_{q} i_{d})
$$

The relationship between the electromechanical torque and the load torque is given as:

$$
\frac{d\omega_r}{dt} = \frac{1}{J_m} (T_{em} - T_l - B_m \omega_r)
$$

$$
\frac{d\theta_r}{dt} = \omega_r
$$

For dynamic simulation, the equations of PMSM presented above must be expressed in state-space form as the following:

$$
pi_q = \frac{1}{L_q} (v_q - ri_q - Po_r L_d i_d - Po_r \lambda_m)
$$

\n
$$
pi_d = \frac{1}{L_d} (v_d - ri_d + Po_r L_q i_q)
$$

\n
$$
po_r = \frac{1}{J_m} (T_{em} - T_l - B_m o_r)
$$

V. SIMULATION AND RESULTS

Figure5. Simulink model for three phase two level inverter fed PMSM Drive

A. Simulation Results of two level inverter fed PMSM drive using CBSVPWM

Figure 7.Output Line Voltage of a two level inverter

0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1 Figure 10.Output Torque of a two level inverter

B. Simulink model of three-level inverter fed PMSM Drive using CBSVPWM:

-20 -15 -10

Figure 11.Simulink model for three phase three level inverter fed PMSM Drive

C. Simulation Results of three level inverter fed PMSM drive using CBSVPWM

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Figure 15.Output Line current of a three level inverter

Figure 16.Output Torque of a three level inverter

Figure 17.Output Speed of a three level inverter Determination of harmonic distortion: By performing FFT analysis we can determine the harmonic distortion in the line current and line voltages.

FFT analysis

Figure 19.Determination of THD of line current of two level inverter

Figure 20.Determination of THD of line current of three level inverter

Figure 21.Determination of THD of line voltage of three level inverter

CONCLUSION

 Table I. Comparison of THD of Two and Three level inverters fed PMSM Drive using CBSVPWM

In this paper, simulation analyses concerning the applications of CBSVPWM control strategy on the two and three level inverters fed Permanent Magnet Synchronous Motor are presented. Carrier Based Space Vector Pulse Width Modulation gives the same results as that of Space Vector Pulse width Modulation, more over it reduces the calculation of dwelling times which simplifies the method .From this analysis author can conclude that multilevel inverter can eliminate the harmonics produced by the normal inverter. From the simulation results obtained we can say that the total harmonic distortion reduces by increasing the number of levels in the output voltage. The switching losses are also reduced by using this technique.

The THD from Table1, for the three level and two level are obtained and observed that the three level produces less harmonics and better speed, torque characteristics compared to two level. Therefore as the level increases we can further decrease the harmonic content and can improve the performance of the drive. Not only this CBSVPWM can easily implemented for n-level inverters.

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