Design of an Op-Amp Based Low Voltage Low Dropout Regulator Using 180nm CMOS Technology

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***Abstract*—This paper describes the designing of a Low Voltage, Low Dropout (LVLD) Regulator with fast self-reacting (FSR) technique in 0.18 µm CMOS process. The LVLD Regulator provides 1.2 V regulated output voltage. The design procedure includes pass transistor, error amplifier, fast self-reacting path and bandgap reference (BGR) circuit. The pass transistor is designed for a desired minimum dropout voltage. The error amplifier has been developed with a gain of 65 dB and UGB of atleast 1 MHz. Curvature compensated CMOS BGR with 1.8 V supply has been developed to produce 0.8 V output voltage with better temperature coefficient.**

***Index terms*—LVLD, pass transistor, error amplifier, FSR, BGR, curvature compensation.**

I. Introduction

Industry is pushing towards complete system-on-chip (SoC) design solutions among which one is power management. The study of power management techniques has increased spectacularly within the last few years corresponding to a vast increase in the use of portable, handheld battery operated devices. The aim of the power management scheme is to decrease the power consumption by prolonging battery life. Today Voltage regulators are found in nearly every electronic device. They provide the DC voltage for all the electronic circuits used in modern day applications. These applications range from High-speed multiprocessors to multi function cell phones. Voltage regulators can be split into two categories- Linear voltage regulators (LVR) and Switch mode power converters (SMPC).

An LVR can be considered as a building block of every power supply used in microelectronics. A dynamically adjusting resistor is sufficient to regulate the voltage. These convert a noisy input voltage into a stable and clean supply voltage by implementing the dynamically changing resistor pass element. Even though the SMPC offers higher efficiency, the switching noise affects the functionality of the circuits driven by it. The output noise available in commercial LVR is lower than SMPC. LVLD is one such LVR. LVLD regulators are used to provide efficient power management in mobile phones.

The proposed scheme gives less dropout voltage [1], desired line regulation, load regulation, PSRR and output voltage. Section II described the architecture of LVLD regulator with FSR technique, Section III deals with Op-amp designing, Section IV discusses the bandgap reference (BGR) biasing circuit, Section V describes the designing of LVLD regulator, Section VI shows the simulation results of LVLD regulator, the conclusion is given at last.

II. LVLD Regulator with FSR Technique

The block diagram of LVLD regulator with FSR technique is as shown in Fig.1. The key features are fast load transient responses, high loop gain, very low quiescent current and small on chip compensation capacitance.

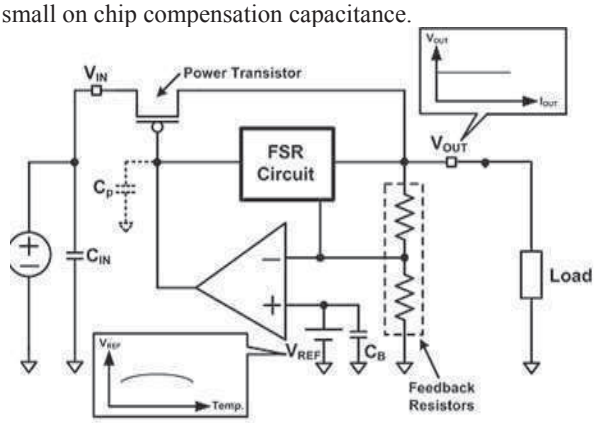

Figure 1. LVLD regulators with fast self-reacting (FSR) technique.

The proposed regulator has one main feedback loop and three ultra fast self-reacting paths. The need for the FSR paths are to decrease the output voltage when load current increases instantly where it achieves the name regulator. The designing of entire LVLD regulator includes pass transistor, feedback resistor, error amplifier and bandgap reference (BGR) circuit.

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III. Operational Amplifier

The Operational amplifier (op-amp) is the fundamental building block of analog integrated circuit design. Here it is designated to be used as an error amplifier. It is designed to achieve the desired gain and UGB of atleast 1 MHz. The schematic of this op-amp is shown in Fig. 2. The loop gain is achieved from the line and load regulations. Gain of the op-amp is given as,

$$A_v = \frac{2}{(\lambda_n + \lambda_p)^2}\sqrt{\frac{k_n k_p \left(\frac{W}{L}\right)_1 \left(\frac{W}{L}\right)_2}{I_{D1} I_{D7}}} \quad (1)$$

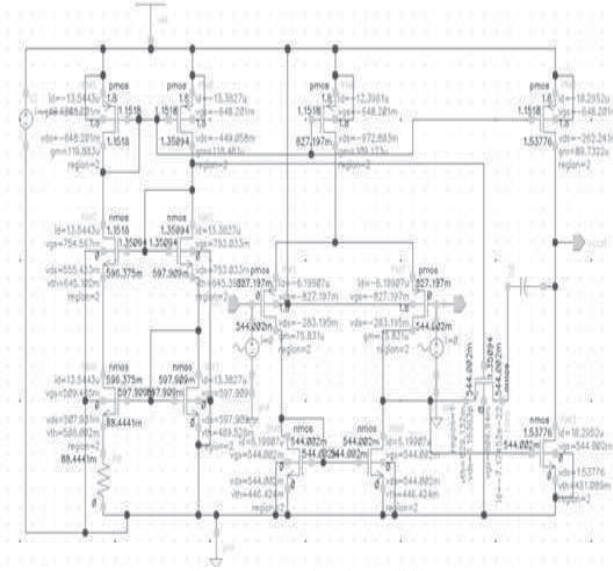

Figure 2. Operational Amplifier

Loop gain is distributed between the error amplifier, pass transistor and feedback resistor ratio. Majority contribution is attributed to the op-amp. The gain of 75 dB and a phase margin of 74.92^o are obtained. The simulated gain plot and phase plot are obtained as shown in Figure 3.

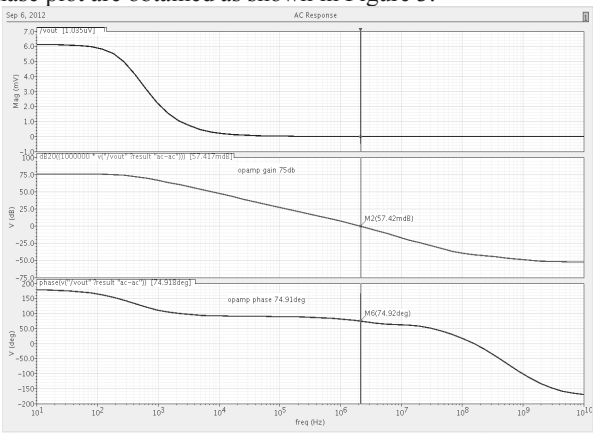

Figure 3. Gain and Phase plot

IV. Bandgap Reference Biasing

The bandgap voltage reference, which was firstly proposed by Widlar and was further developed by Kuijk and Brokaw, is the one commonly used in many advanced designs and many commercial products since it can provide a predictable reference voltage. The proposed reference scheme can provide from 0 V to near supply voltage by adjusting current mirror and resistor. The schematic of bandgap reference circuit is shown in Figure 4.

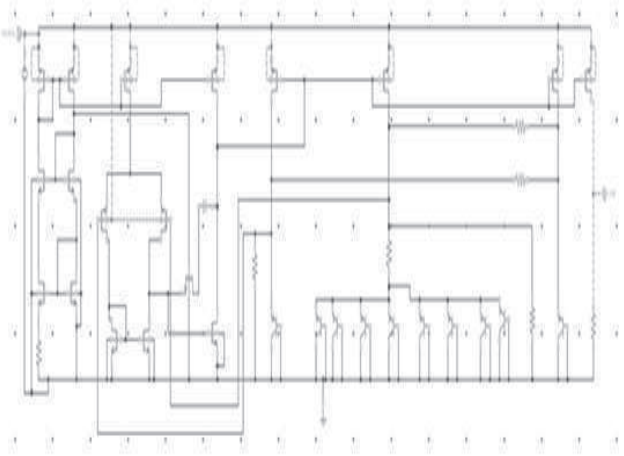

Figure 4. Bandgap Reference circuit

It combines the positive TC[3] of the thermal voltage with the negative TC of the diode forward voltage in a circuit to achieve a voltage reference with a zero TC. The temperature dependence of BGR is shown in Fig. 5.

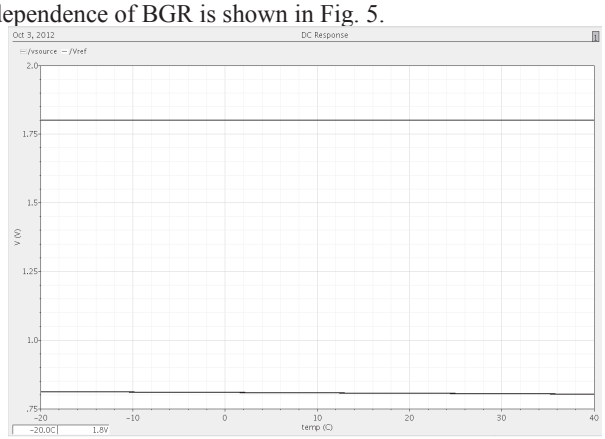

Figure 5. Temperature dependence of BGR

The PSRR plot is shown in Figure 6.

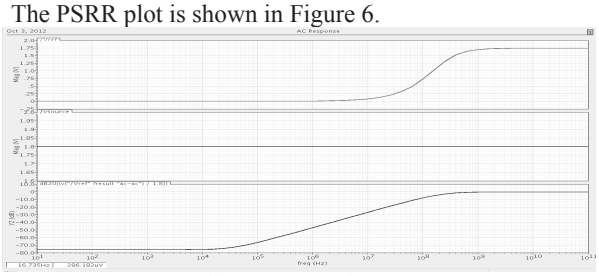

Figure 6. PSRR of BGR

The obtained PSRR is 72 dB at 1 KHz and provides a stable voltage independent of supply, process and temperature.

V. Designing of LVLD Regulator

The pass transistor is designed to deliver a drain current of 100 mA. Careful designing of it is required to have low dropout. The feedback resistor should have a relation one is twice the other. The dropout can be written as

$$V_{dropout} = V_{DSAT} = \sqrt{\frac{2I_{max}}{\mu_p C_{ox}\left(\frac{W}{L}\right)}} \quad (2)$$

The curvature compensation scheme[3] is used pushes the pole at the gate terminal of the power transistor and pole at the

LVLD regulator output towards higher frequency than the UGF. The overall circuit works like a single pole system and hence has high phase margin with good stability. The schematic of the LVLD regulator is shown in Figure 7.

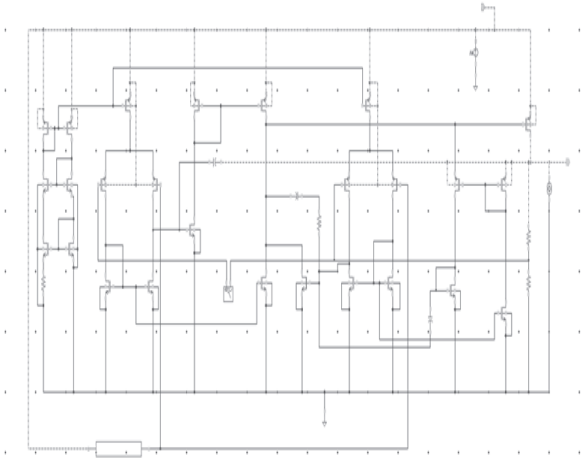

Figure 7: LVLD regulator

VI. Simulation Results of the LVLD Regulator

The frequency response was obtained for zero load current and full load current. The response for zero load current is shown in Fig. 8. The response for full load current of 100 mA is shown in Fig. 9. For full load current LVLD regulator achieves phase margin of 98^o and loop gain of 75 dB. For Zero load current LVLD regulator achieves phase margin of 63^o and loop gain of 65 dB. Fig. 10 shows the line regulation of the LVLD regulator. Fig. 11 shows the load regulation of LVLD regulator. Transient response of LVLD regulator for load current step and line voltage step is shown in Fig. 12 and Fig. 13. The PSRR of LVLD regulator is shown in Fig. 14. Obtained results are shown in Table I.

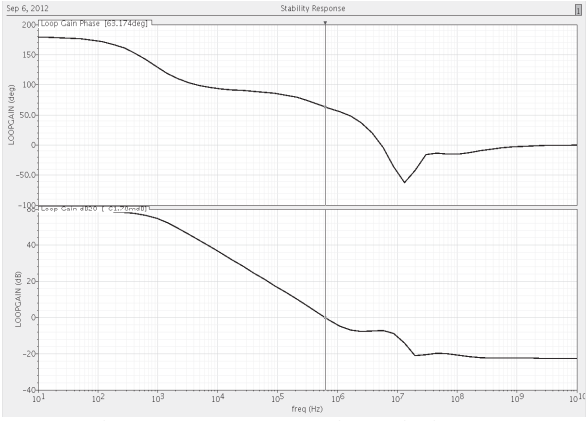

Figure 8: Frequency response for zero load current

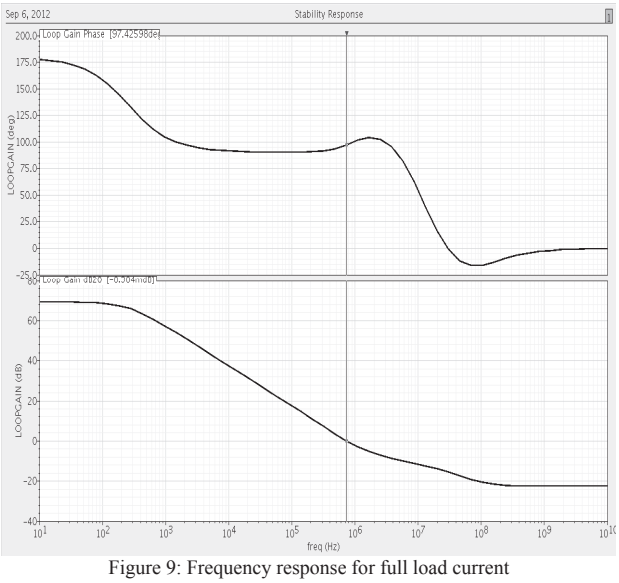

Figure 9: Frequency response for full load current

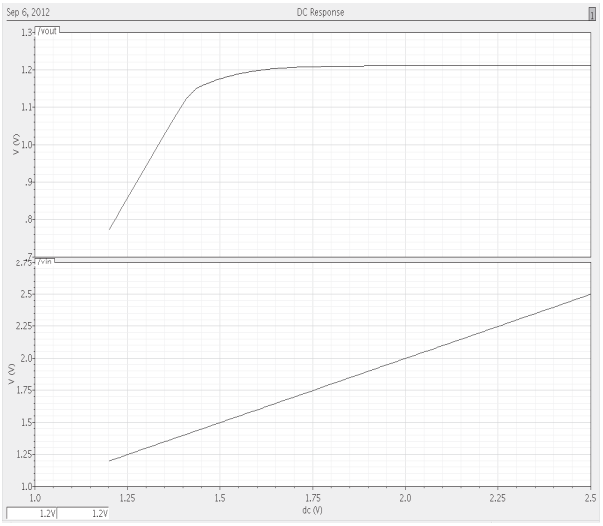

Figure 10: Line regulation of LVLD regulator

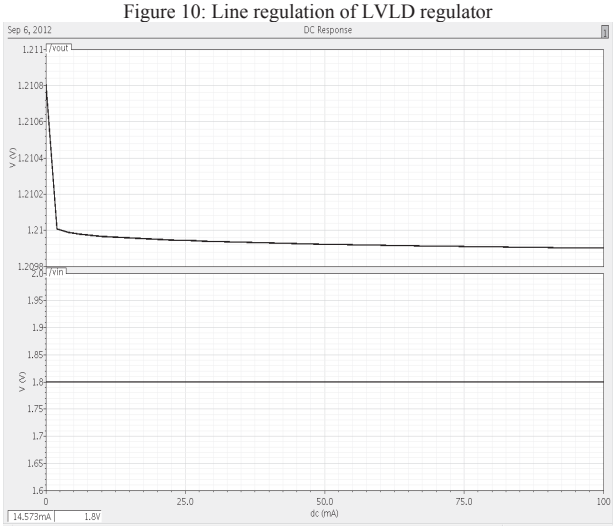

Figure 11: Load regulation of LVLD regulator

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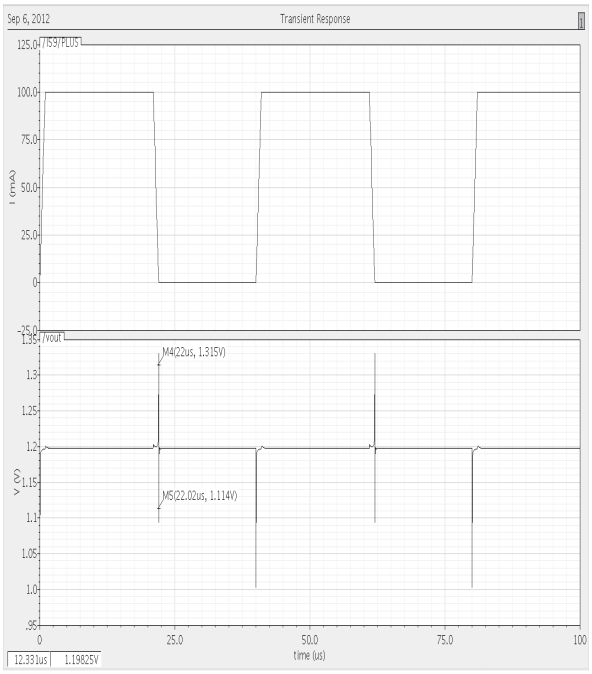

Figure 12: Transient response for load current step

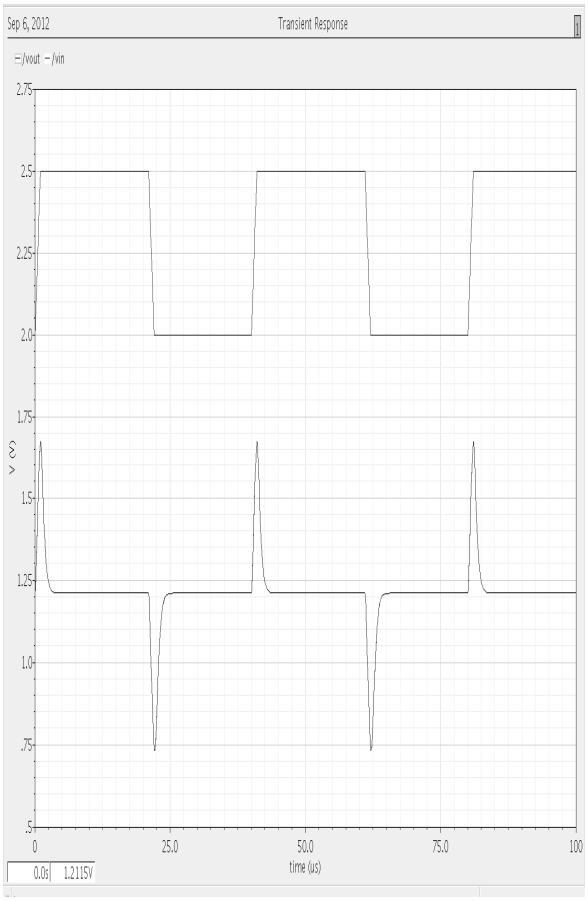

Figure 13: Transient response for line voltage step

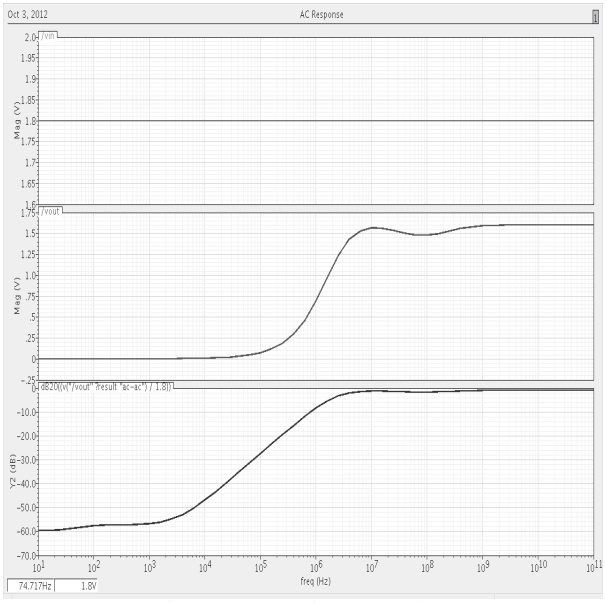

Figure 14: PSRR of LVLD regulator

TABLE I.
OBTAINED RESULTS

Parameter	Obtained value
Technology	0.18 µm
$I_{LOAD(max)}$	100 mA
Load regulation	0.162 mV/mA
Line regulation	1 mV/V
PSRR	52 B

CONCLUSIONS

In this paper a LVR type Low Voltage Low Dropout (LVLD) Regulator using Fast Self-Reacting (FSR) technique is presented. The proposed reference scheme provides from 0 V to near supply reference voltage. An operational amplifier designed with desired gain and UGB used as an error amplifier. Curvature compensation technique is used for stability of the circuit. The regulator has PSRR about 52 dB, Load regulation of 0.162 mV/mA, Line regulation of 1mV/V.

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