Design of Switched Capacitor Integrators using 90nm Technology

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Abstract—**The filters are important blocks in applications like image processing, communication, signal processing etc. Most of the filters are designed by using components like operational amplifiers, resistors, capacitors etc. But, in present VLSI design this direct implementation of RC based filters cannot meet the non functional constraints like high speed, less area and low power etc.**

The RC based analog filters require precise values of components to maintain required frequency characteristics. Hence design of controllable, large value, uniform linear resistor in a less area is difficult in standard VLSI process. By replacing a resistor with a Switched Capacitor principles can solve most of these problems. The switched capacitor filters are designed by using a basic block called as switched capacitor integrators. The switched capacitor integrators and filters require only capacitor ratios to be precise to meet the required frequency characteristics and other parameters. The main aim of this work is to design switched capacitor based integrators for both parasitic sensitive and parasitic insensitive designs using Cadence Virtuoso full custom design flow and 90nm technology.

Index Terms—**Op-Amp, Switched Capacitors, Integrators, VLSI, Filters.**

I. INTRODUCTION

The design and implementation of electrical and electronics systems is done by using passive components like Resistors(R),Capacitors(C) and Inductors(L) in the early stage of IC design area. The advancement in IC technology modified the used of inductors due to its large size and noisy characteristics. Hence the design of IC based circuits used Resistors, Capacitors and Operational Amplifiers (op-amps) etc [1].

The present analog and mixed signal design environment IC circuits must meet performance metrics like area, speed, power and cost etc. This is done by using either Bipolar Junction Transistor (BJT) or Metal Oxide Semiconductor (MOS) transistor technology. The BJT technology is selected for high speed applications and for portable and battery based application products MOS technology is used. In MOS technology the fabrication of resistor is a difficult task. The resistor is designed by using MOS transistors to meet different non functional constraints and other parameters.

The present System on Chip (SOC) analog and mixed signal design applications the resistors are replaced by using Switched Capacitor (SC) circuits consisting of switches and capacitor [2].

The basic concept of switched capacitor circuits is shown in Fig.1 [3].

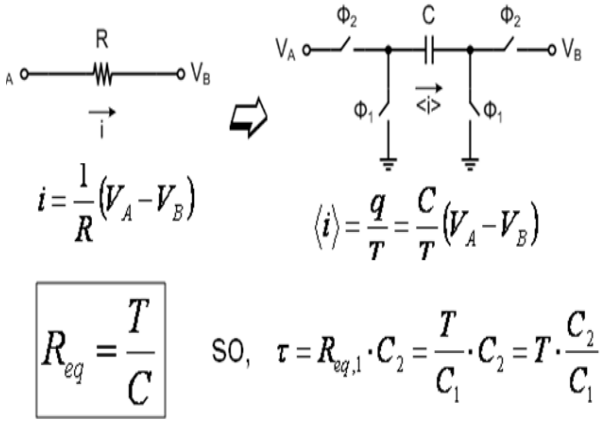

Figure 1: The basic concept of Switched Capacitors

In SC circuit capacitor is charged and discharged by using by using the non overlapping clocks φ1 and φ2 [2].The equivalent resistor of SC circuit is calculated by using the above formula. The non overlapping clocks example is shown in Fig.2 [3-4].

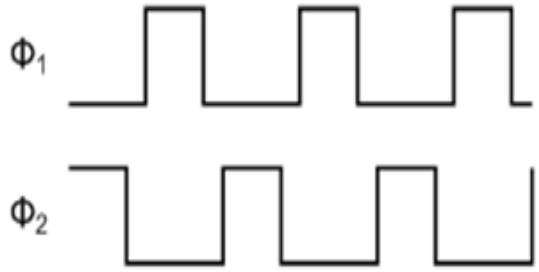

Figure 2: Example of non-overlapping clocks

The filters are important blocks in applications like image processing, communication, signal processing etc. Most of the filters are designed by using components like operational amplifiers, resistors, capacitors etc. The filters are designed by using RC based integrators and Op-Amp components. The RC based integrator and SC based integrators are shown in Figure 3[3-4].

The main aim of this work is to design Switched Capacitor based integrators for both parasitic sensitive and parasitic insensitive integrators two stage op-amp with compensation techniques to using cadence full custom design suite and 90nm technology.

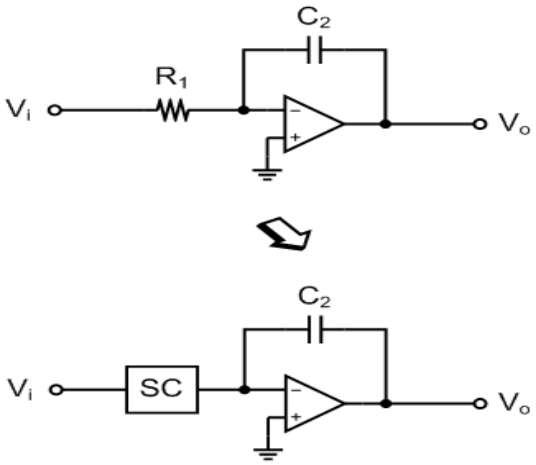

Figure 3: RC and SC based integrators

This paper is organized such that the section II gives general background and information of SC based parasitic sensitive and parasitic insensitive integrators. The section III describes the details of full custom design of SC based integrators using Cadence tools and also describes the simulation results. The conclusion is presented at the end followed by references.

II. SWITCHED CAPACITOR INTEGRATORS

The Switched Capacitor integrators are designed by using the SC circuit of Fig.1, concepts of Fig.2 and using Fig.3. The SC integrator circuits are divided into two types based on the parasitic capacitance effects.

1. Parasitic Sensitive SC Integrator
2. Parasitic Insensitive SC Integrator

The SC integrators are designed by using MOS transistors, capacitors and Op-Amp components. The capacitors are designed by using double poly metals to meet the performance metrics. The op-amp is designed by using basic two stage topology. The basic structure of two stage op-amp is shown in Fig.4 [5, 6].

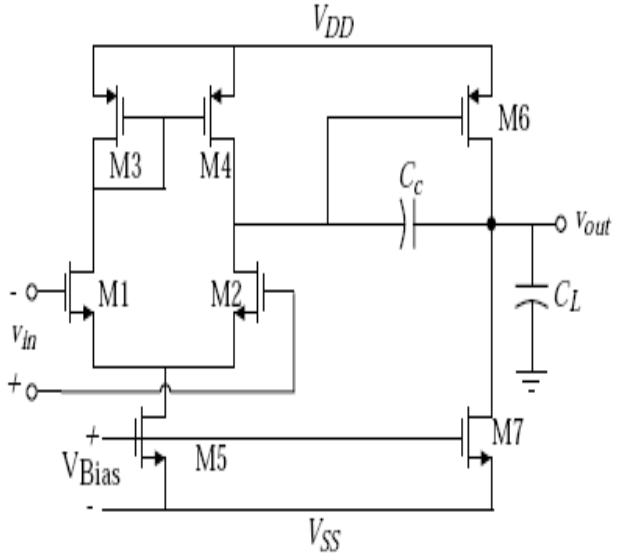

Figure 4: Two stage opamp

The parasitic sensitive SC integrator using above op-amp topology is shown in below Fig.5.

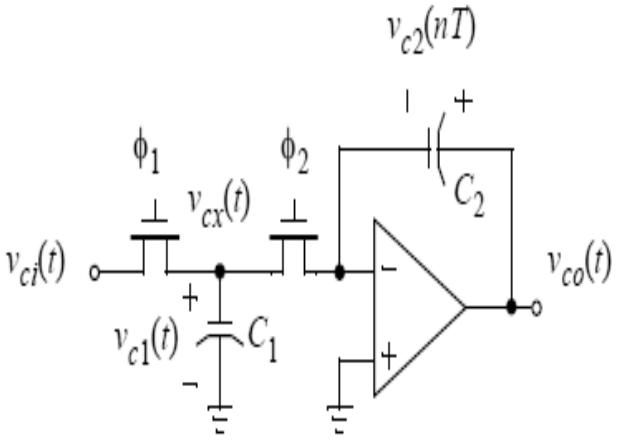

Figure 5: Parasitic Sensitive SC Integrator

The sample waveforms for the parasitic sensitive SC integrator are shown in Fig. 6.

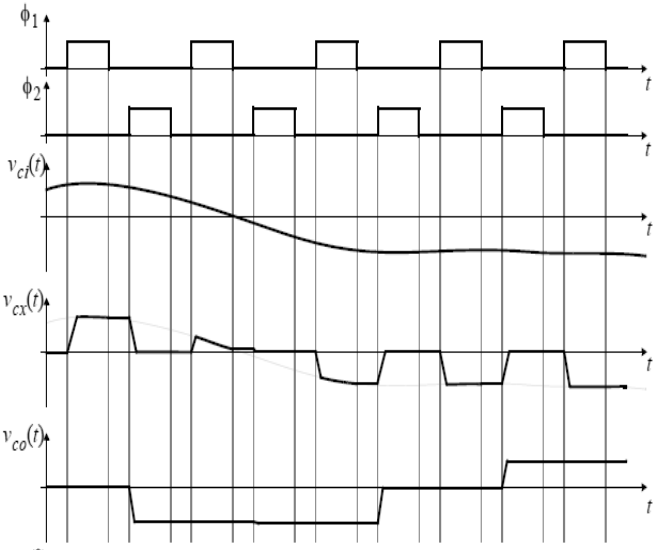

Figure 6: Sample waveform of parasitic sensitive SC integrator

The capacitor of SC integrator is designed by using double poly and there is equivalent parasitic capacitance C_{p1} and C_{p2} across C1 capacitor as shown in Figure 7.

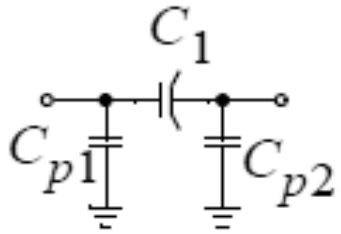

Figure 7: Equivalent parasitic capacitors

The effect of parasitic capacitors can be eliminated by using two more transistors to the switched capacitor circuit and this type of integrator is called parasitic insensitive integrator. The circuit of parasitic insensitive SC integrator is shown in Fig 8.

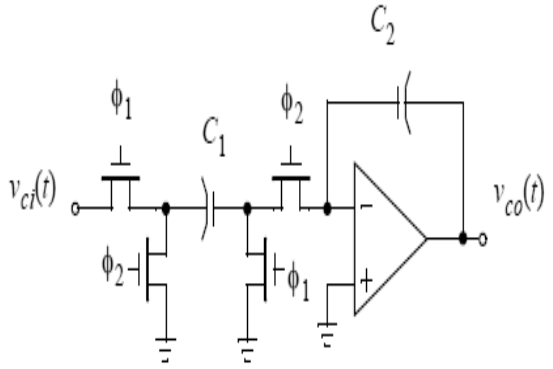

Figure 8: Parasitic Insensitive SC Integrator

III. FULL CUSTOM DESIGN OF SC INTEGRATORS

The Switched capacitor integrators are designed by using full custom IC design flow using 90nm technology. The Cadence Design suite tools are used for the design and simulation with individual tools as listed in Table1.This section gives the information of schematic designs of Switched Capacitor integrators and the simulation results.

TABLE I
CADENCE DESIGN SUITE TOOLS MAPPING

Design Action	Tool Name
Schematic entry	Virtuoso schematic editor
Symbol creation	Virtuoso Symbol editor
Simulation	Analog Design Environment tool
Layout	Assura
DRC	Assura
Layout Vs Schematic	LVS tool
Post layout verification	GDSII or OA
Targeted Technology	90nm

The transistor level full custom design of basic two stage op-amp schematic diagram using Cadence Virtuoso Schematic tools is shown in Figure 9. The symbol for the two stage op-amp design using Cadence Virtuoso schematic editor is also shown in Figure 10, which is used as a basic building block for the SC integrator circuits.

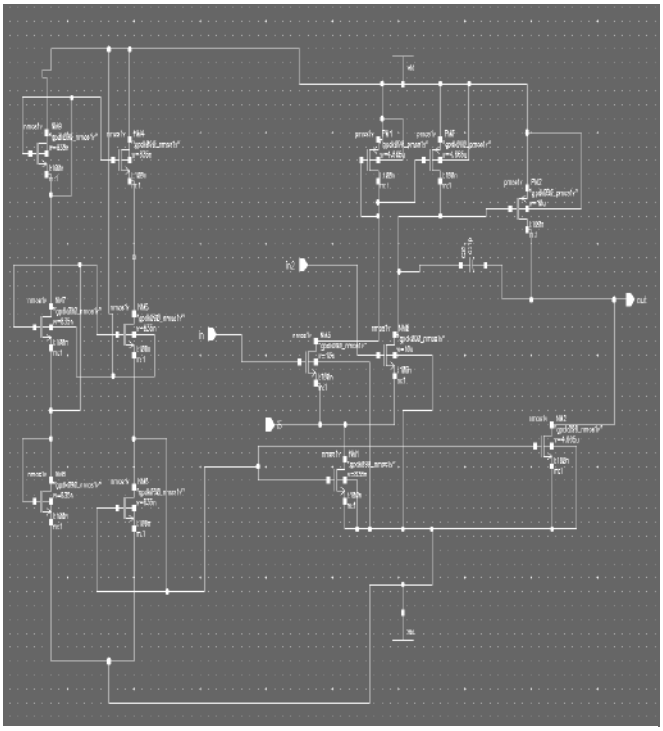

Figure 9: Two stage op-amp schematic

Figure 10: Op-amp Symbol

The schematic diagram of parasitic sensitive switched capacitor integrator using above two stage op-amp symbol is shown in Figure 11.

The simulation result of parasitic sensitive SC integrator is shown in Figure 12 and Gain plot is shown in Figure 13.

The schematic diagram of parasitic insensitive switched capacitor integrator using two stage op-amp symbol is shown in Figure 14.

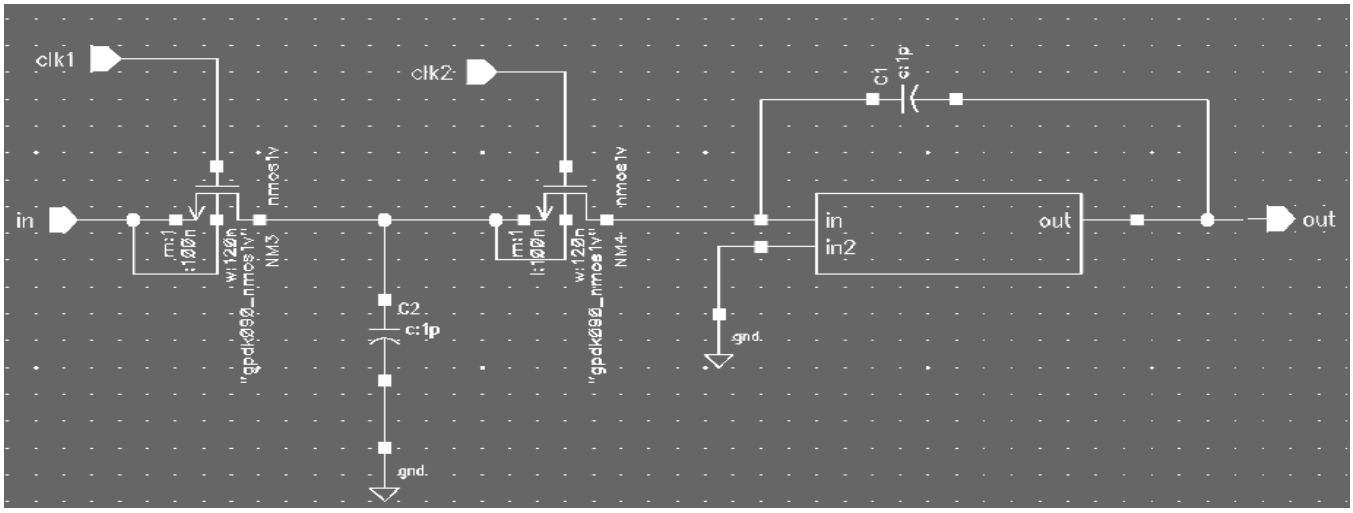

Figure 11: Parasitic Sensitive SC Integrator

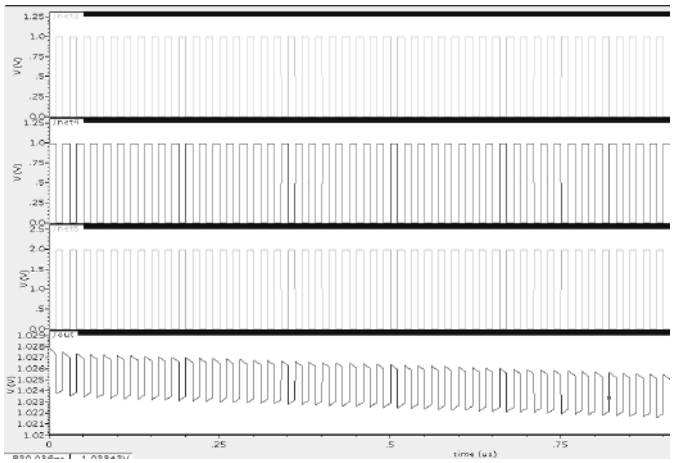

Figure 12: Simulation of parasitic sensitive SC integrator

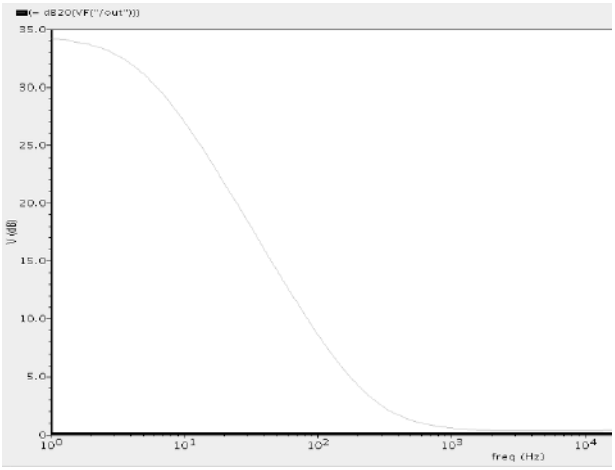

Figure 13: Gain Plot of Simulation of parasitic sensitive SC integrator

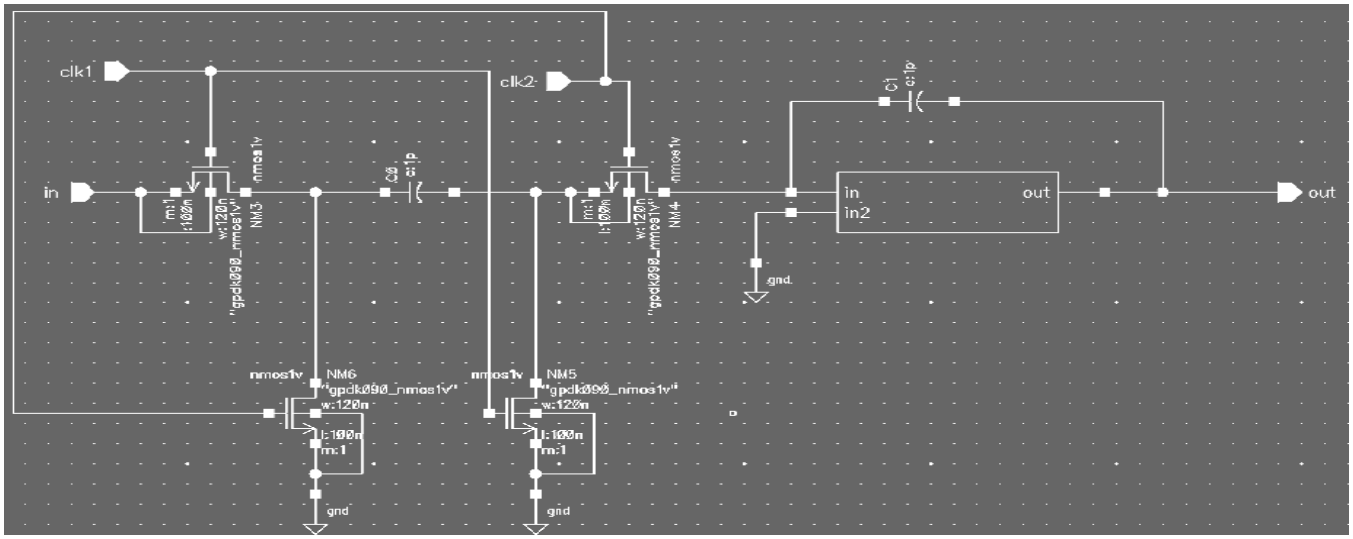

Figure 14: Parasitic Insensitive SC Integrator

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The simulation result of parasitic insensitive SC integrator is shown in Figure 15 and Gain plot is shown in Figure 16.

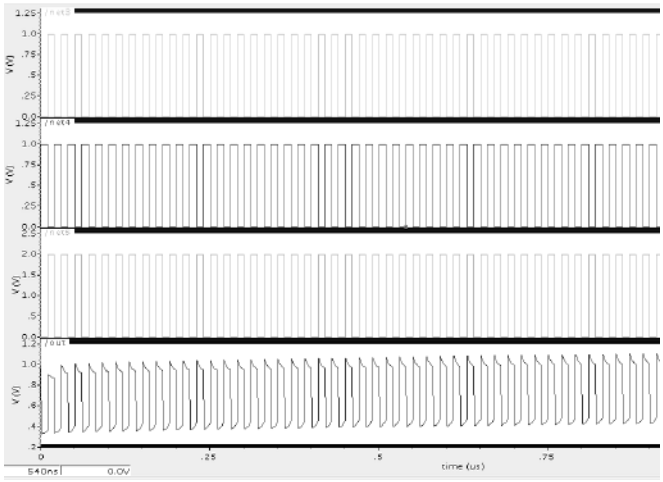

Figure 15: Simulation of parasitic insensitive SC integrator

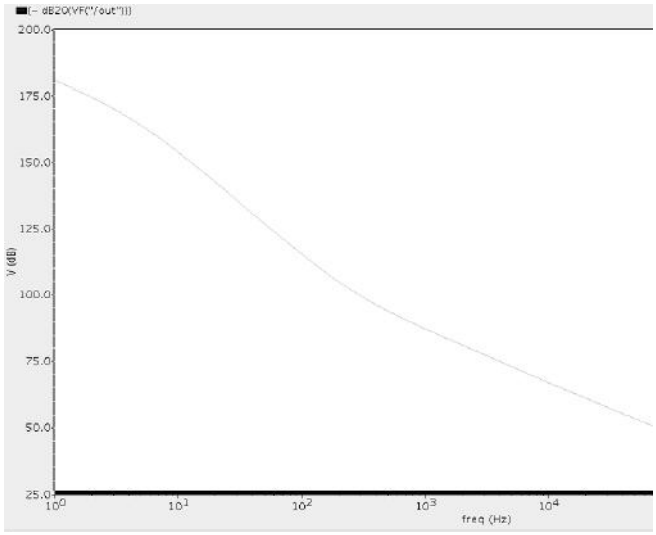

Figure 16: Gain Plot of Simulation of parasitic sensitive SC integrator

The gain comparison for both parasitic sensitive SC integrator (Figure 11) and parasitic insensitive SC integrator (Figure 14) are shown in Table 2. The parasitic sensitive SC integrator has a gain of 34dB and insensitive SC integrator has a gain of 178dB.

TABLE II
GAIN RESULTS COMPARISON

Parameters	Parasitic sensitive SC integrator	Parasitic insensitive SC integrator
Gain	34dB	178dB

CONCLUSIONS

The Switched Capacitor based parasitic sensitive integrator and parasitic insensitive integrators are designed and analyzed by using Cadence ICFB full custom design suite using 90nm technology.

The SC integrator circuits basic building block two stage op amp circuit is designed for simple compensated features using 90nm technology with L=100nm.

The Switched Capacitor based parasitic sensitive integrator is designed for a gain of 34dB and parasitic insensitive integrators are designed and achieved a gain of 178 dB.

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