Implementation of Low Power Sigma Delta ADC for Broadband Communications

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Abstract: **For the broadband communication systems, the high data rate converters are required to achieve high accuracy and higher bandwidth. The mixed signal approach using CMOS technology is mostly preferred for these applications. Now a days, the ΣΔ converters are gaining popularity with their robustness. This design is implemented mainly in digital domain with small analog content. In this paper, a high speed 14-bit ΣΔ modulator with 2 MHz signal bandwidth with low oversampling ratio is designed. To increase the resolution, the dual quantization technique is used. It simplified the design and reduced the hardware circuitry and power consumption.**

Index Terms: **ΣΔ modulator, ADC, DAC, quantization, Over Sampling, Low power and CMOS.**

I. Introduction

The high performance data converters require accuracy and high resolution of 12 to 16 bits, higher bandwidth with less production cost for broadband applications. The ΣΔ converters are mostly preferred for pipelining because of oversampling and robustness of the converter. The CMOS implementation of ΣΔ converter increases the inherent complexity but, improves the speed of the conversion process.

A high speed ΣΔ modulator for signal bandwidth of 2MHz is implemented in deep sub-micron 45 nm CMOS technology. The fourth order ΣΔ architecture is considered for the design [1]. The fourth order ΣΔ modulator consists of four integrators, comparator and amplifiers, ADC and DAC circuits. The amplifier and comparator are the analog blocks, and the remaining blocks are implemented in the digital form. Hence the mixed signal approach is used for the implementation of ΣΔ modulator in this paper.

The specifications of the ΣΔ modulator are considered for the applications of broad band communications. The table.1 represents all the specifications of important building blocks used in the modulator.

II. Building Blocks of ΣΔ Modulator

In this section, the important building blocks of ΣΔ modulator are designed and implemented in the 45nm CMOS technology. All these blocks are operated at the power supply of 1 Volt.

A. Front-end Amplifier

It is difficult to achieve specifications simultaneously, high gain and high speed due to degradation of output conductance in short channel transistors. By including a cascade stage, a better compromise between speed and gain is obtained, so the DC gain of the transistors with minimum length is increased to 80 dB and the gain bandwidth product of 250 MHz, with 37 mW power consumption.

TABLE I.
SPECIFICATIONS OF BUILDING BLOCKS FOR ΣΔ ADC

Modulator	Clock Frequency	60 MHz
	Differential Reference Voltage	1V
	Oversampling ratio	16
	Clock jitter	15ps (0.1%)
	Dual quantization	1bit /4 bit
Front-End Integrator	Sampling capacitor	0.5pF
	Switch on resistance	250Ω
	Capacitor non-linearity	25ppm/V
Amplifier	Open Loop DC gain	2500
	Slew rate	380V/µs
	Gain bandwidth product	235MHz
Comparators	Offset	±10mV
	Hysteresis	10mV
	Resolution time	3.5ns
ADC and DAC	Resolution	4-bit
	DAC INL	0.4% FS

Figure 1 shows a two stage operational amplifier (OpAmp1) with Miller compensation is used to achieve high gain; and high bandwidth is achieved. Miller compensation converts an internal pole pertaining to specific node, to become dominant pole by adding a small physical capacitance, which will be simulated as a large capacitance due to Miller effect and brings the effect of pole with low frequency. This technique is used for the transistors M12 and M13, so that high bandwidth as well as high speed can be achieved.

One more compensation technique called nulling resistor along with miller capacitor can be used to improve stability [2] [3]. The nulling resistor eliminates the zero present in the right half of s-plane. It even brings the zero present on RH side into LH side, so that excellent stability can be obtained. But nulling resistor implemented with MOSFET when coupled through miller capacitor degrades the transient response of integrator, as the output voltage will be reduced

due to compensation capacitor. This technique is used in this implementation as it needs less power to implement and is more stable with temperature and process variations.

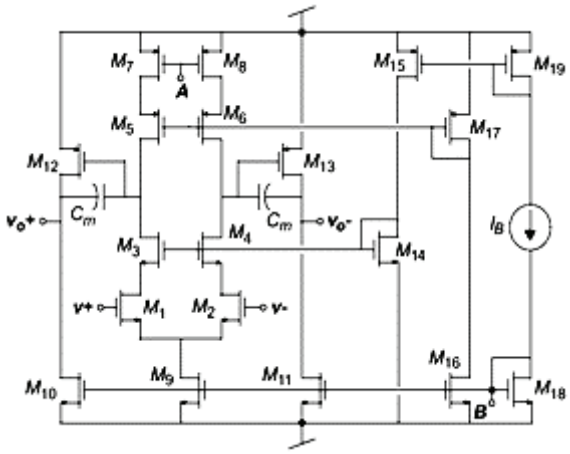

Figure 1. Two stage operational amplifier (OpAmp1) internal diagram with Miller compensation.

The weights used in implementing integrators strongly influences the output swing of the amplifier, when the reference voltage is fixed.

The transient response of the two stage Operational Amplifier used as a front-end integrator in the modulator is presented in the figure 2 [4]. It behaves like a first order system and it settles properly in the given time slot.

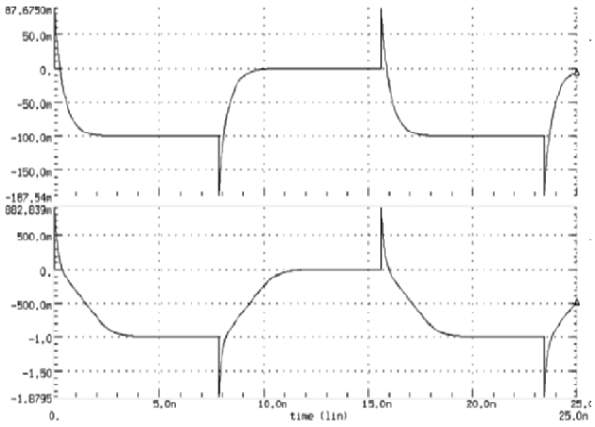

Figure 2. Transient response of two stage operational amplifier (OpAmp1)

The biasing requirement of an amplifier is fulfilled by transistors M14 to M19. The amplifier biasing stage is implemented by transistors M_{14} to M_{19}. A dynamic CMFB net is used to minimize the power consumption to zero static power dissipation. Note that an inverting stage (M_{20}, M_{21}) is added to the basic SC net in order to implement the negative common-mode feedback.

B. Amplifiers other than stage 1

The second stage and next stage integrators require medium DC gain amplifiers. Hence, a cascade single stage amplifiers are used. Telescopic operational amplifiers has advantage of providing signal path by only NMOS transistors, non-existence of mirror poles and a small bias current is required to operate with expected output voltage swing of 1 volt. The disadvantage of telescopic Op-Amp is that its common mode voltage levels at the both inputs must be different and also it requires a precisely controllable voltage reference to get stable and large voltage swing. A folded cascade operational amplifier is used in this design [5]. It has more advantages than telescopic Op-Amp such as, superior frequency response, better PSRR. However both consume equal power.

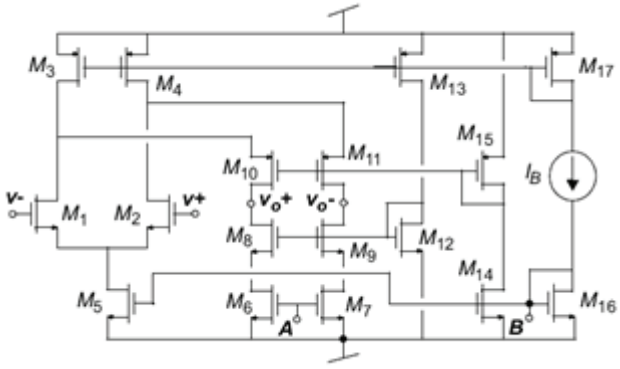

Figure 3. Schematic of Folded-Cascode Amplifier (OpAmp2, OpAmp3, OpAmp4).

The simulated output results of the OpAmp1, OpAmp2, OpAmp3 and OpAmp4 are presented in the table 2. The order of the ΣΔ modulator refers to the number of loops with integrator. These four Operational Amplifiers are used as four integrators in the fourth order ΣΔ modulator. The power consumption, gain and some important parameters are compared among all the operational amplifiers.

The power consumption of OpAmp4 is higher when compared with OpAmp2 and OpAmp3. The reason is that the OpAmp4 has larger load capacitance.

TABLE II.
SIMALTAED OUTPUT PARAMETERS OF THE FOUR AMPLIFIERS

Parameters	**OpAmp1**	**OpAmp2**	**OpAmp3**	**OpAmp4**
DC gain (dB)	80.0	62.8	55.7	62
GB (MHz)	250	311	261	167
PM (Degrees)	67	65	71	79
SR (V/μs)	390	410	320	185
Input Noise (nV/√Hz)	5	3.2	4.1	3.8
OS (Volts)	±2.5	±3.1	±2.9	±3.1
Power (mV)	38.5	4.5	4.0	6.6

The figure 4 shows the simulated output waveform of the second integrator, which is also used for third and fourth integrators in the modulator implementation. The output is linear but has limited slew rate as the applied input is a large step signal. This is tolerable for this design as it reduced the power dissipation.

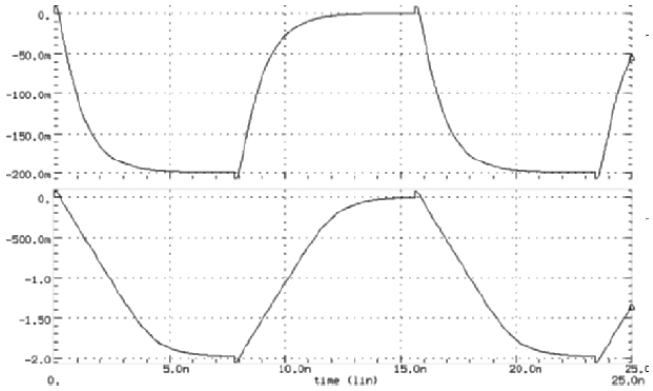

Figure 4.Simulated small- and large-signal transient response of the fourth integrator.

C. Comparators

The comparators used in this design needs low resolution time with large hysteresis voltage of up to 10 mV. Generally, this can be implemented with traditional comparator with pre-amplifier stage, positive feedback circuit used as decision making circuit and output buffer. But it takes large area and more power required for implementation. Instead a dynamic comparator with regenerative latch is used as it does not require the pre-amplification stage and has zero static power dissipation. The regenerative latch used acts as decision making circuit while comparing the two inputs.

Figure 5 shows the architecture employed for the implementation of comparators [6], which has been widely used in ΣΔ modulator design. In practice, this topology is capable of achieving resolutions that required with no pre-amplifying stage.

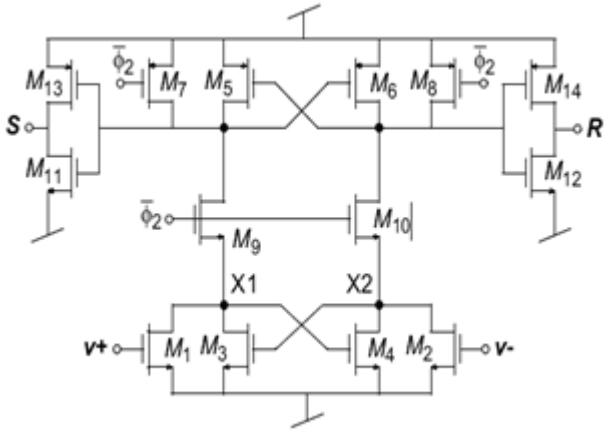

Figure 5.Dynamic comparator with Regenerative latch

The important features obtained after simulating the comparator are shown in the below table III.

TABLE III.
COMPARATOR RESULTS AFTER SIMULATION

Hysteresis	< 10 mV
Resolution time, LH	2.5 ns
Resolution time, HL	2.3 ns
Power consumption	0.65 mW

III. PROGRAMMABLE A/D/A CONVERTER

The switched capacitor 4-bit A-D-A converter is implemented and discussed in this section. It can also be used for 2 or 3 bit resolutions. A fully differential parallel ADC is designed and used to compare the differential voltage as illustrated in the figure.6

A. A/D converter

The fully differential flash architecture is used for A to D converter, which compares the differential input voltage with the reference voltages [7]. The reference voltages are produced by DAC. During the $\Phi_1$phase, Vref positive and Vref negative values are stored in the input capacitors, which are then used to compute the difference during phase Φ_2. At the end of Φ_2, comparators are activated to find the sign of that difference. The thermometer output code of the 15 comparators is then translated to a code using AND gates.

Comparators in the ADC are identical to those used in the 1st and 2nd stage. Multi-metal sandwich capacitors of value are used and the analog switches are identical to those in the SC. The timing scheme of the switches has been adapted to reduce the capacitive load to the fourth integrator. Nevertheless, it suffers from input dependent charge injection from switches controlled by Φ_2. This problem has been overcome by making these switches considerably smaller (for both NMOS and PMOS), with no degradation of the converter performance.

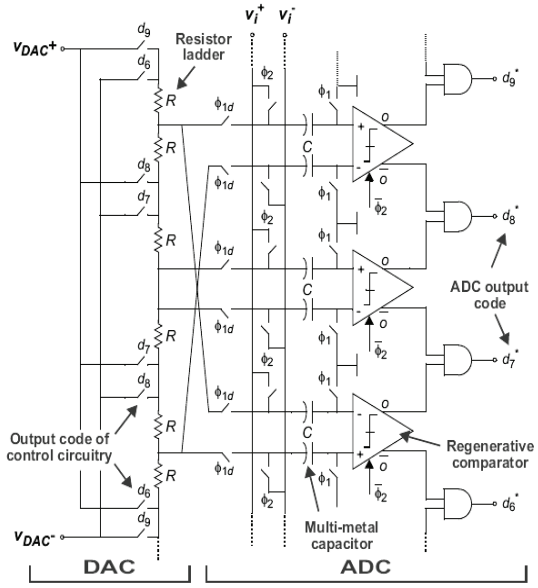

Figure 6. Programmable A/D/A converter: Partial view of the Switched Capacitor implementation.

B. D/A Converter

For the proposed ADC, the ladder type DAC is used. This DAC provides the reference voltage for the ADC. The same DAC is also used for the conversion of digital voltage to analog output voltage in overall A/D/A converter. The ladder resistor network will generate the equivalent output analog voltage based on the selection of resistors corresponding to digital code.

The Resistor ladder network comprises of 30 unit resistors, which are connected between positive and negative reference voltages, +Vref and –Vref respectively. The value of each unit resistor is 50Ω and differential full scale current is 1.33mA. The resistors are implemented by un-silicided poly layers to provide high resistivity, good matching and is independent on variations of temperature. It also provides small settling error.

C. Control Circuitry

The 4 bit A/D/A converter provides 2 or 3 bit resolution with the help of digital control circuitry, which is shown in the figure 7. The selection of the desired resolution is done with two signals, S_{3b} and S_{2b}. The partial view of the digital control circuitry, which is used in the programmable A/D/A converter is shown in the figure 8.

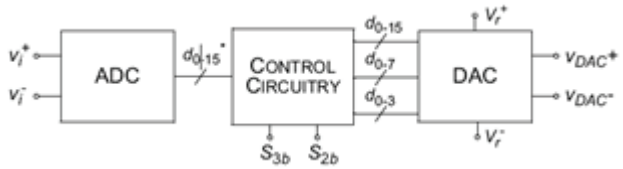

Figure 7. Block diagram of the programmable A/D/A converter.

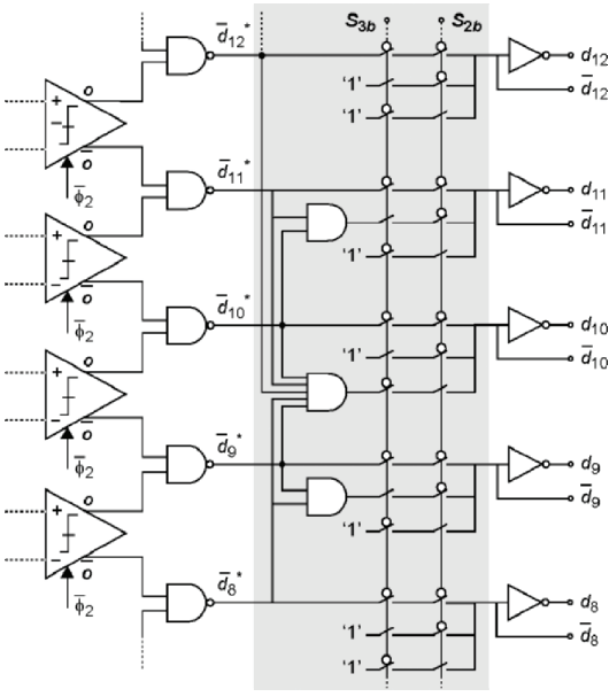

Figure 8. Partial view of the control circuitry.

D. Clock phase generator

The different clock phases are generated using the circuit diagram shown in the figure 9 from external clock. The delayed version of these clock phases are used to reduce signal dependent charge injection [8]. The complimentary cock signals for the phases also generated by this circuit.

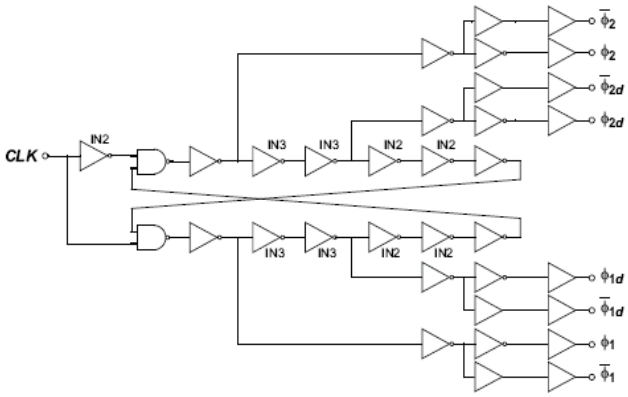

Figure 9. Clock phase generator and drivers.

The complete timing of the different clock phases are used in the ΣΔ modulator as shown in the figure.10

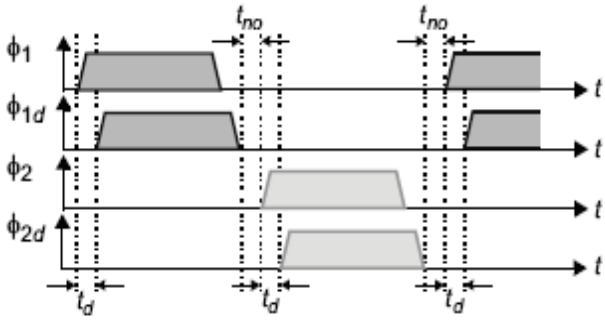

Figure 10. Timing of the clock phases in the ΣΔ modulator.

IV. RESULTS

The functionality of the entire A/D/A converter operation is tested and measured using specific samples. The ADC, DAC and clock driver is also measured using specific test samples.

The code histogram method of sinewaves is used to measure the ADC performance [9]. An amplitude of 1 volt and 103 KHz frequency was applied to the ADC. The corresponding digital codes for 100 input periods were measured by digital tester. The analog and digital voltages are estimated from the 16 bit digital output code.

The 16-bit digital code is applied using digital tester to DAC and measures the performance, and the corresponding analog output voltages of DAC using high accuracy multi meter [10]. The performance measurement results are shown in the table 4. From that table we can conclude that the proposed ΣΔ modulator meets the specifications.

TABLE IV.
PERFORMANCE MEASUREMENTS OF THE A/D/A CONVERTER

Parameter	ADC		DAC	
	%FS	LSB	%FS	LSB
Offset error	-2.014	-0.203	0.302	0.045
Gain error	4.595	0.659	-0.633	-0.098
DNL	2.894	0.453	0.153	0.016
INL	1.652	0.256	0.156	0.018

V. CONCLUSIONS

In this paper, the low power ΣΔ modulator is implemented with resolution of 14 bits for the ADC with signal bandwidth of 2MHz. A 2-1-1 ΣΔ Modulator with 4^{th} order 3 stage cascade topology employing dual-quantization was selected. The dual quantization is only used in the last stages of modulator. The quantization power was reduced without any change in the linearity of the modulator. All the building blocks of the modulator are implemented in SC form using CAD tools. The topology of all the blocks and designs in transistor and gate level are described in this paper.

The entire modulator is implemented in the CMOS technology with power supply voltage of 1V. The low V_t and multi metal capacitors, gates and switches with thick oxide are used to reduce the power in the modulator

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