High Performance ALU Using Carry Look-ahead Adder

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Abstract: **A Low Power 8-bit Arithmetic Logic unit (ALU) using a Carry look-ahead adder (CLA) and placing Low V_t (LV_t) cells in Critical path is anticipated. The ALU is designed in 90nm CMOS technology. ALU is the most essential circuit in any processor. It consists of AE, LE, CLA and CE. This ALU is designed to calculate Arithmetic and Logical operations. Power and Delay values of different 8-bit adders like CLA, Sparse and Ripple Carry Adder (RCA) are designed and compared. The simulation results show that the design of ALU using CLA and incorporating High V_t and Low V_t cells in the CLA gives more power and delay efficient than with only Standard threshold voltage cells.**

Index Terms: **Arithmetic Extender, Logic Extender, Carry Extender, Carry Look-ahead Adder, ALU.**

I. Introduction

ALU is the major power hungry block in any microprocessor and micro controller. It performs both arithmetic and logical operations. Conventional ALU consists of Arithmetic Extender, Logical Extender, Carry Extender and Ripple carry adder. An Adder is an integral part of the ALU and it is a power density block in ALU. Hence, to improve the performance of ALU in terms of Power and delay, High V_t Cells are utilized. The three different types of transistors are

1. Low V_t transistor (LV_t)
   The low V_t transistor type is used for applications where the speed is of primary importance. The disadvantage of this type of transistors is that, due to low threshold Voltage (V_t), the static power is very high.
2. Standard V_t Transistors (SV_t)
   The standard V_t transistor type is used when delay and static power has been traded off.
3. High Vth Transistor (HV_t)
   The High Vth transistor is a favor for extremely low static power consumption.

For reducing power and delay High V_t cells are used in entire ALU and in critical path of CLA, Low V_t transistors are used. The reference [5] and [6] explains about the power reduction of the design using PTL and Gate diffusion technique and [7]-[10] shows the concept of low power techniques in various Arithmetic circuits.

Here the design of an eight bit ALU with three select lines for performing eight operations are shown in Figure-1. Out of these eight operations, four operations are logical and four operations are arithmetic operations. The design includes four basic blocks: They are CLA, Logic Extender (LE), Arithmetic Extender (AE), and Carry Extender (CE). The function of LE is to operate logic operations, AE is to operate arithmetic operations, CE is for carry operations and CLA is for actual arithmetic operations.

II. Conventional ALU

The Arithmetic Logic Unit (ALU) is the further most significant block in microprocessor [1]. This one is used on behalf of executing arithmetic and logic operations alike addition, Subtraction, Logical OR and Logical AND. In the Conventional ALU, Ripple carry adder (RCA) is used, and the delay and power values are more. So, instead of the RCA, Carry look-ahead adder has been selected. Since, ALU requires high speed and Low power. The overall circuit for 4-bit ALU is shown in figure1 [2]. The two different Combinational circuits in front of CLA are LE and AE.

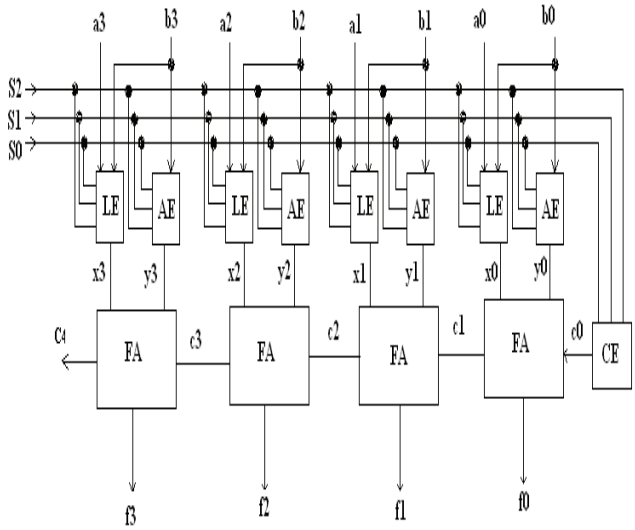

Figure 1. Existing ALU System.

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TABLE I.
ALU FUNCTION TABLE

S2	S1	S0	Operation Name	Operation	X(LE)	Y(AE)	C0(CE)
0	0	0	Pass	Pass A to output	A	0	0
0	0	1	AND	A AND B	A AND B	0	0
0	1	0	OR	A OR B	A OR B	0	0
0	1	1	NOT	A`	A`	0	0
1	0	0	Addition	A+B	A	B	0
1	0	1	Subtraction	A−B	A	B`	1
1	1	0	Increment	A+1	A	0	1
1	1	1	Decrement	A−1	A	1	0

From the functional operation of ALU shown in table-1 the selection input S2 is the main important parameter for selecting Arithmetic operations and Logical operations. When the selection line S2 is '0', then Arithmetic operations are performed and when S2 is '1' then Logical operations are performed. S0 and S1 are going to select any one of the operations.

TABLE II.
TRUTH TABLE FOR LE

S2	S1	S0	X_i
0	0	0	a_i
0	0	1	$a_i.b_i$
0	1	0	a_i+b_i
0	1	1	a_i'
1	X	X	a_i

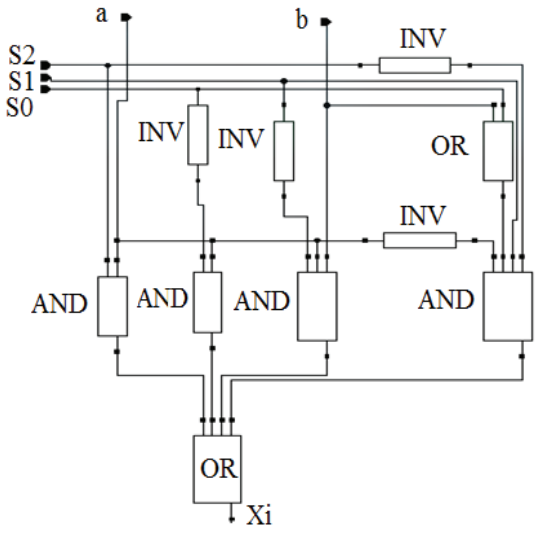

Figure 2. Schematic of LE

In LE and AE blocks all types of logical and arithmetic operations will be carried out. The operands a_i and b_i are inputs to LE and AE. The LE performs the operation based on selection lines (S0, S1, and S2) and inputs a_i and b_i. The schematic diagram and truth table of LE is shown in figure-2 and table-2 respectively.

TABLE III.
TRUTH TABLE OF AE

S2	S1	S0	bi	Yi
0	X	X	X	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

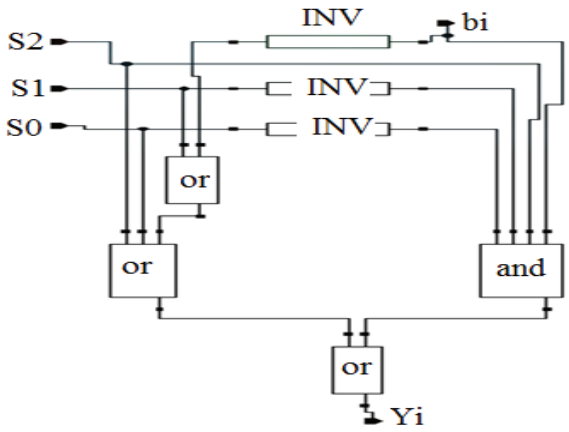

Figure 3. Schematic of AE

TABLE IV.
TRUTH TABLE FOR CE

S2	S1	S0	C0
0	X	X	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

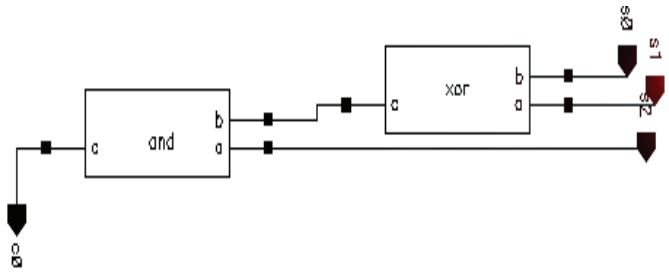

Figure 4. Schematic of CE

AE performs the operation based on selection lines and secondary input bi. It does not depend upon the primary input a_i. The schematic diagram and truth table of AE is shown in figure.3 and table.3. The Carry Extender is another important block in ALU. It depends on selection lines and gives the output of CE to CLA. The schematic diagram and truth table of CE is shown in figure-4 and table-4 respectively. Now the simulation outputs of LE and AE are x_i and y_i respectively. These x_i and y_i act as inputs to the CLA and give the simulation outputs as sum and carry. The selection lines S0, S1 and S2 are three selection lines for 8-bit ALU used to select outputs of LE and AE are x_i and y_i

respectively. The operation of ALU through the selection lines are shown in table-I.

III. Design of CLA

In ripple carry adder each carry-in signal is reliant on the carry out signal from the preceding full adder. The full-adder delay is very extreme. But the carry look-ahead adder [1] doesn't depend on the previous carryout signal. The equations for Carry look-ahead adder from full adder equation [1] is

$$C_{i+1} = x_i y_i + c_i(x_i + y_i) \quad -(1)$$

From the above equation let $g_i = x_i y_i$ and $p_i = x_i + y_i$

Then equation- (1) can be written as

$$C_{i+1} = g_i + c_i p_i \quad -(2)$$

Using equation - (2) expand the expression for designing 4-bit Carry look ahead adder.

For getting C_1 Substitute i=0 in the equation (2),

$$C_1 = g_0 + c_0 p_0 \quad -(3)$$

For C_2 substitute i=1 in the equation -(2)

$$C_2 = g_i + c_1 p_1 \quad -(4)$$

But $C_1 = g_0 + c_0 p_0$, so substitute equation-(3) in the equation -(4)

Then $C_2 = g_1 + p_1(g_0 + p_0 c_0)$

$$= g_1 + p_1 g_0 + p_1 p_0 c_0 \quad -(5)$$

For getting C_3 Substitute i=2 in the equation - (2)

$$C_3 = g_2 + p_2 c_2 \quad -(6)$$

And $C_2 = g_i + c_1 p_1$. Hence, Substitute C_2 in the equation – (6)

$$C_3 = g_2 + p_2(g_1 + p_1 g_0 + p_1 p_0 c_0)$$

$$= g_2 + p_2 g_1 + p_2 p_1 g_0 + p_2 p_1 p_0 c_0) \quad -(7)$$

For getting C_4 Substitute i=3 in the equation – (2)

$$C_4 = g_3 + p_3 c_3 \quad -(8)$$

But $C_3 = g_2 + p_2(g_1 + p_1 g_0 + p_1 p_0 c_0)$.Hence, Substitute equation – (7) in the equation – (8).

And $C_4 = g_3 + p_3(g_2 + p_2 g_1 + p_2 p_1 g_0 + p_2 p_1 p_0 c_0$

$$= g_3 + p_3 g_2 + p_3 p_2 g_1 + p_3 p_2 p_1 g_0 + p_3 p_2 p_1 p_0 c_0 \quad -(9)$$

Using the overhead carry equations, the carry look ahead adder signals from C_1 to C_4 have been produced. The outputs of two input xor gates are sums of CLA. The four bit CLA is shown in Figure.5.

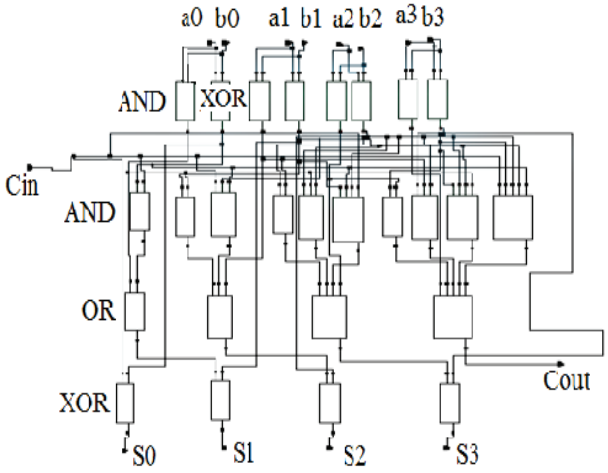

Figure 5. Schematic of 4-bit CLA

IV. Proposed CLA

In this paper three 8-bit Ripple carry adder (RCA), sparse adder and Carry look ahead adder are designed and the power and delay values are calculated. Table- V shows that CLA gives best power and delay values than the other two adders.

The aim of the paper is to reduce the power and delay of the ALU. So CLA has chosen instead of RCA. Since, CLA is a key block of ALU, in order to reduce power and delay, the proposed 4-bit CLA using the High V_t cell concept has been shown. In the present technology, there are different types of MOS transistors. Those are Low V_t cells, High V_t cells and Standard V_t cells etc. The concept of High V_t cells is explained here.

4.1 High V_t Cell concept

The region just below V_t of a transistor is called the sub-threshold region [4]. After the gate to source voltage V_{gs} is less than threshold Voltage V_t, then the leakage current

$$I_{leakage} = \mu(W/L)e^{(-qV_t/\eta KT)} \quad -(10)$$

Where μ = mobility

W = width of MOSFET

L = Length of MOSFET

K = Boltzmann's constant

T = Temperature

q = Charge of an electron

V_t= Threshold Voltage

η=Sub-threshold switching Coefficient

This indicates that the parameters μ, K, q are constants and only V_t and W are dependent on $I_{leakage}$. As the width of MOSFET rises, leakage current also rises and as V_t increases, the leakage current decreases exponentially. This, in turn lessens leakage power. So in this circuit all blocks of the Carry Look-ahead adder are designed and PMOS transistors are replaced with High V_t (HV_t) cells. So the MOSFETs will be operated at their threshold voltage. Because of this, delay increases and power dissipation is reduced greatly.

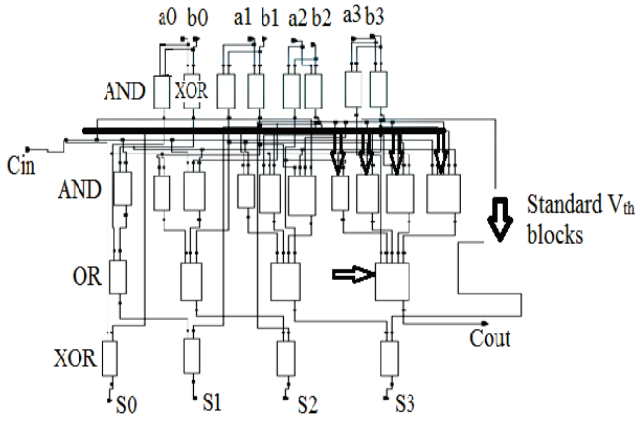

Figure 6. Proposed CLA

This justifies the usage of high V_t devices for low power applications in this design. The aim of this paper is to reduce power and delay. So the combination of these cells will give better performance than using the Standard V_t cells. In this topic, to reduce the delay and power, using Standard V_t cells and High V_t cells has been explained. Hence, in this 4-bit CLA, finding the critical path is quite important. The definition of Critical path has been given below.

Critical path: The longest delay path between inputs to output.

Here, the proposed 4-bit CLA the critical path is shown in Figure.6. It is C_{in}→ Four AND gates → OR gate. So to reduce delay, critical path blocks are designed with Low V_t cells. Next, to reduce power all remaining blocks are designed with High V_t cells.

4.2 Design of 8-bit CLA

The proposed 8-bit CLA is designed with cascading two 4-bit CLA as shown in figure-7. The Carry out waveform of first CLA is connected to the C_{in} of next CLA as shown in figure.7. The output waveform of the 8-bit CLA is shown in Figure-8 and Figure-9

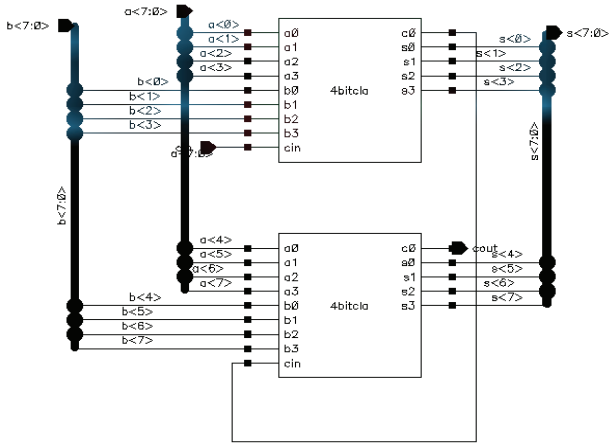

Figure 7. Schematic diagram of 8-bit CLA

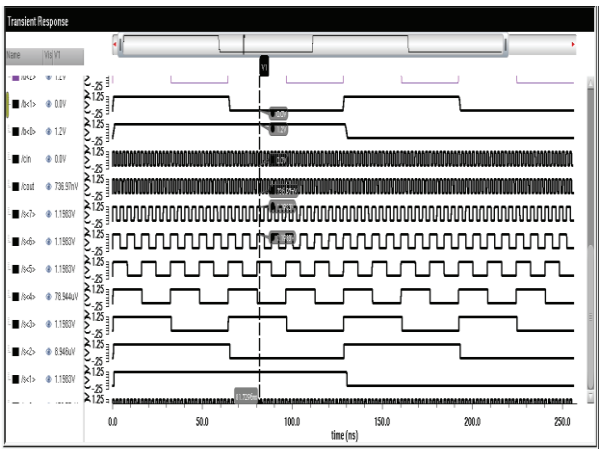

Figure 8. Simulation waveform of CLA-I

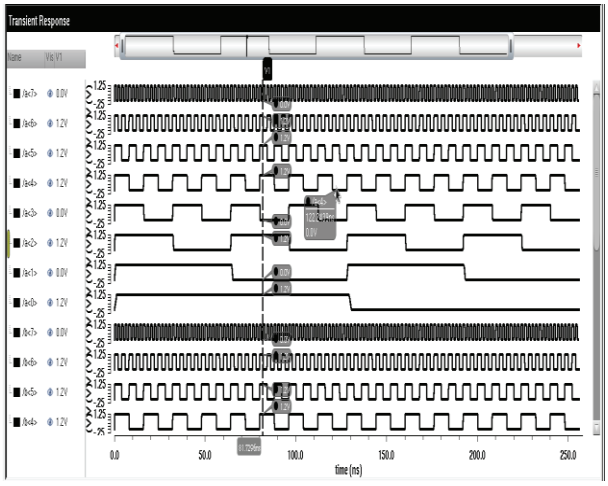

Figure 9. Simulation waveform of CLA-II

The proposed 8-bit ALU is shown in Figure.10. It has three selection lines, two 8-bit inputs a<7:0>, b<7:0> and outputs are Sum<7:0> and Carry. The internal blocks are Logical Extender, Arithmetic Extender and Carry Extender respectively. The simulation waveform of 8-bit ALU is shown in figure.11.

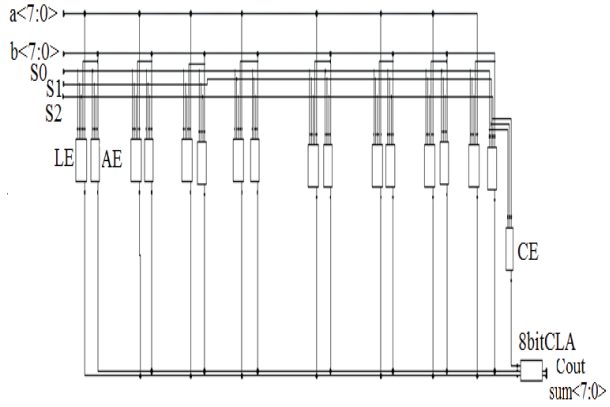

Figure 10. Proposed 8-bit ALU

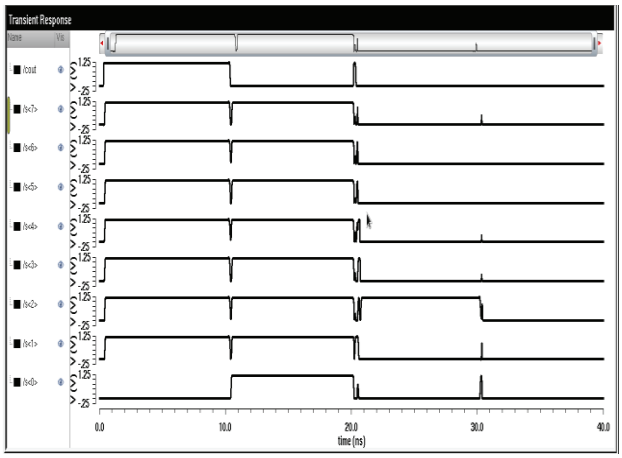

Figure 11. Simulation waveform of ALU

V. Simulation Results

TABLE V.
COMPARISON TABLE OF ADDERS

Parameter	Power(µW)	Delay(pS)
Ripple Carry adder	24.22	64800
Sparse adder	34.97	62400
Carry Look- ahead adder	22.92	81.7

Table –V shows the power and delay values of the Ripple Carry adder, sparse adder and Carry look-ahead adder. In the above mention adders Carry Look ahead adder gives Low power and delay.

TABLE VI.
PERFORMANCE PARAMETERS OF CARRY LOOK-AHEAD ADDER

Parameter	Power(µW)	Delay(pS)
Using Standard Vt Cells	5.619	89.13
Using High Vt Cells	3.81	136.9
Applying Low Vt cells in Critical Path	3.92	102.2

Table.VI shows that the performance of CLA using Standard V_t cells, using High V_t cells and after applying Low V_t cells in the Critical path. The average power dissipation of the Carry look-ahead adder (CLA) is 5.61µW. After applying High V_t cells in all P- MOSFETs, power consumption was reduced to 3.81 µW and delay was increased to 136.9pS. I.e. 47% of power consumption was reduced and 53% of delay was increased. In this ALU design, delay is also an important parameter. So, further reducing the delay, critical path was identified and placed in all the cells in the critical path to Standard V_t cells. Then 2.8% of power consumption was increased and 33.9% of delay was reduced. Hence, this high performance of CLA is used in the ALU.

TABLE VII.
PERFORMANCE OF 8 BIT ALU

Parameter	Power(µW)	Delay(pS)
8bit ALU using Standard V_t Cells	50.8	246.3
8 bit ALU using High V_t cells in CLA	44.32	296.24
8bit ALU Applying Low V_t in Critical Path of CLA	43.58	258.5

Table-VII shows the performance of 8 bit ALU when it is designed with Standard V_t cells, High V_t cells and after applying Low V_t cells in the Critical path of CLA. The average power consumption and delay of ALU is 50.8 µW and 246.3pS respectively. After placing HV_t cells in CLA 14.6% of average power consumption was reduced and 20% of delay was increased. So, to further reduce the power and delay Low V_t cells are placed in critical path of CLA. Then 1.69% of power consumption was reduced and 14.5% of delay was reduced. This shows the best performance of power and delay of 8-bit ALU.

VI. Conclusions

The main goal of this paper is to reduce power and delay. The key element in the 8-bit ALU is the 8-bit Carry look-ahead adder. So, to reduce power High V_t cells are used in the P-MOSFET's of Logic gates, and to reduce delay standard V_t Cells are used in logic gates of critical path. After applying the High V_t Cell concept in CLA, power reduction in ALU was 14.6%, and the delay reduction was 14.5% after placing Low V_t cells in the Critical path of CLA. This 8-bit ALU can be designed for other than these eight operations. This ALU can be extended to 16-bit also. This 8-bit ALU is can operate all Arithmetic and Logical operations. The total 8-bit ALU is designed in 90nm CMOS technology using Cadence tools.

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