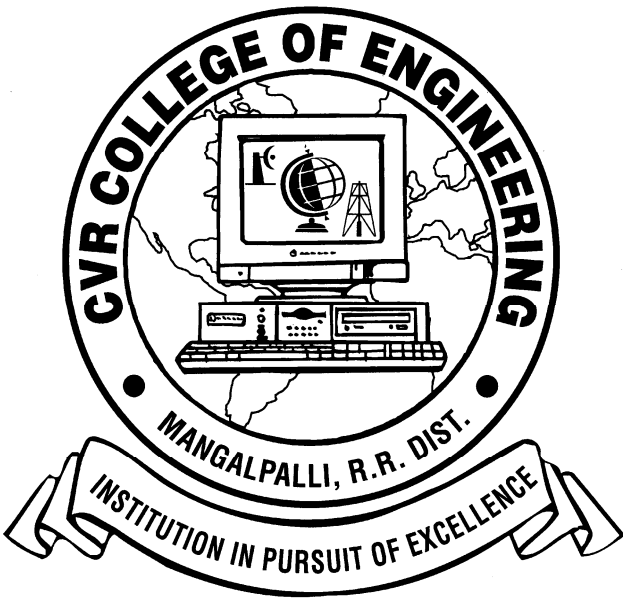
CVR JOURNAL OF SCIENCE & TECHNOLOGY



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EDITORIAL

We are happy to bring out Volume 7 of the Biannual Journal of our college, CVR Journal of Science & Technology, with a wide spectrum of papers from different branches of Engineering, Science and Management. As was the case for the previous volumes, we received a number of papers. Out of the papers received, a limited number of 20 papers were selected for inclusion in the current volume, based on the recommendations made by the members of the Editorial Committee.

The breakup of the papers among the various disciplines is as follows:

CSE - 4; ECE - 8; EEE - 2; EIE - 2; IT - 1; H&S - 2; Mgmt -1

The authors include staff members of our college and some from external institutions as coauthors. Three papers in Computer Science are from outside. The Computer Science papers span the important areas of Networking, Semantic Web and Component-based frameworks.

Topics selected for publication also include research work into advanced subjects like cognitive radio, software defined radio, image processing, chip design, data mining etc.

The papers that are selected from EEE cover advanced topics such as multilevel inverters and smart grid. Steps are already initiated by the government of India to transform conventional grids in to smart grid. The paper covers various aspects of smart meters which include technologies used in smart meters.

We hope that the interest of staff members of all the departments of our college will grow further in contributing their research work in the journal. We have been including some papers from external organizations and it will be our attempt to attract more numbers from outside so as to broaden the scope of our journal.

I am grateful to all the members of the Editorial Board for their help in short listing papers for inclusion in the current volume of the journal. I wish to thank Sri K. Venkateswara Rao, Associate Professor and Sri B. P. Deepak Kumar, Programmer in the Department of CSE for help in the preparation of the papers in camera ready form for final printing.

K.V.Chalapati Rao
Editor

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Component based Frameworks for exporting Graphic functionality through automation layer

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***Abstract*— The Component technology though complex to implement has several advanced features in development of graphic frameworks. Pattern Frames are evolved to solve such complexities. This paper uses Microsoft COM Technology for providing solution. These principles enable common developer to use advanced technology for providing solutions using complex technology in a simple way and providing patterns to common client to use these in simple processes. It presents procedure of building automation process. As Microsoft changes procedures reorienting structures, these processes work in all versions though they are demonstrated in Visual Studio 6.0. Results obtained and code segments are also presented. Abstract pattern frame, Wrapper and other pattern frames and Helper object are presented.**

***Index Terms*— Pattern- Frames, Automation Layer, IDL ODL script, Helper Object, Wrapper, Display files, Semantic graphic behavior, graphic components, graphic frameworks, debug driver tool, Microsoft graphic applications, object oriented models and frameworks. Dynamic display files. Component Object Model COM, Macros, Wizards.**

I. INTRODUCTION

The software Industry is adopting new procedures and technologies for rapid development of software. The requirements of the industry and client are also changing rapidly. Though industry started with business and information processing applications, mainly for railways and other industries, now the industry's concentration is on total simulation of real time environment, knowledge extraction, decision making, rapid application development using frameworks, making developer independent of development environments, using reuse techniques and patterns and frameworks.

In this connection several frameworks are developed in computer graphics, computer based design CAD, Geographical Information system GIS, Industrial Plant designed system and several military systems [8,9,10,11].The Intergraph Solid Edge, Imaginer, Smart Plant, Geological systems (GeoMedia) and several graphic frameworks have been developed in Microsoft Technology. They are exhibiting advanced technical features using Microsoft Technologies, namely COM Technology starting from Visual studio 2.0 from 1994 onwards.

COM technology has many advantages compared with Object Oriented Technology. But its implementation is very complex. Companies like Microsoft have provided several Wizards and frameworks stating from Visual Studio Versions 2.0, 4.0, 5.0, 6.0 and 7.0, and subsequently .NET versions incorporating more and more technical features. The COM Framework of Microsoft implements almost all Design Patterns.

II. OBJECT ORIENTED TECHNOLOGY VERSUS COMPONENT TECHNOLOGY

There are several unsolved problems in the present Object Oriented Technologies. A simple Object Oriented Technology cannot provide solutions to such problems. Typical problems one faces with the present object oriented technology are discussed below. [1-7,12]

1. In cases where new objects are formed inheriting from more than one base class, if two base classes have the same function, the inherited class cannot resolve to which base class it has to map that function.
2. The object hierarchy is too complex for the developer. For example, sometimes the MFC object hierarchy is too confusing to the developer. A typical complex object hierarchy is shown in Fig. 1 .
3. The encapsulation of objects is not perfect. The object details are not encapsulated. The inherited object should know everything about the base class along with its full hierarchy for using it. We are giving extra information to the user in this technology. Giving more information than necessary to the user is against abstraction and information hiding principles and is not advisable in any technology.
4. One more problem is that the objects do not have a common root and the C++ object hierarchies form a disjoint set of trees.
5. We have no solution to handle an unknown objet problem. That means, we cannot hold or perform even a minimum set of operations on an object for which information is unknown.
6. It is difficult to expose the behavior across process boundary

It is difficult to divide any task into independent modules. Tightly coupled modules will enforce restrictions on extendibility of the modules. If modules are loosely coupled, they can be designed and extended independently, without affecting other modules. There are several such problems, for which there is no solution in direct Object Oriented Technology. Today's Component Object Model is providing solutions to such problems. The COM technology is also an object-oriented technology. The COM object is also a C++ object, but the way it manages the data and behavior is entirely different. It adopts several

design patterns to solve above problems. Microsoft provides several frameworks to implement these solutions.

Though it provides solutions to many of the problems, it is too costly to manage. The COM object is not a single object; it is a set of objects. A set of interfaces it supports represents the behavior of a COM object. The COM object encapsulation is perfect. It hides entire object including the object source, object hierarchy and object name. Without knowing even the name of the object, one uses the COM object.

The modules in COM based applications are loosely coupled. They communicate through a set of interfaces, which the components of the module support. The components are assembled with a set of interfaces. COM does not support inheritance. The COM aggregation of components will do the job of inheritance in a more effective way. Aggregating existing components forms new components.

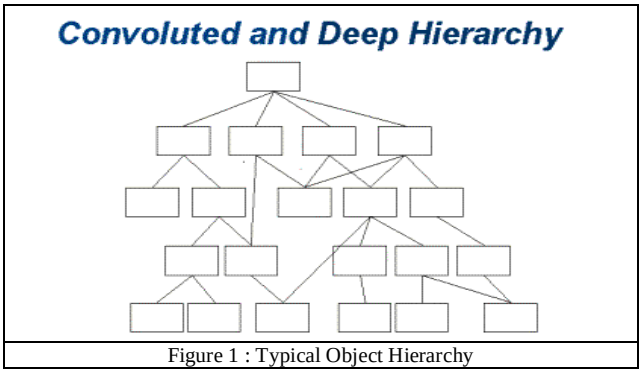


Figure 1 : Typical Object Hierarchy

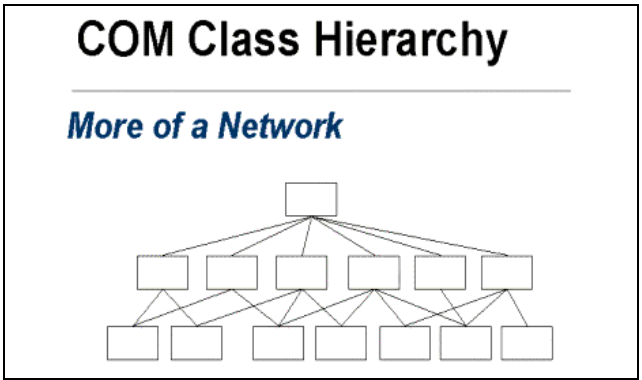


Figure 2 : 2 COM Hierarchy

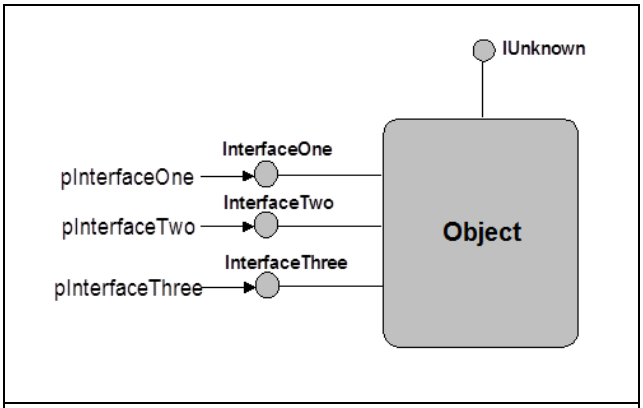


Figure 3 COM Object Model

The Hierarchy of Component Technology is simple. Fig. 2 presents a typical COM object hierarchy. Unlike C++ objects, all COM objects belong to the same family. The COM Hierarchy is a simple tree of depth two. All the COM objects and their interfaces are inherited from the common interface known as IUnknown interface. A Typical COM object is presented in the Fig. 3.

III. FEATURES OF COMPONENT TECHNOLOGY

The COM Concept of Ownership:The COM technology introduces the concept of the ownership subsystem. Each component has an owner. The owner of a component is also a component. A component may be owner of more than one component, but each component has only one owner. Any COM object without an owner is not treated as a full-fledged component. Such components cannot participate in aggregation and other activities of the software environment under consideration. A few special types of components with a specific purpose are without the owner. A class factory object of a COM object has no owner as it is given a special purpose of implementing a design pattern, namely 'Class Factory', which is a creational pattern, the intent of which is to create components in a uniform way through system registry without class name, server location and the type in which component it is implemented.

The owner of a component has full control over the component. A pointer to IUnknown interface of the owner component is stored along with the COM object. A component can become owner of itself but the owner IUnknown interface should not be null.

Fig. 4 presents two COM objects with owners. The first COM object holds its own IUnknown interface. In this case, it is owner of itself. The second COM object has an aggregated COM object in it. The owner of the aggregated COM object is the outer COM object. The outer object also should have an owner. In this case the outer object is the owner of itself. When we query an interface on any component, it will pass the call to the outer object, which is the owner of the object. The outer object also passes the call again to its owner. Finally, the call will reach the owner itself. When we query on the IUnknown interface of internal interfaces, the call will never pass the outer-object. If IUnknown is passed, the system will collapse as ownership gets collapsed, spoiling internal integrity and security.

The IUnknown interface alone can make the object unloaded, by making the interface count zero. That is why, the IUnknown is known as the controlling interface. These concepts will play an important role in the COM aggregation. The IUnknown interface is hidden within the outer-object. This is not given to the other components or procedures. This is as powerful as a pointer to the object.

COM object is a set of assembled components, but the user views it as a single object. Entire internal management is encapsulated through these concepts. Loading, managing

and unloading the inside components are the jobs of the outer object.

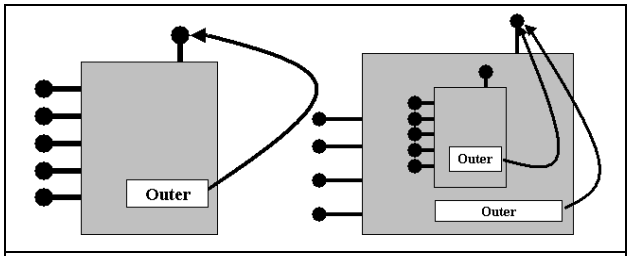


Figure :4 COM Aggregation with Coupling Components with IUnknown Interfaces

TABLE I
IUnknown Interface format

```
class IUnknown
{
  protected:
        ULONG      m_cRef;
  public:
    STDMETHODIMP QueryInterface(REFIID, LPVOID FAR*);
    STDMETHODIMP_(ULONG)        AddRef(void);
    STDMETHODIMP_(ULONG)        Release(void);
}
```

The definition of IUnknown interface is presented in Table 1.

i) The m_cRef means reference count to represent number of objects using the components. Once the count is zero, the object gets deleted automatically.
ii) The AddReff increases the reference count when the new client objects start using the object and decreases the count when it is released.
iii) When the object under the service leaves the component, automatically the count will be decreased; otherwise memory leak and runtime error crash the system. These are major problems in Component based systems.
iv) Query Interface of any Interface can ask other Interfaces from the Component for further use with the Interface ID. Depending on the permission, it releases in a systematic way unlike simple objects for which the number of clients is not known.

The COM Aggregation:

The Components cannot be inherited; as they are windows objects and they are registered objects. The name and location of the header file and server is not known to the client. The COM technology reuses the component using a special technique known as aggregation. The COM aggregation is managed in several ways depending up on the requirement. The way of managing the aggregated object will decides the type of aggregation.

i) Fig. 5 presents a typical COM aggregation. In this, the outer object delegates all the queries to all the aggregated objects in a specified order without seeing the queried interface. This is known as perfect delegation.
ii) Fig. 6 presents another type of COM aggregation. The Line object aggregates two point components. The Line query interface function will decide to which object it has to pass the query.
iii) Fig. 7 presents the COM technique of interface containment. The COM technology uses containment for overwriting the behavior. The outer object will re-implement the interface, which is available in the aggregated object.

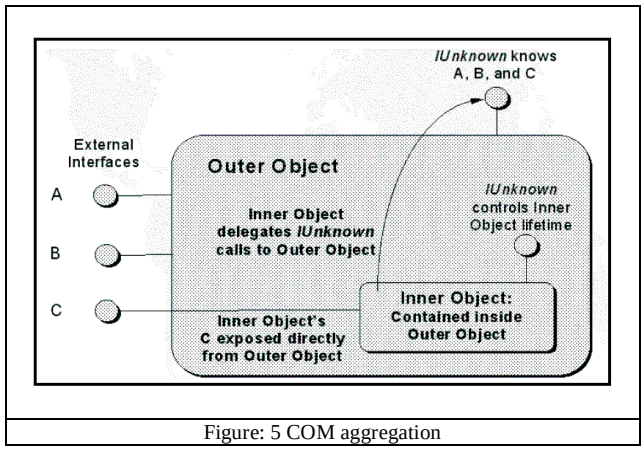


Figure: 5 COM aggregation

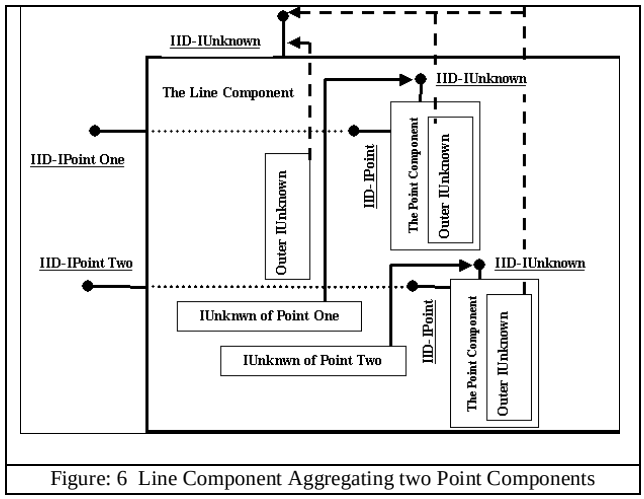


Figure: 6 Line Component Aggregating two Point Components

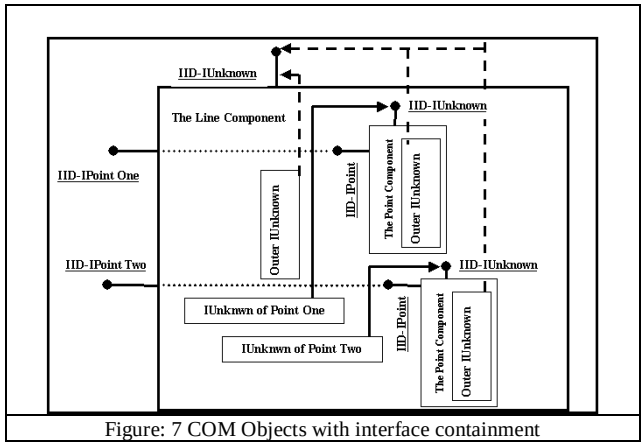


Figure: 7 COM Objects with interface containment

IV. FEATURES OF COMPONENT DEVELOPMENT PROCEDURES AND CONCETS

The component development process is complex compard with simple OOP based C++ application, but it has lots of features that solve several client requirements. The OLE features like cut and past, in place activation, drag and drop, container and server, and several modern requirements are possible only with this technology. As a consequence, often IT industry is forced to adopt these procedures. The steps required to build a simple Beeper object are as follows:

i) The beeper in a direct application needs a single class and a single application to give a beep sound for the given client input signal. In Component model several project and directories are required in a particular hierarchy; the files need to be shared across several projects. Sample files SRC (source files), INCLUDE (for header files), project files, Registration files for registry entry, INTERFACE files for interfaces, BIN for application's executable files (EXE) and DLL for server dynamic link libraries components.

i) The component needs a GUID globally unique ID generated by a special application of Microsoft, namely guidge.exe which generates a unique ID which will be unique across the world. An ID generated once will never get generated again so that Components and interfaces are referred with that ID. If two GUIDs match in any system totally, Windows under use will crash as shown in Table 2.

ii) IDL and ODL files with Interface Description language and Object Description language scripts are used to build automation layer so that functionality is exported to VB application. Compilation of this script gives header file to C++ and type library to VB layer. This exports C++ functionality to VB application.

iii) Microsoft provides various wizards for generating all these facilities automatically for unknown clients.

TABLE II
SAMPLE GUID FILE

```
#ifndef _H_GUID
        #define _H_GUID 1
        #include <windows.h>
        #include <objbase.h>

// {765BFF32-C207-11d0-BC7B-080036603003}
DEFINE_GUID(CLSID_CBeeper, 0x765bff32, 0xc207, 0x11d0,
0xbc, 0x7b, 0x8, 0x0, 0x36, 0x60, 0x30, 0x3);
#endif // _H_GUID
```

iv) The sample procedure to crate a beaper object throught system registry and class fatory presented in Table 3.

TABLE III
COM OBJECT CREATION CODE

```
STDMETHODIMP CBeeperClassFactory::CreateInstance
(LPUNKNOWN punkOuter,

    REFIID riid, LPVOID FAR *ppvObj)
    {
        CBeeper*        pObj;
        HRESULT                 hr;

        *ppvObj = NULL;
        hr=ResultFromScode(E_OUTOFMEMORY);

    if (NULL != punkOuter && !IsEqualIID(riid, IID_IUnknown))
        return ResultFromScode(E_NOINTERFACE);
        pObj = new CBeeper(punkOuter);
        if (NULL == pObj)   return hr;
        if (pObj->Initialize())
            hr = pObj->QueryInterface(riid, ppvObj);
        if (FAILED(hr))     delete pObj;
        else  ServerIncrementNumberOfObjects();
            return hr;
        }

STDMETHODIMP_(ULONG) CBeeper::AddRef(void)
{       return ++m_cRef;    }

STDMETHODIMP_(ULONG) CBeeper::Release(void)
ULONG   cRefT;
        cRefT = --m_cRef;
        if (!m_cRef) {
            delete this;
            ServerDecrementNumberOfObjects();
        }       return cRefT;
        }
```

VI. COMPONENT BASED GRAPHIC FRAMEWORKS

The Component Technology builds an application environment to provide techical services to client requirenents and providing resources without concern to either application domain or funtionality. It provides a communication environment that provides a session to enable client and server to do busness. The same procedures provided in this will be applicable in several requirements and applicaton domains.

The major components of any project environment are client and server. Different types of servers in use are 'In process servers'. They support and provide services through DDLs, local servers, and work in different processes but on same system. The local server works on the same network connected systems to distribute and share services to enable different systems of the same network to share services. An example of this is the DCOM of Microsoft.

New frame works provide several advanced technological features of communicating over Internet based protocol, for examples Simple Object Access Protocols (SOAP), Web services, mobile communications etc. All these Technologies can work like wrappers. The code and traditional technologies still work. Several Wizards are available to the developer for using all these techniques. These Technologies and wizards are little costly and complex. Developer will never get total control

over internal procedures though they decrease the development time and cost of development.

Several layers and code models of development of a Graphic framework and code segments are presented in this section without functional models. The functional design concepts are presented in [1]. Without using code, COM enables all these object oriented graphic frameworks to be exported to VB layer or other web based or mobile based technologies through wizards. But user will never get total control over the requirements for configuration other than using them.

i) The framework is a layered development. All the basic functions required should be developed as libraries, classes and generic object oriented frameworks [1,3]. For the domain considered, dynamic display files are used to simulate several graphic systems like Logic circuits, Printed circuit boards, Debugger driver tools using dynamic display files, shown in Table 4 show sample application oriented functional components [1].

TABLE IV(a)
DISPLAY ALGORITHMS LIBRARIES

```
do-line3d (lc,bc,z,y,z),
do-point3d(lc,x,y,z),
do-circle3d(lc, cx,cy,cz,r,ax,ay,az),
doarc3d(lc,cx,cy,cz,r,sa,ea,ax,ay,az),
do-spehere)lc,cx,cy,cz,r) and
do-poly(lc,sadd,size:

etc…
```

TABLE:IV(b)
SAMPLE DISPLAY FILE INSTRUCTION ALGORITHM

```
void Component::LineTo(int x,int y)
{
        m_iNoOfInst++;
        DF[1][m_iNoOfInst] = 2;
        iPen_X = x;
        iPen_Y = y;
        DF[2][m_iNoOfInst] = iPen_X;
        DF[3][m_iNoOfInst] = iPen_Y;
}
```

TABLE IV(c) :
COMPONENT SEMANTIC DEFINITION FOR AN ELECTRONIC DISPLAY LID COMPONENT

```
void VRLogicLID(Component* ge)
{// Component color
        ge->SetLineColor(ge->GetBkColor());
        ge->RectSolidAt(0,0,100,100);
//  Inside Area
        ge->SetLineColor(LIGHTGRAY1);
        ge->RectSolidAt(0,0,96,96);
        ge->SetLineColor(DARKGRAY1);
        ….
// Designing light on/off status
int k=1;
for (int i=-35;i<=35;i+=10)
{
  if (ge->GetData(k)==1)
        ge->SetLineColor(RGB(0,255,0));
  else if (ge->GetData(k)==0)
     ge->SetLineColor(RGB(255,255,255));
        else if (ge->GetData(k)==2)
        ge->SetLineColor(RGB(255,0,0));
        else
        ge->SetLineColor(RGB(0,0,0));
// 255,255,255 is white(0 or OFF)
// all zeros black (junk data)
// 255 ,0,0 is red(error in output)
//0,255,0 is green(1 or ON)
  ge->RectSolidAt(12,i,15,8);
  ge->SetLineColor(RGB(0,0,0));
  ge->RectAt(12,i,-15,8);
  k=k+1;
}
ge->SetLineColor(DARKGRAY1);
for(int  i= -35; i<= 35; i+=10)
{       ge->MoveTo(-45,i);
        ge->LineRel(-15,0);
}// displaying pins of the component
// displaying text of the components
 ge->TextBkColor(LIGHTGRAY1);
 ge->TextColor(RGB(255,0,0));
 ge->TextAt(-40,25);
 ge->Text11At(-40,-25);
} // end of the procedure
```

TABLE IV(d) :
INTERFACE IDisplayFileInstructions

```
class IDisplayFileInstructions
{
public:
        // Display File Functions
        void virtual  MoveTo(int x,int y) = 0; // 1
        void virtual  LineTo(int x,int y) = 0; // 2
void virtual  TextAt(int x,int y) = 0; // 3  horizontal
void virtual  MoveRel(int x,int y) = 0;  // logical 1
        ____   ____ _______
void virtual  RectAt(int x,int y,int a,int b) = 0;
// 14 Set TextColor
void virtual  TextColor(COLORREF col) = 0;
void virtual  Text11At( int x,int y) = 0; // 15 Text
        ---    -------  -------   ---------
};
```

ii) The COM needs to define interfaces and COM environment to export these components over application environment to the client through proper channel as per permissions and requirements, as shown in the following sample code segments in Table 5.

TABLE V:
TYPICAL GRAPHIC INTERFACE

```
#undef INTERFACE
#define INTERFACE IGPersist
 DECLARE_INTERFACE_(IGPersist, IUnknown)
 {
 STDMETHOD(QueryInterface) (THIS_  REFIID riid, LPVOID FAR
*ppvObj) PURE;
 STDMETHOD_(ULONG, AddRef)(THIS) PURE;
 STDMETHOD_(ULONG, Release)(THIS) PURE;
STDMETHOD(Serialize)(THIS_ CArchive &ar) PURE;
STDMETHOD_(CLSID,GetClsid) (THIS) PURE;
 };
 typedef IGPersist FAR* LPIGPersist;
```

iii) The class and Interface ID models are presented in table 6

TABLE VI
THE CLASS INTERFACE GUIDS AND REGISTRATION FILE MODEL

```
REGEDIT

HKEY_CLASSES_ROOT\CLine = CLine Object
```

HKEY_CLASSES_ROOT\CLine\Clsid = {0D8BAFE2-33C8-11d1-A0B3-0060974FF0B9}

HKEY_CLASSES_ROOT\Clsid\{0D8BAFE2-33C8-11d1-A0B3-0060974FF0B9} = CLine Object

HKEY_CLASSES_ROOT\Clsid\{0D8BAFE2-33C8-11d1-A0B3-0060974FF0B9}\INPROCSERVER32 = H:\COm_PHD\HCOM\COM-CODE\GPCOM1\bin\GCOM.dll

HKEY_CLASSES_ROOT\CComp = CComp Object

HKEY_CLASSES_ROOT\CComp\Clsid = {A445E8CA-216C-11d6-B98C-204C4F4F5020}

HKEY_CLASSES_ROOT\Clsid\{A445E8CA-216C-11d6-B98C-204C4F4F5020} = CComp Object

HKEY_CLASSES_ROOT\Clsid\{A445E8CA-216C-11d6-B98C-204C4F4F5020}\INPROCSERVER32 = H:\COm_PHD\HCOM\COM-CODE\GPCOM1\bin\GCOM.dll

vi) Pattern Frames to mke COM procedures simple

The development procedure of adding components from the frame work need to follow entire COM procedure. For this purpose, the following Abstract COM pattern framework is useful. [4]. Fig. 6 shows a block diagram of abstract component which enables the developer to use COM component like a simple C++ object without complex procedures and with Component features.

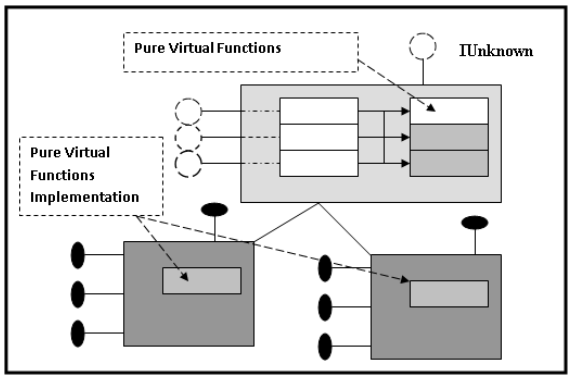


Figure 6 : a model block diagram of abstrat component

The VC client can use the framework like a simple object oriented framework using wrapper object as shown in Fig. 7.

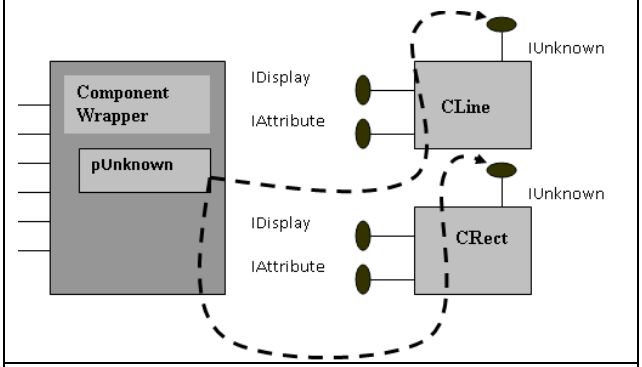


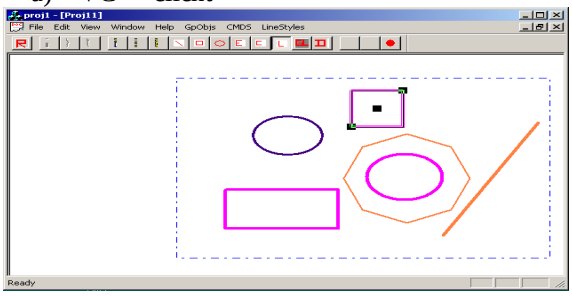
Figure : 7 Block diagram of Wrapper pattern frame

TABLE VII
MODEL WRAPPER DEFINITION

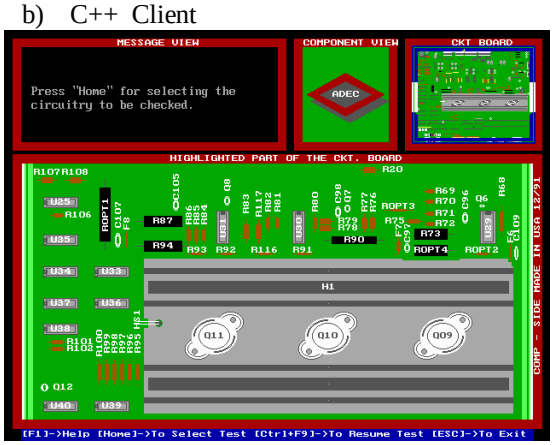
```
#ifndef HGraphicElement
#define HGraphicElement 0
#include <objbase.h>
#include "IGraph.h"
#include "Guid.h"
#ifdef HGraphicSERVER

  class __declspec( dllexport ) HGraphic
#else
   class __declspec( dllimport ) HGraphic
#endif
{

private:
      LPUNKNOWN    m_IUnknown;
      LPIGPersist        m_IPersist;
      LPIGAttributes     m_IAttributes;
      LPIGDisplay        m_IDisplay;
      LPIGEdit           m_IEdit;
      LPIGLocate         m_ILocate;

public:
         HGraphic(CLSID);
       ~HGraphic();

      HRESULT Serialize(CArchive &ar);
      CLSID   GetClsid(void);
      HRESULT SetPoints(ULONG,ULONG,ULONG,ULONG);
      HRESULT GetColor(void);
      HRESULT SetName(CString);
      CString GetName(void);
      HRESULT  GetName(CString* );
  ----  ------
      }
```

The Visual Basic can extract services from automation layer through wizards and ODL and IDL file outputs.

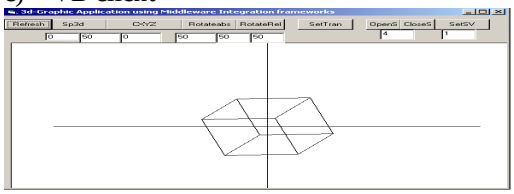
a) VC++ client



b) C++ Client



c) VB client



d) Semantic logic application in VC++ in dot net 2010

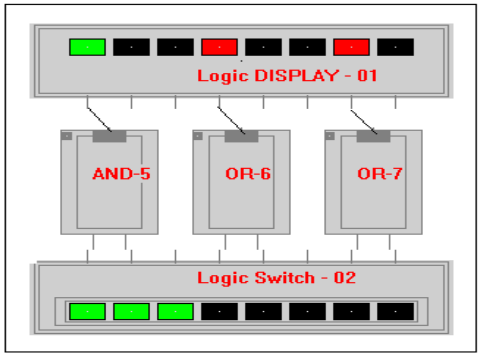


Figure 8 : Graphic application outputs of the framework

A simple visual base code to use server through wrapper objects and wizards is presented in Table 8.

TABLE VIII
SAMPLE VB CLIENT CODE SEGMENT

```
Private Sub Command1_Click ()
 HGP3D1.Sp3d Text1.Text, Text2.Text, Text3.Text, Text4.Text
End Sub

Private Sub Command10_Click ()
HGP3D1.S1
End Sub
4r
Private Sub Command11_Click()
HGP3D1.S2
End Sub

Private Sub Command4_Click()
HGP3D1.RoteteSegmentAbs Text7.Text, Text4.Text, Text5.Text,
Text6.Text
 HGP3D1.ShowAll
End Sub
```

CONCLUSIONS

The component based frameworks, their processes, advantages, problems and features, various processes to make implementation simple, sample graphic application code segments, and outputs of several sample applications have been presented. Details of models are described in some of the papers in references, as indicated at various places in the paper. It is suggested that same procedures can be applied to other domains for the development of the framework for the other domain environment not concerned with domain or application requirements. The application presented can be treated as a model for demonstration of environment. Several wizards are available to pack the Object Oriented Frameworks. They can be used for exporting into new technical environments, but clients will not get total control over configuring the requirements and use totally Component features. The user can use only assigned or permitted services. So implementing core Component features as per layers is advised. Using and developing new pattern frames to make use of Component Technology is also advised.

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Using Domain Ontology and Sequential Rule Mining for Extracting Behavior Patterns from Web Navigation Logs

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Abstract: **Due to unprecedented growth of information on the Web and lack of structure in many Web sites, it became real challenge to the Web users to find relevant information. To solve this problem, Personalization becomes a popular solution to customize the World Wide Web environment toward the user's preferences. Recent studies show that Web Usage Mining plays an important role in designing recommendation systems. Classical Web Usage Mining does not take Semantics Knowledge into pattern discovery and recommendation process. Recent studies show that Ontology as domain knowledge can improve pattern's quality. Our work aims to incorporate semantics knowledge into Web Usage Mining process. ERMiner, a state-of-the art algorithm for Sequential rule mining is applied over the Semantic space to generate frequent Sequential rules. Experimental results shown are promising and proved that incorporating Semantic Knowledge into Web Usage Mining process can provide us with more quality patterns which consequently make the recommendation system more functional, smarter and comprehensive. The experimental results of our Web recommendation system show a significant improvement on the quality of the recommendations.**

***Index Terms*—Web Usage Mining, Semantic Web, Sequential Rule Mining, Ontology, Semantic Web Usage Mining, Web Personalization, Recommendation System.**

I. INTRODUCTION

With the explosive growth of information on World Wide Web, it has become a real challenge for Web users to access relevant information. One possible approach to solve this problem is Web Personalization [1]. Web personalization [2] is the process of customizing a Web site to the needs of each specific user or set of users, taking advantage of the knowledge acquired through the analysis of the user's navigational behavior.

Web recommender system is a specialized personalization system. Understanding the information needs of users has become a crucial task for Web site owners on the Web. A key requirement in developing successful personalized Web applications is to build user models that can accurately represent users interests and preferences. In addition to the above feature, it has to be machine-understandable and machine- processable.

Though user needs may be elicited in many ways, Usage mining of Web logs is a widely used alternative for understanding usage patterns. However conventional Web usage based recommender systems are limited in their ability to use the domain knowledge of the Web application and their focus is only on Web usage data. As a consequence, the quality of the discovered patterns is low. These patterns do not provide explicit insight into the user's underlying interests and preferences, thus limiting the effectiveness of recommendations as well as the ability of the system to interpret and explain the recommendations [3].

Recent studies[4] hint that Ontology which is an explicit representation of the domain knowledge of the application, if integrated with Web Usage Mining, can enhance the quality of generated usage patterns and help in developing effective Recommendation system.

The combination of Web Usage Mining and Semantic Web has created a new and fast emerging research theme – Semantic Web Usage Mining [5].

The key contributions of our work can be summarized as follows:

1) Feeding domain Ontology into Web Usage Mining Process to extract Sequential navigational patterns.
2) A state-of-the art algorithm ERMiner, is used in the Sequential rule mining process to generate frequent Sequential rules.
3) Generated Sequential rules have antecedent and consequent as sequence of ontological instances instead of mere page views.

The rest of the paper is organized as follows: in section II we review recent advances in Semantic Web Usage Mining research. In section III proposed model and architecture is discussed. Experimental set up and Performance evaluation of the proposed model is presented in section IV. Finally section V provides the concluding remarks and sheds light on future enhancements.

II. RELATED WORK

Web Usage Mining is the process of extracting navigational patterns by applying data mining techniques on Web log file. In recent years, Web Usage Mining techniques such as Clustering, Association rule mining, Sequential pattern mining were employed in extracting

navigational patterns and using those patterns in recommendations [4,5]. An extensive literature on Web Usage Mining based recommendation systems is available in [6,7,8]. However the amount of work presenting the combination of Web Usage Mining and Semantic Web is very limited. Work presented by Stumme et al. [9] and Oberle et al. [10] is regarded as first contribution towards the Semantic Web Usage Mining. The authors have sketched out the benefits of combining Semantic Web and Web Mining. The first part of the work is on extracting semantics from Web page. The second part is on the improvement of Web Usage Mining by using Semantics structures in the form of Ontology. Bamshad Mobasher et al. [11] proposed a unified framework based on Probabilistic Latent Semantic analysis to create user models taking into account both usage data and web site contents. The work presented by stumme et al.[12] sketeched different possibilities of combining Semantic web and Web Mining. In a recent work [13], Nasraoui et al, proposed a Web Usage Mining Framework for mining evolving User Profiles of dynamic Web sites by exploiting the external ontology, used for mapping and relating dynamic Web pages. Eirinaki et al [3], presented a system, SEWeP which integrates the Web usage logs with the semantics of Web site's content to improve the personalization. The innovative feature of the architecture was C-logs, an extended form of Web usage log which encapsulates the site semantics. But the framework was limited only to concept hierarchy. Amit Bose et al, [15] proposed a framework for personalization combining usage information and domain knowledge based on ideas from bioinformatics and information retrieval. Vanzin et al.[16] present ontology – based filtering mechanisms for retrieval of Web Usage patterns and the studies presented by Mehdi et al. [17] proposed a framework XPMiner, which mines frequent patterns over ontology based pattern space. The studies assume that meta data of the web page contents can be typically organized into domain ontology and can be used in frequent pattern mining task. The authors have emphasized the importance of semantic relations in the Mining task.

In summary all the above studies attempted to improve the quality of the navigational patterns and subsequently the recommendations by integrating Semantics into Mining tasks. But the content domain ontologies concerned in the above studies share a common limitation. They invariably represent concept taxonomies. Recent approaches which use Semantics knowledge in the form of ontology for extracting behavior patterns from Web navigation logs are presented by Mabroukeh et al. [18] and Yilmaz et al. [19]. Julia Hoxha et al. [20] presented an approach for the Semantic Formalization of Web browsing behavior across multiple sites. The Usage logs are mapped to comprehensive events from the application domain.

III. PROPOSED SYSTEM

The proposed system has extended the classical Web Usage Mining system. It includes the basic steps such as data acquisition, data preprocessing, extraction of Semantic frequent Sequential rules and Web page recommendation. Web Log file forms the main basis of input to the Web Usage Mining process.

A. *Data Preprocessing:*

Data preprocessing phase includes data cleaning, user identification, and session identification. This task along with Sequential Rule Mining task is implemented as offline phase. Generally several preprocessing tasks need to be performed on the Web access database before user navigational patterns are extracted. Due to large amount of irrelevant information in the Web log file, raw usage data need to preprocessed by applying preprocessing techniques and converted into sequential database.

Initially the usage data logs are centrally stored in raw form as produced upon user interaction. We regard each log record as a browsing event. Log files are pruned to remove the non-responded Web requests and also the requests made by software agents such as Web crawlers, and bots are eliminated. The browsing events are grouped into sessions based on user‘s IP address. Then the browsing events are formalized into Semantic form by mapping the URLs into respective RDF form. The formalized browsing events obtained constitute a semantic rich user model and form the basis of the Semantic Web Usage Analysis.

B. Ontology Construction:

An Ontology is defined as "an explicit specification of a conceptualization"[21]. A conceptualization consists of a set of entities (such as objects and concepts) that may be used to express knowledge and relationships. Protégé [22] tool is used for constructing and editing the ontology of the Web application. The Semantic Web Dog Food (SWDF) [23] and DBpedia Ontology [24] are available publicly. OWL and RDF are the popular Semantic Web technologies used in representing Ontology.

C. Sequential Rule Mining:

After preprocessing step, Web access sequence database, consisting of a sequence of page views is obtained. Since the RDF representation of the web resources for SWDF and DBpedia datasets are available, the ontological instances of the objects of the browsing events are obtained. We employed the procedure presented in [20] for Semantic formalization of browsing events. And further frequent Sequential rules are generated by applying Sequential rule mining.

In the proposed system, we preferred Sequential rule mining over Frequent Pattern Mining, since the sequence information in the navigation is retained in the generated rules. In the Proposed System, ERMiner (Equivalence class based Sequential Rule Miner) [25] algorithm is employed to generate Frequent Sequential rules. It relies on a vertical representation of the database to avoid performing database projection and adopts the novel idea of exploring the search space of rules using equivalence classes of rules having the same antecedent or consequent.

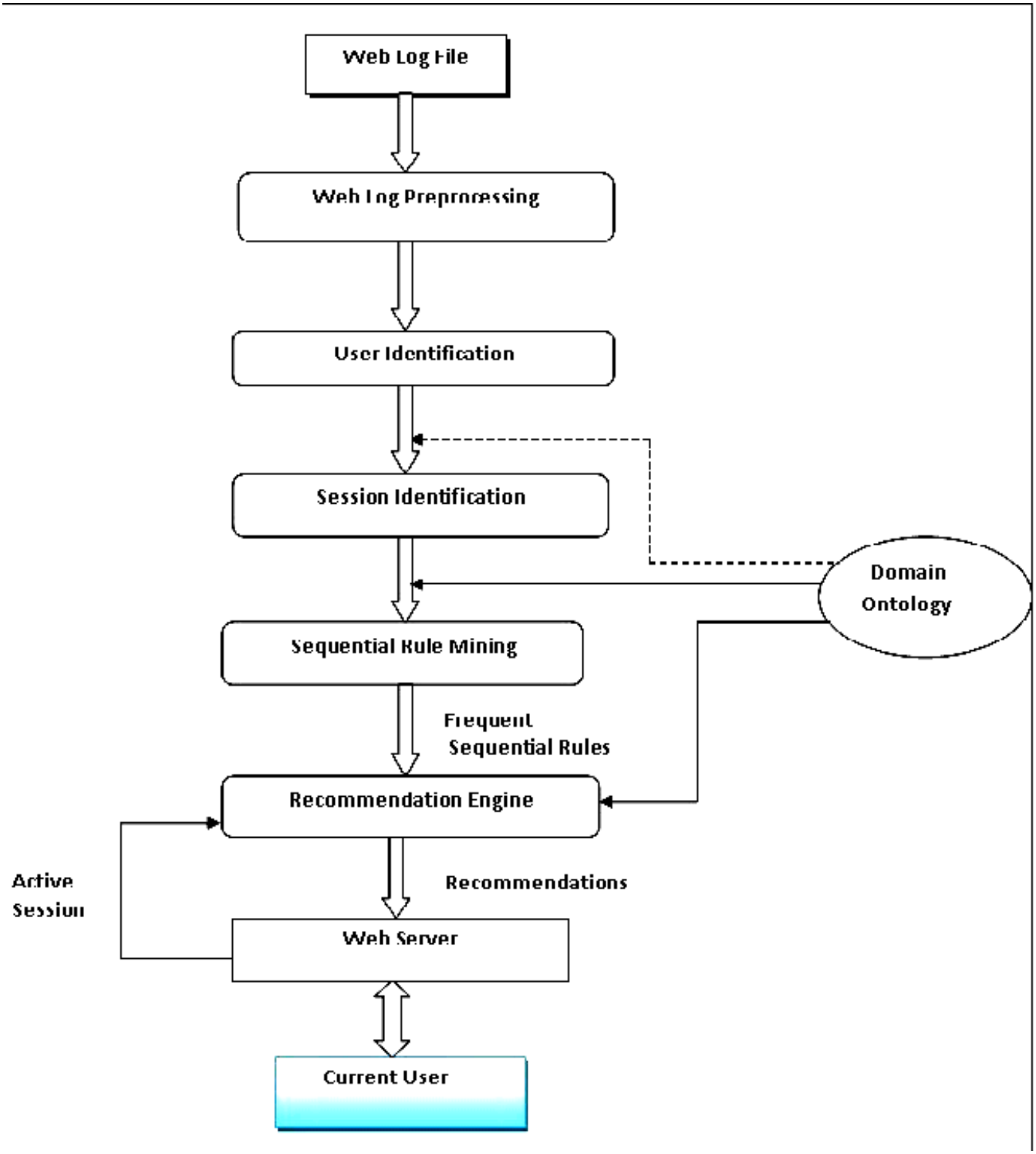

Figure 1 : An Architecture for Online Recommendations using Web Usage Mining and Domain Ontology

SPMF [26] is an open source data mining framework implemented in Java. For extracting frequent Sequential rules we have implemented ERMiner algorithm using this framework.

D. *Generating Recommendation*

In recommendation phase, Sequential rules extracted in the above process and active user's navigation session are compared in order to recommend a new page or pages to the user in real time.

Generally, not all the Web pages in the active session path are taken into account while generating a recommendation set. Window count, a parameter which defines the maximum number of previous page visits to be used while generating a recommendation set to the current user is defined.

The recommendation set constitutes the set of Sequential rules which will be used for generating recommendations. After constructing the recommendation set, the Web Page recommendation begins. The Sequential rules in the recommendation set are ordered by their confidence value and the highest one is taken first for the recommendation. For each Sequential Association rule in the recommendation set, its consequent part is extracted and used for recommending Web resources. The ontological instances of consequent part are reverse mapped to page views before applying recommendation

IV. EXPERIMENTS AND PERFORMANCE EVALUATION

A. *DataSet Description :*

Experiments were conducted on two publicly available real datasets SWDF (Semantic Web Dog Food) and DBpedia. SWDF is a very active Web site of publications, people and organizations in the Semantic Web fields, covering several of the major conferences and workshops. DBpedia is shallow, cross domain ontology representing the Wikipedia information in structured format ie.. in the form of classes and properties.

TABLE I
THE SUMMARY STATISTICS OF THE EXPERIMENTAL DATA SETS.

	SWDF	DBpedia
#sessions	890	1020
Avg #sessions/day	150	187
#triples	27790	34870
Period of Usage data	17-07-09 to 22-07-09	21-04-11 to 26-04-11

B. *Evaluation:*

To evaluate the performance of our system we have employed the evaluation metrics discussed in [27]. We have used the measures such as precision and recall. As precision and coverage are inversely related, a combination measure called the F1-measure giving equal weight to both precision and coverage can also be used. Precision measures the degree to which the recommendation engine produces accurate recommendations. Coverage measures the ability of the recommendation engine to produce all of the pages that are likely to be visited by the user.

10 –fold cross – validation is performed on each of the datasets. Each session t in the test session set *ts* is divided into two parts. The first *n* web pages of test session are used for generating recommendations, and the second part is simulated as the future requests (page visits) which are compared with the output of the recommendation system. w is called the window count , which represents the last n pages in the first part of session called active session window (*asw*).

The recommendation engine takes *asw* and the recommendation threshold μ as the input and generates a recommend list which is denoted by *Rec(asw,μ)*. Note that *Rec(asw, μ)* contains all pages whose recommendation score is at least μ. The set of pages *Rec(asw, μ)* can now be compared with the remaining $|t|-n$, pages in *t*. We denote this portion of t by Eval.

$$Precision\ (Rec(asw,\ \mu)) = \frac{|Rec(asw,\mu) \cap Eval|}{|Rec(asw,\mu|}$$

$$Coverage\ (Rec(asw,\ \mu)) = \frac{|Rec(asw,\mu) \cap Eval|}{|Eval|}$$

We performed experiments with recommendation threshold ranging from 0.1 to 1.0.

The results of these experiments are given below.

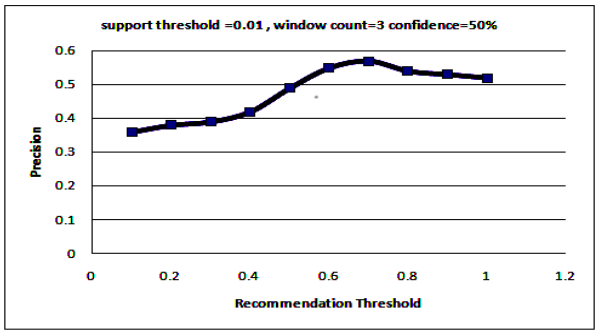

Figure. 2: Recommendation Precision

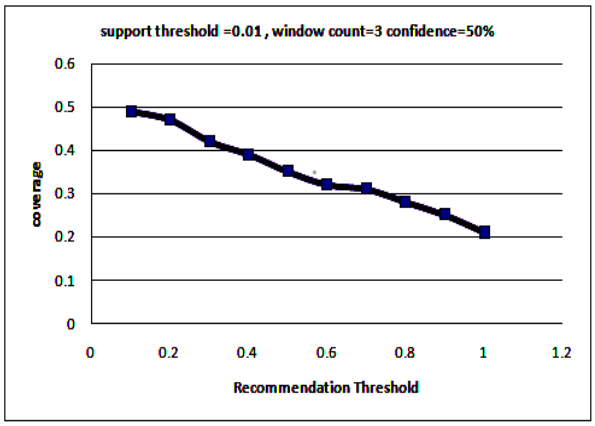

Figure.3 : Recommendation Coverage

V. CONCLUSIONS AND FUTURE WORK

The proposed work extracts interesting Sequential rules using Semantic Web Usage Mining. We have applied an extended version of the state-of-the art Sequential rule mining algorithm ERMiner over Ontological space to extract frequent and interesting Sequential rules. The generated Sequential rules are in terms of ontological instances instead of Web page views. The discovered Semantic Sequential rules form the basis of recommendation engine of the proposed model. Compared with the recommendation system based on classical Web Usage Mining, our proposed model shows promising results.

Experimental results are promising and we believe that the successful integration of Semantic knowledge with Web Usage Mining is likely to lead to the next generation of Personalization tools which will be more intelligent and more useful for Web Users.

Future work includes the development of techniques related to the acquisition of domain ontology, when this is not provided, since it is a crucial component of the Semantic enrichment of usage data with concepts from the application domain. Proposed work can also be extended by combining the clustering and sequential rule mining techniques incorporating domain ontology, making a hybrid recommendation system.

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Improving Performance of 802.11n Networks Using Various Rate Adaption Algorithms

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***Abstract* — In a WLAN subject to variable remote channel conditions, rate adjustment assumes a critical part to more productively use the physical connection. Rate adjustment is a MAC-layer instrument in IEEE 802.11 systems to guarantee proficient usage of fluctuating remote channel. Traditional 802.11 rate adjustment calculations depend on input from the recipient to accurately pick a sending rate, commonly as affirmations (Acks). Without such casings, novel strategies are needed for rate choice. In this paper, the accompanying progressed rate adaption calculations are exhibited:**

a. MAC-Layer Loss Differentiation based rate adaption algorithm
b. High TCP Performance rate adaption algorithm
c. Video-Aware Rate Adaption For HD Video Streaming

***Index Terms*—IEEE 802.11, WLAN, Rate Adaption, ARA Algorithm, DCF, Loss Differentiation, Automatic Rate Fallback.**

I. INTRODUCTION

The utilization of remote neighborhood (WLANs) in homes, work places, and open regions has been spreading rapidly. The overwhelming WLAN benchmarks have been characterized by the IEEE 802.11 working gathering, with their prosperity moved by the Wi-Fi Alliance [1] [2]. Most IEEE 802.11 WLAN gadgets utilize the dispersed Coordination Function (DCF) tagged in the standard [2] to arrange channel by the transporter sensing access with impact evasion . In DCF, when numerous edges are transmitted all the while by distinctive stations, an impact happens, which annihilates all the transmitted casings. To resolve impacts, the stations utilize a twofold opened exponential backoff calculation and retransmission plan. Two right to gain entrance methods are characterized in 802.11 DCF, the default fundamental access and the discretionary RTS/CTS access. Current WLAN items help more than one regulation sorts and information rates. For instance, in 802.11b, 4 information rates, 1 Mbps, 2 Mbps, 5.5 Mbps, and 11 Mbps, are upheld [3]. On the other hand, a higher information rate does not so much yield a higher throughput. When the channel condition is great, a higher information rate gives a higher throughput. In a practical WLAN environment, the channel condition can fluctuate progressively because of multi-way impedance, and developments of stations, and so forth. To oblige diverse channel conditions, rate adjustment (or auto rate) is normally utilized. This is acknowledged by rate adjustment calculations that modify the regulation mode and information rate to upgrade execution when channel condition changes.

Today, features overwhelm Internet activity and by 2015 it is anticipated that about 50% of the feature movement will be 3d or 2d High Definition (HD) [26]. A high portion of HD feature movement will be devoured by clients that get to Wireless Local territory Networks (Wlans) in homes, ventures or open spaces. This vision is energized by two noteworthy engineering patterns. In the first place, late feature streaming innovation benchmarks, for example, H.264/MPEG-4 section 10 AVC [27] lessen HD feature data transfer capacity necessities utilizing Variable Bit Rate (VBR) feature encoding. Second, the IEEE 802.11n [28] WLAN standard offers high remote physical-layer (PHY) information rates (up to 600 Mbps) utilizing Multiple-Input Multiple-Output (MIMO) reception apparatus advances. Notwithstanding these advances, the issue of streaming HD feature in Wlans is a long way from being explained. VBR advances lessen the normal feature streaming rate by effective encoding of moderate moving scenes. On the other hand, the top rate stays high as it is dictated by the full quality encoding of quick movement scenes.

In this paper, for the MAC-Layer based loss differentiation based method, a new auto rate algorithm calledloss-differentiating-ARF (LD-ARF) that is suitable for arealistic WLAN environment where both collision losses andlink error losses can coexist is discussed. Its effectiveness is demonstrated through extensive performance evaluations.

For High TCP Performance algorithm, an efficient and practical rate adaptation algorithm called Advanced Rate Adaptation Algorithm (ARA) is proposed and explained in detail. The key idea of ARA is to make use of the RTS control frame as the probe packet. RTS control frame has several characteristics that make it suitable for such use.

Next For HD streaming, VARA, a Video-Aware Rate Adaptation protocol is used, that optimizes wireless channel probing and PHY rate selection by exploiting the VBR streaming rate information of a video. VARA eliminates the channel probing impact on the video stream by scheduling the probes during the low streaming-rate periods. Furthermore, rather than aggressively trying to find the maximum PHY rate supported by the wireless

channel (like all existing 802.11 rate adaptation protocols), VARA selects the most reliable PHY rate that supports the near-future peak streaming rate. To further reduce the probing overhead, VARA monitors the Frame Error Rate (FER) and adapts probing frequency to the measured wireless channel variability.

The organization of the remainder of this paper is as follows. In Section II, a new loss differentiating ARF algorithm is proposed. The new algorithm involves MAC layer changes only. In Section III, several guidelines for designing an efficient rate adaptation scheme for IEEE 802.11 networks are given and explain the proposed algorithm and how ARA is implemented is explaned .In Section IV, the design of VARA and the multiplexing techniques are presented. In Section V, the conclusion of this paper is given.

II. DESCRIPTION OF LOSS-DIFFERENTIATING ARF ALGORITHM

measures.

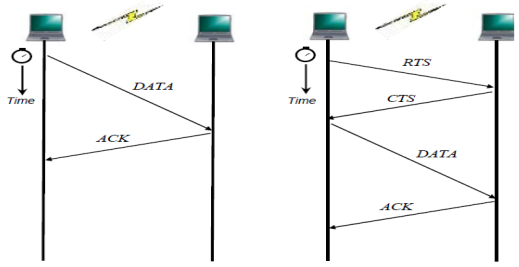


Figure 1. Basic and RTS/CTS access in 802.11 DCF

In this area, firstly, the real idea of this convention is assessed. At that point the LD-ARF calculation, which joins the misfortune separating MAC and the current ARF calculation, is proposed. The following segment will assess its execution.

A. Loss Differentiating MAC Protocol

The misfortune separating MAC layer convention is expected as an improvement of the 802.11 DCF. There are two right to gain entrance methodologies in DCF, fundamental and RTS/CTS. Figure 1 delineates the two right to gain entrance techniques. The alteration to the DCF in the new convention includes both essential and RTS/CTS access techniques. RTS/CTS is a noncompulsory emphasize in a 802.11 WLAN and it is helpful when the information casing size is extensive, the quantity of stations is huge, or there are concealed terminals. It is a 4-way handshake method as indicated in Figure 1. The misfortune separation system in the RTS/CTS access method is clear and the 4-way message trade grouping is not transformed: (i) If both the CTS and afterward the ACK edges are gotten at the sender, the transmission was effective. (ii) If the CTS edge is gotten however the ACK casing is not, the transmission has fizzled, in all probability because of a connection mistake. (iii) If the CTS edge is not gotten, probably a crash has happened. Since RTS and CTS are short and generally transmitted at a low rate, the misfortune separation can be very powerful. Essential access is the default get to in 802.11 DCF. It is a two-way handshake method (see Figure 1). As a rule, e.g., when there is no concealed terminal, the default essential access is more effective than RTS/CTS access. The misfortune separation for essential access is not as direct as that for RTS/CTS access. In the first essential access method, just when the got information casing is right, is an input message (ACK) sent. At the point when the got information casing is in blunder, the recipient does not give any reaction. As clarified beforehand, two reasons, i.e., a crash or connection blunders, may cause a mistaken edge gathering in the essential access technique, and the sender can't separate between these misfortune components and take

Thusly, a component must be consolidated so that the recipient can focus the reason for a fizzled gathering and advise the sender. One of the favorable circumstances of the new misfortune separating MAC layer convention is that the change to the standard DCF capacity has been minimized. No alteration to the PHY layer is required. In this way the convention is not difficult to execute.

B. Loss Differentiating Automatic Rate Fallback Algorithm

It has been clarified that when an impact happens, the information rate ought not be lessened. In this manner the adjustment to the ARF calculation is that the information rate is decreased just when a loss of information casing is brought about by connection slips

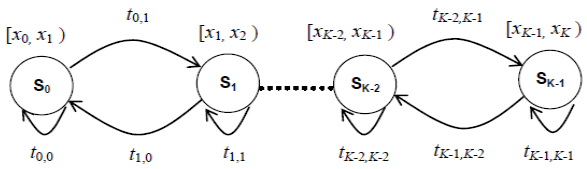
- If an *ACK* is received (the transmission is successful) or rate-up timer expires, then,
  counter_downrate= 0;
  counter_uprate++;
  If (*counter_uprate*≥N_{up})
  {
  physical rate is increased;
  counter_uprate= 0;
  rate-up timer is stopped.
  }

- If a *NAK* is received (a link error loss is detected), then,
  counter_uprate= 0;
  counter_downrate++;
  If (*counter_downrate*≥N_{down}) or the rate was just increased
  {
  physical rate is reduced;
  counter_downrate= 0;
  rate-up timer is started.

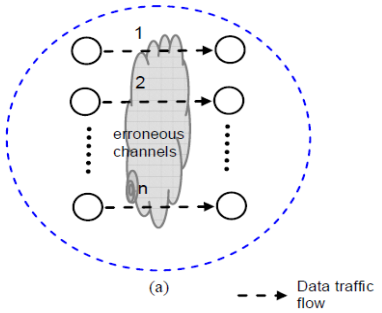
}

The Gilbert-Elliot channel model has been broadly used to model remote channels subject to blast mistakes. Estimations directed on the remote direct in an IEEE 802.11 WLAN demonstrate that the Gilbert-Elliot model gives a decent expectation of WLAN execution. To assess the execution of the proposed LD- ARF calculation under

variable conditions and contrast and that of the ARF calculation, in this paper an augmentation model of the first Gilbert-Elliot model is utilized. It is a K-state Markov divert display as indicated in Figure 2. In the K-state show, the remote divert could be in one of the K states from S_0 to S_{K-1}. In each one state, Si, the relating SNR esteem at each one edge transmission is consistently taken from the scope of [xi, xi+1) db, where xi+1> xi. The visit time in each one state takes after an exponential appropriation (or if discrete time is utilized the comparable Geometric dispersion). This model is truly like the arbitrary walk model, which can be seen as the situation where the two imparting WLAN stations approach and leave haphazardly. In recreations, a 10-state channel model has been utilized. A modestly changing channel model has been viewed as where for each one state, Si,, the normal time span is 1 second, and the move probabilities ti,i-1=ti,i+1. For each one state, Si, the SNR values (in db) are consistently disseminated between [i, i+1]. Accordingly the conceivable SNR qualities created by this model are conveyed between 0 db and 10 db. IEEE 802.11b is utilized as a part of reproductions since it is the most generally utilized WLAN standard by a long shot. Additionally, its physical property has been settled in [11], [12], and [13]. Besides, the Wavelan-II item in which ARF was initially executed has comparable properties to 802.11b1. It is more serious to utilize the control parameter values given in Wavelan-II to analyze the execution of the auto rate calculations. In our reenactments for ARF and LD-ARF, this information rate is essentially circumvent.



In the reproduction situations, all stations are soaked, yet it is accepted that the conclusions got from the reenactment results are pertinent to non-immersed stations also. Expect there is no shrouded terminal and the stations are close enough that when they transmit outlines at the same time, the ensuing impact demolishes the casings included. The information outline payload size is 1000 bytes. The information outline blunder rate, the information outline MAC header lapse rate (HLR), and the control outline mistake rates are dead set individually by their sizes, their rates, and the SNR qualities created from the 10-state channe model when the casing is sent.



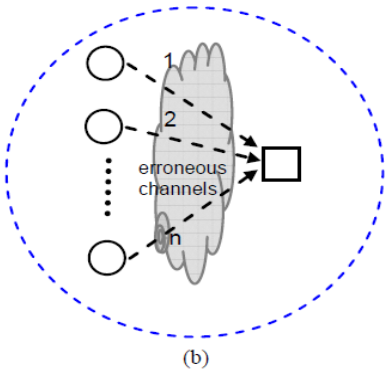


Figure 3. Two Different but performance equivalent WLAN topologies

The MAC header and body parts are transmitted at the same information rate. The essential rates for the control casings take after the principles given underneath. For a RTS outline transmission, its rate is the same as the sending station's information rate for an information outline. For ACK, NAK and CTS, their sending rates are the same as the rate utilized for the got information casing or RTS outline. Note that if the fundamental rate or the header part rate is lower than the information edge rate, the misfortune separating MAC convention can be more powerful. In this manner these settings may not yield the best execution for the LD-ARF. It is going to be demonstrated. The estimation of the rate-up clock was not suggested in [4]. As demonstrated in [7], over a wide range (from a few seconds to around one moment) the rate-up clock esteem does not have a critical effect on execution and the ensuing throughput is equivalent. In our reenactments, we don't put concentrate on this clock and essentially set its esteem to 10 seconds. A circumstance where all the WLAN connections encounter precisely the same channel state in the meantime (Scenario 1) is considered. It can be seen from Figure 3 that when there is stand out connection (i.e., one station sending activity), the two calculations produce comparative throughput. In any case, when there are numerous connections (i.e., various contending stations), the execution of the first ARF calculation debases significantly. At the point when the quantity of connections is 3, the execution change by the new LD-ARF over ARF is extremely noteworthy. At the point when the quantity of contending stations is huge, the new LD-ARF calculation yields more than twofold the throughput of the ARF calculation. In the accompanying situations, more reasonable circumstances where the channel conditions are autonomous are considered. In Scenario 2, each one connection encounters a channel condition that is resolved autonomously from the 10-state channel model. Figure 3 looks at the framework throughput of LD-ARF and ARF for fundamental access and RTS/CTS get to in Scenario 2. Like Scenario 1, when the quantity of contending stations is huge, the throughput change by the new LD-ARF calculation is more than 100%. Indeed so the LD-ARF can attain huge execution pick up over ARF.

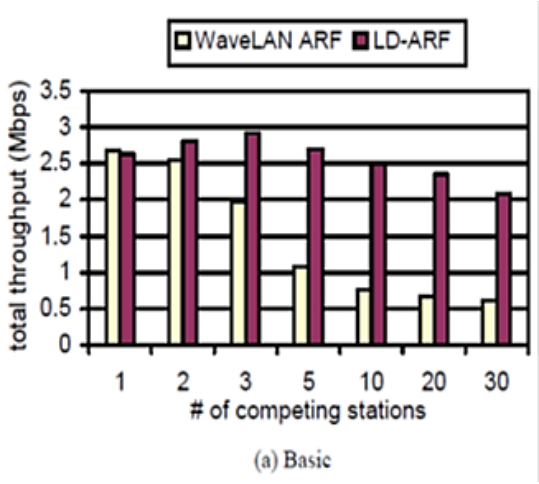
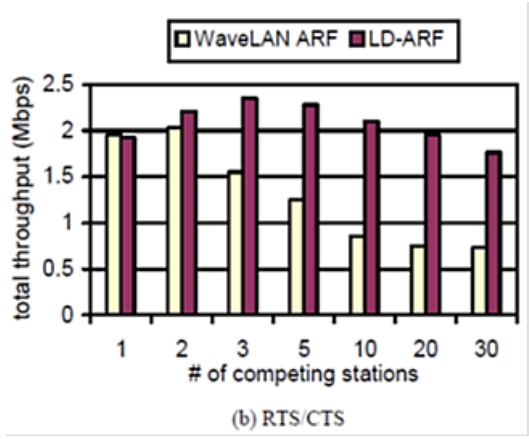


Figure 4. Performance Comparision of Auto Rate algorithms-Scenario 1



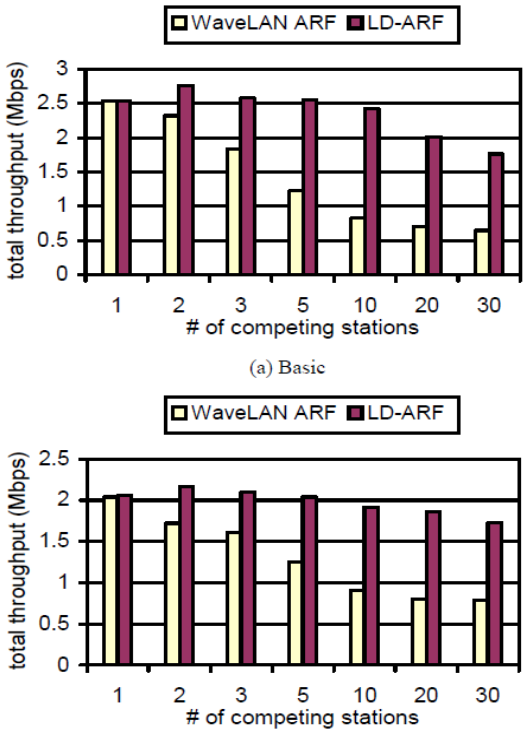


Figure 5. Performance Comparisons of Auto Rate algorithms-Scenario 2

III. DESIGN GUIDELINES AND ARA ALGORITHM

A. Design Guidelines:

- *Ability to Differentiate Frame Losses*

In IEEE 802.11 standard, RTS/CTS control casings trade is impaired of course to minimize overhead. Original rate adjustment plans treat all the casing misfortunes as from channel blurring and decline the information rate at whatever point the edge disappointment proportion achieves certain limit. In the event that an edge misfortune is created by impact, diminishing the information rate won't help take care of the issue yet exacerbate it. Lower transmission rate implies longer transmission time and more extensive show range, which will prompt more crashes and hence exacerbate things. A proficient rate adjustment plan ought to have the capacity to separate the casing misfortunes and react in like manner to these diverse reasons.

- *Ablility to Response to the Variation of Channel Fast*

A productive rate adjustment calculation ought to have the capacity to adjust the nature's domain changes quick, generally, the calculation may lose the chance to send the information outline at a higher rate or continue sending the information outline at a high rate where fruitful conveyance is impractical.

- *A Good Metric to Adjust Data Rate*

A percentage of the current rate adjustment plans alter the information rate by checking the continuous achievement and disappointment number. While this strategy is straightforward, it is not precise. As per RRAA, the likelihood to effectively transmit an information bundle taking after ten back to back victories is just 28.5%. What's more the likelihood of a disappointment in an information transmission after two continuous disappointments is just 36.8%. These insights demonstrate that the sequential achievement or back to back disappointment number ought not be utilized as the metric to conform transmission rate. Different plans utilize the sign to clamor proportion (SNR) as the marker to change the rate. Be that as it may, as per Sample Rate [23] and RRAA, SNR is NOT a decent marker of the channel condition and accordingly ought not be utilized as a part of the metric.

- *Compatibility with Current Commercial Product*

A functional rate adjustment plan ought to be good with current business item, which implies IEEE 802.11 standard can't be adjusted. A few existing rata adjustment plans [20], [21], [22] require the alteration of IEEE 802.11 standard and along these lines are not good with current business items. The over four rules provide for us some essential thoughts on the most proficient method to plan an effective and handy rate adjustment plan. The following area will talk about the proposed calculation in point of interest.

B. ARA Algorithm

In this area, a productive and down to earth rate adjustment calculation called Advanced Rate Adaptation Algorithm (ARA) is proposed and clarified in subtle element. The key thought of ARA is to make utilization of the RTS control outline as the test parcel. RTS control

outline has a few qualities that make it suitable for such utilization. To begin with, it is little in size. As per the IEEE 802.11 standard, it is 20 bytes long. Contrasted with an ordinary information bundle, which is ordinarily bigger than 1000 bytes, a little parcel has a littler likelihood of impacting different parcels on account of its shorter transmission time. Second, RTS/CTS control outlines can save the data transmission. Consequently, a fizzled bundle transmission after a fruitful RTS/CTS trade must be created by channel corruption. ARA separates the edge misfortunes through the utilization of RTS control outline. At the point when an information outline transmission comes up short, a RTS control edge will be sent at the same rate as the fizzled casing. On the off chance that the CTS control edge can be gotten, then present channel condition has a high likelihood of supporting the current transmission rate. Consequently, the loss of the past information casing is created by crash. Then again, if the RTS/CTS trade is fruitful however the accompanying information casing falls flat, then the edge misfortune must be brought about by channel blurring. Through this strategy, ARA can correctly separate the edge misfortunes brought on by both channel blurring and impact. For the second rule, ARA utilizes a quick yet exact rate alteration instrument. As clarified above, if the RTS/CTS trade is fruitful yet the following information casing still falls flat, the disappointment is brought on by channel blurring. In this way, the information rate will be diminished because of such environment changes. On the off chance that the edge misfortune is brought on by crash, the transmission rate will stay unaltered. The rate change in ARA is quick yet exact given the condition that ARA can definitely focus the reason for casing misfortunes. The greater part of the current rate adjustment calculations utilize sequential achievement check or successive disappointment consider their metric to alter the information rate. In any case, this system is incorrect, as well as loses the chance to get the short addition time of solid sign. ARA utilizes RTS and the accompanying information casing to distinguish channel blurring and in this manner have the capacity to decline the transmission rate rapidly and unequivocally. ARA likewise utilizes the achievement tally to expand the information rate however it doesn't essentially need to be continuous. As expressed beforehand, the likelihood of a fruitful transmission after ten sequential achievement transmission is just 28.5%. By fulfilling the greater part of the rules showed in the above area, a proficient and reasonable rate adjustment calculation is proposed. Figure 6 demonstrates the state move graph for ARA.

C. Implementation

ARA is actualized on Madwifi, which is an open source IEEE 802.11 gadget driver for Atheros cards in Linux and Freebsd. In this variant, ARA characterizes two limit parameters named (Ts = 8) and (Pth = 1), Ts is the edge used to expand the transmission rate. Pth is the edge used to start the RTS/CTS trade. In the event that an information transmission falls flat, ARA will enter a state where RTS/CTS trade strikes help separate the reason for this casing misfortune. It likewise holds two rate file sets, specifically rix and cix. rix is utilized to situated the current information transmission rate list and cix is utilized to set the current RTS transmission rate file. A rate list relates to the genuine transmission rate, for instance, in IEEE 802.11g, there are altogether 12 diverse transmission rates. Going from 1 Mbps to

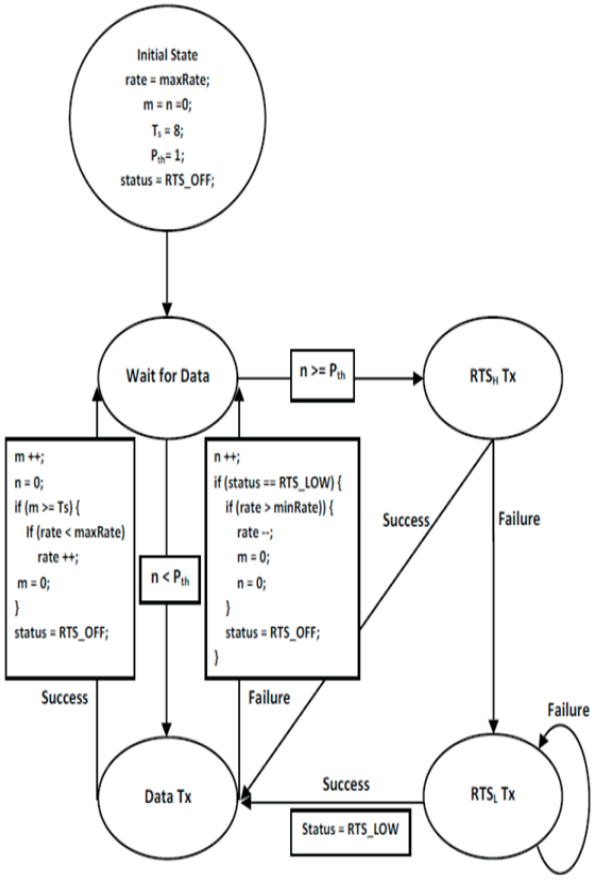


Figure 6. ARA Algorithm

54 Mbps and the rate file ranges from 0 to 11, separately. Toward the start of the state move, ARA sets the introductory rate to be the most extreme rate. It likewise instates variables m, n, and status. m is utilized to hold the quantity of casings being effectively conveyed at current transmission rate and n is the disappointment check. It must be brought up that despite the fact that n is the disappointment include; it is NOT utilized the rate alteration metric to decline the information rate. It is just utilized as a condition test to choose whether ARA needs to start RTS/CTS trade. status holds the current status: Rts_off and Rts_low. After the variables have been instated, ARA will sit tight for the impending information outlines. At whatever point an information edge is found in the transmission line, ARA will attempt to send the information without the assistance of RTS. On the off chance that the information is conveyed effectively, ARA will build m by 1 and reset n to 0. It will likewise reset status to Rts_off on the grounds that next edge will be transmitted without the assistance of RTS/CTS. At the point when m achieves the limit Ts and current transmission rate is not greatest rate, the rate will be expanded. In any case, if a transmission falls flat, ARA

will build n by 1. Note that right now, m is not reset on the grounds that whether outline disappointment is in fact brought on by channel corruption or not will be not known. At the point when n is equivalents to 1, it implies the past information transmission has fizzled. ARA will attempt to separate the reason for this disappointment. It will first send a RTS at the same rate as the fizzled information outline (cix = rix), indicated as Rtshtx. On the off chance that the comparing CTS can be gotten, a few things can be affirmed. In the first place, the channel condition may help the current transmission rate since RTS is transmitted at the same rate as the fizzled casing. Second, there is a high likelihood that the past casing misfortune is brought on by crash. Third, the transmission capacity has been held as a result of the fruitful trade of RTS/CTS. Since the reason for the past information outline misfortune is impact, it is not expected to change the transmission rate record rix. Achievement tally m will be continued on the grounds that the channel condition has not change. It must be called attention to that the length of the channel condition does not change, m ought not be changed. This is truly not quite the same as other rate adjustment plans and is one of the reasons why ARA is more proficient. Notwithstanding, it is still conceivable that the Rtshtx fizzled, this happens when the channel condition debases. Since RTS has a little size and has a low likelihood to impact, there is a high likelihood that the disappointment is created by channel blurring. To affirm this, ARA will send the RTS at the most reduced rate (cix = 0), indicated as Rtsltx, furthermore status will be set as Rts_low

As of right now, it has a high likelihood that Rtsltx will be transmitted effectively in light of the little size and powerful transmission rate. After the relating CTS has been gotten, the transfer speed has been saved for the following information parcel. Review that the information rate list rix is still not changed in the above steps. Thusly the information will in any case be transmitted utilizing the first rate. It is likely that this casing won't be conveyed effectively. Since the reason for this disappointment is unmistakably because of channel blurring, the transmission rate will be diminished and each variable is reset. ARA falls again to introductory state and the entire procedure rehashes.

D. Evaluation

- *Static Station in a Collision Free Network*

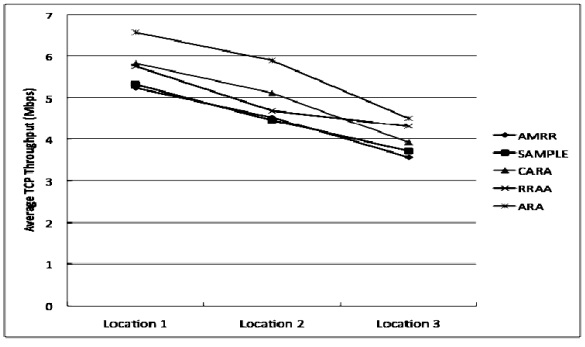


Figure 7. TCP Throughput for a Static Station in a Collision Free Network

- Static Station in a Collision Dominated Network

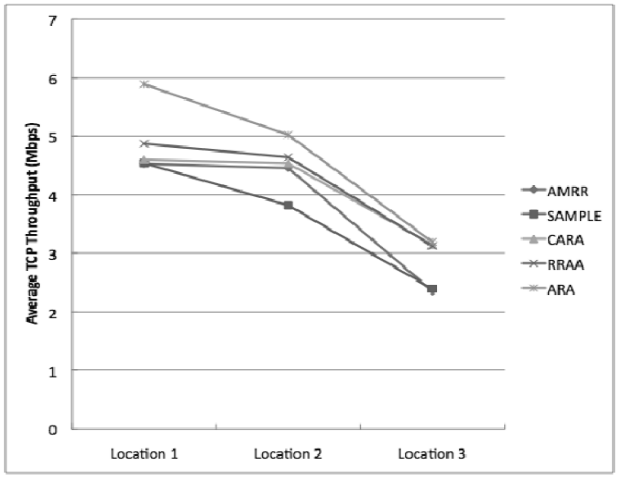


Figure 8. TCP Throughput for a Static Station in a Collision Dominated Network

- *Mobile Station in a Collision Free Network*

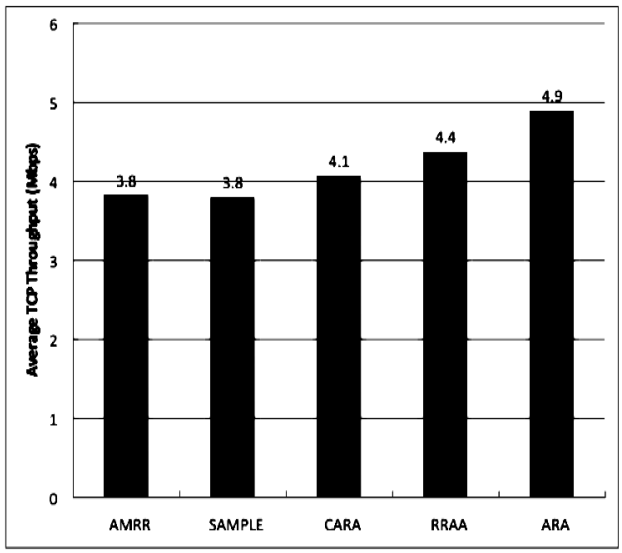


Figure9. TCP throughput for a Mobile Station in a Collision Free Network

- Static Station in Campus network

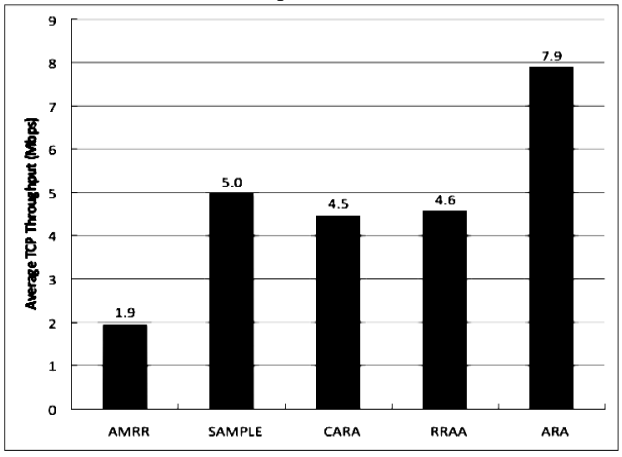


Figure 10. TCP Throughput for a Static Station in Campus Network

IV. VARA DESIGN

VARA is a cross-layer, feature mindful PHY rate adjustment convention. Its essential thought is to utilize a feature streaming rate waveform from the application layer to guide the adjustment of the remote PHY rate. For any put away feature in a remote home system feature server, such a waveform can be effortlessly produced with a play once more amid feature recording. VARA partitions time into variable-sized windows. For every window, VARA endeavors to discover a PHY rate that yields limit over the crest feature streaming rate in the window. VARA adjusts the window sizes to consider the remote channel variability and testing overhead. First and foremost, Algorithm 1 figures the measure of the following window focused around past estimations of channel variability taken amid the current window. At that point, Algorithm 2 refines this size to fulfill rate prerequisites of the examining that Algorithm 3 may run amid the following window. In the event that the PHY rate of the current window can't help the top feature streaming rate of the following window, Algorithm 3 tests the remote channel for a suitable PHY rate. Toward the start of the following window, Algorithm 1 sets the PHY rate found amid the past steps. In the following sub-segments, it is portrayed in more detail the operations of these three calculations.

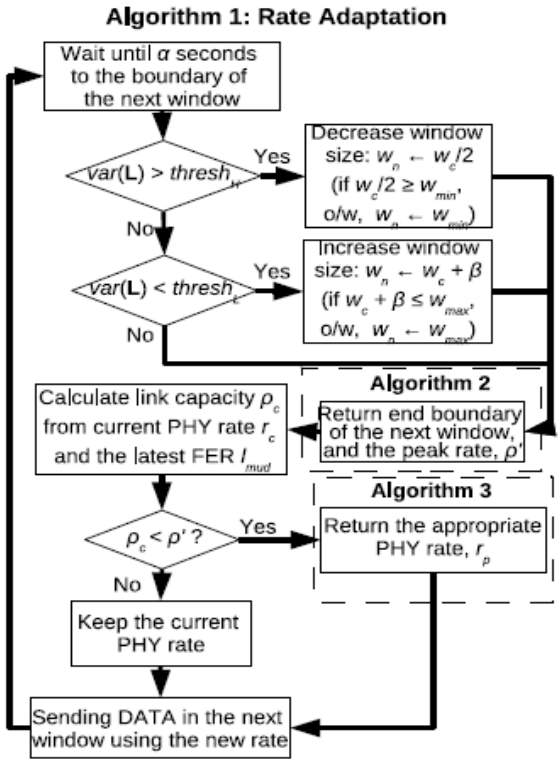


Figure 11. Algorithm 1 Rate Adaptation

A. Algorithm 1: window size and PHY rate adaptation

Algorithm 1 is the "expert" calculation that conjures algorithms 2 and 3. Algorithm 1 is conjured α seconds before the end of the current window. The parameter α is a framework set parameter and is sufficiently high to incorporate the calculations and probingsdepicted underneath. Window size adjustment. Calculation 1 registers the measure of the following window focused around the remote channel variability of the current window. Ln_{total} be the total number of MAC frames (including MAC re-transmissions) transmitted during the current window. The channel variability is computed as the variance var(L) of a set of N Frame Error Rate (FER)values, where $L = \{l_1, \ldots, l_N\}$. The i-th FER valuel_i, is the fraction of lost MAC frames within the i-th block of c transmitted MAC frames during the current window.

PHY rate adaptation. Algorithm 1 compares the calculated channel capacity,ρ_c, with the peak streaming rate, ρ' , returned by Algorithm 2. If ½c exceeds ½0, the PHY rate r_c of the current window will be used in the next window. Otherwise, Algorithm 3 is called to probe the channel and determine the appropriate PHY rate to use. Once the PHY rate of the next window is determined, Algorithm 1 sets it at the beginning of the next window

B. Algorithm 2: Window Size Refinement

Algorithm 2 refines the size of the next window computed by Algorithm 1 to handle the probing overhead. Since probing only occurs near the end boundary of the window, the position of the end boundary should be carefully chosen to minimize the impact of probing on video streaming performance. Let b_n be the end boundary of the next window computed by Algorithm 1. Based on the streaming rate before b_n, Algorithm 2 calculates a probing window size η that cansupport all probing packets. More specifically, η is computed to satisfy the following:

$$\int_{b_n-\eta}^{b_n} f(t)dt \geq \eta_p (P_{802.11})(|R| - 1)$$

where f(t) is the video streaming rate at time t, η_p is the number of ongoing data frames used for probing at each PHY rate, $P_{802.11}$ is the average WLAN frame size used for video streaming, and R is the set of 802.11n PHY rates. The average video streaming rate ½a from time $b_n - \eta$to $b_n$should also satisfy:

$\rho_a < \rho_u$

The maximum rate requirement ½u exists to ensure that the probing overhead will not cause the rate to exceed the peak video streaming rate ½0 of the next window. Such probing overhead causes capacity penalty. The average capacity penalty in our testbed is 20%. Let h be the average capacity penalty caused by probing, then:

$$\rho_u = \frac{1}{1+h}\rho'$$

If (5) is not satisfied, Algorithm 2 moves the end boundary of the next window in steps of » seconds until it is satisfied. If the current window size was increased by Algorithm 1, Algorithm 2 moves the end boundary later; otherwise it moves it earlier.

C. Algorithm 3: Channel Probing

Algorithm 3 probes the channel when the capacity ρ_c of the current window cannot support the peak streaming rate ρ' of the next window.

Amid operation, an IEEE 802.11n framework must select among 16 PHY rates, that incorporate both SDM and STBC MIMO modes. Calculation 3 decreases examining overhead by lessening the quantity of tested PHY rates. This is attained by utilizing the property that FER is an expanding capacity of PHY rate inside every MIMO 802.11n mode (STBC or SDM). This thus intimates that, for either STBC or SDM mode, the limit as a capacity of PHY rate has a solitary greatest.

Algorithm 3 tests each of SDM and STBC modes independently as takes after. To begin with, it decides the testing bearing by examining a PHY rate one stage lower and a PHY rate one stage higher than the current rate r_c. For each one rate it utilizes certain examining, i.e., it sends n_p back to back information edges of the continuous activity at that PHY rate and measures the FER. At that point it utilizes Equation (1) to figure the comparing limit. On the off chance that both limits are lower than the limit ρ_c of r_c, Algorithm 3 furnishes a proportional payback r_c onthe grounds that it yields most extreme limit for this mode. Something else, if the lower (higher) step rate gives higher limit than ρ_c, Algorithm 3 keeps testing all rates at lower (higher) steps one by one until it discovers one with a limit higher than the top rate prerequisite ρ'. In the event that no such rate is discovered, Algorithm 3 yields the PHY rate of most extreme limit. At last, Algorithm 3 thinks about the limits of the two PHY rates found for SDM and STBC modes and comes back to Algorithm 1 the PHY rate whose limit surpasses ρ' and has a lower FER (i.e., it is more vigorous). On the off chance that none of these two limits surpass ρ' Algorithm 3 comes back to Algorithm 1 the PHY rate of higher limit between thetwo.

D. *Evaluation*

In this section, we experimentally evaluate VARA's performance using our MIMO 802.11n wireless testbed. We first show that compared to the default auto rate adaptation protocol, VARA significantly reduces packet loss and achieves perfect, or close-to-perfect, video quality in terms of PSNR. We then show that VARA can efficiently adjust windows and schedule probing for different window sizes and video streams. Finally, we show that our multiplexing strategies improve the support for multiple simultaneous video streams.

VARA in Static Environment

VARA's performance against the default auto rate of the RT2880 Ralink cards (the legacy rate adaptation algorithm) in a static environment is compared. Therefore, both the AP and the clients are placed in fixed locations. Locations L1, L2, and L3 are selected to yield different wireless channel qualities. L1 has the best, L3 the worst. Table I shows the properties of different HD movie clips used in this experiment. Panda1080p represents the high streaming rate video, while Panda720p and MonsterAliens represent the medium and low streaming rate videos, respectively. Each experiment run consists of two back-to-back streaming of each HD video between the AP and each client location, first using VARA and then auto rate. Each run is repeated five times and the average. At the best channel quality location L1 auto rate supports all videos perfectly with zero loss. However, at location L2 it cannot support Panda1080p, the highest rate video. In contrast, VARA supports all videos perfectly at both locations L1 and L2. In L3, auto rate cannot support any of the videos perfectly. In contrast, VARA supports all videos perfectly except Panda1080p. This is expected because Panda1080p has a higher peak rate (26.12Mbps, Table I) than the maximum capacity of L3. With Panda1080p VARA achieves a 2% burst loss lasting for two seconds during the peak rate period, while auto rate results in a burst loss of 35% lasting for six seconds during the peak rate period. It has been found that even a burst loss rate as small as 12%, as Panda720p suffers, can cause a significant degradation of video quality. In terms of subjective video quality, although a video with a PSNR of 25dB to 30dB could still be acceptable, it demonstrates obvious jitters, blocking and blurring. A video with a PSNR around 40dB is considered as a high quality video without any observable defect. It is observed that VARA achieves perfect PSNR3 for two videos, and increases PSNR about 50% for the high rate video over auto rate.

VARA in a Mobile Environment

Performance of VARA is now evaluated when the channel condition changes more drastically. A controlled mobility scenario is used where a client moves along the path L4-L5-L6 at walking speed.FERs and capacities are first measured at these locations by sending UDP packets in different PHY rates. Table II shows the averages of these two quantities over five experiment runs. As the client moves from L4 to L5 and then to L6, the FER of a particular PHY rate changes.

For example, when 39Mbps PHY rate is used and when the client moves to L4, L5 and to L6, the FER increases from 0, to 45% and to 59%, respectively. At the same time, the capacity decreases. Then an experiment is performed in which a client moves with the same mobility pattern using VARA and auto rate while the *Panda720p* HD movie clip is being streamed. VARA computes different window sizes when the client is in different locations. Window size increases as the variation of FER is small when the current PHY rate is used. (It is worth noting that a large FER does not necessary mean a large FER variation.) When the end boundary of each window approaches, VARA evaluates if thecurrent PHY data rate can provide the capacity large enough for the peak rate of the next window

TABLE I
HD MOVIE CLIPS PROPERTIES

Data Rate	19.5	26	39	52
L4	-	-	0, 30.34	98.5, 0
L5	-	0.12, 19.24	0.45, 10.27	0.79, 0.02
L6	0, 16.75	0.49, 5.89	0.59, 3.92	-

TABLE II
AVERAGE FER & CHANNEL CAPACITY

Movie Name	Average rate	Peak rate	Variance
Panda1080p	10.26	26.12	28.71
Panda720p	5.96	15.94	10.82
MonsterAliens	5.06	14.64	5.22

V. CONCLUSION

In this paper the issue experienced by the current auto rate calculations in IEEE 802.11 Wlans with different stations producing substantial activity has been explored. Another LD-ARF calculation with misfortune separation capacity is proposed to more precisely perform the rate adjustment methodology. Examinations with the first ARF demonstrate that more than 100% change in throughput can be attained by LD-ARF when the quantity of contending stations is huge.

This paper investigates the current delegate rate adjustment plans and partitions them into two eras. The original plans do not separate the casing misfortunes and treat all the misfortunes as being brought on by channel debasement and subsequently perform ineffectively in an environment where there are many crashes. The second era plans separate the casing misfortunes and perform much better than the original plans in the blockage predominant system. In any case, while most second era rate adjustment plans may separate edge misfortunes brought on by channel debasement, they cannot decisively separate the casing misfortunes created by crash. This paper proposed a rate adjustment calculation called Advanced Rate Adaptation (ARA) that can decisively separate edge misfortunes brought on by both channel debasement and impact. In the investigation, ARA is contrasted with other agent rate adjustment conspires in both controlled investigations and field test. ARA beats other rate adaption conspires in many situations. In the field test, through a facilities remote system, ARA gives 300% throughput change over a portion of the original rate adjustment plans and 78% throughput change over second era rate adjustment plans.

Supporting HD VBR feature in Wlans is an opportune and testing issue. Despite the fact that WLAN innovations, for example, 802.11n MIMO help high remote PHY rates, it has been demonstrated that in practice the examining overhead of existing condition of the craftsmanship 802.11n PHY rate adjustment conventions can be inconvenient to feature execution.

Our remote rate adjustment convention (VARA) addresses this issue by adjusting the recurrence and timing of remote examining to the feature streaming rate and the remote channel varieties. Three novel Shifting procedures to productively multiplex HD features by minimizing top total streaming rate, blackout time and blackout territory were additionally proposed.

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Influence of Router Buffer Size on TCP Execution

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***Abstract* — In this paper, Internet Protocol router buffer size's impact on the TCP execution is dissected. TCP Start-Up, TCP Flows and High Speed TCP (HSTCP) Performance--these are the different variables considered in breaking down the execution. In this paper, a general investigation of the Slow Start (SS) Phase is introduced as a capacity of the system and TCP parameters, and after that a correlation of the execution on ways with expansive and little buffers is given. Next the buffers' sizing task will be considered for TCP Flows. Finally, the impact of buffer size on the throughput of High-speed TCP is concentrated on.**

Index Terms—**Blockage Control, High Speed Networks, Transmission Control Protocol, Throughput Analysis, Buffer Sizing, Real-Time Traffic Loss**

I. INTRODUCTION

The internet's transport protocol is TCP [9, 12]. Utilizing a blockage window (W), it controls the stream of packets as a capacity of network blockage. W speaks to the most extreme number of packets the source can transmit without the receipt of any affirmation (ACK) from the object. Toward the start of a TCP association, a Slow Start stage (SS) is called to build W rapidly and easily. It is trailed by a slower build stage called Congestion/Blockage Avoidance (BA) [9]. The changing from SS to CA happens at a window called the SS limit (Wth) which is the source appraisal of the network system limit. By channel size or by network system limit it is implied that in the continuation the most extreme number of packets can be fit on the way between the source and the objective.

The primary SS stage is known to damage the execution of short TCP exchanges particularly on long defer connections, for example, connections in the satellites [1, 2, 3] and this issue is one amongst the primary issues talked about in the TCPSAT working gathering of the Internet Engineering Task Force. The principal reason is that on long defer joins, W needs quite a while to achieve huge qualities. Amid this time, network system assets are underutilized. The arrangement proposed to this issue comprises in quickening the window increment amid SS. By Byte Counting [1] it has been known that the quantity of parcels secured by an ACK while expanding the window is considered as opposed to the quantity of ACKs. The point is to beat any postponement of ACK component at the end of the line. It is likewise observed that the Large Initial Window recommendation [2] comprises in beginning the association with a window bigger than 1 parcel, but less than 4 full parcels.

The next issue is related to the losses in the first SS stage. On the off chance that Wth is not situated properly toward the start of this stage, then before changing to CA itself the blockage can occur. This blockage brings about numerous from the same window as a result of the quick window increment amid SS. A long Timeout is obliged to recoup from these misfortunes [6]. This Timeout is trailed by different diminishments in W^{th} and another SS stage. A strategic distance from the effect of these undesirable losses on the execution needs to be maintained. For this, a recommendation has been made in [8] to gauge a more precise quality for the SS edge toward the start of the association. Ordinarily, this edge is situated to the window publicized by the collector. The creator in [8] proposes to utilize the stream of Acks toward the start of SS to gauge the Bandwidth-Delay Product (BDP) of the way and after that to set Wth to this quality.

In this paper the assignment of estimating buffers for TCP streams in 802.11e WLANs is likewise considered. Center is accentuated on the commonplace arrangement situation where a framework mode WLAN is arranged with the Access Point (AP) going about as a remote switch between the WLAN and the Internet. TCP activity is of specific significance in such Wlans as it presently conveys the incredibly larger part (more than 90% [17]) of system movement. Impacts of buffer related issues in Wlans have received little consideration in the writing. Exemptions incorporated[14] which demonstrate that fitting buffer estimating can restore TCP transfer/download injustice, and [16] in which TCP execution with settled AP support sizes and 802.11e is examined. The current paper amplifies the past chip away at buffer measuring for voice traffic [13], and is the first work concentrating on how to tune cradle sizes for TCP activity in 802.11e WLANs.

Next we consider the instance of HSTCP. In high bandwidth delay item networks, because of improbable demands of TCP's reaction capacity, TCP cannot open its window sufficiently expansive to use the accessible data transmission. TCP is upgraded to High Speed TCP [19], to address the above mentioned central issue, which adjusts the window progress for high blockage window (low loss) administration. After a certain window limit, High Speed TCP expands its blockage window forcefully to get the accessible data transmission and on misfortunes, it decreases the window gradually to stay smooth. Since High Speed TCP's window progress go live just everywhere window (low loss) administration, High Speed TCP does not change TCP conduct in situations with high to gentle blockage (common for Low Speed systems.) In high bandwidth deferral systems in which High Speed TCP

sends blasts of substantial number of packets, the measure of buffer accessible in the bottleneck switch is a paramount issue to keep the switch profoundly used amid blockage periods. The current designs oblige router producers to give a buffer whose size is tantamount to the bandwidth delay product (BDP) of the way which scales straightly with line speeds. As the connection limit increments to many Gbps, giving such a colossal buffer might definitely build the expense of the routers and force mechanical issues, for example, dispersion of heat, on-chip board space and expanded memory access inertness. An expansive buffer expands delay and delay fluctuation which antagonistically influences constant applications (e.g., feature diversions, gadget control and feature over IP applications.) So in this manner it is very critical to find the impacts of buffering on High Speed TCP execution, for example, throughput, merging to decency and communication in the vicinity of RED. Prior suggestions have been surrounding around enhancing the execution of High Speed TCP or different variations to scale TCP in High Speed situations, e.g., [22], [23], [24]. None of these studies expressly analyzed the impact of support size on the proposed TCP variations. A logical model for High Speed TCP is inferred and altered point strategy is utilized to numerically illuminate for the use attained by contending long lasting HSTCP streams the model catches how the execution of High Speed TCP is influenced by the buffer through RTT.

The presentation of the rest of this paper is as per the following. In Section II, a model for the assessment of TCP is given and, the TCP execution is concentrated on account of a high Wth. In Section III, a Network is setup and the execution with altered supports and the technique for versatile cushion measuring are exhibited. In Section IV, the altered point method to process the use of HSTCP streams vieing for a bottleneck with a given cradle size is portrayed furthermore numerical and reproduction results are introduced; then the settled point system to register the use of HSTCP streams going after a bottleneck having RED AQM with given cushion size is depicted furthermore the numerical and recreation results are displayed.

II.IMPACT OF BUFFER SIZE ON TCP START-UP

A. A Model for TCP Performance

Consider a TCP association that exchanges documents of size S over a way of bottleneck transfer speed µ. The broadly executed Reno rendition of TCP [6] is utilized all through the paper. Nonetheless, the investigation can be connected to alternate forms too. The system is demonstrated with a solitary bottleneck hub of rate µ and of Drop Tail Buffer of size B. T means the consistent part of the Round Trip Time (RTT) of the association (the two-way spread postponement in addition to the administration time of TCP bundles in system hubs). This is the model which has been utilized regularly as a part of the writing to study the execution of TCP [1,4,5,7,10].

The characterization of TCP conduct amid the first SS stage requires the count of the window at which losses happen amid SS expecting that Wth is situated to a high esteem. This later window is known as the flood window and it is signified as WB. Alternate works expect certainly that it is equivalent to the pipe size (B + µt). It will be demonstrated later that for a little cushion measure, this window can be free of the bottleneck transmission capacity and just a capacity of B and the window build rate. Note here that all through the paper, it is expected that the recipient window is situated to a high esteem so it doesn't restrict the development of W. Notwithstanding µ, T and B, the flood window is a capacity of the rate at which TCP expands its window amid SS. This rate is known as the forcefulness or the burstiness of SS. It is displayed with an element d characterized as takes as follows.

- *The aggressiveness factor d*

Let W(t) signify the blockage window in parcels at time t. It is gathered that after one RTT, W is expanded amid SS by W(t)=d bundles. d can be the consequence of the recipient deferring Acks and sending an ACK each d parcels. d = 1 implies that the beneficiary is recognizing all the parcels and d = 2 models the Delay ACK system broadly executed in TCP recipients. d can likewise display the loss of ACKs on the return way. It might likewise represent any window build strategy at the source not the same as that of standard TCP. A case is Byte Counting [1], where upon the receipt of an ACK, the window is expanded by the quantity of recognized bundles instead of by one parcel as in standard TCP.

- *The overflow window WB*

This window is obliged to comprehend the effect of the distinctive parameters on the execution. As in [4, 10] a SS stage is isolated into smaller than expected cycles (MC) of length of time RTT. Let W(n) be the quantity of packets transmitted

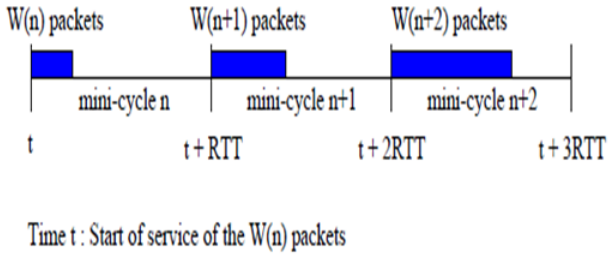


Figure 1. Start of service of the W(n) Packets

amid MC n. The following MC begins when the ACK for the first bundle of these W(n) packets achieves the source. As indicated by our meaning of the parameter d, the window size amid the following MC is equivalent to:

$$W(n+1) = W(n) + W(n)/d = \alpha W(n) \quad (1)$$

with $\alpha = (d+1)/d$.

Assume that the repetitive connection (1) is legitimate for each n ¸ 0. Assume additionally that SS begins with a window equivalent to one parcel. Consequently,

$$W(n) = \alpha^n W(0) = \alpha^n.$$

Amid SS, packets leave the bottleneck in long blasts at rate μ. A blast of length W(n) is served amid MC n and it is trailed by an unmoving period until the entry of the blast of the accompanying MC (Figure 1). This unmoving period between blasts vanishes when the window size surpasses μt. The source transmits additionally packets in long rushes because of the ACKs of packets of the past MC. Given that the quantity of packets transmitted amid a MC increments by a component α, it can be gathered that the long blasts transmitted by the source have a normal rate αμ. Therefore, toward the start of MC n, the source begins to transmit a blast of length W(n) at a normal rate αμ. At the point when a source blast achieves the bottleneck, a line begins to develop in B at a rate αμ-μ=μ/d. Here, two cases must be considered. The main case is when B doesn't contain any parcel from the past MC when the first bundle of the blast of the current MC achieves the bottleneck. The second case is the point at which a few packets from the past MC are even now holding up in B. Note here that in alternate works [4, 5, 10], just the first case has been considered. This is right when the buffer size is little contrasted with the BDP. Nonetheless, the second case acquainted licenses us with record for all the buffer sizes. In the first case, a blast of size B(d + 1) is obliged to fill the cushion and reasons a flood. Let n_B^1 be the quantity of the MC amid which B floods. The quantity of packets transmitted amid this MC must be bigger than B(d + 1). Anyway, the quantity of packets transmitted amid the past MC must be short of what B(d + 1) generally the flood would have happened amid the past MC. Along these lines, n_B^1 satisfies,

$$\alpha^{n_B^1-1} < B(d+1) \leq \alpha^{n_B^1}$$

As per our meaning of d, the transmission of a blast of B(d + 1) packets obliges an increment in W by B packets since the start of MC n_B^1. It takes after that,

$$W_B = W(n_B^1 - 1) = \alpha^{n_B^1-1} + B \qquad (2)$$

Presently, the second case is considered. The window size is bigger than μt. The blast size needed to fill the cradle is short of what B(d+1) since there are a few packets holding up from the past MC. This is equivalent to the quantity of unfilled spots toward the start of the MC times (d+1). The increment in the window between the start of the MC and the flood is equivalent to the quantity of void spots. Assume that the flood happens amid MC n_B^2. At that point, W_B gets to be equivalent to:

$$W_B = W(n_B^2 - 1) + B - (W(n_B^2 - 1)\mu T)$$
$$= B + \mu T \qquad (3)$$

Two declarations for W_B are then accessible. On the chance that the window size amid MC $n_B^1 - 1$ is short of what μt, then W_B will be given by mathematical statement (2), else it will be given by comparison (3). These two representations can be joined into a solitary one as said in the accompanying hypothesis.

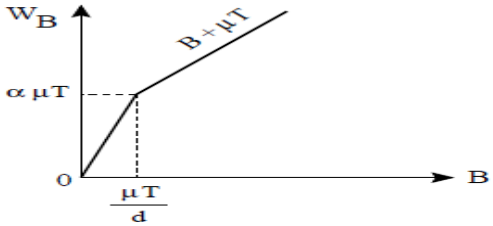


Figure 2. The overflow Window W_B vs. B

Theorem 1: *In the event that SS is not ended before the event of misfortunes, the cushion at the entrance of the bottleneck connection will flood at a window:*

$$W_B = B + \min(\mu T, \alpha^{n_B - 1}), \qquad (4)$$

B. Impact of High W_{th} on Performance

Here, the situation where Wth is situated higher than WB and where TCP uses its SS calculation to gage the system limit is considered. Misfortunes happen and the execution is a capacity of W'_{th}, the new system limit evaluate after the recuperation from misfortunes.

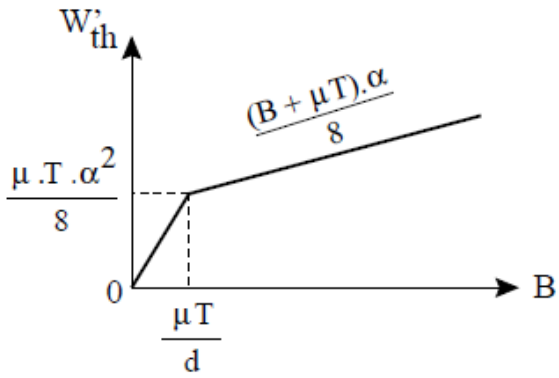


Fig 3. The new capacity estimate vs. B

- *Calculation of W'_{th}:*

The buffer flood is caught one RTT after its event. Amid this RTT, W increments by αwb unless the source gets in CA. This is the situation when WB < Wth < αwb. Blockage is located at a window WD equivalent to:

$$W_D = \min(W_{th}, \alpha W_B) \qquad (5)$$

Here, TCP sets W and W_{th} to half W_D and begins to recoup from misfortunes. Frequently, it succeeds to locate the initial two misfortunes through Duplicate Acks. The third and the ensuing misfortunes require a Timeout to be recognized [6]. Reno partitions its window by two upon each misfortune recognition. Hence, in the greater part of the cases, the SS limit after the Timeout is situated to one eighth WD. It is situated to one fourth WD when the second misfortune can't be recognized through Duplicate Acks. In the continuation, it is accepted that W'_{th} = W_D=8.

It is similarly expected that Wth is situated much higher than αwb so that the is constantly caught at WD = αwb.

- *Impact of B and d on Performance:*

Utilizing the line as a part of Figure 2, Figure 3 is plotted, the variety of W'_{th} It is well seen that the evaluation gave by SS moves to zero when the cushion size does. Above μt=d, the reduction in execution is created by the diminishing in the channel measure however the forcefulness of TCP amid SS has no effect on the evaluation. Nonetheless, underneath μt=d, the cradle gets to be not able to assimilate the bursty activity of TCP and the blockage shows up before arriving at the funnel size. An increment in TCP forcefulness for this situation diminishes the appraisal and may break down the execution as opposed to enhancing it. It is concentrated on in the accompanying, this communication between cradle size and TCP forcefulness. Two cases are viewed as: First it is assumed that the forcefulness is controlled at the collector which recognizes each d information packets. For this situation, both SS and CA are

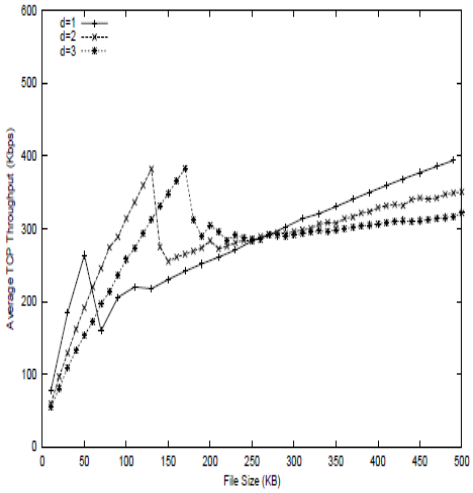


Figure 4. Throughput vs. file size for B=20 packets

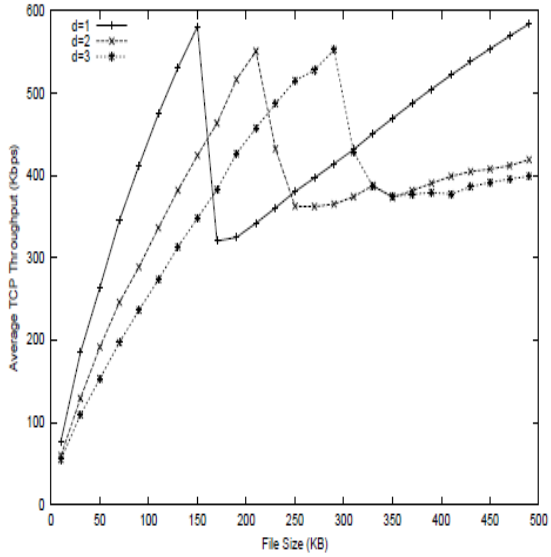


Figure 5. Throughput vs. file size for B=70 Packets

influenced. Second, the situation where the forcefulness is controlled at the source is considered. During this situation, the source can recognize SS and CA and can accordingly receive diverse elements d amid each stage.

A receiver-controlled d: As seen from Figure 3, if there should be an occurrence of a B littler than μt=d, an increment in d enhances the system limit assess after the Timeout. This ought to prompt a change in the execution. Be that as it may, on account of a collector controlled d, the increment in d abates likewise the window development amid CA. The increase attained in W'_{th} when expanding d will be repaid later by the slower window development amid CA. The execution begins in order to break down after a little change. This conduct is seen in Figures 4 and 5 where it has been plot for two diverse B, 20 packets and 70 packets, the throughput as a capacity of the record size. Three estimations of d are considered. For a given d, it is perceived that toward the starting, the throughput increments rapidly with the record size. Little records are exchanged totally amid the SS stage and the quick increment in the throughput is because of the quick window increment amid SS.

For every d, a descending bounce in the execution for some document size can be seen. This relates to the presence of misfortunes amid the SS stage. After this bounce, the source gets in CA bringing about a slower increment in the throughput. The more distant the source gets in CA, the littler is the influence of the first SS stage. After this jump, the source gets in CA resulting in a slower increase in the throughput. The farther the source gets in CA, the smaller is the impact of the first SS phase.

The normal throughput ought to keep expanding in an asymptotic way until the normal throughput in the unfaltering is arrived at. Typically, the greatest normal throughput or the most extreme usage of system assets is a capacity of B, μ and T and not the forcefulness. The forcefulness decides the rate at which it unites to the consistent state. A little d is quite greater to an extensive one at whatever point the document is exchanged without misfortunes. Once these misfortunes happen for the little d (the more forceful form), the substantial d begins to give better execution on the grounds that it keeps away from the Timeout. This will keep on proceeding until misfortunes happen for the substantial d too. In the event of little supports, regardless of the possibility that misfortunes show up for the extensive d, it keeps on going preferred execution over the little d for specific records sizes because of the higher system limit gauge given by it. Be that as it may, the CA stage of it is excessively moderate so it loses this benefit later. In the event of expansive cradles nonetheless, the lessening of the forcefulness doesn't enhance the appraisal. Along these lines, the execution of a huge d gets to be more awful than a little d when misfortunes happen. In this way, a collector controlled d influences both SS and CA. The most minimal conceivable d must be utilized amid CA to ensure a quick meeting to the relentless state. The most generally utilized component is d = 2 (Delay ACK instrument). Amid SS, d must be picked in such an approach to build the window as fast as would be prudent to the fill the funnel. The best execution

is gotten when it is begun by a little d then changed to a bigger one equitable before the flood of cushion and it is proceeded like this until the channel size is arrived at. This comprises in lessening SS burstiness with the increment in the blockage window. Such component is hard to execute given that TCP is not mindful of the cradle estimate in system hubs. In any case, this provides for us a rule on the best way to change the element d on ways with little buffers.

A sender-controlled d: In this segment the effect of a change in the window expand rate amid SS on the execution is contemplated. The window expand rate amid CA is kept unaltered. This allows an end of the effect of d on the CA stage. Such conduct obliges a change at the source on the grounds that it is the main component ready to recognize the two stages. It is expected in the accompanying that the collector

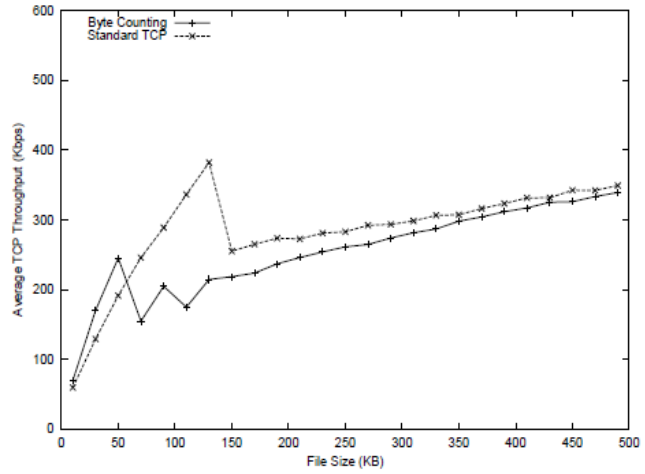


Figure 6. Throughput vs. file size for B=20 packets

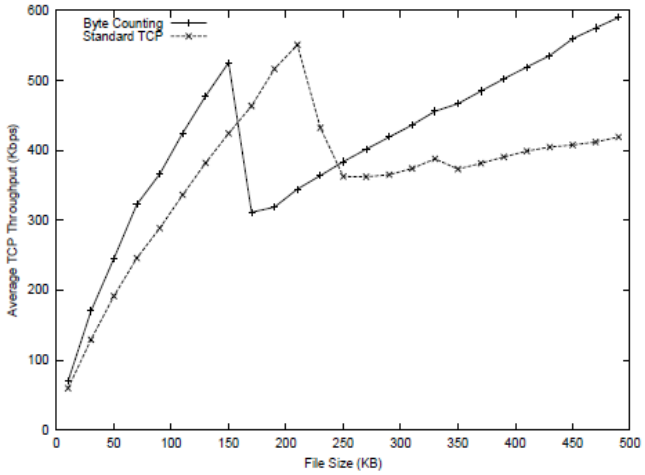


Figure 7. Throughput vs. file size for B=20 packets

is recognizing each other information parcel and that the source executes standard TCP amid CA. Changing the variable d at the source can be fulfilled by changing the measure of the window increment upon the receipt of an ACK. Given that Acks are postponed at the objective, standard TCP compares to d = 2. Byte Counting [1] relates to d = 1. Changing d from 2 to 1 has been demonstrated to enhance the execution [1, 3]. Our investigation demonstrates that this can be the situation on ways with substantial supports. Then again, on ways with little cradles, expanding the forcefulness decreases the system limit appraise and decays the execution. Figures 6 and 7 clarify this issue. These figures demonstrate the throughput as a capacity of the record size for the two cradles 20 parcel and 70 packets. In each one figure, one of the two lines speaks to standard TCP and the other line speaks to Byte Counting. For an expansive cradle, Byte Counting works superbly and gives better execution. On the other hand, for a little cradle, Byte Counting is aggressive to the point that it fills the cushion before filling the channel. This gives lower appraisal and consequently lower execution for the vast majority of the document sizes.

III. BUFFER SIZING FOR TCP FLOWS

A. *Network Setup*

The situations where the Access Point (AP) goes about as a remote switch between the WLAN and the wired Internet are considered. Transfer streams are from remote stations in the WLAN to server(s) in the Internet, while downloads are from wired server(s) to stations in the WLAN. At the MAC layer, IEEE 802.11g parameters are utilized as indicated as a part of Table I. The transfer speed between the AP and server(s) is 100 Mbps. TCP Reno with SACK is utilized. It is noted that in Wlans, TCP ACK packets without any prioritization can be effortlessly lined/dropped because of the way that the essential 802.11 DCF guarantees that stations win a generally equivalent number of transmission opportunities. In point case consider n stations each one convey one TCP transfer stream. The TCP Acks are transmitted by the AP. While the information packets for the n streams have a total n/(n + 1) offer of the transmission opportunities the TCP Acks for the n streams have just a 1/(n+1) offer. Issues of this sort are referred to debase TCP execution altogether as lining and dropping of TCP Acks upset the TCP ACK timing system. Taking after [3], this issue is tended to utilizing 802.11e. At the AP and each one station, TCP Acks are dealt with as a different activity class, gathering them into a line which is allocated high need through Cwmin = 3, Cwmax = 7, AIFS = 6. This makes use of 2 out of the 4 available queues in 802.11e.

TABLE-I
MAC AND PHY PARAMETERS

$T_{SIFS}(\mu s)$	10
Idle slot duration	9
Retry limit	11
Packet size (bytes)	1000
PHY data rate (Mbps)	54
PHY basic rate (Mbps)	6
PLCP rate (Mbps)	6

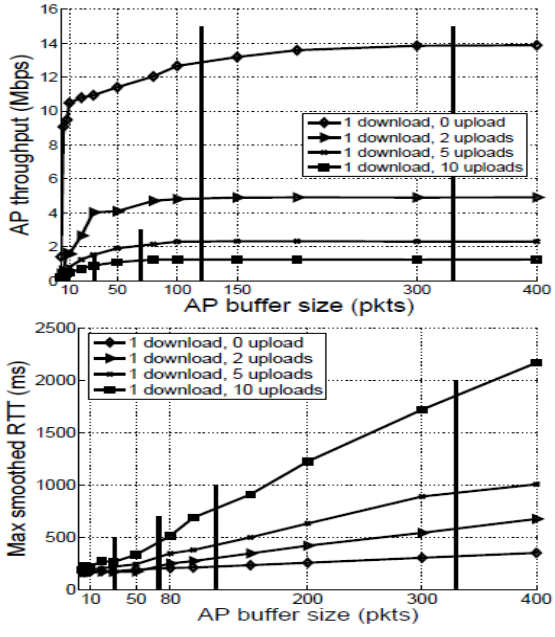


Figure 8. Performance with fixed buffer sizes. Data shown for 1 download flow and 0, 2, 5, 10 uploads – corresponding BDP values marked by vertical lines. One upload flow per wireless station. Max smoothed RTT denotes the maximum TCP srtt value observed. Wired backhaul link bandwidth 100Mbps, RTT 200ms.

B. Performance with Fixed Buffers

Rather than wired systems, the mean administration rate at a remote station is not settled yet rather relies on the level of channel discord and the system load. This is represented in Fig. 1 where the throughput and postponement of a download stream are plotted as a capacity of the AP support size when the quantity of contending transfer streams (with one transfer stream every remote station) is differed. So also to wired systems, the throughput dependably increments monotonically with the support size, arriving at a most extreme over a limit cushion size. It can likewise be seen that the download throughput falls as the quantity of contending transfers increments. The variety in throughput can be significant, e.g., the greatest throughput transforms from 14mbps to 1.25mbps as the quantity of contending transfers transforms from 0 to 10. Thus, the BDP – checked by vertical lines in Fig. 1 – additionally changes fundamentally and this is reflected in buffering prerequisites. For instance, it can be seen from Fig. 1 that with no contending transfers the limit cradle measure above which the AP attains most extreme throughput is 338 packets, while for 10 contending transfers this cushion size tumbles to give or take 70 packets. In perspective of this conduct, one conceivable methodology is to size supports focused around most detrimental possibility conditions, i.e., focused mainly around the specific conditions obliging the biggest buffering to attain high throughput. Notwithstanding, while guaranteeing high throughput, this takes on at the

expense of high dormancy. For instance, it can be seen from Fig. 1 that when an altered cushion size of 338 packets is utilized (which as a part of this illustration guarantees greatest throughput paying little heed to the quantity of battling stations), the round outing inertness experienced by the download stream is around 300ms with no transfers yet climbs to around 2s with 10 fighting transfer stations. This happens in the absence of the fact that TCP's blockage control calculation tests for transmission capacity until bundle misfortune happens thus download streams will have a tendency to fill supports with any sizes. In addition, the mean lining deferral of a support of size Q with mean administration rate B is Q/B. Consequently, the lining postponement at the AP relies on upon the administration rate, which thusly relies on upon the quantity of battling remote stations and their offered burden. For a settled size support, an abatement in the administration rate of a component b. On the other side, estimation of the buffer to attain lower inactivity over all system conditions has a go at the expense of decreased throughput, e.g., a support size of 30 packets guarantees inertness of 200-300ms for up to 10 fighting transfer stations yet when there are no battling transfers the throughput of a download stream is just around 75% of the greatest achievable.

Notwithstanding varieties in the mean administration rate, it is additionally noted that the arbitrary nature of 802.11 operations prompts brief time-scale stochastic variances in administration rate. This is generally not quite the same as wired systems and straightforwardly effects buffering conduct. Stochastic vacillations in administration rate can prompt early line flood and lessened connection usage. Case in point, from Fig. 1 with 10 transfers the most extreme download throughput is 1.25mbps, yielding a BDP of 31 packets. On the other side, it can be observed that at this support estimate the accomplished download throughput is just around 60% of the most extreme – a cushion size of no less than 70 packets is obliged to attain 100% throughput. The stochastic variances in administration rate lead to a necessity to build the cradle measure over the BDP with a specific end goal to suit the effect of these changes. The measure of over-provisioning obliged may be limited utilizing measurable contentions, yet it is not sought after further here because of space obligations. It is to be noted that, then again, that a basic however compelling methodology is to over-procurement by a settled number of packets over the BDP. For instance, from Fig. 1 it can be seen that over-provisioning by 40 packets is sufficient for the scope of conditions considered, and it is observed that this methodology meets expectations all the more for the most.

C. Adaptive Buffer Sizing

Roused by the previous perceptions and the trouble of selecting a settled cushion size suited to a scope of system conditions, the consideration of the utilization of a versatile support estimating procedure is done. It is noted that a remote station can promptly measure its own administration rate by perception of the between administration time, i.e., the time between bundles touching base at the leader of the system interface line ts and being effectively transmitted te (which is demonstrated by getting accurately the relating MAC ACK.). Note that

this estimation can be promptly executed in genuine gadgets and causes minor calculation load. Let Tserv(t) be the between administration time at time t, exponential smoothing is utilized to figure the mean between administration time Tserv = αtserv + (1 - α)(te - ts) where α = 0.999

Utilizing this estimation the accompanying versatile procedure is proposed. Let T be the target lining delay2. The cradle size Q is chosen as per Q = min(t/Tserv,qmax) where Qmax is situated to be 400 bundles. This will diminish the support size when the administration rate falls and expand the cradle size when the administration rate climbs, in order to keep up a roughly consistent lining postponement of T seconds. This viably controls the support size to stay equivalent to the BDP as the mean administration rate differs. To record for the effect of the stochastic nature of the administration rate on cushion size necessities, this upgrade guideline is adjusted to Q = min(t/Tserv+a,qmax) is an over-provisioning add up to suit fleeting vacillations in administration rate.

Taking into account the estimations in Fig. 1 and others, it has been discovered that a quality equivalent to 40 parcels functions admirably over an extensive variety of system conditions. The viability of this straightforward versatile calculation is delineated in Fig. 2. Here the plot is given for throughput rate and smoothed RTT of download streams as the quantity of download and transfer streams is differed. It can be seen that the versatile calculation keeps up high throughput productivity over the whole scope of working conditions. This is accomplished while keeping up the inertness roughly steady at around 400ms – the idleness climbs somewhat with the quantity of transfers because of the over-provisioning a to suit stochastic variances in administration rate. Fig. 3 exhibits the capacity of the versatile algorithm to react rapidly to changing system conditions. At time 200s the quantity of transfers is expanded from 0 to 10. It can be seen that the cradle measure rapidly adjusts to the changed conditions while keeping up high throughput product.

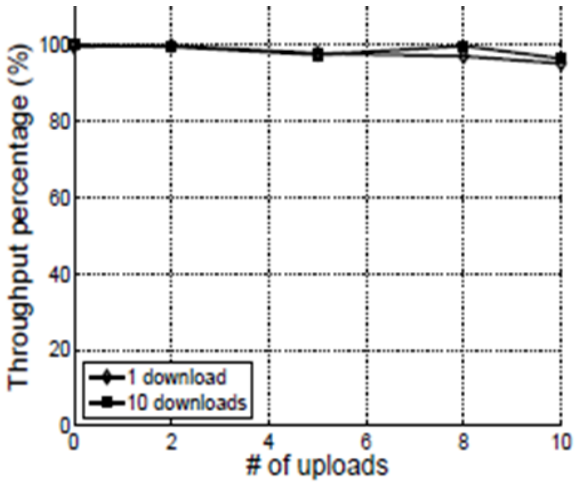


Figure 9. Throughput Percentage

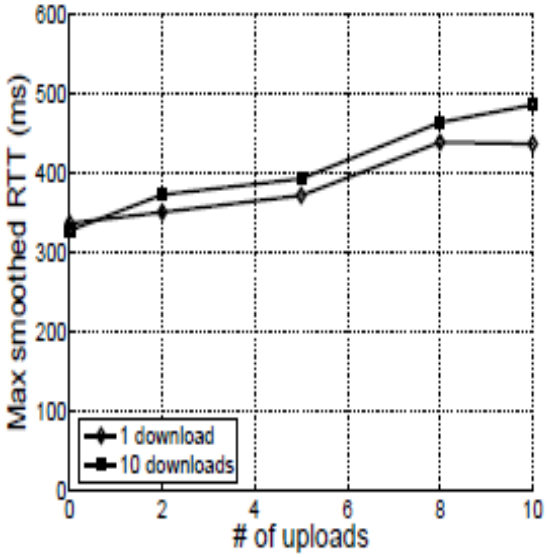


Figure 10. Max Smoother RTT

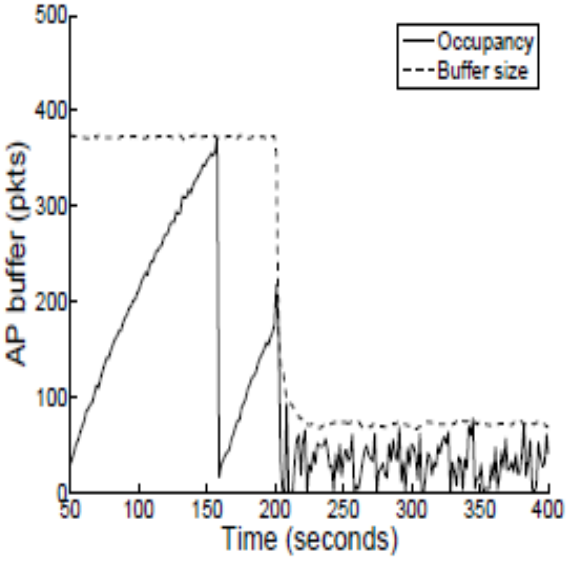


Figure 11. AP Buffer

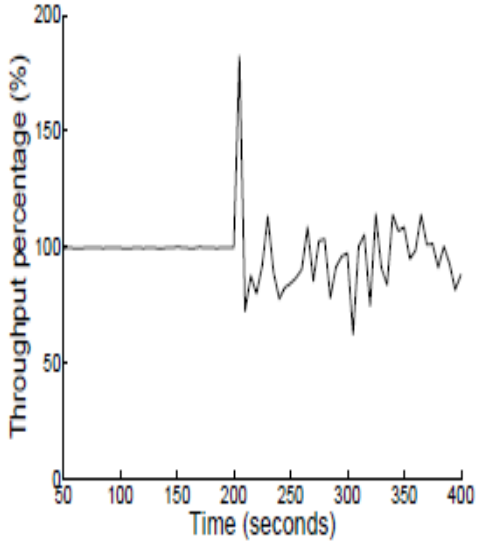


Figure 12. Throughput Percentage

IV. INFLUENCE OF ROUTER BUFFER SIZE ON HIGH SPEED TCP

A. *Fixed Point Approximation with Drop Tail*

In this area, the altered point iterative technique to assess HSTCP accepting a M/M/1/K model of the bottleneck line is depicted. The heap on the bottleneck connection is given by:

$$\rho=\frac{1}{C}\sum_{i=1}^{N}\lambda_i(p,RTT_i)$$

From established M/M/1/K results:

$$\rho=\frac{\rho^K(1-\rho)}{1-\rho^{K+1}}\;;R_i=2d_i+\frac{MSS}{C}\frac{\rho}{1-\rho}-\frac{K\rho^K}{1-\rho^K}$$

where d_i is the proliferation deferral of the ii-th association and MSS the most extreme portion size. So the heap can be gotten from Eq. (4):

$$\rho=\frac{1}{C}\sum_{i=1}^{N}\lambda_i\frac{\rho^K(1-\rho)}{1-\rho^{K+1}}.2d_i+\frac{MSS}{C}\frac{\rho}{1-\rho}-\frac{K\rho^K}{1-\rho^K}$$

It is watched the right hand side of Equation (5) is consistent in ρ∈[0,1]. The throughput, λ, of HSTCP is constant in p pand p pis persistent in ρ Therefore, in any event there exists an altered point for Eq. (5). The estimation of the subsidiary of the iterative capacity relies on upon the cushion size and consequently, the uniqueness of the altered purpose of the capacity relies on upon the buffer.

Evaluation: The impact of cushion sizes on the usage accomplished by 10 perpetual High Speed TCP associations beginning at diverse times is reenacted. The topology is demonstrated in Figure 13. The normal connection, R1-R2 R2is 1gbps with 50ms deferral. The Rtts of the associations are diverse extending from 115.5ms to 124.5ms and normal RTT is 120ms. The cushion size at R1-R2is fluctuated as a small amount of 12500 1kb-parcels (80% of BDP of the biggest RTT.) The BDP of just

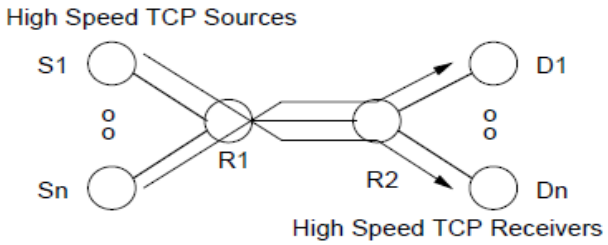


Figure 13. Simulation Topology

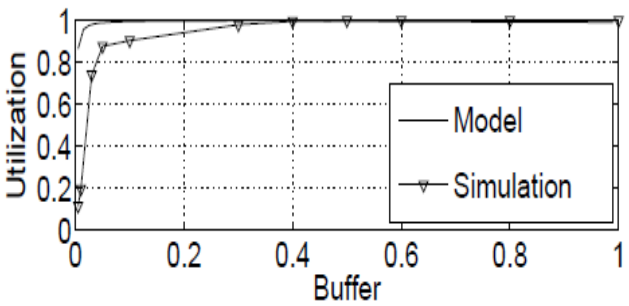
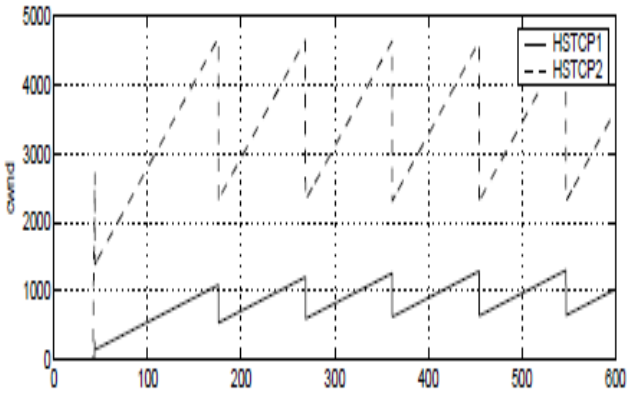


Figure 14. Throughput as function of Buffer size fraction (max 12500)

R1-R2 is 12500 bundles. In the investigations, the estimations of ω_h=83000, ω_l=38, p_h =10^{-7} and p_l=10^{-3} have been used. Observing the bottleneck utilization as a function of buffer size in Figure 14, it is found that results from simulations and our analytical model are quite close. In simulations, it is found that the loss rate is mostly equal to p_l. It is observed that buffer size equal to 10% of the bandwidth-delay product can sustain more than 90% utilization. The discrepancy between the two curves in Figure 14 mainly arises from our M/M/1/K assumption and simplifying approximations that have been made in deriving the closed form throughput expression. In the next experiment, the bandwidth of the common link R1-R2 is changed to 2.5Gbps and delay to 10ms. The RTTs of the connections are different ranging from 38ms to 142ms and average RTT is 90ms. The buffer size is varied as a fraction of 6250 1KB-packets (35% of BDP of largest RTT connection.) The BDP of just R1-R2 is 6250 packets. The window and queue evolution of two competing High Speed TCP flows in case of under-buffered and over-buffered (Figure 15) bottleneck router using the topology shown in Figure 13 are plotted. The RTT of HSTCP1 is almost twice that of HSTCP2. The bottleneck bandwidth is 1Gbps with 10ms of delay. The unfairness evident from the window dynamics is due to difference in RTTs of the two connections. It also seen that a larger bottleneck buffer reduces the unfairness between two connections. Thus, one should consider the effect of buffer size on the tradeoff between RTT fairness and utilization.



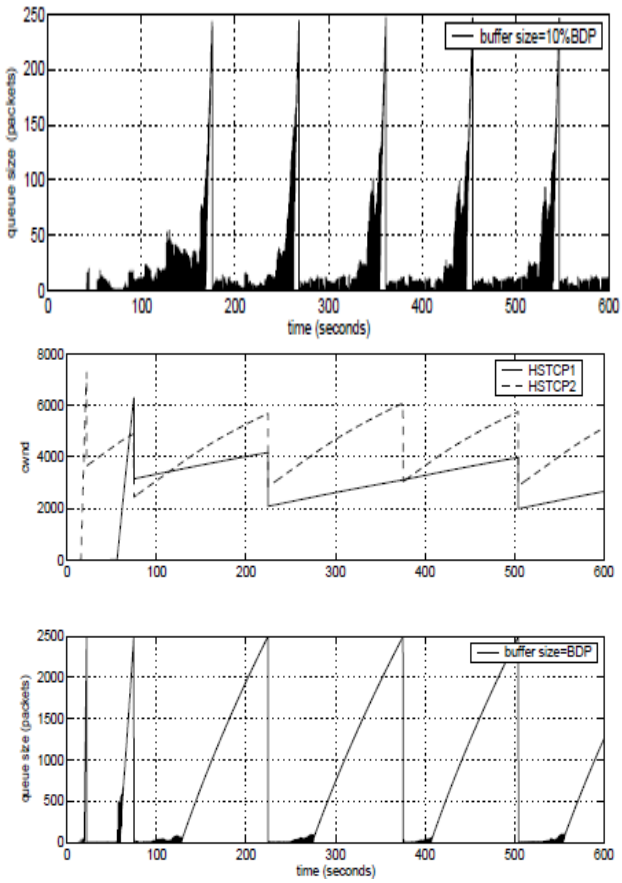


Figure 15. Window behavior of two High Speed TCPs and drop tail queue size in over-buffered case

Fixed Point Approximation with RED AQM

In this area, the execution of High Speed TCP under RED is assessed. The investigative model of RED is taken after. RED aides in uprooting the predisposition against bursty streams and blast sizes are extensive on account of High Speed TCP streams. Utilizing the PASTA property, the drop likelihood of a bundle at a RED line is given by:

$$p_{red} = \sum_{n=0}^{k} \pi(n)p(n)$$

$$= 0 \qquad if\ n \leq min_{th}$$

$$= \frac{(n - min_{th})p_{max}}{max_{th} - min_{th}} \qquad else$$

Evaluation: The impact of support size on the usage accomplished by 10 perpetual High Speed TCP associations under RED is reenacted. The normal connection R1-R2 2is 1.0gbps with 50ms postponement. The cradle size is differed as a small amount of 12500 1kb-bundles. The associations begin at distinctive times furthermore their Rtts are diverse going from 115.5ms to 124.5ms and normal RTT is 120ms. Versatile RED is utilized as a part of which min_{th} and max_{th} are powerfully balanced. In our numer1ical assessment basic RED is utilized for numerical tractability; min_{th} = 40% of full support size and max_{th} to full cushion size are situated. The use of High Speed TCP in the vicinity of RED is plotted in Figure 16. The misfortune rate is 10-7 for cradle degree ≥0.1

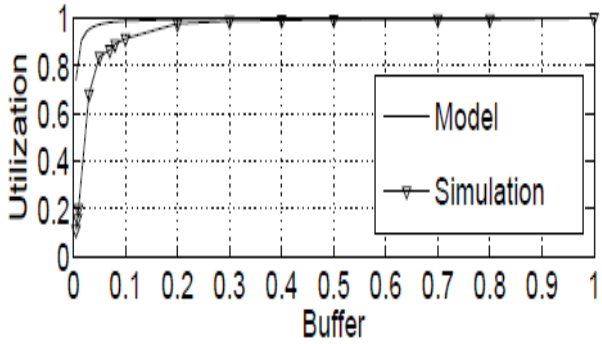


Figure 16. Throughput as function of buffer size, min_{th}=0.4xmin (BDP, buffer size), max_{th}=min (BDP, buffer size), N=10, C=1 Gbps

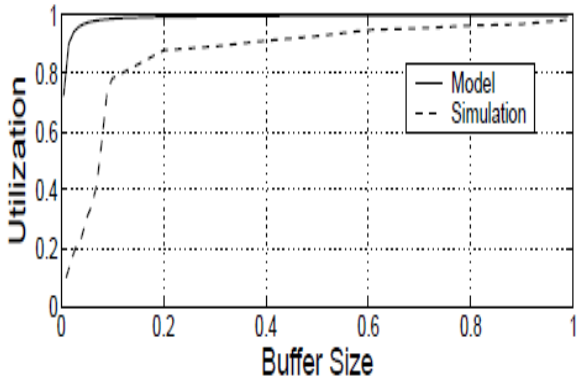


Figure 17. Throughput as function of buffer size, min_{th}=0.4xmin (BDP, buffer size), max_{th}=min (BDP, buffer size), N=10, C=2.5 Gbps

A comparable investigation is plotted in Figure 16 where the limit is changed to 2.5gbps and postponement to 10ms. The Rtts are diverse running from 38ms to 142ms and normal RTT is 90ms. The cushion size is differed as a small amount of 6250 1kbpackets. It is observed that the misfortune rate is around 10-6. In spite of utilizing Adaptive-RED in the reenactments, close concurrence with the numericals.

V. CONCLUSION

In this paper, the conduct of TCP amid the first SS stage has been concentrated on. This allowed us to assess the execution of shorts exchanges and the viability of the suggestions made to enhance this execution. It is discovered that, on ways with little cushions contrasted with their BDP, the blockage amid SS may seem ahead of schedule before filling the funnel size. Subsequently, the worth to provide for Wth toward the start of the association, keeping in mind the end goal to dodge misfortunes must record for the cushion measure overall misfortunes may not be dodged. Additionally, for this situation, it is discovered that any increment in TCP forcefulness falls apart the execution as opposed to enhancing it. A rule for how to expand the window in these ways is displayed.

Next, the assignment of measuring cradles is considered for TCP streams in 802.11e Wlans. Various essential new issues emerge contrasted with wired systems, including the way that the mean administration rate is reliant on the level of channel conflict and parcel between administration times change stochastically because of the arbitrary nature of CSMA/CA operation. Propelled by these perceptions, a versatile support measuring calculation is proposed which imitates the traditional BDP lead and exhibits its viability through recreations. Support estimating while rate adjustment is empowered is left as future work, in spite of the fact that it is accepted that the proposed calculation will work. Future work likewise incorporates thought of the likelihood of diminishing cushion sizes when multiplexing happens [10].

From our numerical results obtained utilizing the altered point strategy and also from reproductions, it is presumed that regularly, an industrious High Speed TCP association crossing a bottleneck join has a low sending rate when the cushion size is little. The throughput increases as cradle size increases. It is found that a cushion size of 10% of the data transmission delay item can keep up no less than 90% usage. Expanding the support estimate past 10% builds the use barely arriving at very nearly 98% when the cushion size is around 20% of the data transfer capacity delay item. Then again, a little cushion measure below 10% of the transmission capacity delay item causes numerous bundle drops, which prompt an uncommon drop in the use and may decrease High Speed TCP to consistent/standard TCP. It is noted that our results are predictable with a late free study, which demonstrates that the general guideline of setting the support size equivalent to the transfer speed deferral item is difficult. The results are introduced considering a solitary bottleneck. Then again it is accepted that cradle prerequisites will have comparable patterns on account of numerous congested bottlenecks. However one needs to accept that, inspite of the fact that it has just been centered around long lasting streams, it

will be fascinating to explore the execution of brief streams and consistent rate streams (e.g. UDP) on rapid connections with distinctive cushion sizes.

In our future work, it is proposed to explore the impacts of support size on the execution of other rapid TCP variations, e.g. Quick TCP [21] which transform its window as per cushion delay.

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Mathematical Analysis of Interference Issues and Study on Pathloss, Fading and Shadowing Effects on Cognitive Radio Networks

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***Abstract*—Handling interference in wireless communication system is a challenging task. This paper aims about mathematical analysis of interference in general and also in cognitive radio networks. This paper concentrates on various sources of interferences such as pathloss, fading and shadowing. Interference system model was created by considering spatial distribution of nodes, wave propagation characteristics and mobility of the interferers. Interference from active set of nodes and aggregate interference was analyzed mathematically. Finally, interference in cognitive radio network was analyzed under different circumstances. Simulation results showed that the outage probability of secondary user to sense the transmission between primary transmitter and receiver with respect to pathloss, fading and shadowing.**

***Index Terms*—Interference, pathloss, shadowing, fading, cognitive radio and mathematical model**

I. INTRODUCTION

In wireless communication environment, the major constraints which effects the performance of the system are

- Thermal noise
- Interference issues
- Propagation losses

A.Thermal noise

It is common phenomenon in most of the transmission lines and communication devices. Random electron motion is the main reason for thermal noise. It is also called as white noise and it will distribute uniformly along the full spectrum. For defined bandwidth, noise voltage is given as

$$V^2 = 4KT\int_{f_1}^{f_2} RdF \qquad (1)$$

R= Resistance
T= Temperature
f1 and f2= lower frequency and upper frequency of defined spectrum
V= Integrated RMS value between upper and lower frequencies.

B. Propagation losses

Losses occurred during the propagation of the signal is called as propagation loss. Attenuation and distance are inversely proportional to each other. As the propagation distance increased, radiated energy will spread and hence path loss will occur. The pathloss between two isotropic antennas can be represented as

$$L = 20\log_{10}\left(\frac{4\pi d}{\lambda}\right) \qquad (2)$$

Where d is the distance between transmitter and receiver, λ is wavelength and L is pathloss. Propagation losses will also occur due to the effects of Multipath fading, shadowing and etc…

C. Intereference issues

If one receiver accumulates the signal from not only defined transmitter but also other transmitters, interference problem will exists. Interference may disrupt the signal and sometimes it modifies the content of the original signal. It will reduce both coverage and capacity of the network. The following figure 1 shows various possibilities of interference sources. It explains about how the signals from other system will affect required system performance. Due to this effect overall Carrier to Interference ration (C/I) decreases.

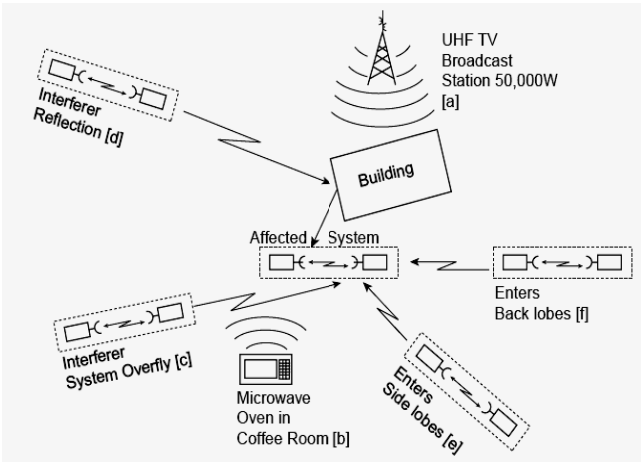

Figure 1.Possibilities of interferences

II. INTERFERENCE SOURCES

Main sources of interferences are classified into 3 broad categories.

1. Antenna parameters (Overlapping)
2. Out of band emitters
3. In band emitters

A. Antenna parameters

ISM configured issues: Industrial, Scientific and Medical (ISM) fields will use unlicensed spectrum for their general applications. These bands were unlicensed and subjected to use under ISM fields. Hence, the users use these bands in their equipment's. These bands will create interference among themselves and also to the licensed spectrum.

Reflections: The complex building structures and other forms will create reflections. Signal reflection is main source for Multipath fading. Reflections from different surrounding will create different path lengths. These reflected signals will reach to the receiver and if they are in out of phase with each other, it leads to overlapping of signals. This is also one of the important reason for generation of interference.

B. Out of band emitters

Intermodulation: Nonlinear power amplifiers and other external components may create interference. Broadband power amplifiers are using in the final stage of communication system. The linear characteristics of those amplifiers are precise, any non-linearity will create cross reference signal which is near to original signal. The mixing of these two signals will lead to interference.

Desensitization: placement of receivers near high frequency transmitters or devices will also create interference. This only happens if the design of pre selection filter is not good. This effect will disturb linearity characteristics and creates nonlinear amplification nature. This will lead to intermodulation distortion and causes data errors.

C. In band emitters

The designers are also using Non-licensed spectrum for variety of applications. Frequency Hopping Spread Spectrum (FHSS) used by some wireless Local Area Networks (LAN) within this non licensed spectrum. This is close frequency band to in home applications such as microwave oven. Hence, these two operating in same environment will leads to interference.

III. MODELLING OF NETWORK INTERFERENCE

Modelling of network interference with respect to Ultra Wide Band (UWB) is always a challenging task. Impact of these UWB on narrowband applications such as GSM is a major focus in current research area. Andrew c et al proposed Finite Difference Time Domain method (FDTD) for interference modelling for indoor wireless applications.

The perfect interference model should concentrate on some physical parameters which effect interference. Some of them include propagation characteristics of channel, transmission characteristics of interferers and spatial distribution of interferers. There is no Unified network interference model which gives spectral efficiency, power spectral density, and throughput and bit error rate. This paper was proposed unifying model which can meet all above constraints.

System model - Physical scenario and distribution of nodes:

Consider two dimensional infinite plane (x, y). Place all nodes according to homogeneous point process method on plane. The probability of existence of node in defined particular region R over total area AR is given as

$$\text{P \{Number of nodes (n)in region R\}} = \left[\frac{(\lambda A_R)^n}{\text{n!}}\right] e^{-\lambda A_R}$$

Where, λ = spatial density of selected region R.

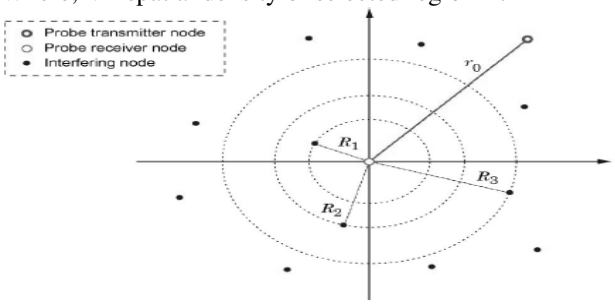

Figure 2. Distribution of Nodes

All nodes in defined area should operate in interested frequency band so that they act as interfere nodes. Density of interference nodes and the distance between interfering node and probe receiver mode will define the amount of interference. Network topology of these nodes has negligible effect on this process. From Fig.2, the distance between receiving node and actual transmitting node is r_0. By considering all other nodes as interference nodes, their distance from receiving node is shown as R1, R2 and R3.

Characteristics of wave propagation:

Transmitting node will send the signal to receiving node with transmitting power level of Pt. The receiver receives the signal with power Pr. the relationship between these two power levels is given by

$$P_r = (P_t \pi_k Z_k)/R^{2b} \quad (3)$$

Here we are considering Pt as average power measured from 1m away from transmitter, Z_k is other loss parameters which include shadowing and fading and b is amplitude loss component. The value of b is variable; it may range from 0.8-5. Depending on the traffic density, b value will change. If path loss component is 1, it will represent free space propagation. The proposed model considered all following situation to become unified model. They are

- Assuming there is no fading and only pathloss will exist
- Pathloss and fading is also existed (Nakagami fading)
- Pathloss and shadowing effect
- Pathloss, shadowing and fading effect

By taking time as an important and considerable factor, the relationship between transmitter and receiver can be represented in Equivalent Low Pass (ELP) representation. For received signal, expected ELP is given as

$$Y(t) = \left(\frac{\pi_k \sqrt{Z_k}}{R_b}\right) \int h(t,\tau) X(t-\tau) d\tau \quad (4)$$

X(t) is the transmitted signal and $h(t,\tau)$ is impulse response of channel.

Importance of movement of other nodes (interferers):

Obstructions in the path of both transmitter and receiver results fluctuations in power flow. These fluctuations cause the effect of shadowing on communication. Change in distance between interfere nodes and receiving node will also leads to effect of shadowing. It is assuming that the distance and shadowing effect is almost constant for

particular duration of symbol [9]. Let ρ represents the shadowing and distance parameter. Here, there are two possibilities were existed i.e. slow varying and fast varying ρ.

In slow varying ρ, interfere nodes has long life time and in fast varying ρ, they has short life span. Measurement of outage metrics is possible in slow variation mode and average metrics are possible in fast variation mode.

IV. INTERFERENCE DISTRIBUTION

Let, real Random Vector (RV) which represents interference from all receivers is given byY = [y1, y2…yn]. Then the aggregate interference can be represented as

$$Y = \sum_{i=1}^{\infty}(Q_{i/R_i})F_A(Q_i,R_i) \quad (5)$$

Here

$$F(Q_i,R_i) = \begin{cases} 1 & \text{when } (Q,R) \in A \\ 0 & \text{when otherwise} \end{cases}$$

Where QI represents associated with interferer i. In analysis of shadowing and fading, we can use variable. $F(Q_i,R_i)$ is the function which relates information about selection of nodes which are responsible for overall interference. A represents the set of elements (assuming that all elements are active). Now let us try to calculate the overall interference from number of elements which are in active set.Let R1, R2, R3… Rn are the distance between original node and active set elements. The general representation of these distances is $\{R_i\}$, i=1, 2… ∞.

The aggregate interference from all active elements is given by

$$Y = \sum_{i=1}^{\infty}(Q_{i/R_i})F_A(Q_i,R_i) \quad (6)$$

Here η >1 and the characteristic function is given by $\emptyset_y(W,A)$ and is represented as

$$\emptyset_Y(W,A) = \exp\left(-2\pi\lambda \iint \left(1 - e^{\left(jw\frac{q}{R}\right).F(Q_i,R_i)}\right) f_Q(q)dq.dr\right) \quad (7)$$

Where $f_Q(q)$ is the probability distribibition function of Q.

For above equation,

If A= {(q,r): $r \in I$,

Then

$$\emptyset_Y(W,A) = \exp\left(-2\pi\lambda \int_I \left(1 - \emptyset_Q\left(\frac{W}{R}\right)\right)rdr\right) \quad (8)$$

From the above equation for η =b and I=[0, ∞), then it modify as

$$\emptyset_Y(W) = \exp\left(-2\pi\lambda \int_0^{\infty}\left(1 - \emptyset_Q\left(\frac{W}{R^b}\right)\right)rdr\right) \quad (9)$$

If the function is random variable, then the above equation can be modified as

$$\emptyset_Y(W,A) = \exp\left(-2\pi\lambda \int_0^{\infty}\left(1 - \emptyset_0\left(|\frac{W}{R}|\right)\right)rdr\right) \quad (10)$$

This is the modified characteristic function of aggregate of interference.

V. ANALYSIS OF COGNITIVE NETWORKS

Cellular and data traffic is increasing from day to day. All telecom operators were operating in their respective licensed spectrum. Now, spectrum became one of the scarce resources. To increase the usage efficiency of spectrum, cognitive radio concept was introduced.The concept of secondary user introduced in this technology. Secondary user can use the same licensed spectrum of primary user without making any interference. Spectrum sensing technique is the best example of cognitive behavior. Now, we will see the interference model set up in cognitive radio to avoid aggregate interference. If there is a transmission between primary transmitter and receiver, receiver will transmit beacon with power pr. This beacon will sense the secondary user to not to occupy the channel. But, the effects of shadowing and fading will disturb this beacon sometimes and make secondary user free environment (no transmission between primary transmitter and receiver).The probability that the second user can sense the transmission between primary transmitter and receiver is given as

$$p_d(r) = P_{\{z_k\}}\{(p_{pri}\pi_k Z_k)/R^{2b}\} \quad (11)$$

This is also called as threshold power or minimum power to sense by secondary user.

Calculation of interference by secondary users:

The generated power for particular secondary user is given as

$$I_{sec} = \sum_{i=1}^{\infty}(P_{sec}Z_i/R_i^{2b})F_A(Q,R) \quad (12)$$

From the expression of$\emptyset_y(W,A)$,

Put η =2b and$Q = P_{sec}Z$, it can be modified as

$$\emptyset_{I_{sec}}(w) = \exp\left(-2\pi\lambda_{sec}\int_0^{\infty}\int_0^{(p^*R^{2b}/P_{pri})}(1 - f_z(Z)rdzdr\right) \quad (13)$$

$f_z(Z)$ is the probability distribution function of Z_i

Analysis on propagation phenomenon:

To regulate the interference flow, it is essential to identify the beacon generated by the primary user. To control this phenomenon, propagation characteristics have to be studied under various circumstances.

- Pathloss
- Pathloss and Nakagami fading
- Pathloss and shadowing
- Pathloss, fading and shadowing

Pathloss:

It considers the radius of the primary receiver. The radius is given by $(\frac{P_{pri}}{p^*})^{1/2}$

Secondary node has to detect beacon whether it is inside the radius of primary receiver or not. Then, the probability characteristics can be modified as

$$P_d(r) = \begin{cases} 1 \ when \ 0 < r < (\frac{P_{pri}}{p^*})^{1/2} \\ 0 \ whenothercondition \end{cases} \quad (14)$$

Combination of pathloss and fading:

This fading is existed only when it crosses maximum radio diversity combining. This type of fading consideration is suitable for multipath scattering with large time delays. In this case, the probability that the second user can sense the transmission between primary transmitter and receiver is given as

$$P_d(r) = 1 - (1/\Gamma(m))\gamma_{inc}(m,\frac{p^*R^{2b}}{P_{pri}}m) \quad (15)$$

This equation is obtained from the Cumulative Distribution Function (CDF) of gamma. Gamma function is a continuous probability distribution function and also it follows maximum entropy probability distribution. Assuming that, for wireless communications, this distribution function is

taken as ideal one. The function is an incomplete function. The modified probability that the second user can sense the original transmission with respect to m is given as

(16)

Here,

Combination of pathloss and shadowing:

The patterns like big obstacles or hills will produce shadowing effect. This shadowing may represented as log-normal distribution or log-distance path loss model. If we consider n number of individual events, the multiplicative product of all those independent variables were represented by log normal distribution. This condition is exactly suits for wireless environment and hence log normal distribution was used to represent shadowing effect.

Using Gaussian Q function the probability distribution of secondary user to detect transmission between primary transmitter and receiver is given as

(17)

VI. SIMULATION RESULTS

Let Pout is the probability of interference generated as an outcome of presence of second user. By considering conditions that $R/P_{sec} = 1$; b = 2; = 10, Pout was simulated and result is shown in following figure.

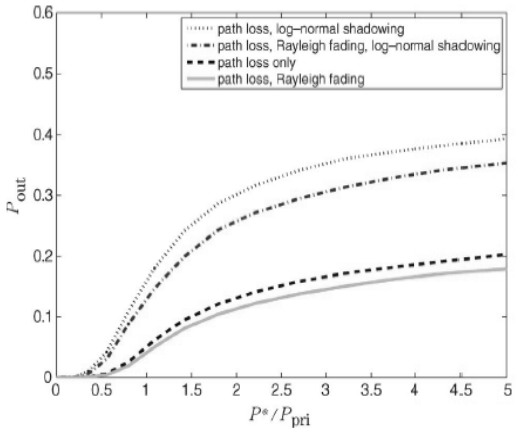

Figure 3.Pout vs for R/Psec = 1; b = 2; = 10

CONCLUSIONS

In this paper, Mathematical model of interference was investigated and simulated. By creating a physical scenario, aggregate interference generated by the all other nodes on primary receiver was developed and analyzed. The main parameters of interference viz. pathloss, fading and shadowing was also explained in detail. Interference handling in cognitive radio network was explained mathematically. Finally, the probability of sensing (between primary transmitter and receiver) was computed for different cases. Simulations carried on this paper only based on mathematical model. Simulations showed that the relationship between outage probability and. Still, perfection is needed in mathematical analysis to adopt to practical cases.

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Design of Switched Capacitor Integrators using 90nm Technology

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Abstract—**The filters are important blocks in applications like image processing, communication, signal processing etc. Most of the filters are designed by using components like operational amplifiers, resistors, capacitors etc. But, in present VLSI design this direct implementation of RC based filters cannot meet the non functional constraints like high speed, less area and low power etc.**

The RC based analog filters require precise values of components to maintain required frequency characteristics. Hence design of controllable, large value, uniform linear resistor in a less area is difficult in standard VLSI process. By replacing a resistor with a Switched Capacitor principles can solve most of these problems. The switched capacitor filters are designed by using a basic block called as switched capacitor integrators. The switched capacitor integrators and filters require only capacitor ratios to be precise to meet the required frequency characteristics and other parameters. The main aim of this work is to design switched capacitor based integrators for both parasitic sensitive and parasitic insensitive designs using Cadence Virtuoso full custom design flow and 90nm technology.

Index Terms—**Op-Amp, Switched Capacitors, Integrators, VLSI, Filters.**

I. INTRODUCTION

The design and implementation of electrical and electronics systems is done by using passive components like Resistors(R),Capacitors(C) and Inductors(L) in the early stage of IC design area. The advancement in IC technology modified the used of inductors due to its large size and noisy characteristics. Hence the design of IC based circuits used Resistors, Capacitors and Operational Amplifiers (op-amps) etc [1].

The present analog and mixed signal design environment IC circuits must meet performance metrics like area, speed, power and cost etc. This is done by using either Bipolar Junction Transistor (BJT) or Metal Oxide Semiconductor (MOS) transistor technology. The BJT technology is selected for high speed applications and for portable and battery based application products MOS technology is used. In MOS technology the fabrication of resistor is a difficult task. The resistor is designed by using MOS transistors to meet different non functional constraints and other parameters.

The present System on Chip (SOC) analog and mixed signal design applications the resistors are replaced by using Switched Capacitor (SC) circuits consisting of switches and capacitor [2].

The basic concept of switched capacitor circuits is shown in Fig.1 [3].

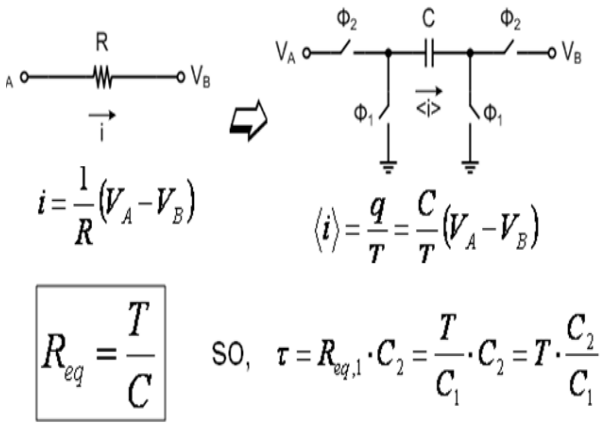

Figure 1: The basic concept of Switched Capacitors

In SC circuit capacitor is charged and discharged by using by using the non overlapping clocks φ1 and φ2 [2].The equivalent resistor of SC circuit is calculated by using the above formula. The non overlapping clocks example is shown in Fig.2 [3-4].

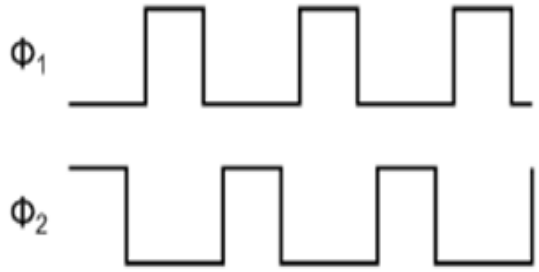

Figure 2: Example of non-overlapping clocks

The filters are important blocks in applications like image processing, communication, signal processing etc. Most of the filters are designed by using components like operational amplifiers, resistors, capacitors etc. The filters are designed by using RC based integrators and Op-Amp components. The RC based integrator and SC based integrators are shown in Figure 3[3-4].

The main aim of this work is to design Switched Capacitor based integrators for both parasitic sensitive and parasitic insensitive integrators two stage op-amp with compensation techniques to using cadence full custom design suite and 90nm technology.

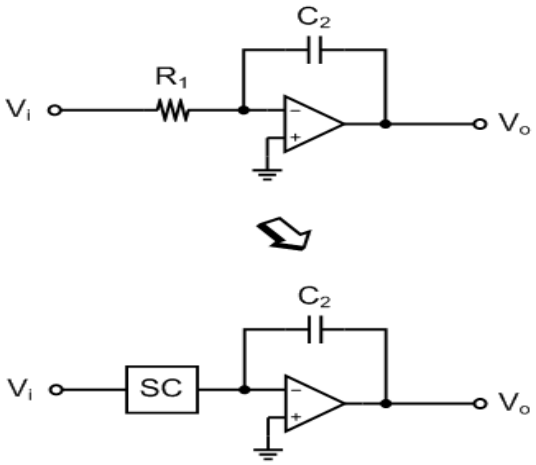

Figure 3: RC and SC based integrators

This paper is organized such that the section II gives general background and information of SC based parasitic sensitive and parasitic insensitive integrators. The section III describes the details of full custom design of SC based integrators using Cadence tools and also describes the simulation results. The conclusion is presented at the end followed by references.

II. SWITCHED CAPACITOR INTEGRATORS

The Switched Capacitor integrators are designed by using the SC circuit of Fig.1, concepts of Fig.2 and using Fig.3. The SC integrator circuits are divided into two types based on the parasitic capacitance effects.

1. Parasitic Sensitive SC Integrator
2. Parasitic Insensitive SC Integrator

The SC integrators are designed by using MOS transistors, capacitors and Op-Amp components. The capacitors are designed by using double poly metals to meet the performance metrics. The op-amp is designed by using basic two stage topology. The basic structure of two stage op-amp is shown in Fig.4 [5, 6].

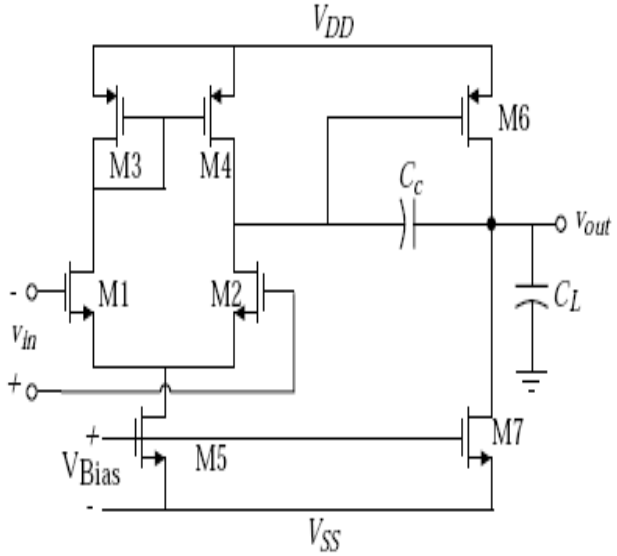

Figure 4: Two stage opamp

The parasitic sensitive SC integrator using above op-amp topology is shown in below Fig.5.

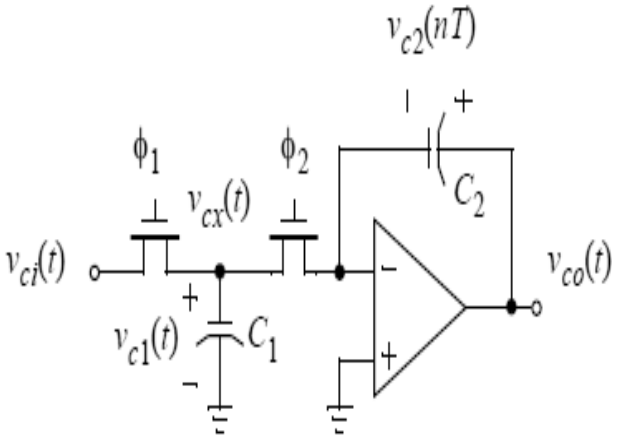

Figure 5: Parasitic Sensitive SC Integrator

The sample waveforms for the parasitic sensitive SC integrator are shown in Fig. 6.

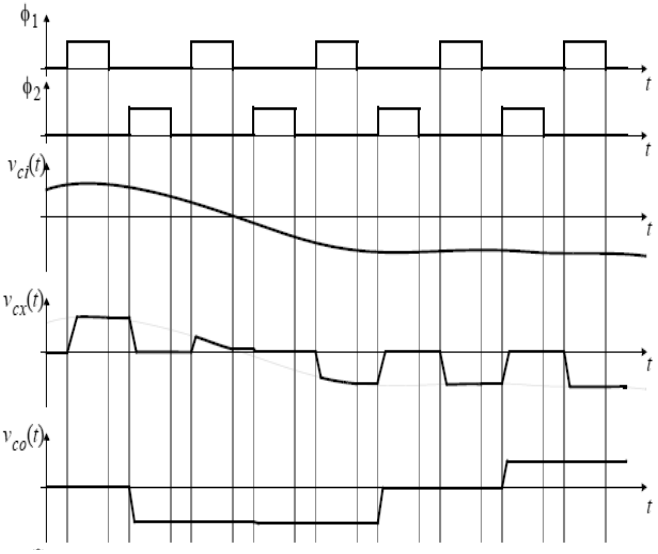

Figure 6: Sample waveform of parasitic sensitive SC integrator

The capacitor of SC integrator is designed by using double poly and there is equivalent parasitic capacitance C_{p1} and C_{p2} across C1 capacitor as shown in Figure 7.

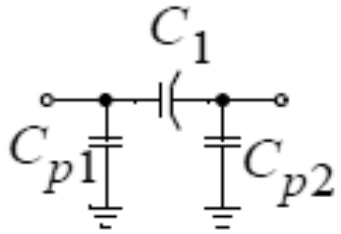

Figure 7: Equivalent parasitic capacitors

The effect of parasitic capacitors can be eliminated by using two more transistors to the switched capacitor circuit and this type of integrator is called parasitic insensitive integrator. The circuit of parasitic insensitive SC integrator is shown in Fig 8.

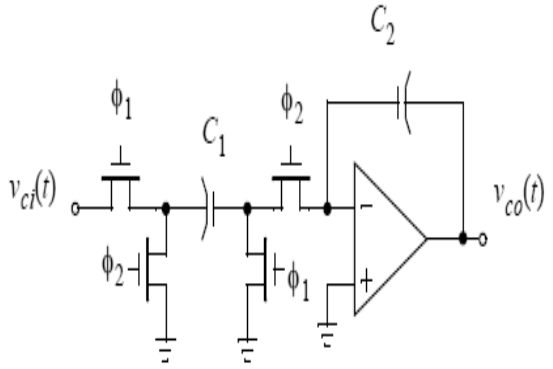

Figure 8: Parasitic Insensitive SC Integrator

III. FULL CUSTOM DESIGN OF SC INTEGRATORS

The Switched capacitor integrators are designed by using full custom IC design flow using 90nm technology. The Cadence Design suite tools are used for the design and simulation with individual tools as listed in Table1.This section gives the information of schematic designs of Switched Capacitor integrators and the simulation results.

TABLE I
CADENCE DESIGN SUITE TOOLS MAPPING

Design Action	Tool Name
Schematic entry	Virtuoso schematic editor
Symbol creation	Virtuoso Symbol editor
Simulation	Analog Design Environment tool
Layout	Assura
DRC	Assura
Layout Vs Schematic	LVS tool
Post layout verification	GDSII or OA
Targeted Technology	90nm

The transistor level full custom design of basic two stage op-amp schematic diagram using Cadence Virtuoso Schematic tools is shown in Figure 9. The symbol for the two stage op-amp design using Cadence Virtuoso schematic editor is also shown in Figure 10, which is used as a basic building block for the SC integrator circuits.

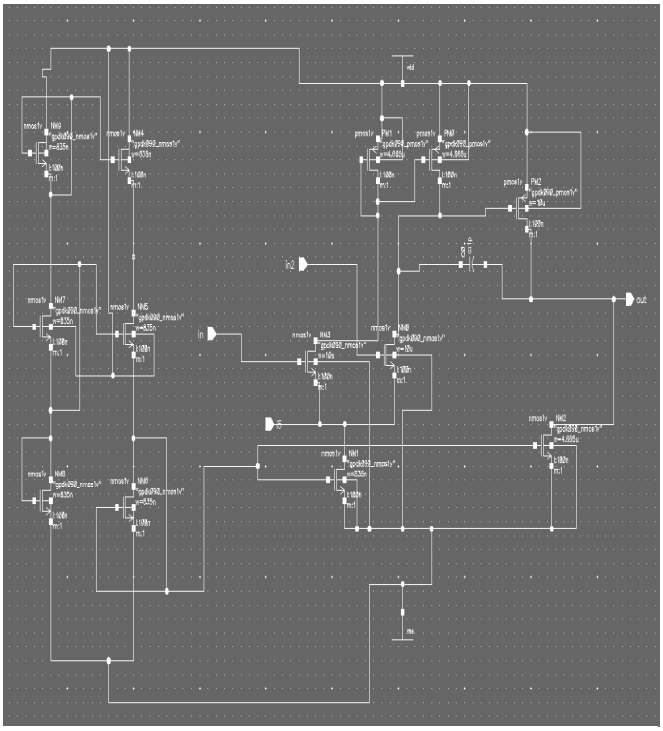

Figure 9: Two stage op-amp schematic

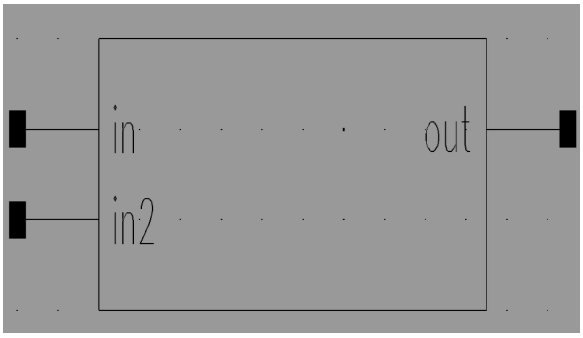

Figure 10: Op-amp Symbol

The schematic diagram of parasitic sensitive switched capacitor integrator using above two stage op-amp symbol is shown in Figure 11.

The simulation result of parasitic sensitive SC integrator is shown in Figure 12 and Gain plot is shown in Figure 13.

The schematic diagram of parasitic insensitive switched capacitor integrator using two stage op-amp symbol is shown in Figure 14.

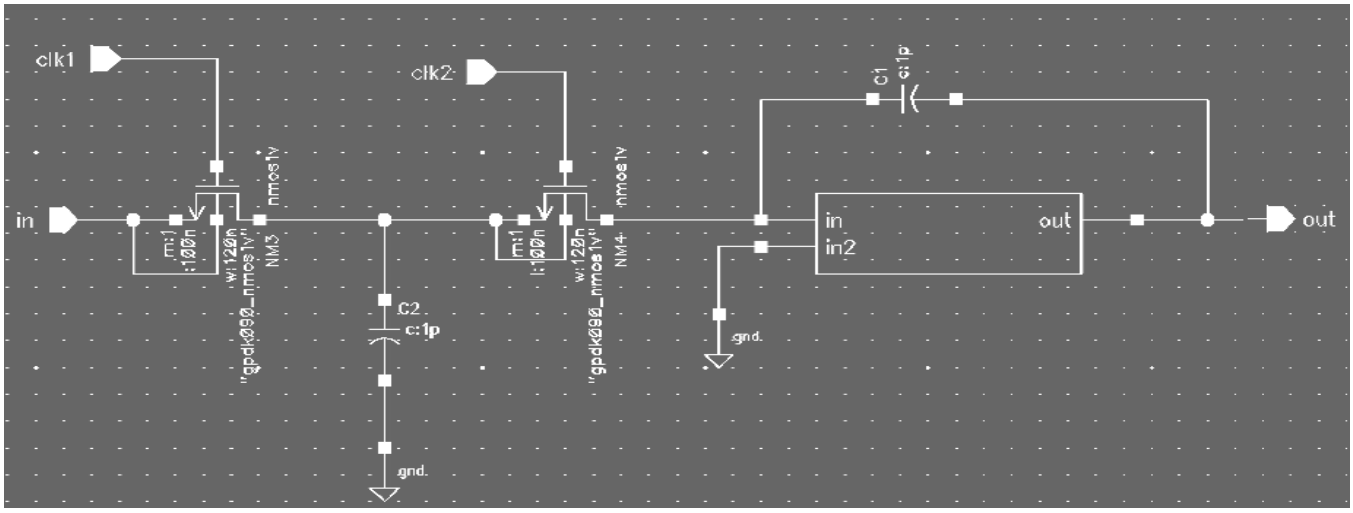

Figure 11: Parasitic Sensitive SC Integrator

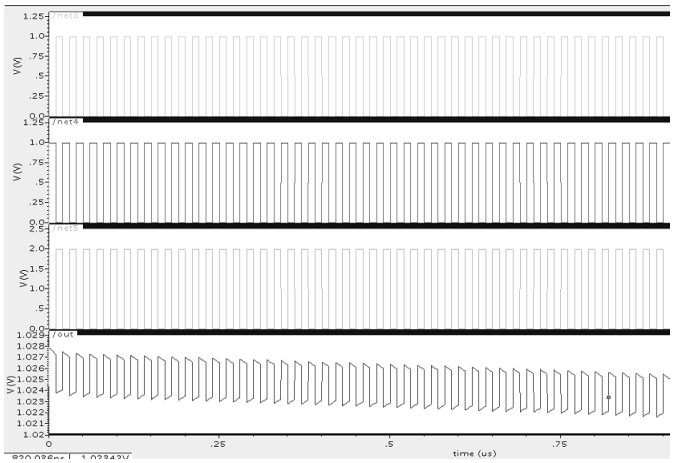

Figure 12: Simulation of parasitic sensitive SC integrator

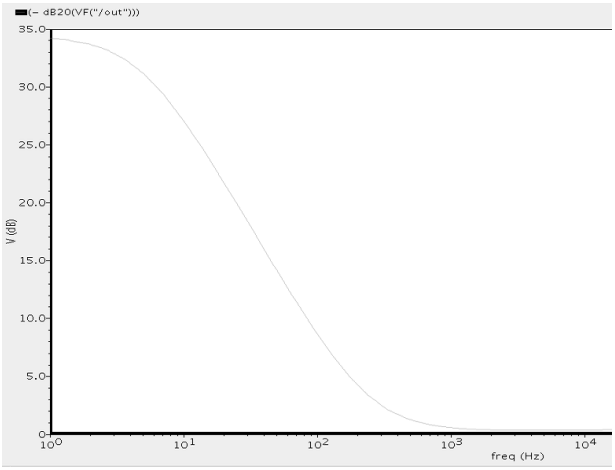

Figure 13: Gain Plot of Simulation of parasitic sensitive SC integrator

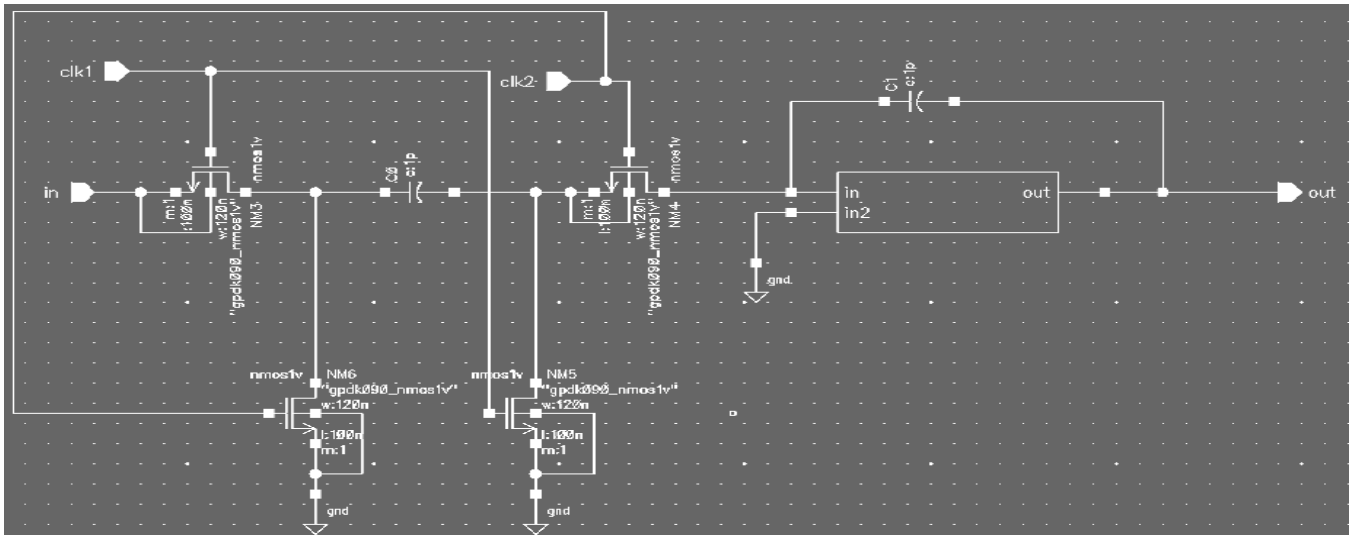

Figure 14: Parasitic Insensitive SC Integrator

The simulation result of parasitic insensitive SC integrator is shown in Figure 15 and Gain plot is shown in Figure 16.

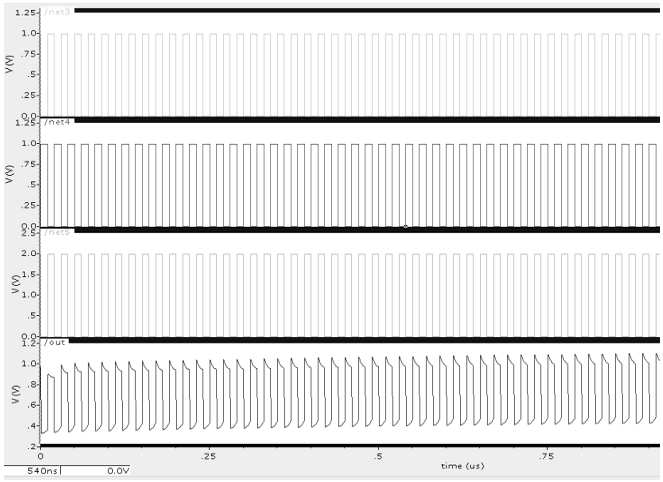

Figure 15: Simulation of parasitic insensitive SC integrator

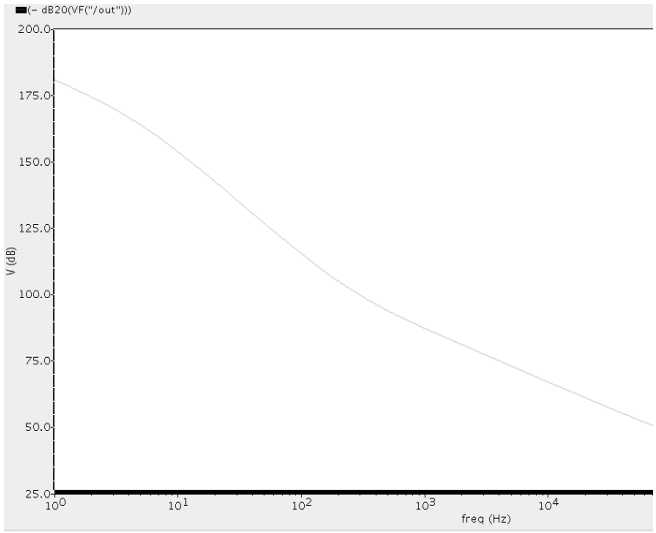

Figure 16: Gain Plot of Simulation of parasitic sensitive SC integrator

The gain comparison for both parasitic sensitive SC integrator (Figure 11) and parasitic insensitive SC integrator (Figure 14) are shown in Table 2. The parasitic sensitive SC integrator has a gain of 34dB and insensitive SC integrator has a gain of 178dB.

TABLE II
GAIN RESULTS COMPARISON

Parameters	Parasitic sensitive SC integrator	Parasitic insensitive SC integrator
Gain	34dB	178dB

CONCLUSIONS

The Switched Capacitor based parasitic sensitive integrator and parasitic insensitive integrators are designed and analyzed by using Cadence ICFB full custom design suite using 90nm technology.

The SC integrator circuits basic building block two stage op amp circuit is designed for simple compensated features using 90nm technology with L=100nm.

The Switched Capacitor based parasitic sensitive integrator is designed for a gain of 34dB and parasitic insensitive integrators are designed and achieved a gain of 178 dB.

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Hazards and Glitch Power Reduction of CMOS Full Adder in 90nm Technology

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Abstract — **In This paper we discuss the glitch and hazard power compensation techniques which involves reducing the undesired switching of combinational circuits in order to save the dynamic power for CMOS stander cell designs in 90nm. In nanometer CMOS technologies the power consumption is become a serious concern. The total power consumption is mainly due to the dynamic and leakage power consumptions. In CMOS circuits a glitch occurs when differential delay at the inputs of a gate is greater than inertial delay, which gives an amount of power consumption. In lower technology nodes this glitch power is a major prominent. Experimental results gives 12% to 50% reduction in top 10 peak undesired transition. The proposed methodology has been validated using cadence 90nm gpdk technology libraries.**

Index Terms—**CMOS, Full Adder, Glitch, BTBT, Path Filtering, Sizing.**

I. INTRODUCTION

In a digital CMOS circuits there are three sources of power dissipation. The first is due to signal transitions. As the "nodes" in a digital CMOS circuit transition back and forth between the two logic levels, the capacitance associated with the nodes get charged and discharged. Heat dissipation in the channel of the transistors due to the current flows and electrical energy through the channel of the transistors gets converted into the heat. This portion of heat dissipation is proportional to the supply voltage. Given that the voltage swing in most cases is simply equal to the supply voltage, the power dissipation due to transitions varies over all as the square of the supply voltage.

The second source of power dissipation comes from the short-circuit currents, When the P-network and N-network of a CMOS gate conduct simultaneously then the short-circuit current flows directly from the supply to the ground. However, when the input of a gate changes the output response of the gate is also switches, so both subnetwork conduct simultaneously for a small interval. The duration of interval depends on transition (rise or fall) times of the input and the output and so does the short-circuit dissipation. The power dissipation in CMOS circuits are related to transition (rise or fall) times at gate outputs and are therefore collectively referred to as dynamic power dissipation.

The third and the last source of dissipation is due to the leakage currents, which flow when the inputs to and, therefore, the outputs of a gate are not changing and is called static power dissipation. One of the reasons CMOS circuits are in widespread use is that the only static dissipation in standard CMOS circuits is due to leakage currents and magnitude is very small usually. But to reduce dynamic power as long as the supply voltage is being scaled down, to maintain performance low threshold voltage transistors to be used, yet the lower the threshold voltage, the greater the standby leakage current. The reasons for such behavior of transistors will be explained in the in the following.

II.BACKGROUND

At the macro-chip level, the most significant trend is the increasing leakage power contribution in the total power dissipation of an IC design in CMOS technology. For a long time, the dynamic power was the major component of the total power dissipated due to the switching component by a circuit. However, in order to maintain power dissipation and power delivery costs under control, the supply voltage 'Vdd' was scaled down at the rate of 30% per each technology generation. In conjunction, to improve the performance of transistor and circuit the threshold voltage Vt was also reduced at the same rate, so that a large gate overdrive (V_{dd} -) is maintained. However, transistor sub-threshold leakage current (I_{sub}) is increase exponentially because of reduction in Vt. Furthermore, other components of leakage current, e.g., reverse-biased junction, Band To Band Tunneling (BTBT) and the gate leakage become important as we scale fabrication technology to 90nm and further. In other hands such as gate-induced drain leakage(GIDL) and drain-induced barrier lowering (DIBL) will also become increasingly significant.

Another dimension of drawback is added by the fact that unlike dynamic power, leakage power increases exponentially with temperature. We have been continuously scaling the supply and threshold voltages In order to improve performance. While this results in high frequency of operation, temperatures rise due to large active power consumption. Further increasing temperature there is a strong function of temperature. This circular situation is depicted in Fig.1. A positive feedback between leakage power and temperature can result in thermal runaway, if heat cannot be dissipated effectively. Such a situation can have disastrous consequences, including permanent physical damage of the circuit, the processor if the temperature increases beyond safe limits most processors are now equipped with thermal sensors and hardware circuitry that will stop.

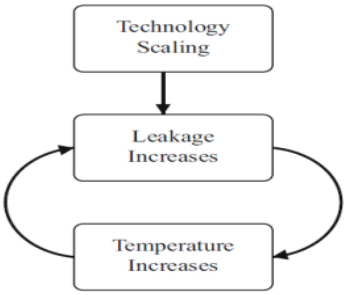


Figure.1. Leakage increases exponentially with the temperature.

A. *DYNAMIC POWER*

The dynamic power dissipation in a CMOS gate is due to the charging and discharging of load capacitance driven by the gate. This capacitance consists of internal capacitances of the gate, wire capacitance of the fanout net and the capacitance of the gate terminals of the transistors being controlled by the fanout net. This power dissipation can be calculated by the following equation(1).

$$P_{dyn} = \frac{1}{2} C_{load} V_d^2 \text{ ……..(1)}$$

Where

- P_{dyn}: dynamic power dissipation of gate,
- C_{load}: load capacitance of the gate,
- f:clock frequency & V_{dd}: supply voltage,
- D: transition density of the output of the gate.

The transition density is the average number of transitions during a clock cycle. The dynamic power dissipated is thus proportional to the number of transitions occurring at agate. Thus, an accurate estimation of the transition density in a circuit will give an accurate estimation of the dynamic power dissipated in the circuit. In earlier technologies, dynamic power accounted for most of the power used by CMOS circuits. But with the advent of deep sub-micron technology of the other components of consumption are also becoming significant. However, several low power techniques have concentrated on minimizing dynamic power, as will be explained later. Dynamic power can be classified into necessary transition due to unbalanced paths in the circuit. The latter component of dynamic power dissipation is the glitch power and is elaborated in the next section.

B. *HAZARDS AND GLITCH POWER*

In a digital circuit signals before to reach steady state, gates can have multiple transitions. Since the power dissipation is directly proportional to the number of transitions, these necessary transitions increase power consumption. These undesired transitions power dissipation are called glitch power or hazards. Glitches are produced in a digital CMOS circuit due to the difference in signal arrival times at the inputs of the gates. Power dissipated by glitches is called glitch power and it typically about 20% of the overall power consumption of the chip and even 70% in some typical cases as the combinational adder[4].

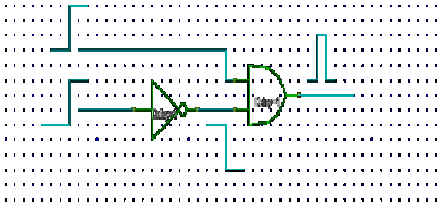


Figure.2. An example of static hazard

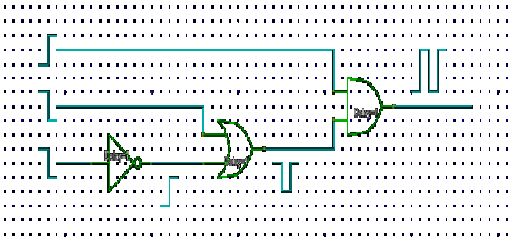


Figure.3. An example of a dynamic hazard

Consider the example of fig.2. with each gate having one unit of delay due to the difference in arrival time of signals at the inputs of the AND gate the logic value glitches or emits a pulse of 1 unit width, which equals the inverter delay. This known as static hazard, In fig.3. the OR gate produces a static hazard of 1 unit. The transient consists of three edges, two rising and 1 falling. This is a dynamic hazard with a combined width of 2 units.

The number of arriving signals at the gate is may equal to the number of edges in transients at the output of a gate. The maximum width of the possible glitch at the circuit output and also the maximum difference in arrival time of signals at the inputs of gate is called differential path delay. A hazard producing gate has more than one input and has non-zero differential path delay. Every gate has a internal delay due to the finite switching speed of the transistors. It is the time a device takes to switch the output after the cause for the change has occurred at the input[5]. Inertial delay plays a major role in distorting glitches produced at the gates and in the next section we present ways of eliminating glitch by either making the differential path delay zero or by increasing the inertial delay of the gate.

III.EXISTING TECHNIQUES

A. *PATH BALANCING*

Path balancing is one of the earliest works that targeted glitch power reduction. The glitches are proposed due to difference in arrival time of signals at gat inputs. The idea behind this technique is to prevent glitches from occurring by balancing the delays of paths such that at any given gate the signals arrive at its input terminal at the same time. Consider the example circuit shown in fig.4, This signals at the inputs of the gate arrive at different times which would probably results in glitches. This behavior can be suppressed by resulting the circuit as shown in fig.5. However, as next example illustrates, a simple resulting of gates may not be sufficient for some circuits.

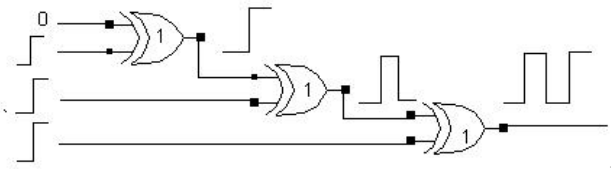


Figure.4. Glitching behavior of an ill-structured circuit

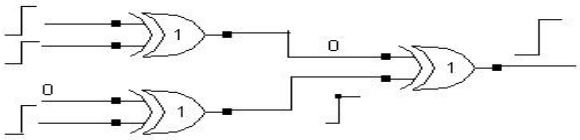


Figure.5. Removal of glitches after restructuring of the circuit in fig.4.

A method of balancing delay for circuit by the inserting buffers at selected inputs of the gates. The addition of buffers is done such that it will not increase the critical delay, but will effectively eliminate spurious transitions. The buffers are inserted only in the fast paths of the circuit and since the slowest paths determine the speed of the chip they are left untouched. The circuit in fig.6 cannot be path balanced without the introduction of buffers as shown in fig.7. However the addition of buffers increases the switching activity of the circuit which may offset the reduction in power due to elimination of glitches.

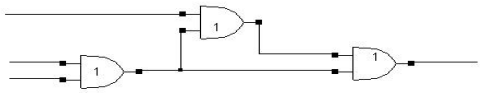


Figure.6. Glitching behavior of a circuit where simple restructuring will not balance paths.

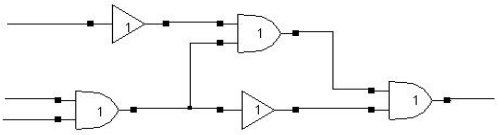


Figure.7. Path balancing of a circuit in fig.6. by buffers.

In CMOS circuits the fanout load significantly affects the gate delay. To account for this developed a delay buffer insertion procedure using a chain of buffers, thus eliminating the need for merging the common delay of all the faout branch buffers into the corresponding fanout stem buffer. The problem of delay buffer insertion on a multiple fanout net simplified by assuming that only one size of delay buffer is used. This method permits a quick estimation of the number of buffers needed to balance the circuit and can therefore be usedin heuristics for logic restructuring.

B. HAZARD FILTERING

This method eliminates glitches in the circuit using inertial gate delays. Inertial delay is the interval that elapses after an input change before a gate can produce an output change. When the time between successive edges in the input signal is less than the inertial delay of the gate, the effects of these edges are suppressed. This is known as filtering effect of the gates [5]. CMOS gates have a built-in delay called the inertial delay of the gate and they suppress signals that are of smaller width than the inertial delay from passing through the gate. This is known as the filtering effect of the gate. Instead of balancing the delays of the gate inputs to be exactly equal, this method evaluates the differential delay of inputs and increases the inertial delay of the gate exceed the differential delay such that the glitch will be suppressed within the gate.

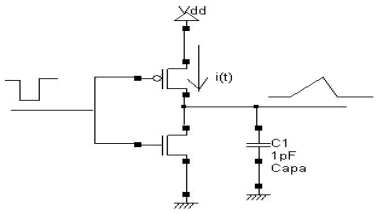


Figure.8. Energy dissipation in an inverter

Consider the example inverter shown in Figure.8 with the total capacitance at the output node as C and the short circuit impedance R. when an input pulse as shown is incident at the input, a charging current i(t) flows through the upper transistor charging the capacitor C. This charging raises the output voltage until time t=τ when the rising edge occurs at the input. The energy consumed by the gate is

$$E(\tau)=CV_{dd}^2\left(1-e^{-\frac{\tau}{RC}}\right) \quad \ldots\ldots\ldots(2)$$

For hazard filtering, we increase the time constant RC of the gate and thus increase the charging time needed for the capacitor reach Vdd. When the time constant is large, there is practically no energy dissipation in the gate due to the short glitch of length τ. Energy dissipation for various values of the time constant with respect to the width of the pulse τ is given in above equation(2).

A simulated example of a full adder circuit showed that the method reduced power by 42%. The glitch- free circuits had gates whose speed was decreased to 20% of their original speed but with very little reduction in overall speed of the circuit. This was because those gates were mainly on non-critical paths and so did not contribute much to the critical path delay of the circuit.

C. GATE SIZING

Gate sizing is defined as assigning load drive capabilities to the gates of a network, such that a given delay limit is obeyed, and the total minimal cost in terms of power consumption[5]. Similar to the hazard filtering technique, this method also uses the filtering effect of the gates but achieves the increase in inertial delay by resizing the gates in the circuits. The delay model frequently used for solving this problem is as shown below [5]:

$$\tau_{gate} = \tau_{int} + c\,C_{load} \quad \ldots\ldots(3)$$

$$C_{load} = C_{wire} + C_{in} \quad \ldots\ldots\ldots(4)$$

where

- τ_{gate} : Delay of the gate
- τ_{in} : Internal delay of the gate
- C_{load}: Capacitive loading experienced by the gate

- C: A constant
- C_{wire}: Routing capacitance of the output net of the gate
- C_{in}:capacitive loading due to gates in the fanout cone

Berkelaar and Jacobs [9] use a parameter called the speed constant to reformulate the delay model but this converts the problem into non-linear domain. Berkelaar et al. [8] have tried to solve the near-LP problem with the use of a piecewise linear simulator ad have published results for all ISCAS benchmark circuits. This method was found to be faster than the LP method for circuits with less than 1000 gates but was not very useful for larger circuits. Berkelaar and Jacobs [9] have tried to formulate the gate sizing problem as an LP problem but the non-linear structure of their delay model posed problems in finding the global optimum solution. The details of this are dealt with in the next sections.

Berkelaar and Jacobs [9] have tried gate sizing under a statistical delay model but the resulting problem was a non-linear problem that caused their program to consume considerable time and resources. Also, this method could not be used for circuits with more than 1000 gates.

D. TRANSISTOR SIZING

Transistor sizing similar to gate sizing but the essential difference is that in gate sizing all the transistors of a gate are sized together but in transistor sizing each transistor can be sized independently. Traditionally, transistor sizing is done to reduce the area and delay of a VLSI chip.

Data et al. [10] have considered static CMOS circuits transistor sizing for low-power and high performance. To obtain a better power and delay performance the transistors on the critical paths of the circuit are scaled size. In the circuit block to improve the switching speed and the output transition characteristics of a particular circuit block on the critical path one may seek to increase the widths of the transistors. This results in an increased current drive and better output transition time. A transition time implies lower rush-through current for faster input/output, hence smaller short –circuit power dissipation. It is to be noted, however, that even through the delay of a particular block and its succeeding block are reduced, an increase in transistor widths increases the capacitive loading of the preceding block and may severely affect its power and delay. Thus, the issues regarding delay and power dissipation are fairly inerter linked. The algorithm described [10] minimizes the delay. The area and the power dissipation of a circuit by optimizing the sizes of the gates on the critical paths of the circuit However. The constrant set for this model becomes non-linear and hence the solution for large circuits becomes tedious and complex.

E. LINEAR PROGRAMMING (LP) APPROACH

A linear program determines a set of variables such that an objective is minimized under given constraints.To eliminate the glitching power from a circuit the inertial delay of the gate has to be alerted as dictated by a hazard filtering technique. But the altering has to be done without affecting the critical path of the circuit and also taking into account the change in delay of the gates in the fanout cone whose delay will effect the delay of the gate in question. There can be infinite number of solutions and finding a global optimum makes this problem an optimtization problem. The linear programming model guarantees the global optimum for every feasible solution of the problem.

A variety of LP models have been investigated to express the glitch removal problem. This have described a gate level model to express the problem. The variables consist of inertial delays of gates in the circuit and also delays of buffers that may need to be inserted in the circuit for complete glitch removal. The constraints are written by path enumeration from the gate inputs to the primary inputs (PIs). Hence, the number of constraints grows exponentially with the size of the circuit. In the mathematical model proposed by Berkelaar et al.[9] the gate delays were described at transistor level. This introduced some no-linearity in the model which increased the complexity and decreased the accuracy of the solution. Another linear programming technique has been proposed by Raja et al.[4]. This is a gate level mathematical model whose constraint set grows linearly with the size of the circuit. Hence, this technique has been proven to be applicable to large circuits also. This detail of this linear program is given below.

IV. CMOS FULL ADDER CIRCUIT

To process the fundamental arithmetic operations addition is an obligatory operation. It is widely used extensively in many VLSI design paradigms and is by far the most frequently used operation in a general purpose system and in application specific processors. Addition is often seen as an indispensable part of the arithmetic unit. It is dubbed the heart of any micro-processor, DSP architecture and data processing system.

In arithmetic operation it usually involves a carry ripple step which must propagate a carry signal from each bit to its higher bit position, so addition is a very crucial operation. This results in a substantial circuit delay. Therefore, which lies in the critical delay path, effectively determines the system's overall speed. On the other hand, the operation of reducing the power consumption of the designed adder, which for many years has been a narrow specialty, has recently been gaining prominence. This can be attributed to the emergence and increasing popularity of smaller and more durable mobile computing and communication systems. Low power dissipation allows a portable system to operate longer with the same battery.

A full adder adds two binary numbers with a carry-in. The structure representation of the conventional CMOS full adder appears in fig.9. It is constructed of the two HA's and an OR gate. There are a total of three inputs for the FA, two for the input numbers A and B, and one for the carry-in, Cin. The outputs are the sum and carry-out. According to the truth table of FA, the logic function corresponding to terminals SUM and CARRY OUT are as follows

SUM=A xor B xor Cin ……..…...(5)

Cout = (A xor B) . Cin + A . B ……(6)

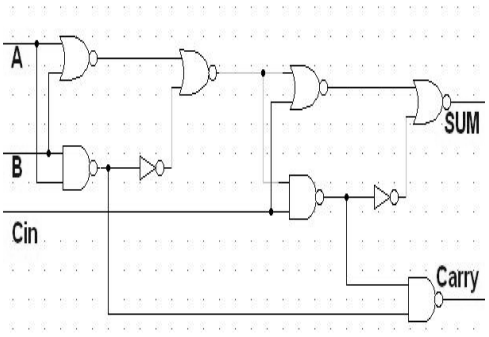


Figure.9. Logic circuit of the conventional full adder.

The SUM (S) output has been generated using two XOR gates. The XOR function is obtained using a pass transistor-based XNOR gate followed by an inverter to restore the logic levels. For generating the carry output, transmission gates have been used instead of single pass transistors to pass inputs A or C_{in}. This resulted in improved logic levels at the output of the transmission gate leading to fully restored logic level at C_{out} and fig.10 shows the circuit diagram of proposed full adder. In practical digital circuits, a functional block is driven through a gate / inverter and is required to drive a gate. The design of a digital circuit, therefore, should be tested with inputs applied through an inverter and another inverter / gate connected as load. The circuit in fig.10 was tested with inputs applied through inverters and similar inverters connected as load. Both the input and load inverters are included in the circuit diagram. The optimum performance of the circuit in terms of speed, fully restored logic levels was obtained by choosing appropriate geometry of individual MOSFET. The pMOS and nMOS transistors used in the inverters have (W/L) ratio of (5/2) and (3/2), respectively. Inverters used in the full adder are also of same type. All transistors in XNOR gates have (W/L) of (6/2). The pMOS and nMOS transistors used in transmission gates have (W/L) of (6/2) and (3/2), respectively.

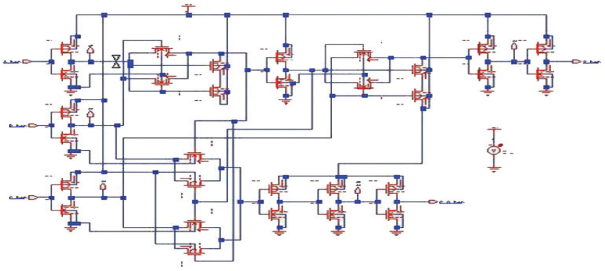
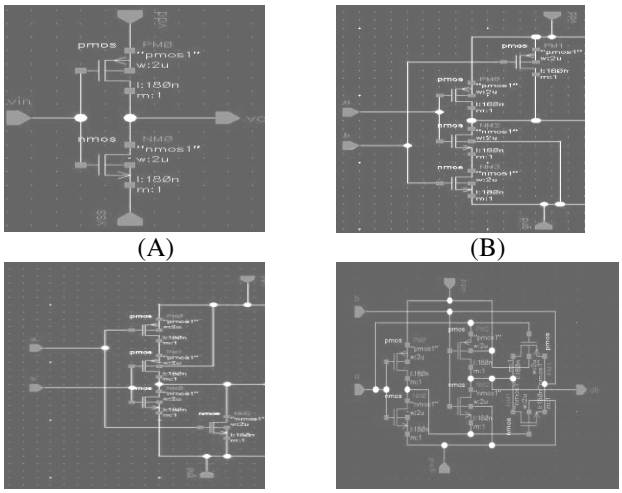


Figure.10. 20-transistor Full Adder circuit

V. SIMULATION RESULTS

Here the present paper is aim to be to reduce power and delay parameters. Cascading of two 1 bit half adder circuits implements a full adder. In order to build transistor level adder, the idea is to begin with the basic gates. So as to reduce the circuit area, power dissipation and propagation delay each individual logic gate used in the circuit is constructed by minimum transistors. The performance criteria of each gate is individually investigated and analyzed for the full adder as shown in Fig.9.

The implementation consists of four types of logic gates such as Inverter, 2-input NAND gate, 2-input NOR gate and may be 2-input XOR gate is also used. The schematic of all the Logic gates implemented using CMOS 90nm technology is shown in Fig.11 below.



(A) (B)

(C) (D)

Figure.11. Schematic of (A) Inverter (B) 2-Input NAND gate (C) 2-Input NOR gate (D) 2-Input XOR gate.

Here both proposed and conventional full adder to show the reduced transistor count & both full adders are implemented in the cadence tool as shown in fig.12 and fig.13.

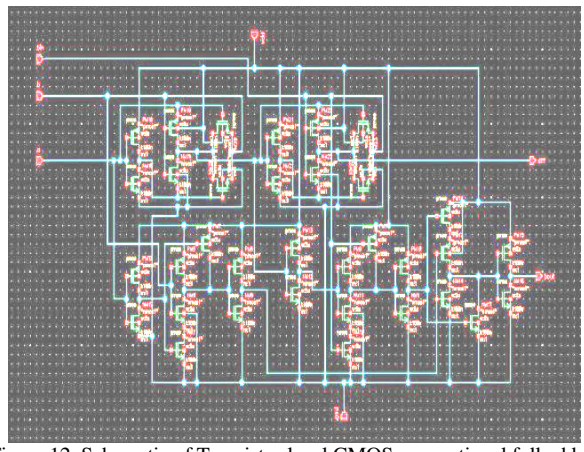


Figure.12. Schematic of Transistor level CMOS conventional full adder.

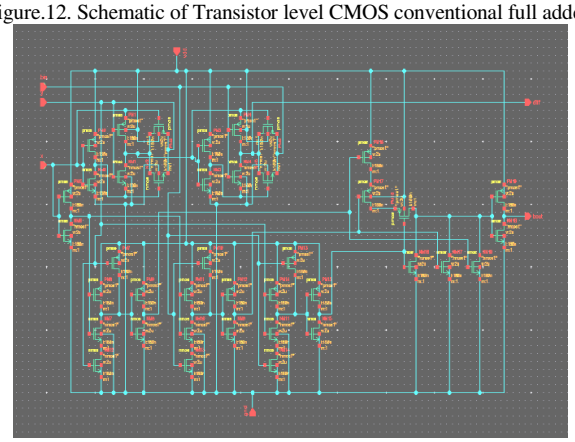


Fig.13. Schematic of Transistor level CMOS Full Adder with minimum glitches

TABLE.I:
PERFORMANCE OF LOGIC GATES IN 90NM

LOGIC GATE	Propagation Delay	Power Dissipation
NOT	7ps	18µW
NAND	14ps	25 µW
NOR	13ps	23 µW
XOR	20.4ps	28 µW

TABLE.II
PERFORMANCE OF FULL ADDER IN 90NM

PARAMETER	CONVENTIONAL FULL ADDER	GLITCH FREE FULL ADDER
Propagation Delay: A to S	110ps	250ps
Propagation Delay: B to S	100ps	140ps
Propagation Delay: C to S	80ps	100ps
Propagation Delay: A to C_0	120ps	220ps
Propagation Delay: B to C0	100ps	120ps
Propagation Delay: C to C0	60ps	120ps
Power Consumption at 500MHz (µW)	94.5	50.7

It can be seen that the output logic levels are fully restored and are free of glitches. The each path propagation delay, and power dissipation as determined are given in Table.II. The conventional full adder path delay is more than compared to the glitch free full adder because to remove the glitches in each path by balance path delay to occur inputs of all gates/transistor at same time. The power consumption was determined by multiplying the power supply voltage with average current drawn from the power supply, the power consumption mentioned in the Table.I and Table.II. The response characteristics such as propagation delay and power dissipation were computed using cadence tool using 90nm technology libraries.

CONCLUSIONS

Unfortunately, the power density increased prominently as a consequence, glitches or hazards are expected to result in further increases in power density for technology node below 90nm. This paper summarized some of the contributions made to reduce glitch power in CMOS digital circuits. A new 20-transistor full adder circuit has been implemented in 90nm technology. In this work different skills and techniques were gained, applied in a fundamental part. Indeed. This full adder is able to design, implemented and successfully analyzed the characteristics. The completion of this task was satisfactory since the theoretical expectations matched with experimental results. This full adder offers better performance than the other full adder circuits (implemented in same technology) reported in the literature. This design is particularly suited for use in a binary multiplier circuit where a number of full adder circuits need to be cascaded. Any logic level degradation in such application would adversely affect the speed of the multiplier. The performance of the full adder was assessed in terms of area, speed and power consumption, also quality of the output signals by comparing the timing measurements of each basic gate.

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Evaluation of Image Inpainting Algorithms

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Abstract- **Image inpainting is a technique to repair damaged images or to remove/replace selected regions. It was used to repair old artwork and also a part of movie special effects. This paper presents review of many successful algorithms for image inpainting which are Texture based algorithms, Diffusion(PDE) based algorithms, Exemplar and search based algorithms and Sparsity based algorithms. Here an evaluation of two classes of algorithms: Partial Differential Equations (PDEs) based algorithms and Exemplar-Based algorithms are presented. The results show the advantages and disadvantages.**

Index Terms- **Image inpainting, PDEs-based algorithm, Exemplar-based algorithm.**

I. INTRODUCTION

Image inpainting is the technique of filling in the missing regions of an image using information from surrounding areas. In image inpainting, the missing region is often referred to as hole, and is usually provided by the user in the form of mask or can be obtained by automatic or semi-automatic means. Some of the earlier nomenclature referred small region filling as inpainting and large area inpainting as image or video completion. In this work however, we do not make any such distinctions and these techniques are commonly referred as Digital Image and video inpainting algorithms. Digital inpainting has found widespread use in many applications such as removal of undesired objects and writings on photographs, restoration of damaged old paintings and photographs, transmission error recovery in images and videos, computer-assisted multimedia editing and replacing large regions in an image or video for privacy protection. The inpainting means a technique is to modify the damaged portion or region in an image or video. Then the inpainted region is undetectable to a neutral observer is described in [1]. The objective of image inpainting is to reconstitute the damaged portions or regions of the imge, then that image is more legible and restore its unity. Based on the context of operation, the goal of the inpainting can range from making the damaged image or video appear as close to the original to completely providing an alternate completion which is virtually unnoticeable to human observer.

Image inpainting is an ill-posed inverse problem that has no well-defined unique solution. To solve the problem, it is therefore necessary to introduce image priors. All methods are guided by the assumption that pixels in the known and unknown parts of the image share the same statistical properties or geometrical structures. The first category of methods, known as diffusion-based inpainting, introduces smoothness priors via parametric models or partial differential equations (PDEs) to propagate (or diffuse) local structures from the exterior to the interior of the hole. Many variants exist using different models (linear, nonlinear, isotropic, or anisotropic) to favor the propagation in particular directions or to take into account the curvature of the structure present in a local neighborhood. These methods are naturally well suited for completing straight lines, curves, and for inpainting small regions. These are not well suited for recovering the texture of large areas, which they tend to blur.

The second category of methods is based on the seminal work of Efros and Leung [2] and exploits image statistical and self similarity priors. The statistics of image textures are assumed to be stationary (in the case of random textures) or homogeneous (in the case of regular patterns). The synthesis is taken place by learning process for texture from the known part of the image or from similar regions in a texture sample. The Learning process is done by sequentially with starting of sampling, and by copying or stitching together patches (called examplar) taken from the known part of the image. The corresponding methods are known as examplar-based techniques. With the advent of sparse representations and compressed sensing, sparse priors have also been considered for solving the inpainting problem. The image (or the patch) is in this case assumed to be sparse in a given basis [discrete cosine transform (DCT), or wavelets]. Known and unknown parts of the image are assumed to share the same sparse representation. Examplar-based and sparse-based methods are better suited than diffusion-based techniques for filling large texture areas. Hybrid solutions have then naturally emerged, which combine methods dedicated to structural (geometrical) and textural components.

II. IMAGE INPAINTING TECHNIQUES

In this section, the different image inpainting techniques and corresponding approaches are explained.

A. Texture synthesis based inpainting

The texture synthesis based inpainting is one of the earliest modes of image inpainting methods. This method was use to complete the missing regions in general texture synthesis algorithms. The texture synthesis methods are use to synthesize new image pixels from an initial seed picture or video and strive to preserve the local structures

of the image. To fill the holes by sampling and copying pixels from neighboring areas, earlier inpainting techniques utilized these methods only [2-7]. In [2], A Markov Random Field (MRF) is used for the synthesis of textures. This MRF method is used to model the local distribution of a pixel and new texture of the given image. It is synthesized by querying existing texture and finding all similar neighborhoods in the image. Their differences lay mainly in how continuity is maintained between the existing pixels and the inpainted hole. These querying synthesis based methods perform good only for a select set of images where completing the hole region with homogenous texture information would result in a natural completion.

Next this work was extended to a fast synthesizing algorithm[3]. In this algorithm, the new technique is introduced that is referred as image quilting. This technique is used to stitching together small patches of existing images. The authors, Heeger and Bergen was developed a new synthesizing technique i.e a parametric texture synthesis algorithm. This algorithm is used to synthesize a matching texture and given target texture [5]. This synthesis was done by matching the first order statistics of a linear filter bank. This filter bank roughly match to the texture discrimination capabilities of Human Visual System (HVS). Igehy et.al included a combined step to the above synthesis method to generate synthetic and real textures [7]. Yamauchi et.al introduced a multi-resolution texture synthesis method for image inpainting. This method can generate texture under varying brightness conditions[8]. Recently, Fang et.al introduced a fast multi-resolution based for image inpainting which is image completion based on texture analysis and synthesis[9]. In their method, a patch based method using Principal Component Analysis (PCA) was used to analyze the input image and to speedup the matching process a Vector Quantization (VQ) based technique was used for the texture inside the hole region. To create textures, so many texture synthesis methods discussed here and comparison taken place for different statistical characteristics of those methods and to generate textures under gradient, color or intensity variations. The texture synthesis based inpainting methods perform very well in approximating textures in the images. But these methods have difficulty in handling natural images as they are composed of structures in the form of edges. These methods have the problem of complex interactions between structure and texture boundaries. Sometimes they also require the user to mention what texture to be replaced. Hence we conclude that these methods can use to solve small subset of image inpainting issues only and these methods may not suitable for a wide variety of image inpainting applications.

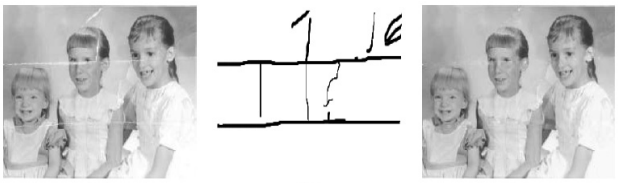
B. Partial Differential Equation (PDE) based inpainting

Bertalmio et.al proposed a iterative algorithm which is based on Partial Differential Equation (PDE) [10] given the way for modern image inpainting. Figure 1 shows the result these algorithm for damaged images.

This iterative process propagates linear structures (edges) of the surrounding area by using the ideas of manual inpainting also called Isophotes, into the hole region denoted by Ω, using a diffusion process. This diffusion process is given by

$$I^{n+1}(i,j) = I^{n}(i,j) + \Delta t \cdot I_t^{n}(i,j), \forall (i,j) \varepsilon \Omega \quad \text{---- (1)}$$

Where Δt is the rate of the change of inpainting, (i, j) are pixel co-ordinates, n is the iteration time, $I_t^n(i,j)$ is the update factor on the image $I^n(i,j)$.



(a) (b) (c)

Figure 1: Digital image inpainting Example : (a) Original Image (b) Hole or Damaged regions in the form of mask. (c) The proposed algorithm Inpainted image in[10].

The Laplacian operation is applied to obtain a smoothed image update factor in the above equation in the direction perpendicular to the gradient in an iterative fashion. The following equation represents the PDE form of the above process.

$$I_t = \nabla(\Delta I).\nabla^{\perp} I \quad \text{---------} \quad (2)$$

where $\nabla(\Delta I)$ is the Laplacian smoothness operation on the gradient and $\nabla^{\perp} I$ is the isophote direction. For the replication of large textured regions, this technique underperforms in due to blurring artifact of the diffusion process and this technique lack of explicit treatment of the pixels on edges of the images. This problem is treated as main drawback in this technique. Based in this work, the Total Variational (TV) inpainting model was proposed by Chan and Shen which uses Euler-Lagrange equation and anisotropic diffusion based on the strength of the isophotes [11]. Let E be the adjoining region and D be the inpainting region around the hole, a function u found by the variational inpainting model on the ex-tended inpainting domain adjoining the hole boundary $E \cup D$, such that under the denoising constraint on E, it minimizes a regularity functional $R(u)$. The function $R(u)$ is given below:

$$R(u) = \int_{E \cup D} r(|\Delta u|) dx dy \quad \text{------} \quad (3)$$

where r is an appropriate nonnegative real function for nonnegative inputs.

This technique neither creates texture patterns nor connects broken edges. But it performs well for noise removal applications and small regions. The Total Variational (TV) model was extended to Curvature Driven Diffusion model (CDD) in [12]. This model included the

curvature information of the isophotes to handle the curved structures in a better manner. The vector valued regularization under anisotropic diffusion framework was introduced by Tschumperle et.al [13] which one of the PDE based technique. Mainly these algorithms were focused on maintaining the correct structure of the inpainting area only and due to blurring artifacts these method could not perform as well in texture filling.

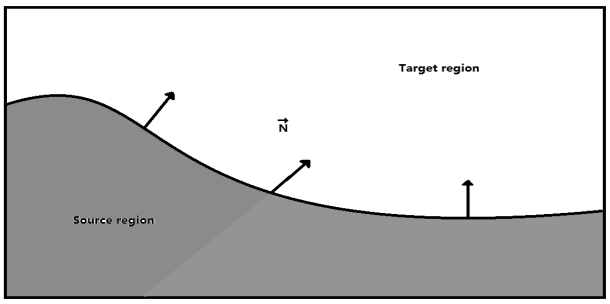


Figure 2: An image with source region, target region and vectors N. (By Sheng Li)

In Figure 2 gives the target region, source region and vectors. For propagate information from source region to target region, compute its change along the $\vec{N}$ directions. The $\vec{N}$ is the direction of smallest spatial change. Keep doing this, until reach the boundary of target region.

C. Exemplar and search based Inpainting

If the inpainting regions are large, then the mathematical method may not be suitable. So exemplar-based inpainting is the better choice for them. An algorithm based on texture-exemplar inpainting was introduced by Criminisi et al [14]. Extension of texture synthesis methods as a way to fill in large regions with pure textures repetitive two-dimensional textural patterns with some stochastically. There are some other algorithms for texture synthesis, such as, stochastic texture synthesis, pixel-based texture synthesis and patch-based texture synthesis. The damaged region is filled by copying color values from the neighborhood. Patch-based (exemplar-based) technique is a part of texture synthesis, it is more cheaper and effective than others. Criminisi et al [14] presents a novel and efficient algorithm that combines the "texture synthesis" algorithms generating image regions from sample textures and inpainting techniques that fill the small image gaps. This algorithm described as follows:

1. Determine the parameters of algorithm. A user selects a target region, Ω, to be restored. So the source region Φ is entire image minus the target region. Then the size of exemplar texture ψ. Those template textures called patches that contain a color value and a confidence value, which determines a pixel has been filled.

2. Compute patch priorities $P(p)$. The algorithm performs a best-first filling algorithm that determines the priority of every pixel. The priority is given as first the product of confidence term $C(p)$ and second is data term $D(p)$.

1) $P(p) = C(p)D(p)$

2) $C(p) = \dfrac{\sum_{q \varepsilon \psi p \cap \Omega} C(q)}{|\psi p|}$

3) $D(p) = \dfrac{|\nabla Ip \cdot np|}{\alpha}$

3. Propagate texture and structure information. To find the best matches texture, the SSD (the sum of squared differences) of position of these patches is the measure. When the best one is found, propagate the information to the fill region.

4. Update confidence values. After filling the patch, the confidence of the patch is updated.

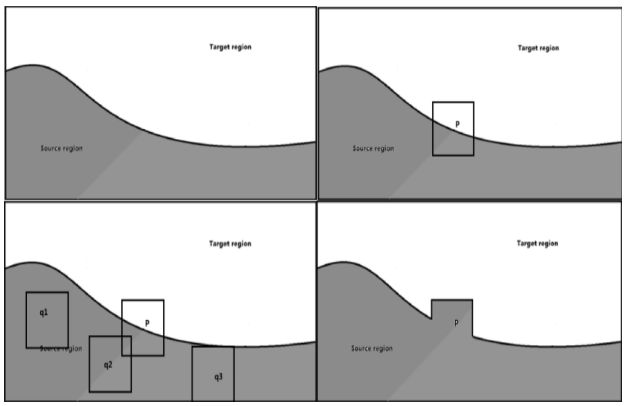


Figure 3: An example of exemplar-based algorithm. (By Sheng Li).

Figure 3 shows a single process of exemplar-based algorithm. The top-left one is the original image, the top - right one has a patch P. The bottom-left one has three patches P1, P2 and P3. In the bottom-right, the patch P be restored.

C. Patch Sparse Representation for inpainting

In this section ,we use a sparse linear combination of examplars to infer the patch in a framework of sparse representation to inpaint a selected patch on the boundary of missing region. Next, the regularization is taken place through linear combination of patches by the sparseness prior (regularization) on the combination coefficients. By this regularization technique only very few examplars contribute to the linear combination of patches with nonzero coefficients. This representation of patches is called patch sparse representation.

This sparse representation model extends the patch diversity. The patch diversity preserves texture without introducing smooth effect by sparseness assumption. Finally, the patch sparse representation and structure sparsity at the patch level constitute the patch sparsity. The patch structure sparsity is related to natural image which is inspired by the recent progress on the research of sparseness prior of natural image inpainting. However, it models the sparseness of nonzero similarities of a patch

with its neighboring patches instead of high-frequency features.

The previous sparseness prior generally models the sparseness of image's nonzero features, e.g., filter responses or gradients. This kind of method has been applied to the denoising of the image, super-resolution, inpainting, deblurring of the images and so on. The recent progress on sparse representation, which assumes that the image is represented by the sparse linear combination of an over-complete library of bases or transforms under sparseness regularization. This work has been widely applied to denoising of the images, recognition, edge detection, super-resolution, texture synthesis, etc., and finally achieves the performance of the state-of-the-art. In this work, the exampler- based inpainting method and sparse representation idea was combined under the assumption that the missing patch can be represented by the sparse linear combination of candidate patches. Then a optimization model is designed for patch inpainting for the given natural images.

D. Hybrid digital inpainting

In the hybrid digital inpainting the texture synthesis and PDE based inpainting methods are combined for completing the holes. The main idea behind these hybrid approaches is to decompose the image into separate texture region and structures. Then the corresponding decomposed regions are filled by texture synthesis techniques and edge propagating algorithms respectively[15-17]. If the fill region is large, then these algorithms are computationally intensive. The important direction for the general inpainting process is by structure completion through segmentation. This approach consists of two-stages: the first stage is the structure completion stage. In this structure completion stage, segmentation, using the algorithm of [19], is performed based on the insufficient geometry, color and texture information on the input and the partitioning boundaries are then extrapolated to generate a complete segmentation for the input using tensor voting [20] followed by texture synthesis. The second stage consists of synthesizing texture and color information in each segment, again using tensor voting.

III. RESULTS & COMPARISION

To compare PDEs algorithm and exemplar-based algorithm, the processing time, memory usage and the quality of result are three main aspects.All these three images, the two algorithms have been applied. For different image with different situation, the result shows the difference between those two algorithms. The A image has two different grayscale parts, the inpainting region is connection part. The B image is a wall with windows. The mission is repaired a half window. The last one C as the same as B, but the objective is to remove the window. The A image tested the inpainting of simple geometry image. The B image show the restoration of image with a complex background. The C image will be removed a big object with simple background.

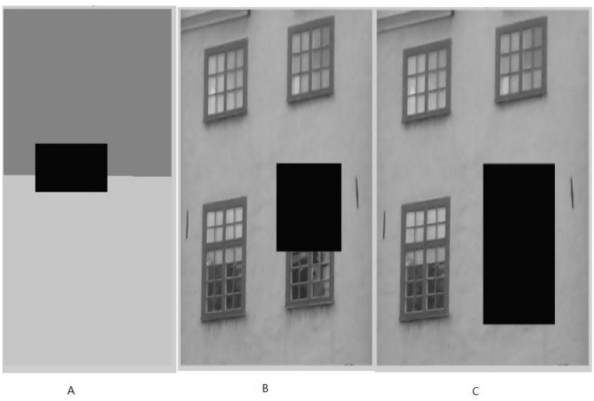


Figure 6: To be restored area of each image. (By Sheng Li).

TABLE I
INFORMATION OF INPAINTING IMAGE RESOLUTION AND TO BE RESTORED AREA.

	Resolution	Size to be Restored
A	200*400(80000) pixels	4505
B	503*491(246973) pixels	21033
C	503*491(246973) pixels	37349

The figure 7 shows the result of each algorithm. The a, b and c are implemented exemplar-based texture algorithm. The d, e and f are implemented PDEs algorithm. From the result, the exemplar-based algorithm can retouch the image. It can partly repair the image. But the c shows a drawback of exemplar-based inpainting. The PDEs algorithm looks like the blur of the image. But the f shows a good result. It is suitable for a narrow or small region filled and the object with a simple background deletion.

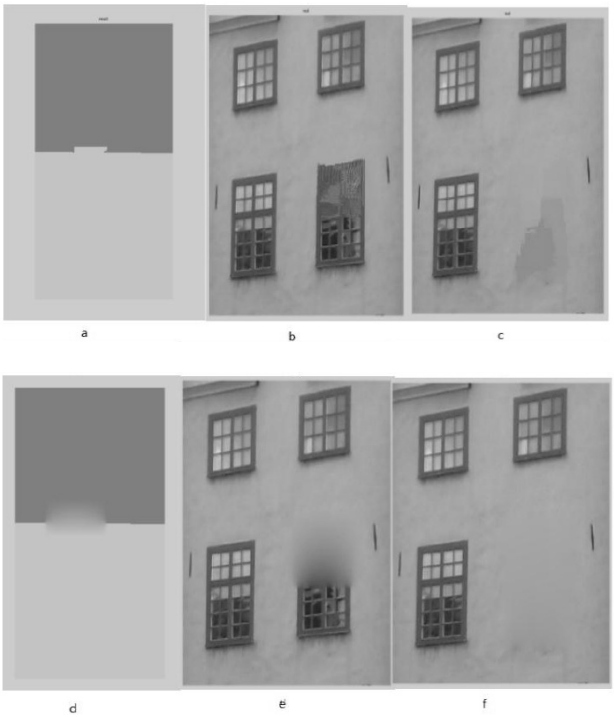


Figure 7: The result of different image. (By Sheng Li)

TABLE II
THE PROCESSING TIME OF EACH IMAGE ON EACH INPAINTING ALGORITHM.

	A	B	C
Exemplar	8.90s	194.04s	390.09s
PDEs	0.34s	0.45s	7.42s

From the Table II, implemented different algorithm on the same image, the processing time of PDEs algorithm is faster than the exemplar, but the quality of exemplar is better than PDEs. With the target region increase and more complex, the exemplar based inpainting algorithm can get a better result than PDEs. But if the background of target region is simple, the PDEs get an ideal result. In my case, the PDEs algorithm is faster than exemplar-based algorithm. But the PDEs is an optimized MATLAB function. It is not fair for comparison. It gives us a future research: How to optimize the algorithm.

CONCLUSIONS

In this work, this paper just finds the suitable method. These inpainting algorithms are successfully restore the images. They are all suitable for small region inpainting. And the PDEs are good at remove object that if the background is simple. Otherwise, the result will looks like blurring. Exemplar-based inpainting algorithms are good at restoration of missing region. But the processing time is a problem. Too many computations on find the best matches patch. If the source region is larger, the time will be longer. If the source region is small, the quality of the result will be bad. The weakness of my exemplar-based inpainting algorithm is the choice of size of patches. If the size of source patch is too big, the best patch may not suitable. If otherwise, the size of source region is too small, the algorithm couldn't find the best match.

Though the exemplar-based algorithm is a suitable method, but it still needs to improve. If the image has a big resolution of 3264*1840, the processing time almost 10 minutes. So the algorithm is not yet suitable to implement on mobile device. It has to be suitable for today's mobile devices. For the PDEs algorithms, the processing is faster than texture algorithm, but it only suitable for narrow and simple region inpainting. When imply the algorithm on big region, the result looks like the blur of the region. But the algorithm would work on today's devices.

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An efficient sense amplifier design for STT-RAM in 45nm hybrid CMOS process

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***Abstract*— in this paper different sense amplifier (SA) circuits for Spin Torque Transfer – Random Access Memory (STT-RAM) have been designed. Their performance is evaluated in 45nm hybrid-CMOS process. The goal is to design an efficient sense amplifier with lower power consumption, better read cycle stability and to reduce the access time. Analysis and design have been done for two circuit's i.e. conventional self-reference sensing (CSRS) scheme and non-destructive self-reference sensing (NDSR) scheme. The results show that CSRS provides good sense margin by trading power and performance. NDSR on the other hand improves the access time, reduces power consumption but with a reduced sense margin.**

***Index Terms* — STT-RAM, hybrid CMOS process, Magnetic Tunnel Junction (MTJ), conventional self-reference sensing, Non-destructive self-reference sensing,**

I. INTRODUCTION

STT-RAM is an emerging non-volatile memory technology. It has the characteristics of fast speed, low power consumption and good scalability. STT-RAM technology is based on spin-polarized current induced magnetic tunnel junction (MTJ). The theory of spin transfer torque was first proposed by Berger [1] and Sloncewski [2]. Further research was carried out by Stiles and Zangwill [3]. Those studies showed that a spin polarized current can reverse the magnetization of a ferromagnetic layer by the so called spin-transfer effect. This mechanism occurs in a sandwich structure of two ferromagnetic layers separated by a barrier layer made of MgO. This structure is called the Magnetic Tunnel Junction (MTJ). S. Yuasa et al.[4] and Parkin et al. [5] showed that very large Tunnel Magneto Resistance (TMR) ratios up to 200% at room temperature could be obtained with MgO Magnetic Tunnel Junction (MTJ).

Sense amplifiers are needed in memory cells to sense the bit line voltages and read the logic state stored in the memory cell. The sense amplifier should perform reliably during the read cycle and also be resistant to noise. This is called read stability. In order for the sense amplifier to function properly, it must accurately read the stored values in the memory cells. In this paper effort has been done to design an efficient sense amplifier for STT-RAM cells.

A. STRUCTURE OF A STT-RAM CELL.

The main element of the STT-RAM is the MTJ cell. Figure 1 shows the MTJ structure consisting of two ferromagnetic layers
separated by MgO barrier layer.

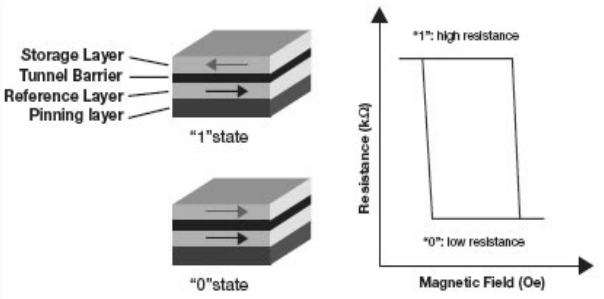

Figure 1. MTJ structure representing antiparallel ('1' state) and parallel ('0' state) [Alexander Driskill et al, Grandis corporation]

The resistance of the MTJ is determined by the relative magnetization directions of the two ferromagnetic layers. When the magnetization directions of the layers are parallel, the MTJ is in low resistance (R_p) state (representing a bit 0), whereas if the layers are antiparallel, the MTJ is said to be in high resistance (R_{ap}) state (representing a bit 1). Data storage is realized by switching the MTJ between high and low resistance states [6]. The ratio of the resistances R_p and R_{ap} is called the tunnel magneto resistance (TMR) and defined as:

$$TMR = \frac{Rap - Rp}{Rp}$$

The basic structure uses an MTJ as the storage element and an N-channel MOSFET (1T-1MTJ) as the selection device [7]. The circuit and cross section of the structure is shown in figure 2. In the STT-RAM cell the source of the NMOS transistor is connected to the source line (SL). The free layer of the MTJ is connected to the bit line (BL) while the other pinned layer to the drain of NMOS. The word line (WL) is connected to the gate.

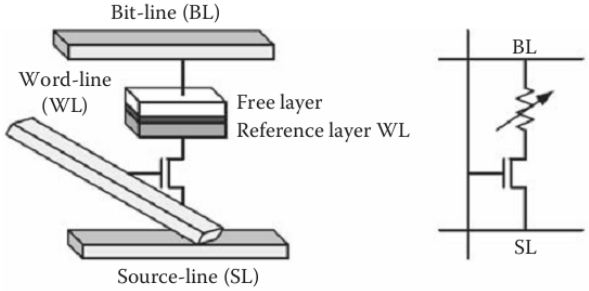

Figure 2. 1T-1MTJ STT-RAM (a) cross section and (b) circuit diagram.

B. READ AND WRITE MECHANISM OF STT-RAM CELL.

The switching of the states in MTJ is obtained by altering the direction of current through it. When a logic '0' is to be written the current flows from BL to SL, whereas when writing '1' the current flows in opposite direction i.e. from SL to BL. When the MTJ terminal is biased to $V_{dd,}$ the cell access transistor operates in the linear region and does not limit the current through the MTJ. Therefore a resistor is connected to limit the current through it. In the reverse bias case, the access transistor operates in a diode connected manner and thus the threshold drop across the access device limits the voltage drop across the MTJ. This voltage drop places an upper limit on the switching current that can be applied to the cell.

The data read operation is slightly different from that of conventional memory cell. The STT-RAM requires a reference voltage to compare the output generated by the sense amplifier. Generally the reference voltage is chosen as the voltage drop across the resistance $(R_p + R_{ap}) / 2$ where R_a and R_{ap} are the resistances of MTJ in parallel and anti-parallel states respectively. The read operation consists of making the word line as high, this selects the access transistor. By applying a read voltage to the selected memory cell, the generated current on the bit line can now be compared to the reference signal in the sense amplifier.

II. SENSE AMPLIFIER DESIGN

There are two main categories of sense amplifiers. Differential sense amplifiers, also known as voltage mode sense amplifiers, and non-differential amplifiers also known as current mode amplifiers [8]. Voltage sense amplifiers include both static and dynamic designs. Static designs are latch based and read the difference between the bit-lines once and hold that output. Dynamic amplifiers on the other hand constantly evaluate the difference between the bit-lines and adjust their output accordingly [9].

A good sense amplifier has to accurately read the logic states stored in the memory cell. Due to process variations, decision failure is a severe issue in STT-RAM design. Consequently, many sensing schemes have been proposed to alleviate this problem. In this paper two sensing schemes, i.e. conventional self-reference scheme and non-destructive self-reference scheme has been designed and evaluated in 45nm hybrid-CMOS process using cadence tools.

A. CONVENTIONAL COMMON READ-OUT SENSING SCHEME

The conventional common read-out mechanism is shown in figure 3. By applying a read voltage (current) to the selected memory cell, the generated current (voltage) on the bit-line can be compared to a reference signal in the sense amplifier. If the generated current (voltage) is higher than the reference, the data storage device (i.e. MTJ) in the memory cell is in the low (high) resistance state. The reference signal is normally generated by applying the same read voltage (current) on a dummy cell, whose resistance is ideally $(R_p + R_{ap})/2$.

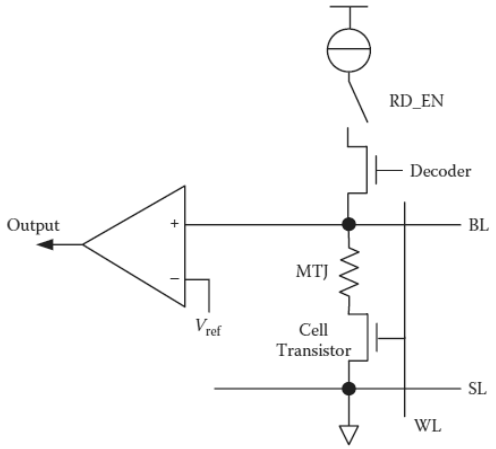

Figure 3. Conventional common read-out sensing.

However this scheme is intolerable to process variation. Due to process variation decision failure can occur in STT-RAM cells. For accurate reading of the logic state and to avoid decision failure, the reference voltage should satisfy the equation:

$$Vbl(L) = Ir.(Rl + Rtr(L)) < Vref < Vbl(H) = Ir.(Rh + Rtr(H))$$

Where *V*bl (L) and *V*bl (H) respectively stand for the bit-line voltages *V*bl when the MTJ is in the low and high resistance states. R_{tr} represents the transistor resistance. R_l and R_h are the resistances in the low and high state respectively. I_r is the read current. Equation 2.1 indicates that sensing voltage in a high (low) resistance state of STT-RAM must be higher (lower) than the reference voltage.

B. CONVENTIONAL SELF-REFERENCE SENSING SCHEME(CSRS)

The motivation for a conventional self-reference sensing scheme (CSRS) is to directly compare the bit-line voltage generated by the original data stored in an MTJ with the bit-line voltage generated by reference data in the same MTJ [10]. Since the generated reference signal is from the same memory bit, the MTJ resistance variation is excluded from the sensing operation. Figure 4 shows the CSRS scheme. The read procedure is as follows: (1) Read the original data by applying a reference read current (I_{r1}) to generate bit-line voltage V_{bl1}. (2) Write '0' into the same MTJ (3) Read '0' by applying another read current (I_{r2}) that generates voltage V_{bl2}. (Here I_{r2} is slightly greater than I_{r1}) (4) Write back the original data back to the memory cell. If the current ratio $\alpha = I_{r1}/I_{r2}$ can be adjusted, then the impact of process variation can be minimized. However, the CSRS has the limitation that two write operations are required which introduces long latency (delay) and additional power consumption.

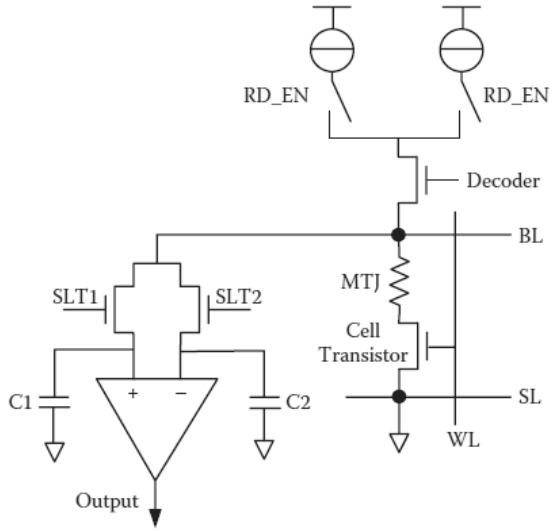

Figure 4. Conventional self-reference sensing scheme.

C. NON-DESTRUCTIVE SELF-REFERENCE SENSING SCHEME (NDSR)

NDSR is based on the unique characteristics of MgO based MTJs [11]. The MTJ has the characteristics of asymmetric static R-V curve which means that current roll-off slope of the high resistance state is much steeper than that of the low resistance state. NDSR has only two read steps without overwriting the original value in the STT-RAM cell. Figure 5 shows the scheme for NDSR.

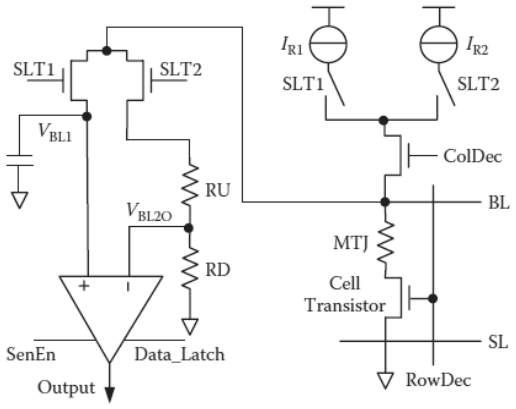

Figure 5. Non-destructive self-reference sensing.

The read procedure is as follows: (1) First apply a read current (I_{r1}) to generate bit-line voltage V_{bl1}, which is stored in capacitor C1. (2) Another read current I_{r2} ($I_{r2}>I_{r1}$) is applied and generates the bit-line voltage V_{bl2}. The V_{bl2o} is the voltage produced by a voltage divider with a voltage ratio $\beta = V_{bl2o} / V_{bl2}$. Proper selection of beta and read current α is necessary for better read stability and to reduce the latency in the access time of the memory cell.

III. DESIGN AND SIMULATION

The sense amplifier for a STT-RAM storage cell has been designed in 45nm CMOS process. Both CSRS and NDSR circuits have been simulated using cadence tools and their performance has been evaluated. The circuit schematic for CSRS and NDSR sensing scheme are shown in figure 6 and 7 respectively.

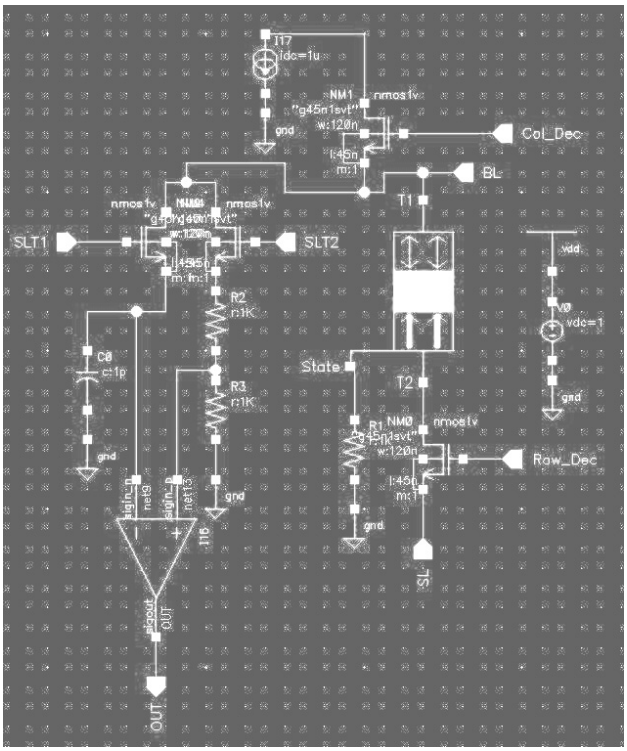

Figure 6. Conventional self-reference circuit.

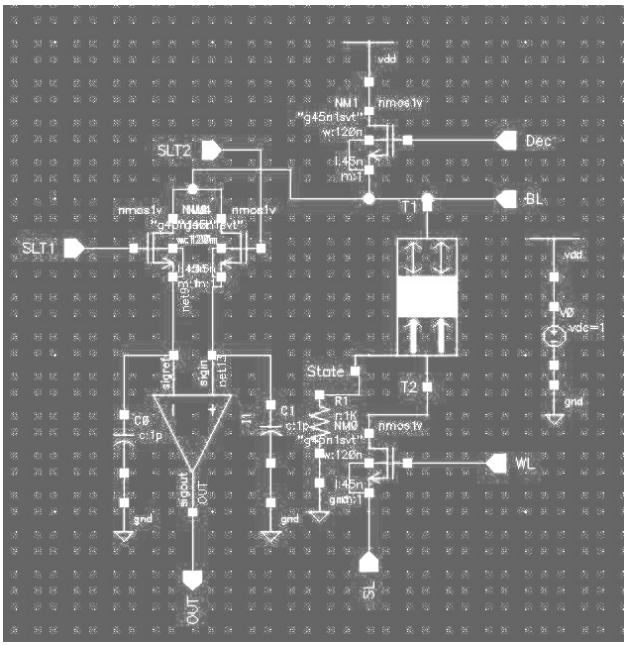

Figure 7. Non-destructive self-reference circuit.

Proper choice of read and reference current were chosen to read accurately the data stored in the MTJ in both the low and high states. The outputs generated are shown in figure 8 and 9 respectively for CSRS and NDSR circuits.

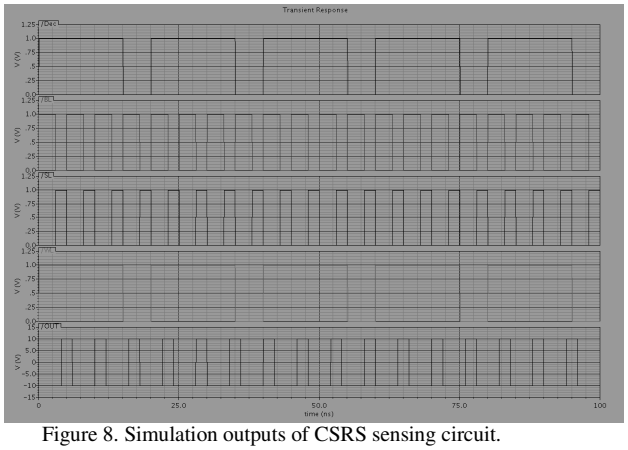

Figure 8. Simulation outputs of CSRS sensing circuit.

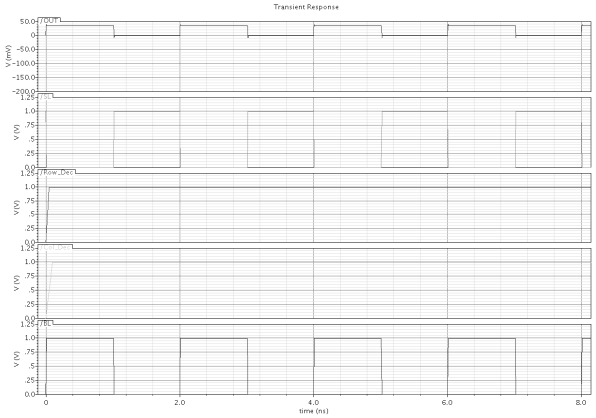

Figure 9. Simulation outputs of NDSR sensing circuit.

A comparison of the two schemes in terms of latency and power consumption is shown in Table 1.

TABLE I
LATENCY AND ENERGY COMPARISON OF CSRS AND NDSR SENSING CIRCUITS.

Designs	Read '1'	Read '0'	Latency
CSRS	20.2 pJ	20.0 pJ	40 ns
NDSR	2.16 pJ	1.12 pJ	15ns

CONCLUSIONS

This paper presented the sense amplifier design for STT-RAM cells in 45nm CMOS process. Two types of sensing circuits, conventional self-reference sensing and Non-destructive self-reference sensing circuits were designed and evaluated for their performance.

The results show that CSRS has much high power consumption. This is because it has two write steps - erase and write back original data. Comparatively NDSR has less power consumption since it has only two read steps. The latency in CSRS is also slightly higher than

that of NDSR because capacitor charging requires a finite amount of time.

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Reduction of ISI using RRC filter for Convolution codes with Viterbi Decoding

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***Abstract*—The transmission of data over wire and wireless communication system is at high modulation rates through the band limited channel , as the signal bandwidth is more than the channel bandwidth then channel introduces a distortion is called ISI(Inter Symbol Interference) i.e. one symbol is interfere with the another subsequent symbols. This distortion is mainly caused by multipath propagation and non-linearity frequency of the channel. Even in the presence of ISI receiver must be able deliver the data to its destination. To reduce ISI we are using the pulse shaping filter is used at the transmitting and matched filter is used at the receiving end. In this paper the binary data will be pulse shaping can be achieved by RRC (Root Raised Cosine)filter transmitter as well as receive filter which does reduces the ISI and channel noise effects on the pulses transmitted over the band limited channels. Noisy base band symbols are received and first matched filtered using RRC filters ,these filtered symbols are then demodulated and symbol to bit de mapping will be done by 16-QAM (Quad rature Amplitude Modulation)demodulator. Mat lab simulation is performed.**

***Index Terms*—RRC filter, ISI, 16-QAM,**

I. INTRODUCTION

In day to day life digital technology ramps up, will involve the transmission of data over one point to another point by increasing the number of R.F applications. These data are modulated by RF carrier such as in cell or mobiles phones T.V and modems, in each case analog data is converted into the digital data like 1's and 0's transmitted by communication mediums in the form of pulses and detected by the receiver. At the receiver to maximize the probability for accurate binary decision can be taken by sampling signal at an optimal point in the pulse duration. i.e. fundamental shape of the pulses does not interfere with the other pulses, such interference called ISI[2][3]. These pulses are not interfere only when the shape of the pulses such that amplitude decays rapidly outside of the interval also zero crossings at the sampling point of all pulse interval. But available bandwidth is limited by data rate and noise in communication systems.

II. INTER SYMBOL INTERFERENCE

Ideally data is transmitted in the form of square pulses, but these pulses are hard to generate and also requires too bandwidth. So the shape of data bits is transmitted in the form of pulses. Let consider the transmitted data is 1, 0, 1, 1, 0,1in rectangular pulses and dotted lines shows the data is in the form of pulses is shown in Fig.1, this data is received through either wire or wireless communication mediums. In this paper data is received through the AWGN channel .Energy from symbols 1and 2 interfere with symbol 3.and reaming symbols interfere with the subsequent symbols is shown Fig.2, the circle area shows the interference is called ISI. This interference occurs due to the non-linearity and charging effects from the frequency selective fading channel[1]. To reduce the ISI slowdown the data symbol and transmit the next data symbol only after allowing, the received symbol has damped down .But time it takes for symbol die down called delay spread

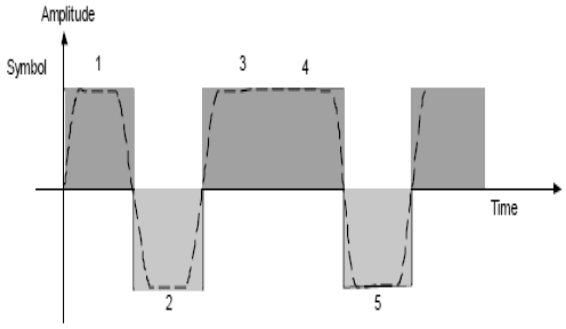

Figure1. Transmitted sequence represented by dashed line.

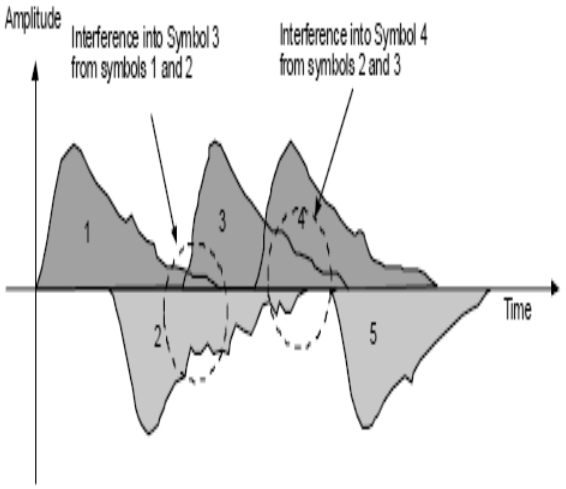

Figure 2. Each symbol in the medium (channel)

III. PROPOSED SIMULATION METHOD

The proposed simulation model is shown in Fig 3.To control the error transmission input data is encoded by convolution encoder. The modulator generates one symbol for 4-data bits. The symbol generated by the modulator is up sampled and pulse shaped (filtered) to comply with the channel bandwidth restrictions. Typically, the pulse shaping is the last stage of transmitter.RRC filter filters out the signal (i.e., equalizes to give a nearly zero ISI, (if sender is also using RRC filter pulse shaping).The output is sampled at the optimum points (i.e., down-sampled) to give four sample per constellation symbol. The 16-QAM demodulator finds out which quadrant the received sample falls and based on that decision generates a pair of bits.

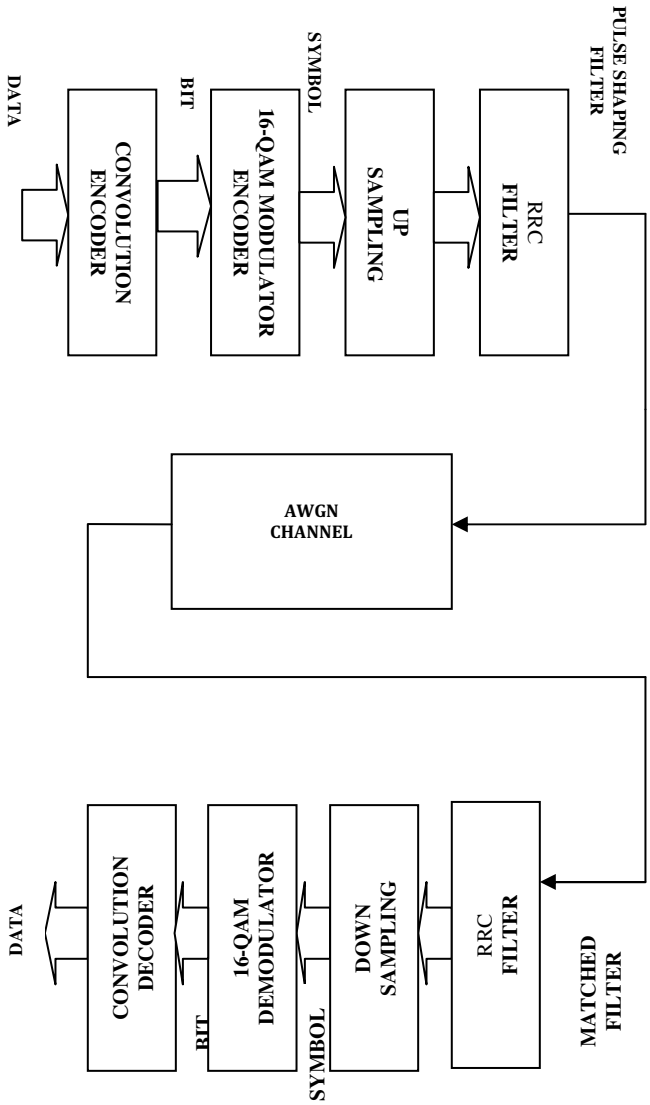

Figure 3.Block diagram of simulation method

The up sampling and down sampling is done at the sending and receiving end, because filters are to be cascaded to obtain a Niquist pulse shape at the output i.e. cascade filters means that no nonlinear operation is allowed between the pulse shaping filter output and matched filter input. To reduce the probability error the matched filter impulse response must be time reversal i.e. H(f)=H(-f).to reduce the ISI the pulse shaping filter response must be zero crossing at multiple of symbol period and sampling rate must be twice the symbol rate. since QAM is not a constant amplitude signaling scheme this leads to bit errors. To avoid this we have to scale the maximum amplitude of the impulse response of the root raised cosine must be oversampling rate is done at the transmitter side. In this paper the design and modification is done to the equation for calculation of the impulse response depending up on the over sampling rate the impulse response thus calculated is used for both pulse shaping at the transmitter and the matched filtering at the receiver.

A. Convolution Encoder

Convolution encoders are popular because they are error detecting and correction codes. To perform this original bit sequence is altered in noise environment communication system. Data bits are encoded either single or multiple bits at a time produces a output based on the generator polynomial. These bits are altered in communication system because of noise and other external factors. To minimize the noise factor, certain additional bits are added to the encoded output which makes the bit error checking more successful and it will also yields more accurate results. This transmission of bits more than the original data bits even in the presence of noise. So that convolutional codes are popular because of these codes are error detecting and correcting codes. Generally these codes are represented by (n, k, m) where n is encoded output sequence ,k number of input bit sequence length and m is the register length.

B.16-QAM modulation

The purpose of modulation in communication system to transmit the data for long distance .in this model encoded bit sequence are modulated by 16-QAM modulator .It converts input bit into 4 symbol mapping in constellation diagram .these symbols are up sampled at the transmitting side and down sampled at the receiver side to obtain the Niquist sample instants .these symbols are shaped by RRC filter and analyzed efficiently over the AWGN channel.

C.AWGN Channel

In communication system, AWGN (Additive White Gaussian Noise) channel introduces most of the noise in real data. It is actually a mathematical model that represents physical phenomena in which the impairment is the linear addition of white noise with a constant spectral density with the distribution of Gaussian form.

D .Viterbi Decoder

The encoded and filter symbols passed through the AWGN channel and received it .At the receiving end these bits are decodes by hard viterbi algorithm. In the decoding process , there are various steps involves they are Quantization, synchronization, branch metric computation, path metric computation and decision making at the output of each state block record each branch and path metric

values .decoding path is selected which ever path is having less path metric values.

IV.RRC FILTER

In communication system pulse shaping can be achieved by RRC filter to control the ISI, starting and ending portions are attenuated in the symbol period. The width of the pulse sis depends on roll of factor alpha .in this simulation alpha value is used is 0.25and the impulse response is shown in fig.4

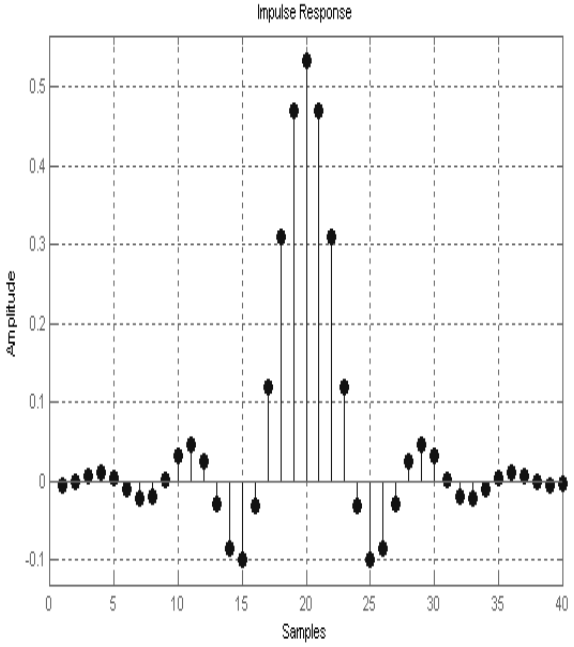

Figure 4: Impulse response of RRC filter.

The response of the filter looks somewhat like square pulse a range of bandwidths are possible depending on the chosen the bandwidth can be anywhere from $1/2R_s$ for the sinc pulse and to Rs for the square pulse.

When the equation becomes pure square pulse. The advantage is that if the transmit side filter is stimulated by an impulse, then they receive side filter is forced to filter an input pulse shape that is identical to its own impulse response, thereby setting up a matched filter and maximizing signal to noise ratio while at the same time minimizing ISI[11].

The transfer function of the RRC filter is

$$H(f) = \begin{cases} 1 & for\ |f| \le \frac{(1-\alpha)}{2T_s} \\ \cos^2\left[\frac{\pi T_s}{2\alpha}\left(|f| - \frac{(1-\alpha)}{2T_s}\right)\right] & for\ \frac{(1-\alpha)}{2T_s} \le |f| \le \frac{(1+\alpha)}{2T_s} \\ 0 & for\ |f| > \frac{(1+\alpha)}{2T_s} \end{cases}$$

V. SIMULATION RESULTS

In this paper all the simulations are done using Mat lab.The simulation parameters and their values are shown in Table1.

TABLE I.
SIMULATION TABLE

Parameter	Value
Convolution Code rate	1/2
Modulation scheme	16-QAM
Bit energy to Noise power spectral density, (E_b/N_0)	10 dB
RRC filter order	40
Viterbi Trace back length	32
RRC filter roll of rate	0.25

In this paper the random data is encoded by the convolution encoder with a code rate of ½.theses bits are converted into the symbol of 4-bits long by the 16-QAM modulator. These four symbols are passed through the up sampling then given to the RRC filter order 40 and roll of factor 0.25, these symbols are passed through the AWGN channel it add the nosie 10dB of white noise . in the receiver side these noise is removed by same RRC filter it acts as a matched filter[1] , these filtered symbols are down sample it and demodulate by 16-QAM demodulator and perform the decoding by viterbi .

The proposed method is simulated in Mat lab by the following steps

- Generating a Random Binary Message
- Encoding the Bits is encoded by convolution code of code rate 1/2.
- Bit-to-Symbol Mapping by binary to Gray Code conversion
- Modulate by 16-QAM
- Pulse Shaping Signals Using an FIR RRC
- Adding AWG Noise to the Transmitted Signal
- Filtering Received Signals Using the RRC Filter
- Signal recovery
- Received signal by 16-QAM demodulator
- Bits recover from symbols by gray code to binary conversion
- Decoding by viterbi algorithm.
- Calculate the BER with and without convolution coding.

In digital communication system sending the data in the form of one's and zero's in pulses. Eye diagrams are generated by super imposing two pulses on each other by several times, the generated pattern are looks like human eye. In this paper these diagrams are generated with 4-bit interval of time and repeatedly place for the modulated signals as shown in figure 5. The received signal can be sampled without error can be indicated by eye width. Noise margin and best sample can be taken at the opening of human eye. Actually carrying information is eye amplitude.

These eye patterns are pulse shaped and oversampled a symbol stream before transmission by RRC filter .Practically the pulse shaping RRC filters are windowed. The window length can be controlled by three ways filter order, filter order in symbol durations, and Minimum order to achieve a given stop band attenuation.

In this paper the given proposed design roll off factor is 0.25and up sampling factor is 4 with filter order 40 is shown in figure it compares the data before and after filter.

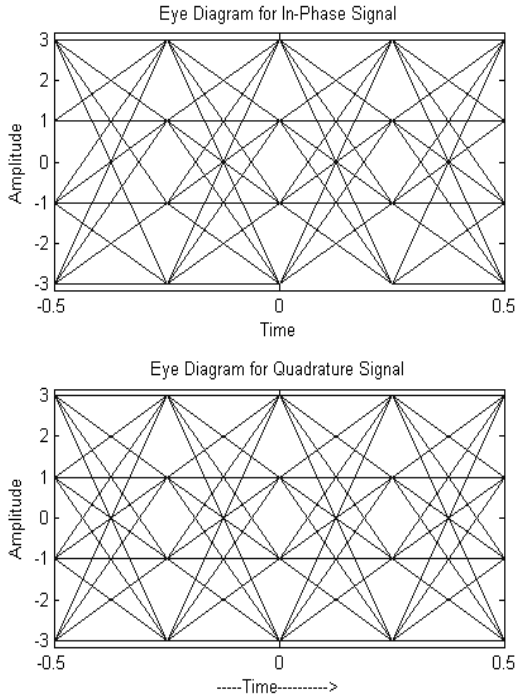

Figure 5: Eye diagram of modulated symbols

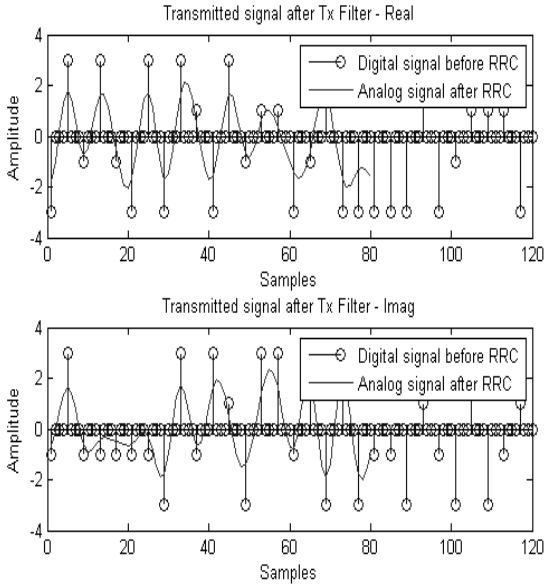

Figure 6: Comparison of modulated signal before and after the filter.

Now the signal is encoded and filtered transmitted through the AWGN channel .it add the additive white noise to the transmitted data .the scatter plot show the transmitted and received signal is shown in figure 7.

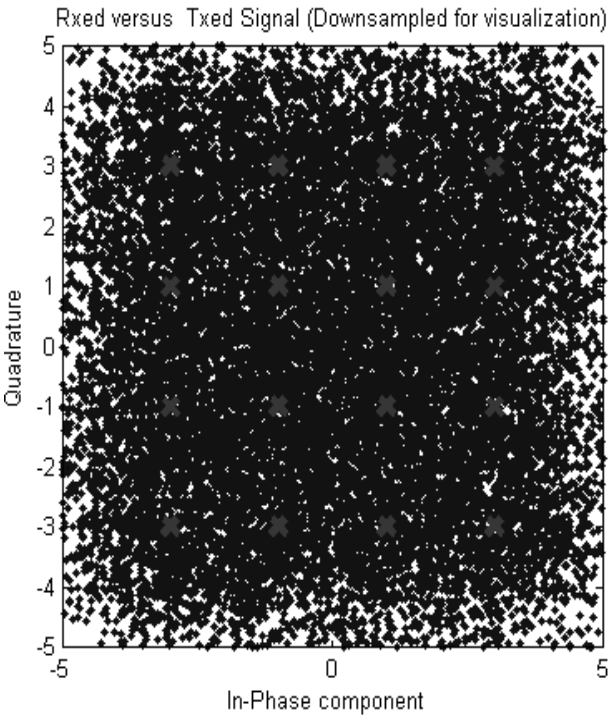

Figure 7: Transmitted and Received signal

Received signal can be recovered from the matched filter by down sample the signal is shown in figure 8 represents the transmitted and received signal after RRC after filtering the signal can be demodulated by 16-QAM demodulator i.e. symbol to bit mapping is done.

These bits are decoded by viterbi decoding.

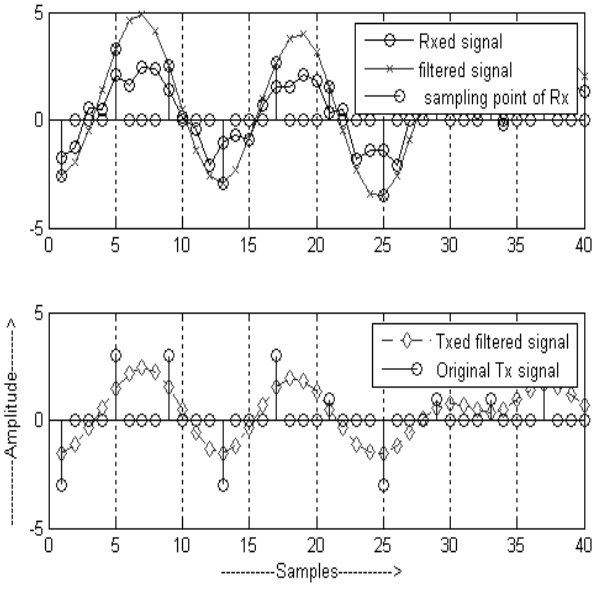

Figure 8: Comparison of signal before and after RRC .

CONCLUSIONS

From the results shown in above prove that ISI and additive white noise can be suppresses for the band limited channels by pulse shaping filters. Also bit error rate is

reduced by using the convolution encoding and Viterbi decoding of 16-QAM modulator. The application of QAM can be seen in color television to multiplex the chrominance signals, in old telephony systems, in wireless internet modem, power line communication (PLC), digital audio and video broadcasting and wireless ATM transmission system.

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Implementation of BIST Technique for A to D Converters in FPGAs

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Abstract—**When designing an Analog to digital Converter (ADC) it is desirable to test its performance at two different points in the development process. The first is characterization and verification testing when a chip containing the ADC has been taped-out for the first time, and the second is production testing when the chip is manufactured in large scale. It is important to have a good correlation between the results of characterization and the results of production testing. This paper investigates the feasibility of using a built-in self-test to evaluate the performance of embedded ADCs in Field Programmable Gate arrays (FPGA), by using the FPGA fabric to run necessary test algorithms. The idea is to have a common base of C code for both characterization and production testing. The code can be compiled and run on a computer for a characterization test setup, but it can also be synthesized using a high-level synthesis (HLS) tool, and written to FPGA fabric as part of a built-in self-test for production testing. By using the same code base, it is easier to get a good correlation between the results, since any difference due to algorithm implementation can be ruled out. The algorithms include a static test where differential nonlinearity (DNL), integral nonlinearity (INL), offset and gain error are calculated using a sine-wave based histogram approach. A dynamic test with an FFT algorithm, that for example calculates signal-to-noise ratio (SNR) and total harmonic distortion (THD), is also included. All algorithms are based on the *IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters* (IEEE Std 1241). To generate a sine-wave test signal it is attempted to use a delta-sigma DAC implemented in the FPGA fabric. For the static test there was a perfect match of the results to 10 decimal places, between the algorithms running on a computer and on the FPGA, and for the dynamic test there was a match to two decimal places.**

Index Terms—**FPGA, built in Self Test (BIST), ADC, dynamic test, static test, linearity, DNL, INL, offset, gain error, FFT, SNR, THD, delta-sigma, sigma-delta, Digital to analog converter (DAC), high-level synthesis, HLS, IEEE Standard 1241**

I. INTRODUCTION

A field-programmable gate array is a type of programmable logic circuit, which can be used to realize integrated circuit designs. In contrast to an application specific integrated circuit (ASIC) an FPGA is not manufactured to fit a certain application, but can instead be used in a large variety of applications. One of the advantages is that the development time for a design can be much shorter for an FPGA than for an ASIC, and thus the time-to-market is shorter. Another advantage is flexibility. If there is an error in the design, the bug can be fixed and the device reprogrammed with the correct version of the design. If a product is produced in large volumes, ASICs have the advantage that they are cheaper to manufacture per unit, but since there is a high initial cost for manufacturing integrated circuits, FPGAs are more cost effective for lower volumes.

This paper explains the testing of analog-to-digital converters (ADCs) that are embedded in field-programmable gate array (FPGA) chips. By exploiting the fact that an FPGA can be reprogrammed, its fabric can be utilized as part of a built-in self-test (BIST) for the embedded ADC, and the test logic can then be removed when it is not needed anymore. If the test algorithms are written in C code, and mapped to the FPGA using high-level synthesis, then the exact same algorithms can also run on a computer as part of larger test setup. The BIST is suitable for production testing and demonstrations, and the computerized test setup is suitable for more versatile characterization testing. By using the same code base it is easier to get comparable measurement results from the two. In order to test the ADC a test signal also has to be generated, and this can possibly be done with the help of a delta-sigma modulator realized in the FPGA fabric. These two topics are using C code for an FPGA ADC test, and generating a test signal with a delta-sigma modulator in the FPGA fabric and are investigated in this paper. The C code test algorithms are mainly based on an IEEE standard for ADC testing [5], and related research papers, and the delta-sigma modulator is inspired by an application note from Xilinx[4]. C code test algorithms and Verilog code for delta-sigma modulators were developed in Xilinx's Vivado design suite.

The ADC test covered in this paper can be divided into two parts as static test and dynamic test and each of these two tests consist of a set of algorithms. The algorithms were tested with artificial data generated in Matlab. For the static test an ADC model was written using an if-statement to represent the transition levels of an ideal 4-bit ADC, and then errors were introduced by changing some of the transition level from their ideal values. The model was then used to quantize a sine-wave and the resulting ADC codes were used to test the static test algorithms. For the dynamic test a sine-wave with a specific signal-to-noise ratio was generated using the built-in additive white Gaussian noise function in Matlab. Harmonics of the signal were also added to the signal and the resulting array of data was then used to test the dynamic test algorithms. After these tests with artificial data, the algorithms were ported into C code and the C code was tested using the same artificial data to see that it matched the models in Matlab. Then the codewas synthesized into a RTL representation using HLS and tested in a co-simulation. In the co-simulation both the C

code and its synthesized RTL representation are simulated using the same C code test bench. This way the results can be compared to make sure the synthesized design is working as expected. The top-levels of the BIST, one for a dynamic ADC test and one for a static ADC test, were written in Verilog. They are basically finite state machines that collect ADC data and start the test when a button is pressed. In Vivado there is a catalog of IP cores, which are ready-made pieces that can be used in designs by generating code and then instantiating it in Verilog. The HLS blocks (the synthesized C code) can be imported into this library and then instantiated into the design in the same manner as other IP cores. This way the synthesized ADC test algorithms were integrated into the Verilog top-levels. The top-level designs with instantiated HLS blocks were simulated, synthesized, implemented and generated into bitstreams using Vivado, and then tested on the FPGA. When testing them, output codes from the ADC were probed using ILAs and then used as test data in Matlab and C simulations. In this way the results from the BIST could be compared to the results of algorithms running on a computer processing the exact same data, and thus the correlation between them could be investigated.

II. ADC TESTING

This paper is based on the IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters (IEEE Std 1241). The performance measurements of interest here can be divided into two categories; static test and dynamic test. The static test measures an ADC's excursion from its ideal behavior when sampling a slowly varying (relatively low frequency) signal. The dynamic test measures the spectral purity of the of the ADC's digital output signal, when the ADC sample a relatively high frequency signal. The IEEE standard 1241 attempts to provide a common ground for ADC tests and testing methods. If test methods and definitions from this standard are used, and if they are disclosed properly when presenting the results, it is easier to compare ADCs and to reproduce measurement results. This makes the information more usable, and thus more valuable.

A. *Static test*

The idea behind what is usually referred to as a static ADC test, is to excite the ADC with an input signal of low enough frequency so that the signal can be considered a DC, or static signal. The output codes of the ADC are then compared with what is expected from an ideal ADC model. When designing a static ADC test there are a number of choices to be made. There are several, equally valid, ways to define the ideal behavior and the ADC's excursion from this ideal behavior. The static test consists of finding the transition levels of the ADC and compares these voltage levels to the ideal ones. The difference between the tested device and the ideal case is then quantified by four metrics: gain, offset, differential nonlinearity (DNL) and integral nonlinearity (INL).

i. Performance metrics

There are four metrics which are used to quantify the difference between the transfer function of the ADC under test and the ideal transfer function. These are: gain, offset, DNL and INL. Which are defined [1] as Gain is the value by which the input values are multiplied to minimize the mean square deviation from the output values. Gain error is the deviation from the ideal gain in percent. Offset is the value by which the input values are added to minimize the mean square deviation from the output values. Differential nonlinearity (DNL) is the difference between a specified code bin width and the average code bin width, divided by the average code bin width. Integral nonlinearity (INL) is the maximum difference between the ideal and actual code transition levels after correcting for gain and offset.
The gain and offset is calculated using the following equation

$$GT[k] + V_{OS} + \varepsilon[k] = LSB \cdot (k-1) + T_1 \qquad (1)$$

where G is the gain, T[k] is the measured transition levels, Vos is the offset, ε is the error for each index k and T_1 is the ideal position of the first transition level. For the mid-riser convention the ideal position of the first transition level is at one LSB above the minimum input voltage, so T1 is equal to V_{min} + 1LSB. The right-hand side of Eq. 1 is the ideal transition levels. For the first one, k is equal to 1, so it is located at T_1, which is V_{min} + 1LSB. For the second one k is equal to 2, so it is located at V_{min} + 2LSBs, etc. On the left-hand side are the measured transition levels *T* [*k*]. The task is to find the gain *G* and the offset *Vos* which minimizes the mean squared deviation from the best-fit (linear regression) line. This is done by minimizing the sum of square of the errors (SSE). In this case Eq. 1 can be rearranged as

$$\varepsilon[k] = LSB \cdot (k-1) + T_1 - GT[k] - V_{OS} \qquad (2)$$

The index k is the index of the transition levels and runs from 1 to 2^N- 1 and by assuming T_1 is equal to V_{min} + 1LSB the SSE can be expressed as

$$SSE = \sum_{k=1}^{2^N-1} \varepsilon^2[k] = \sum_{k=1}^{2^N-1} (LSB \cdot k + V_{\min} - GT[k] - V_{OS})^2$$

This is a function of the two variables G and Vos and to find the minimum, the partial derivatives are calculated and set to zero.

$$\frac{\partial(SSE)}{\partial V_{OS}} = -2\sum_{k=1}^{2^N-1} (LSB \cdot k + V_{\min} - GT[k] - V_{OS}) = 0$$

------ (3)

$$\frac{\partial(SSE)}{\partial G} = -2\sum_{k=1}^{2^N-1}(LSB \cdot k + V_{\min} - GT[k] - V_{OS})T[K] = 0$$

------ (4)

Eqs. 3 and 4 form an equation system which can be solved for *G* and *Vos*. Doing so results in the following expressions for gain and offset:

$$G = \frac{LSB \cdot (2^N - 1)\left(\sum_{K=1}^{2^N-1} kT[k] - 2^{(N-1)}\sum_{K=1}^{2^N-1} T[k]\right)}{(2^N - 1)\sum_{K=1}^{2^N-1} T^2[k] - \left(\sum_{K=1}^{2^N-1} T[k]\right)^2} \quad (5)$$

$$V_{OS} = LSB \cdot 2^{(N-1)} + V_{\min} - \frac{G}{2^N - 1}\sum_{K=1}^{2^N-1} T[k] \quad (6)$$

DNL and INL are calculated with Eq. 7 and Eq. 8 respectively [2].

$$DNL[k] = \frac{G \cdot (T[k+1] - T[k]) - LSB}{LSB} \quad (7)$$

$$INL[k] = \frac{G \cdot T[k] + V_{OS} - LSB \times (k-1) - T_1}{LSB} \quad (8)$$

The DNL is the difference in code bin width *W*[*k*], after compensating for gain, to the ideal code bin width, which is 1 LSB, expressed in LSBs. The INL is the error of each transition level, after compensating for gain and offset, expressed in LSBs.

B. Dynamic test

In the dynamic test the ADC is excited with a sine-wave signal of high enough frequency so that dynamic errors occur. A number of samples from the sine-wave are collected and the discrete Fourier transform (DFT) is used to analyze the data. The DFT can be calculated using an FFT algorithm[7].

i. Performance metrics

The DFT gives the frequency spectrum of the ADC codes and a number of performance metrics can be calculated from this spectrum. An example of a spectrum obtained from the DFT is illustrated in Figure 1. The dynamic performance metrics defined in the IEEE Std 1241 are given as Total harmonic distortion (THD) is, using a pure sine wave input of specified amplitude and frequency, the root-sum-of-squares of all the harmonic distortion components including their aliases in the spectral output of the ADC. IEEE Std 1241-2010 suggest the ten first harmonics are used to estimate THD. THD is often expressed as a decibel ratio with respect to the rms amplitude of the output component at the input frequency. The total harmonic distortion (THD) is calculated by summing up the harmonics of the fundamental signal, i.e. summing up the power in frequency bins that are at integer multiples of the frequency bin of the input signal. The ratio of the distortion power to the signal power (the difference in dB) is then the THD.

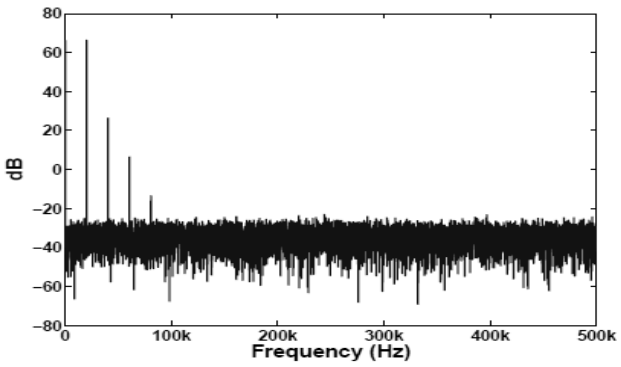


Figure 1: Spectrum, of a 20 kHz sine-wave, obtained using DFT

The signal-to-noise ratio (SNR) is calculated by summing up the noise, i.e. the power in all the frequency bins up to Nyquist frequency, except for the bins containing the DC, the fundamental signal and its harmonics. The ratio of the signal to the noise (the difference in dB) is then the SNR. Signal-to-noise ratio is the ratio of the rms amplitude of the ADC output signal to the rms amplitude of the output noise, using a pure sine wave input of specified amplitude and frequency. This does not include the harmonic distortion components that are used for the estimate of THD. Signal-to-noise-and-distortion ratio (SINAD) is the same as SNR with the only difference that the harmonics are included in the noise summation[9]. The spurious free dynamic range (SFDR) is the ratio of signal to the highest noise spur (the difference in dB) in the spectrum. Lastly the effective number of bits (ENOB) is calculated using the SINAD in the formula for SNR for an ideal ADC (Eq.9). Replacing SNR with SINAD in this formula and solving for N gives the ENOB[8].

$$SNR = 6.02N - 1.76dB \quad (9)$$

Effective number of bits is a measure of the signal-to-noise-and distortion ratio used to compare the actual ADC performance to an ideal ADC.

III. BUILT-IN SELF-TEST

Built-in self-test(BIST), means that extra circuitry is added to a design in order for the design to be able "perform operations on itself to prove correct operation" [2]. This is then combined with a so called scan technique which allows the registers in the design to be read, so that the result of the test can be examined. Because of the added circuitry, there is a circuit overhead related to the test, but because the test time can be reduced the overall system cost may be lower. A BIST in a FPGA has the advantage that it does not have the circuit overhead

normally associated with a BIST. When the BIST circuitry is not needed in the design anymore it can be removed and the design re-synthesized, which is a huge advantage compared to a BIST in an ASIC. In Figure 2 a block diagram of the BIST is shown. A delta-sigma modulator in the FPGA fabric is used to generate a test signal. This signal is fed out through the I/O of the FPGA and is then filtered by an external analog filter before going to the dedicated analog inputs of the ADC. The filter is necessary to remove high-frequency quantization noise. The test signal is generated continuously and the ADC is sampling at a fixed sample rate. The top-level Verilog block consists of a finite state machine (FSM). When a start button on the KC705 board is pressed the top-level collects samples from the ADC, and when enough samples have been collected it starts algorithms that calculates the performance of the ADC based on the collected samples. These are the algorithms that were written in C code and synthesized using HLS. Once the algorithms are finished, a done signal is returned and the top-level FSM goes to an idle state where it resides until the start button is pressed again.

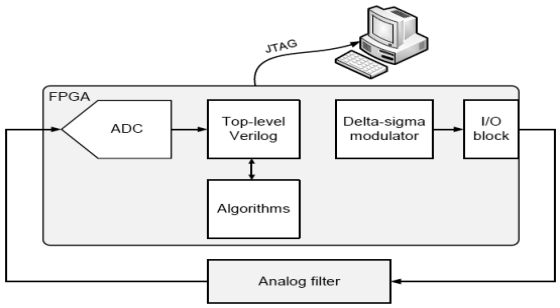


Figure 2: Block diagram of the BIST

Integrated into the design are ILAs which can be used to read the test results. Each ILA has a trigger and a capture signal that can be chosen by the designer. If the ILA is armed, this is done in Vivado's hardware manager; it starts to capture data from a designated register in the design when the trigger signal goes high. The register is then sampled by the ILA each clock cycle a chosen condition, based on the capture signal, is met. If for example the condition is that a capture signal C0 is equal to one, then the register will only be sampled at the clock cycles where "C0 = 1". If there is no capture condition set, however, the ILA will sample the register every clock cycle after the trigger goes high. Each sample that an ILA collects is stored in its memory, which consists of block RAM, and the data capture continues until the memory is full. The memory content can then be read through a JTAG interface using Vivado's hardware manager[3]. There is a data ready signal that goes high one clock cycle for each ADC conversion, and this signal can be used both as trigger and capture signal for an ILA that captures ADC codes from the ADC data register. Thus data from the ADC can be obtained in a convenient way.

One important thing to note about this setup is that there are no external active components used in the test. Typically a signal generator or external DAC would be used to generate the test signal for the ADC. The argument for not using external active components is that those components then would have to be calibrated, or their accuracy somehow guaranteed in order to ensure that the errors found in the test are indeed in the ADC itself and not the test signal. It is desirable to avoid this situation. The Specifications of test case ADC are shown in the following Table 1.The first four parameters after the resolution in Table 1 integral nonlinearity, differential nonlinearity, offset and gain errors are measures of the ADC's static performance. Regarding gain and offset error there is a setting for automatic calibration which gives smaller errors, but the un calibrated values are shown here. The sample rate can be chosen between 0.1 and 1 MS/s, but usually it is the performance at the highest possible sample rate that is of most interest. Signal to noise ratio and total harmonic distortions are measures of the ADC's dynamic performance. The ADC supports both uni-polar and bipolar mode. For the bipolar mode a fully differential input signal can be used. For a 1 MS/s sample rate a 26 MHz ADC clock frequency is needed, but a higher frequency system clock can be divided down and used as ADC clock.

TABLE I
SPECIFICATIONS OF TEST CASE ADC

Parameter	Value
Resolution (bits)	12
Integral nonlinearity (LSB)	±3
Differential nonlinearity (LSB)	±1
Offset error (LSB)	±6
Gain error (%)	±0.5
Sample rate (MS/s)	0.1 – 1
Signal-to-noise ratio (dB)	60
Total harmonic distortion (dB)	70
Unipolar input range (V)	0 – 1
Bipolar input range (V)	-0.5 – 0.5
Unipolar common mode range (V)	0 – 0.5
Bipolar common mode range (V)	0.5 – 0.6
ADC clock frequency (MHz)	1 – 26

IV. SYSTEM IMPLEMENTATION

This paper consists of two main parts; investigating signal generation with a delta-sigma modulator realized in FPGA fabric, and mapping C code algorithms for ADC testing to FPGA fabric using HLS. A second-order delta-sigma modulator was investigated because it gives a sufficient SQNR with a reasonable oversampling ratio. Its implementation in Verilog is discussed below. Two BISTs for ADC testing were developed, one for dynamic test and one for static test.

A. The Delta-Sigma DAC

The delta-sigma modulator was implemented in Verilog and a block diagram of the design can be seen in Figure 3 It consists of four adders, two flip-flops and a quantizer. The signals in the design are represented as 24-bit fixed point two's complement numbers so the buses in the design are 24 bits wide. The adders therefore add 24-bit

words and the flip-flops in the diagram represent 24 parallel flip-flops each. Four of the bits are integer bits and 20 are fractional bits. It was found that four integer bits was enough to avoid overflow and 20 fractional bits gave sufficient accuracy. The quantizer is basically a comparator which feeds back +1 if the output is positive, and -1 if the output is negative. Through the output *Xout* one bit is fed out, and that is the inverted sign bit from the 24-bit representation. This way the DAC outputs 1, which corresponds to +VDD volts, if the output of the modulator is positive and 0, which corresponds to 0 volts, if the output of the modulator is negative.

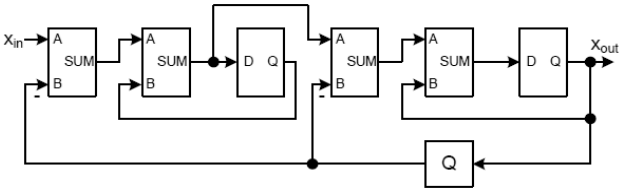


Figure 3: Block diagram of the second-order delta-sigma modulator.

The test setup used for the delta-sigma DAC can be seen in Figure 4. A direct digital synthesizer (DDS) was used to generate a half-scale digital sine-wave of 20 kHz. The DDS is a pre-made design block which is available in Vivado's IP library and can be instantiated in the design. The sine-wave codes are fed to the delta-sigma modulator with the clock rate 8 MHz . The output of the modulator goes through an I/O, traces on the KC705 board and is then fed out to a spectrum analyzer using a GPIO SMA connector. The I/O blocks of the FPGA can be set in many modes (many I/O standards) but for this experiment the choice of standard was limited to the standard LVCMOS18. Before implementing the design two settings to the I/O could be adjusted: drive strength (4-24 mA) and slew rate (fast/slow). For this experiment 8 mA drive strength and fast slew rate were chosen.

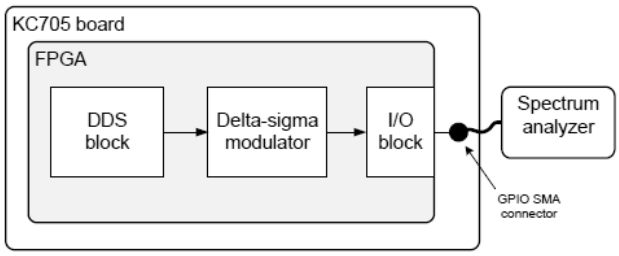


Figure 4: Setup for testing delta-sigma DAC

V. RESULTS

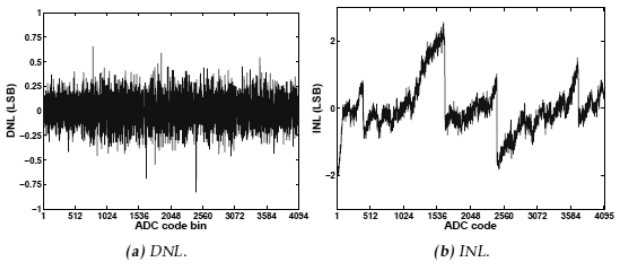
In order to evaluate if synthesizing C code algorithms for ADC testing with HLS is feasible, the test results between code running on a PC and the synthesized design were compared. Except for matching results between PC and BIST, measurement time and FPGA utilization was also considered.

TABLE II
COMPARISON BETWEEN STATIC BIST TEST, C CODE RUNNING ON PC AND MATLAB TEST MODEL USING PROBED HISTOGRAM.

	Matlab model using measured histogram	C code (on PC) using measured histogram	C code algorithms running on FPGA
gain error (%)	-0.1814590398	-0.1814590398	-0.1814590398
offset error (LSB)	-11.4587839949	-11.458783994	-11.458783994
DNL min (LSB)	-0.8265005955	-0.8265005955	-0.8265005955
DNL max (LSB)	0.6550577276	0.6550577276	0.6550577276
INL min (LSB)	-2.1075215934	-2.1075215934	-2.1075215934
INL max (LSB)	2.5614670437	2.5614670437	2.5614670437

In Table 2 a comparison between the BIST, C code running on a PC and the Matlab model for the static test can be seen. The ADC was set in uni-polar mode and an external signal generator was used to generate the input signal. The signal was a single-ended sine-wave with an offset of 500 mV and an amplitude of 550 mV, and the frequency was set to around 20 kHz but non-harmonically related to the sampling frequency. The frequency was somewhat arbitrarily chosen. A lower frequency might be desirable, but the purpose with this experiment was to evaluate the functionality of the BIST rather than evaluate the ADC itself. In the test 200,000 samples were collected and used to generate the histogram. In order to compare the BIST with the C code and Matlab code running on a PC, the histogram was probed with an ILA. Using Vivado's hardware manager the data from the ILA can be obtained in a CSV-file. This way the histogram from the BIST test could be used as input data in Matlab and a C code test bench. Ideally the ADC codes would be probed directly and the histogram would be regenerated with code on the PC, but the ILAs cannot save enough samples. In this comparison, using 10 decimal places, the results match exactly and it can be concluded that synthesizing the algorithms into RTL and running them on the FPGA was successful. Comparing the result to the specifications of the ADC (see Table 1) it can be seen that the test results are reasonable. All results meet specifications except for the offset error, which is probably due to that the accuracy of the offset setting of the signal generator was not good enough.

Figure 5 shows DNL and INL plots from the measurement. The INL has jumps at certain codes where the DNL is large. Note that the INL curve does not start off from zero because the best-fit approach was used and not the terminal based approach.



(a) DNL. (b) INL.

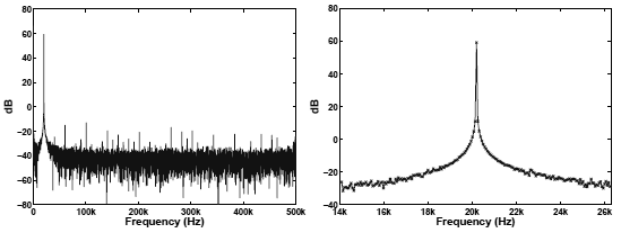
Figure 5: Static test results illustrated with data probed with ILAs.

In Table 3 measurement results from the dynamic BIST are compared with the C code algorithms running on a PC and a MATLAB model. In this case the ADC codes were probed directly with an ILA, a CSV-file with the data was obtained and this data was used in a test bench on the PC. Unfortunately the last ADC sample was not probed correctly by the ILA so to be able to make the comparison, including the FFT, the code of the last sample was estimated by interpolating the curve[10]. Despite this, the results match to two decimal places, except for the THD which matches to one decimal place. This is close enough to deem the experiment successful, and based on the experience from the static test, the match is probably even better in reality. Some difference is expected though, because the design uses floating point operations and the floating point operators used in the FPGA design are not 100% accurate [6].

TABLE III
COMPARISON BETWEEN DYNAMIC BIST TEST, C CODE RUNNING ON PC AND MATLAB TEST MODEL USING PROBED ADC CODES AND PROBED SPECTRUM.

	Matlab model using measured ADC codes	Matlab model using measured spectrum	C code Algorithm running on PC	C code algorithm running on FPGA
THD (dB)	66.030626 9531	66.021016 7941	66.030626 9531	66.021016 7941
SFDR (dB)	47.521079 2495	47.519112 7127	47.521079 2495	47.519112 7126
SINAD (dB)	42.313995 3465	42.313232 9784	42.313995 3465	42.313232 9784
SNR (dB)	42.332489 9726	42.331765 4022	42.332489 9726	42.331765 4022
ENOB	6.7365440 775	6.7364174 383	6.7365440 775	6.7364174 383

Table 3 does show a good match between the algorithms running on a PC and on the FPGA, but the measurement results are much lower than the specification of the ADC (Table 1). One reason for that is that the input signal from the signal generator was not filtered and is therefore not as spectrally pure as desired. Also, and more importantly, there is significant spectral leakage that affects the result. The reason behind the spectral leakage is probably that the frequency of the input signal could not be set with sufficient precision. This highlights a potential difficulty of dynamic ADC testing in a BIST environment. It can be hard to control the input signal frequency accurately enough. In Figure 6, the spectrum obtained by an ILA probe during the test run can be seen. The DFT is calculated directly from the ADC codes and the amplitudes in the resulting frequency spectrum are not normalized. Since the performance metrics are calculated as ratios of the signal and distortions/noise in the spectrum, no normalization is necessary.



(a) Frequency spectrum. (b) Zoomed in around the fundamental.

Figure 6: Frequency spectrum calculated by FFT algorithm and probed with ILA.

CONCLUSIONS

The concept of having a common base of C code for running on a PC and for synthesizing with HLS into a BIST running on an FPGA proved feasible. When testing ADCs a number of choices have to be made, especially for the static test. There are multiple ways to define the performance metrics of interest, there are many ways to measure them and the choice of definition and method will affect the result. The IEEE Std 1241 can be used as guidance when making these choices. Definitions and measurement methods are usually not expressed explicitly on data sheets which makes it harder to compare the performance of ADCs.

For the static test, it has to be considered that the accuracy of gain and offset calculations depends on the accuracy of the amplitude of the sine-wave input signal. If very accurate measurements of gain and offset are needed, either the amplitude must be controlled very precisely, or some other measurement method must be used. Perhaps the feedback loop approach can be used to find two of the transition levels and then calculate the amplitude and offset of the input using this information.

For the dynamic test, the precision of the signal frequency setting must be considered carefully. Otherwise windowing or some method to avoid spectral leakage must be used. Lastly, depending on the intended applications, it could be considered to use the BIST to test more aspects of the ADC. For example step response, code noise and two-tone tests.

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Comparative Analysis of Various Enhancement Methods for Satellite Images

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Abstract—**In this paper, a comparison of the satellite image contrast enhancement techniques is being carried out. Satellite images are being used in many fields of research. One of the major issues of these types of images is their resolution. Here discrete wavelet transform (DWT) is used as a base and two techniques for enhancing the images are compared. The DWT technique decomposes the input image into the four frequency subbands and in the first method it estimates the singular value matrix of the low–low subband image, and, then, it reconstructs the enhanced image by applying inverse DWT. The second technique is based on the interpolation of the high-frequency subbands obtained by discrete wavelet transform (DWT) and the input image. The high-frequency subband images and the input low-resolution image are interpolated and then combined together to generate a new resolution-enhanced image by using the inverse DWT technique. The experimental results show the comparison between the two methods which help us to make a choice for better satellite image enhancement technique.**

Index Terms— **Discrete wavelet transform, image equalization, interpolation, satellite image resolution enhancement.**

I. INTRODUCTION

Satellite images are used in many applications such as astronomy, study of geosciences and geographical systems. In the satellite images contrast plays a vital role in judging the quality of an image. The difference in the luminance reflected from two adjacent surfaces gives contrast whereas in the case of visual perception it is determined by the difference in the colour and brightness of an object with other objects.

The contrast of an image must be optimized in order to preserve the information when it is highly concentrated on a specific range. In order to overcome the above problem techniques such as general histogram equalization and local histogram equalization have been proposed in the literature [1]–[4].

In image processing interpolation technique is used to increase the number of pixels in an image. Interpolation technique has been widely used in many image processing applications, such as the facial reconstruction [5], the multiple description coding [6], and the image resolution enhancement [7]–[9]. Image enhancement using interpolation technique has been widely used in literature for providing a good quality of images. There are three popular interpolation techniques found in literature namely the nearest neighbour, the bilinear and the bicubic. Bicubic interpolation is more sophisticated than the other two techniques and produces smoother edges compared to the other two techniques.

Wavelets play a significant role in many image processing applications. The 2-D wavelet transform results in four decomposed subband images referred to as low-low (LL), low-high (LH), high-low (HL), and high-high (HH) bands covering the full frequency spectrum of the original image.

In this work, the results are compared with two state-of-the-art techniques. In the first method the singular value matrix of the low–low subband image is estimated and then the enhanced image is reconstructed by applying inverse DWT. The second technique is based on the interpolation of the high-frequency subband obtained by applying discrete wavelet transform (DWT) to the input image. The high-frequency subband image and the input low-resolution image are then interpolated and combined to generate a new resolution-enhanced image by using inverse DWT.

II. SATELLITE IMAGE ENHANCEMENT BASED ON SVD TECHNIQUE

The singular-value-based image equalization (SVE) technique as shown in [10, 11] is used for equalizing the singular matrix which is obtained by using decomposition of singular value matrix. The decomposition of an image, usually obtained in the form matrix is shown below:

$$A = U_A \sum_A V_A^T \quad (1)$$

where U_A and V_A are the orthogonal matrices and the $\sum_A$ is a matrix that contains singular values sorted along its diagonal element. The purpose of using the decomposed image is for the fact that it gives the intensity information of a given image [12].

In the literature work ([10], [11]), the decomposition method was used to overcome the illumination problem. The above method uses the ratio of the largest singular value matrix which is normalized and has mean of zero and variance of one, over a normalized input image which is obtained according to the equation shown:

$$\xi = \frac{\max(\sum_{N(\mu=0,\text{var}=1)})}{\max(\sum_A)} \quad (2)$$

where $\Sigma_{N(\mu=0,\text{var}=1)}$ is the normalized singular value matrix and the equalized image can be obtained using the equation shown below:

$$\Xi_{equalized_A} = U_A(\xi \sum_A)V_A^T \quad (3)$$

where $\Xi_{equalized_A}$ represents the equalized image *A* and the task is to eliminate the illumination problem.

A comparative method is introduced for the satellite image enhancement which is an extension of the SVE method. DWT is used to separate the input low contrast image into different frequency subbands, where the LL subband concentrates on the illumination information. Thus the LL subband goes through the SVE process, which preserves the high-frequency components (i.e., edges). Hence, after inverse DWT (IDWT) the resultant image will be sharper with good contrast.

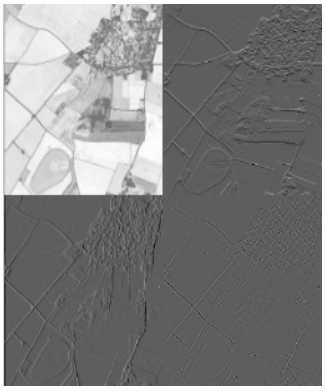


Figure.1 LL, LH, HL, and HH subbands of a satellite image are obtained by using DWT.

There are two significant parts in the proposed technique, firstly using the SVD technique and then applying the DWT method. LL band gives the information of illumination and the edges are concentrated in the other subbands (i.e., LH, HL and HH). Thus the high-frequency subbands are separated to protect from image degradation and the enhancement is applied only to the LL subband. Hence the final reconstructed image will be much enhanced and sharper compared to the original image.

The general histogram equalization method is used to process the input image *A* and the processed image is designated as $\bar{A}$. The correction factor for the singular value matrix for all the four subbands obtained from DWT method is calculated as shown below:

$$\zeta = \frac{\max(\sum_{LL_{\hat{A}}})}{\max(\sum_{LL_A})} \quad (4)$$

where $\sum_{LL_A}$ is the singular matrix of the Low-Low band for an input image and $\sum_{LL_{\hat{A}}}$ is the singular matrix of the Low-Low band for the output image using the proposed method. Finally the new Low-Low band image is obtained by

$$\bar{\sum}_{LL_A} = \zeta \sum_{LL_A}$$
$$\overline{LL}_A = U_{LL_A} \sum_{LL_A} V_{LL_A} \quad (5)$$

Now, the $\overline{LL}_A$, LH_A, HL_A, and HH_A subband images of the original image are recombined by applying IDWT to generate the resultant equalized image $\bar{A}$

$$\bar{A} = IDWT(\overline{LL}_A, LH_A, HL_A, HH_A) \quad (6)$$

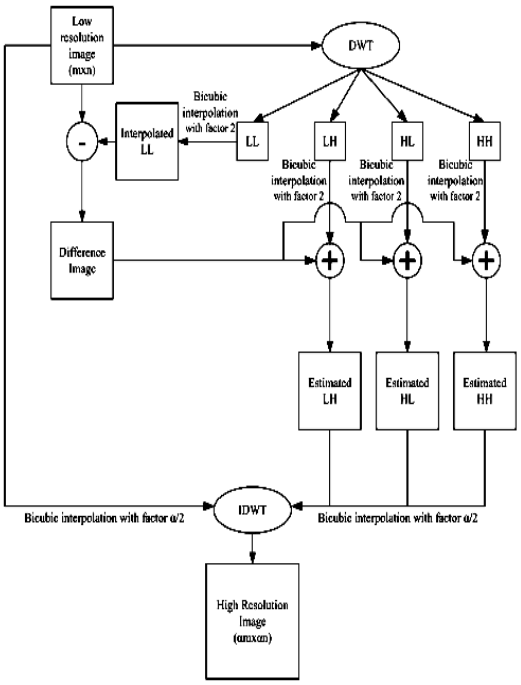


Figure.2 Block diagram of the proposed resolution enhancement algorithm

III. SATELLITE IMAGE ENHANCEMENT BASED ON DWT-BASED RESOLUTION ENHANCEMENT

In satellite imaging, resolution proves out to be an important feature and enhancement of the same becomes very important for the images. Enhancing the resolution of the input satellite images will affect the performance of the system. The high frequency components usually get affected or lost when interpolation technique is applied for enhancing the resolution of the satellite image. Preserving the edges becomes very important to increase the quality of an image. In this technique, the frequencies in high band are usually preserved by employing DWT [13] to the image. DWT method separates the image into four subband images namely LL, LH, HL, and HH. High-frequency subband contains the high frequency component of the input image. The interpolation method can be applied to these four subband images as shown.

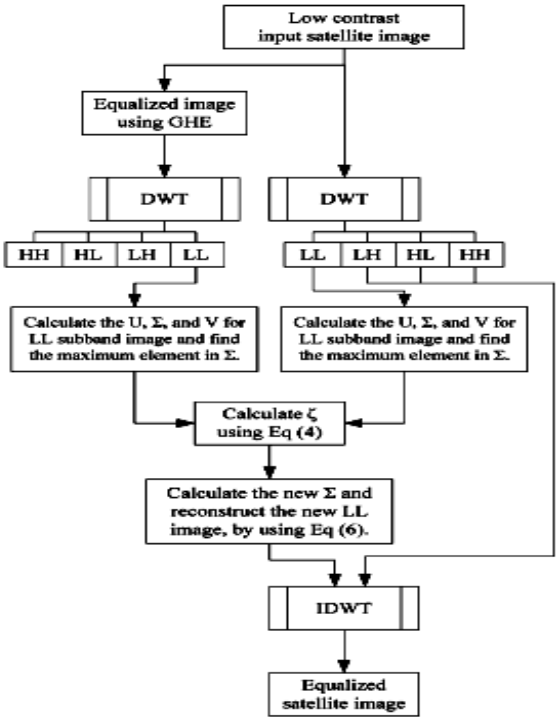


Figure.3 Algorithm for proposed equalization technique

A low-resolution image is obtained from the high-resolution image as in [14], [15], and [13] by making use of a low pass filter. The low resolution image (LL band) obtained without quantization is used as the input for the resolution enhancement process. Images with low frequencies contain less information as compared to the original image, so they are usually passed through the interpolation process and the resultant image is taken as input. Thus the input image is first interpolated with half of the interpolation factor $\alpha/2$ and then it is used to interpolate the high-frequency subbands as shown in Fig.2. To preserve the edges perfectly an intermediate stage is introduced in the high frequency band and a sharper enhanced image is obtained.

The low-resolution input image and the interpolated LL image will be highly correlated and the difference between them will give high-frequencies. Then an intermediate process is used to correct the estimated high-frequency components. The estimation is then carried out by interpolating the high-frequency subbands by a factor 2 and the obtained difference image is included into the high-frequency images. Finally the obtained image is interpolated by a factor $\alpha/2$ so that the process reaches the required size for IDWT process. The intermediate process will give significantly sharper and clearer enhanced image.

IV SIMULATION RESULTS

Figs. 1(a), 2(a) show the low-contrast images taken from aerospace and geosciences resources. These images have been equalized by using GHE [Figs. 1(b), 2(b)], SVE i.e. the proposed technique [Figs. 1(c), 2(c)] and the Enhanced Image [Figs. 1(d), 2(d)]. The proposed equalization method proves out to be better in terms of quality than general histogram equalization method. It produces sharper and brighter edges.

The technique using Bicubic Interpolation is tested on several satellite images. When this technique is applied on a low-resolution satellite image, the enhanced images are shown in the figures below.

It is evident from the obtained figures that the proposed technique produces sharper edges than the other techniques. Fig.7 shows (a) Low-resolution image (b) high-resolution image obtained by using bicubic interpolation on LL Subband, (c) interpolation on HL Subband, (d) Interpolation on HL Subband, (e) Interpolation on HH Subband.

Figs. 4, 5 and 6 show the effectiveness of the proposed SVD and DWT based Resolution Enhancement methods over the standard GHE, the Bicubic interpolation and the Bilinear Interpolation based satellite image resolution enhancement techniques. Different benchmark images with different features are used for the comparison.

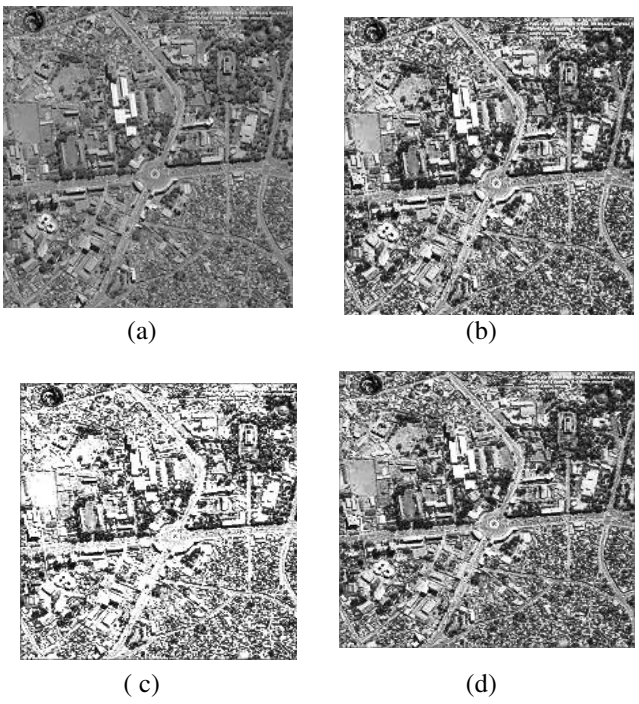


Figure. 5. (a) Original low-contrast image. Equalized image by using (b) GHE, (c) Proposed technique (d) Enhanced Image

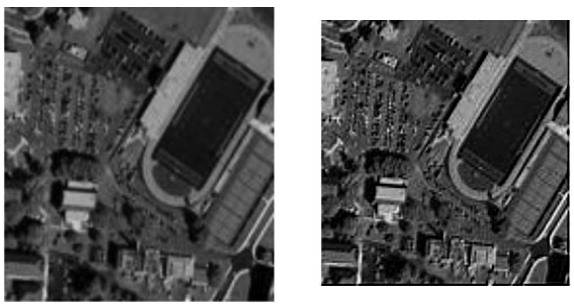
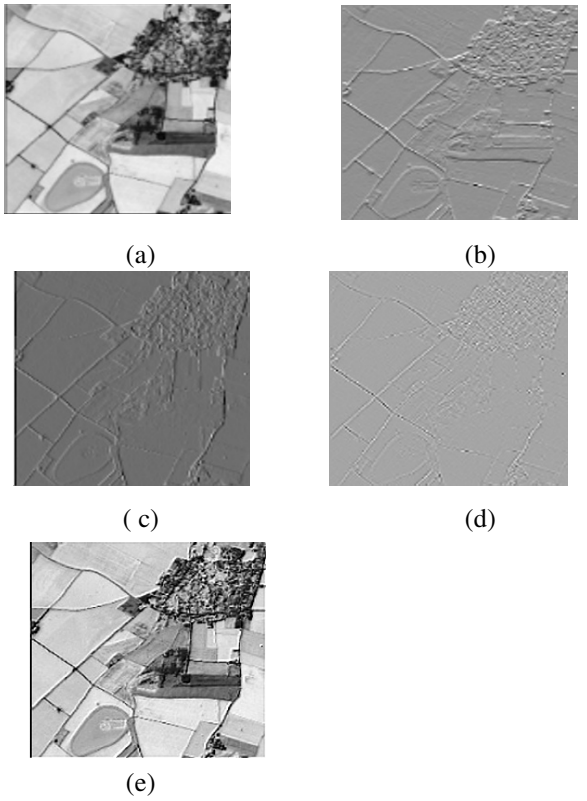


Figure.6 Low Resolution (a) Input Image (b) High Resolution Output Image, High Resolution Image

(c) (d)

Figure.6 Low Resolution, (c) Bicubic Method (d) Bilinear Method



(a) (b)

(c) (d)

(e)

Figure 7 (a) Low-resolution image (b) high-resolution image obtained by using bicubic interpolation on LL Subband, (c) interpolation on HL Subband, (d) Interpolation on HL Subband, (e) Interpolation on HH Subband.

CONCLUSIONS

In this work, a comparative analysis on satellite image contrast enhancement techniques is shown based on the DWT and the SVD methods. In the former, making use of DWT method, singular value matrix of the LL subband is obtained and then updated, and finally the enhanced image is reconstructed by using IDWT. The technique is also compared with the GHE method. On the contrary, the later technique is based on the interpolation of the high-frequency subband images obtained by DWT of the input image and the visual comparison is seen through the simulation results obtained.

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Design of Multilevel Multicarrier H-Bridge Inverter fed Induction Motor Drive

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***Abstract*—The design of H-Bridge Multilevel-multicarrier inverter fed variable frequency drive is discussed. A nine level inverter is proposed to drive a half hp induction motor. Simulation studies carried out on Single phase and three phase inverters using Simulink/MATLAB. The results are compared with a hardware module of single phase multi carrier inverter. The design aspects of three phase multicarrier inverter including the transformer design are presented in this paper.**

Index Terms*—Multilevel, H-bridge, SPWM, induction motor control, variable frequency drive, Total Harmonic Distortion (THD)*

I. INTRODUCTION

Multilevel inverter is one of the areas in which a lot of research is taking place. Multilevel inverters are used in many applications like interface between photovoltaic systems and utility grids[1][2], motor drives [3], amplifiers used in broadcasting [4], and Power system applications like FACTS controllers [5]. Multilevel inverters can be classified into: 1. Cascaded H-Bridge 2. Diode clamped and 3. Flying capacitor type. Each type mentioned above can be designed in different topologies like basic stepped wave, Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM). The design of H-Bridge Multicarrier inverter using SPWM topology is presented using a simple control circuit. It is a s low cost option compared to multilevel inverters using advanced digital controllers like FPGA, DSP etc.,[6]. Another low cost alternative is the microcontroller based basic stepped wave inverter. But it has high THD value.

II. CASCADED MULTI LEVEL INVERTER

The H-Bridge inverter comprises of different H – bridges connected in series as shown in figure 1. Each H-Bridge will be fed from an isolated DC power supply. The switching logic of the MOSFET/IGBTs in the bridge decides the output pattern of voltage and it's THD. A three level inverter output voltage swings over three levels of voltages (+v 0 -v). The three voltage sources share the load current depending on the active period conducted by the switches of the bridge concerned. Two bridges required for designing a five level inverter. The general expression for the number of levels is n = (2b+1), where b = number of bridges.

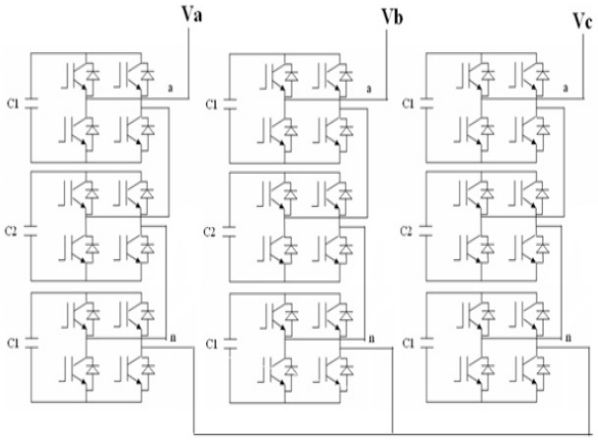

Figure.1 Three-phase 7-level cascaded multilevel inverter (Y-configuration)

III. SPWM TOPOLOGY

One of the methods of describing voltage-source modulation is to illustrate the intersection of a modulating signal (duty cycle) with triangular waveforms.

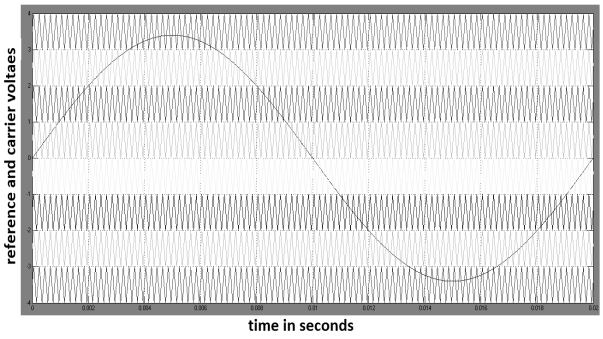

Figure.2. Comparative view of reference and carrier signals

If modulation index (MI) is not an integer, there may exist sub harmonics at output voltage. If the normalized carrier frequency (m_f) is not odd, DC component may exist and even harmonics are present at output voltage. m_f should be a multiple of 3 for three-phase PWM inverter. The carrier-based modulation schemes for multilevel inverters can be generally classified into two categories: phase-shifted and level-shifted modulations. Both modulation schemes can be applied to the cascaded H-bridge (CHB) inverters. A level shifted modulation scheme with eight carrier signals are shown in figure 2.

An m-level CHB inverter using level-shifted multicarrier modulation scheme requires (m-1) triangular carriers, all having the same frequency and amplitude. The (m-1) triangular carriers are vertically disposed such that the bands they occupy are contiguous.

IV. EXPERIMENTAL RESULTS

Based on the simulink software, simulations are performed to verify the performance of multilevel inverter. Figure 3 and figure 4 shows the simulation results of 9 level multicarrier inverter and figure 5 shows the THD result. The simulation parameters are set as follows: The DC input voltages to the H-bridges is 80 V, the switching frequency is chosen to 1 kHz. The modulation index is set to 0.95. The load resistance is 1KΩ.

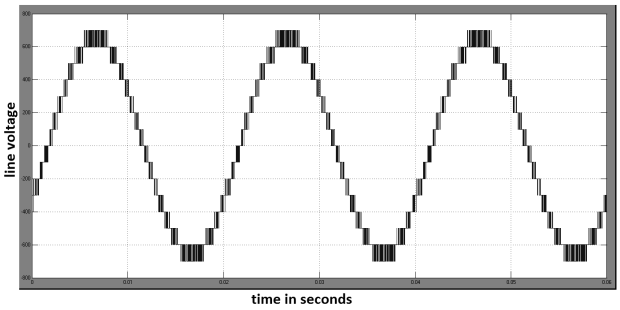

Figure 3. Line voltage of 9-level inverter

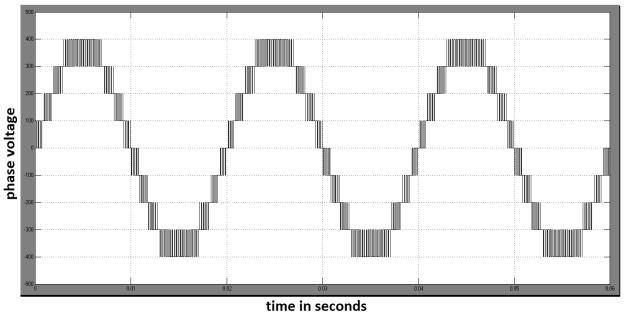

Figure 4. Phase voltage of 9-level inverter

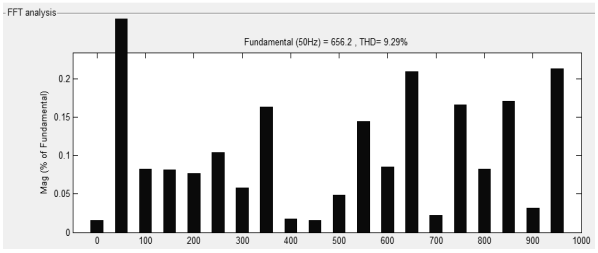

Figure 5. THD (9.29%) of 9 level inverter

The simulation results for the modulation index 0.8 are shown in figures 6 and 7. The THD result is shown in figure 8.

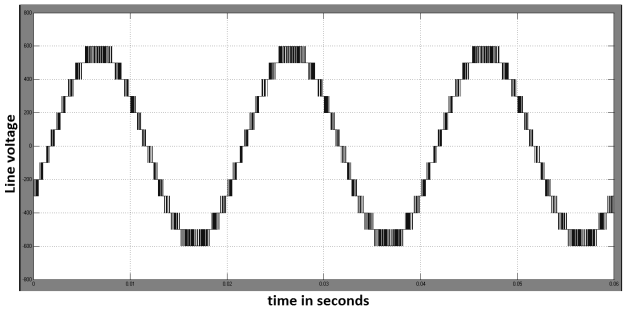

Figure 6. Line voltage at MI=0.8

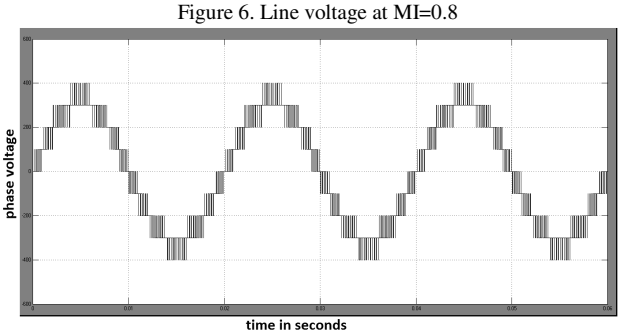

Figure 7. Phase voltage at MI=0.8

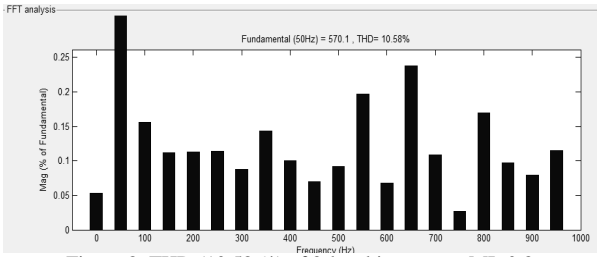

Figure 8. THD (10.58 %) of 9-level inverter at MI=0.8

V. HARDWARE DESCRIPTION

Hardware design of this 9-level inverter involves two main parts. a) Control circuit, b) Power circuit.

The control circuit comprises of a reference sine wave which is stepped down from 230v AC line. A phase shifter circuit is used to produce three phase reference signals shown in figure 9. A triangular wave is generated from an analog IC (XR2206) and is clamped to eight desired levels using clampers (level shifters) shown in figure 10. The phase and level shifters are designed using 741 op-amps.

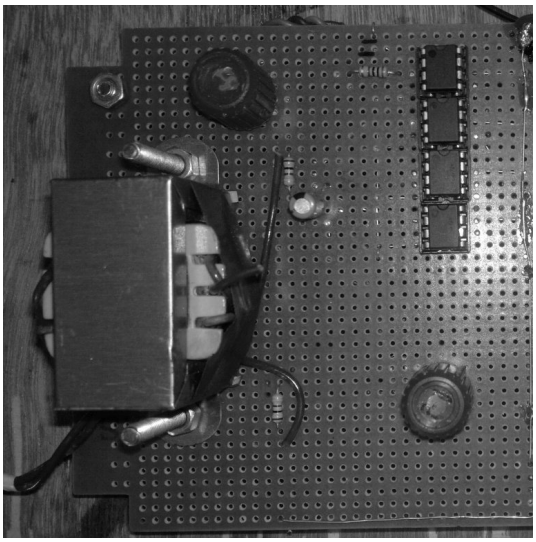

Figure 9. Op-amp 741 based Phase shifter circuit

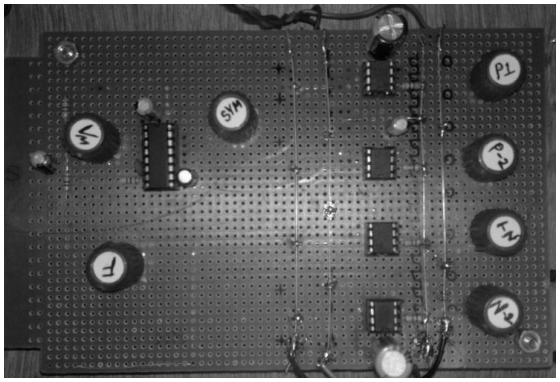

Figure 10. Triangular wave generator and clampers

Each phase of sine wave signal is compared with 12 comparators to generate triggering pulses for 4 switching states per phase. Each MOSFET requires an optocoupler and a separate DC supply is required to drive the optocoupler and hence the MOSFET. Each bridge requires three isolated dc power supplies (typically 12v) and therefore total 36 sources are required for the complete three phase 9 – level inverter (four bridges / leg).

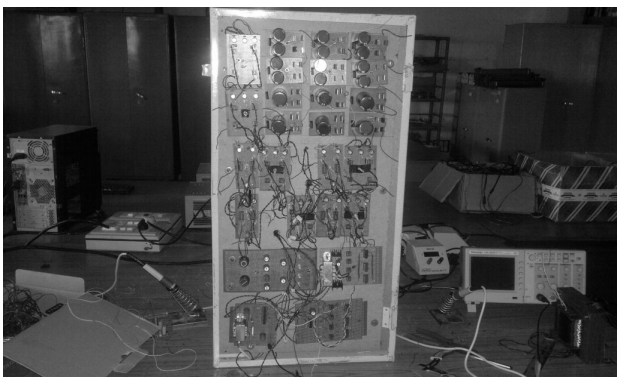

Figure 11. Hardware module of 9 – level CHB inverter

In addition to this, each bridge requires its own DC link power source. So, total 12 DC power sources required for the inverter. Each power supply rated V_{peak} / (no. of bridges in a leg) = (230*1.414)/4 = 81v. The specifications of the transformer are given in the Table 1. The power and optocoupler transformers are shown in figure 12.

TABLE I
DESIGN SPECIFICATIONS OF TRANSFORMERS

	Vp	Ip	Vs	Is	Np	Ns	Sec. coils
Power transformer	230v	2.5A	81v	0.6A	345	122	12
Optocoupler transformer	230v	100mA	12v	50mA	432	23	36

Transformer winding calculations

1. Power transformer (575VA)

   E = 4.44*f*B*A*N

   Therefore, turns/emf = 1 / (4.44*f*B*A)

   For steel core, B = 1 ~ 1.3.

   Let B = 1.2.
   Cross section area of 575VA core is 5x5 cm^2 = 25cm^2.
   Turns / emf = 1.5 turn / volt.
   For primary: 230*1.5=345 turns, 19AWG.
   For secondary: 81*1.5=122 turns, 25AWG.

2. Optocoupler transformer (23VA)

3. Cross section area = 4x5 = 20cm^2

   Emf / turn = 1.88 turn/volt

   For primary: 432 turns, 30AWG

   For secondary: 23 turns, 30AWG

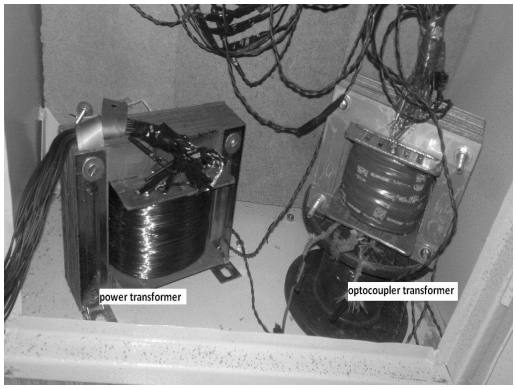

Figure 12. Power and Isolation Transformers

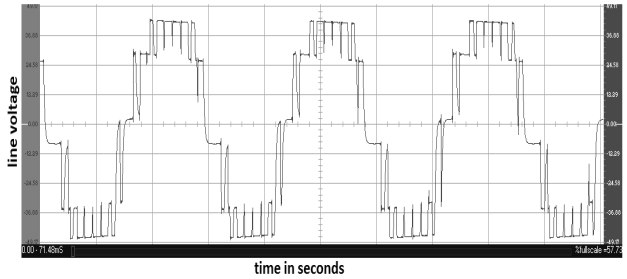

Figure 13. Output of 5 – level CHB inverter

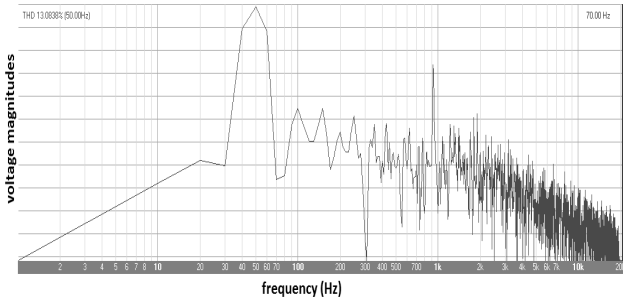

Figure 14. THD of 5 – level CHB inverter

CONCLUSIONS

The H-bridge inverter is designed and fabricated with the proposed concept and is fed to a 1/2hp induction motor drive shown in figure 11. The practical THD results are approximately equal to the simulation results and are shown in the figures 13 and 14. A detailed study on designing a transformer made the module simplified and compact in size. The experiment is conducted on low power motor but the power modules are designed for full load 7A motors. So, this set up is capable of driving medium level motors too.

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Smart Meters in Future Power Grid: A Review

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Abstract— **Smart meter is the most important modern energy meter in smart grid. Apart from measuring energy consumption, it also provides additional information to the utility company and the consumers for effective energy management. Integration of smart meters into electricity grid involves implementation of various communication technologies and software depending on the features that the situation demands. This paper outlines some features and benefits of a smart meter, current status as well as various future projects of smart grid development in top five electricity generating countries worldwide. In addition, it introduces some basic communication technologies used in smart grid and the challenges of smart meters in the future.**

Index Terms— **Smart grid, Smart meter, Communication technologies, Advanced Metering Infrastructure (AMI).**

I. INTRODUCTION

A traditional grid is an electrical system that supports operations like generation, transmission, distribution and utilization of electricity. The conventional power grids are generally used to carry power from a few central generators to a large number of consumers but there is no two-way communication that allowing interaction between end users and the grid. A smart grid is a modern electrical grid in which electricity and information flows in two-way to improve reliability, efficiency, sustainability and economics of the grid. By utilizing modern information technologies, the smart grid is capable of delivering power in more efficient ways and it could respond to events that occur anywhere in the grid. Table I shows a brief comparison between the existing grid and the smart grid [1].

One of the important way to modernize the present electric grid into a smart grid is the use of smart meters. It is a modern energy meter which gathers information from the users, load equipment and calculate the energy usage of consumers therefore provides additional information to the power company and / or the system operator.

A variety of sensors and control devices and supportive communications infrastructure are used in smart meters.

TABLE I
COMPARISON BETWEEN THE TRADITIONAL GRID AND THE SMART GRID

Conventional grid	Smart grid
communication is one-way	communication is two-way
electromechanical	digital
centralized generation	distributed generation
limited control	pervasive control
manual monitoring	self monitoring
manual restoration	self-healing
failures and blackouts	adaptive and islanding
limited sensors	more sensors
less customer choices	more customer choices

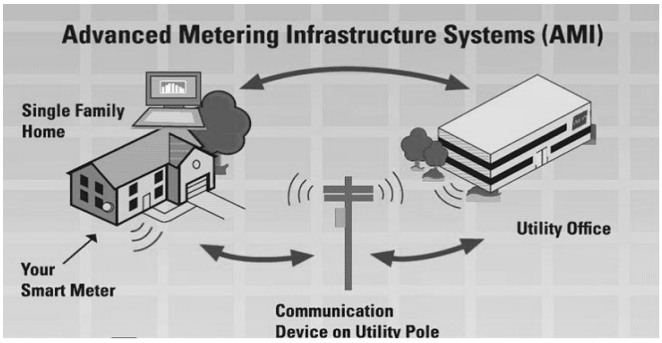


Figure 1. The Advanced Metering Infrastructure (AMI) System

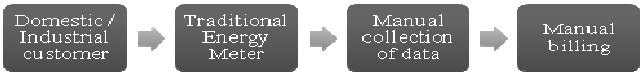
AMI network is shown in figure 1. It is in fact the collective term to describe the whole infrastructure that includes smart meters, two-way communication network and control center equipment. The control center equipment is connected to all the applications that gather and transfer energy usage information in real-time. AMI makes two-way communications with customers and is the backbone of smart grid. The objectives of AMI are remote meter reading with error free data, network problem identification, load profiling, energy audit and partial load curtailment in place of load shedding.

The remaining paper is scheduled as follows. section II describes smart meter design, functions and benefits; section III aims different countries government's present and future policies in brief; section IV outlines communication network and its related issues; section V explains the challenges of a smart meter and conclusions are drawn in Section VI .

II. SMART METER

A smart meter is usually an electronic device that records consumption of electric energy in intervals of an hour or less and enables real-time communication of energy usage data between customers and their utility companies for monitoring and billing purposes. The vast majority of these meters are installed at the residential level. In order to carry out a meter reading using a conventional meter, the meter reader needs to physically visit the customer premise and take the reading. This reading will be sent to the utility company for billing. But in case of smart meters this can be done automatically. The system operator will create a meter read request from the utility company office thus avoids manual intervention during meter reading and provides more accurate, real-time data to the utility company. Figure 2 shows the block diagrams of a traditional energy meter and a smart meter [2].

Conventional Energy Meter



Smart Energy Meter

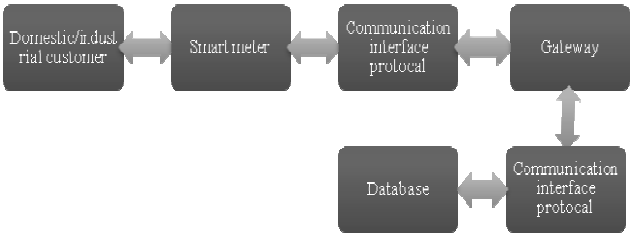


Figure. 2. The architectures of a conventional energy meter and a smart meter

A smart meter consists two units. One unit of the metering device is in the custody of the distribution or utility company and the other is the display unit which is at consumer's place. A smart meter has designed with built-in-technology to disconnect and reconnect certain loads remotely. Smart meters are implemented to monitor as well as to control end users and appliances to manage demand and load flow in the future. Smart meter's data comprises the unique meter identifier, data timestamp, the electricity utilized values and so on. Smart meters can gather diagnostic information about the distribution grid and home appliances and measures energy consumption from them to identify parameters and transfer the data to utilities and send back to the command signals in order to calculate the customer's bill and power consumption accordingly. Sometimes, a smart meter can also communicate with the other smart meter. Figure 3 shows the original model of a smart meter. Smart meters, which enable real-time communication of energy usage data between consumers and their utility companies, generate electric usage readings for every 15 minutes or one hour.

Figure 3. An actual model of a smart meter [3]

A. The main functions of a smart meter

Generally, smart meters are expected to have the following features like:

1. Two-way communication
2. Data collecting, recording and storing
3. Load control function
4. Programming function
5. Security function
6. Display function
7. Billing function

B. Advantages of a smart meter

The benefits of installing smart meters are numerous for many different stakeholders in different aspects of the smart grid system [4].

Smart metering advantages to consumers:

- It gives the customer more accurate and timely electrical billing.
- Consumers are able to estimate bills from the collected information of smart meters thus manage their energy consumption to reduce their electric bills.
- It helps the customer in a better way to use the electrical equipment during the expensive hours. Time of Use (ToU) tariff will offer choice to consumers to reduce the electricity consumption during peak hours which will bring considerable savings in their bills.
- It facilitates customers to switch/delay their electrical equipment to less expensive hours. For e.g. it offers homeowners and business owners a new level of energy intelligence with near real-time energy use data.
- There exists a high speed communication system between utility and customer.
- The smart meter will help in a faster restoration of the grid in case of faults or disturbances.

Smart Metering advantages to utilities:

- Lot of money can be saved by improving the remote area reading and billing system.
- Utility can better manage during peak load times.
- It makes more efficient use of energy and grid resources. Smarter systems will help integration of renewable energy to the grid and by deploying smart micro grids and encouraging distributed generation; power will be accessible to the remote areas as well.
- It offers a new tariff model in the electricity market.
- It improves the transformer load management for the transmission line.
- Utilities can control the power supplied to consumers.
- The accuracy of smart meter enables enhanced monitoring of system resources, which detects and mitigates energy threats on the grid by cyber-terrorist.
- AMI systems that track energy usage will help monitor power almost in real time thus leading to increased system transparency thus prevents loss due to electricity theft.
- Smart meters can also be used to shut off service to households and commercial establishments that don't pay their bills.

- Using smart meters, the companies can limit the maximum electricity consumption and tries to encourage users to reduce their demands in the periods of peak load.
- The data collected by smart meters is used by utility to realize real-time pricing.
- Utility company can terminate or re-connect electricity supply to any consumer with a proper mechanism remotely in order to optimize the power flows according to the information sent from demand side.

Smart Metering advantages to Governments:

- It stimulates the economy by investing in smart metering networks.
- By increasing the awareness of consumption pattern, there will be a reduction in electricity consumption.
- Better load forecasting can be obtained for power grid and it will prevent large-scale black outs.
- The data given by smart meters helps in improving efficiency and reliability of service.

III. PRESENT CONDITION IN TOP FIVE ELECTRICITY GENERATING COUNTRIES

A. China

The advancing smart grid construction in China spurred the constant growth of smart meter demand. A primary element of this transformation is the deployment of interactive technologies, including smart meters for residences and businesses. The installed smart meters in China will reach 377 million by 2020, growing from 139 million in 2012. The emerging rate for smart meters will reach 74 percent in 2013 and the figure is expected to hit 500 million in 2015. The main reasons for this progress are [5]:

- The main force behind the efforts to construct the country's smart grid is the State Grid Corporation of China (SGCC). It is the government-owned electric utility that leads the market by a large margin
- China's metering program initially had the goal of installing smart meters in 95 percent of household by 2015, but the end date has been pushed forward to 2017 due to some reasons.
- Profiles are provided more than 40 main industry players, classified by different industries, along with forecasts for smart grid revenue and smart meter shipments through 2020.
- Tenders were invited by SGCC for smart meters as early as 2009 and as of September 2014, 21 tenders for a total of 310 million smart meters were invited, in which 3 tenders for 61.877 million smart meters were completed during Jan-Sept. 2014.

B. USA

The number of installed smart meters in the US grew by 33% between May 2012 and July 2013. Figure 4 illustrates the historic and estimated path of smart meters installation in the US through 2015. This represents approximately 675,000 smart meters installed per month between now and the end of 2015 [6].

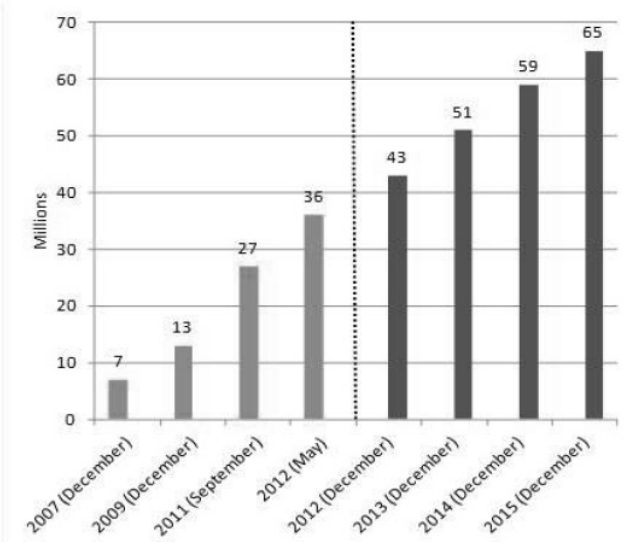


Figure .4, smart meter installations in the US: 2007-2015 (millions)

Some other policies regarding smart meters are:

- As of May 2012, Institute of Electrical Engineers (IEE) found that almost one-in three households now have a smart meter. By mid- decade, more than half the households in the country will have a smart meter [7].
- Based on submitted and approved AMI business plans, responses to survey questions and other public information, IEE finds that as of May 2012, 36 million smart meters have been installed and IEE estimates that approximately 65 million smart meters will be deployed by 2015.
- The electric power sector is providing benefits to consumers through information gathered by smart meters. By the end of 2012, 22 utilities in 16 states will have smart meters fully deployed to their entire consumers , representing 29 million consumers.
- Millions of utility customers already have their energy usage data recorded by smart meters and the industry is working to translate the detailed smart meter data into customer-friendly information.

C .Russia

Russia is pursuing the state policy of innovation activity in the electricity sector. This applies to energy efficiency, renewable energy and smart grids. The energy strategy of Russia for the period up to 2030 aims at ensuring high energy, economic and environmental efficiency in the production, transport, distribution and demand of electricity. Russia has recorded a major reduction in losses and an increase in capacity to supply more power to customers since implementing a smart metering system [8].

Some National policies on smart meters are, such as:

- Smart meters and accounting systems should be installed at all participants of electricity market and thermal power in power plants and substations, in enterprises, and with the year 2012 in accordance with

the Federal law No. 261-FZ dated 23.11.2009. The U.S. Company, in a partnership with Perm Energo – a division of the MRSK group and one of Russia's largest utility providers, was awarded a contract to network 10,000 homes as part of a 50,000 home test project that will be monitored by the Russian government for potential rollout across the country.

- Russia wants to reduce energy intensity - a measure of usage by 40 percent by 2020 to modernize Soviet-era companies.
- Echelon - which operates in Russia in partnership with local firm Energo Audit Control (EAC) said it should sell 200,000 meters in Russia next year, up from 100,000 in 2012.

D .Japan

Tokyo Electric Power Company (TEPCO)'s 27-million unit smart meter project is not just about smart meters but also about creating an end-to-end, citywide energy management platform meant to link meters, utility enterprise platforms and smart devices in homes and businesses [9]. TEPCO and its fellow utilities recently saw their smart meter deployment plants put on an increasingly fast track in hopes of managing the country's ongoing post-Fukushima energy crisis, as well as to prepare for a potential shift to a deregulated energy market in 2016.

Here's how this project is breaking new ground.

TEPCO wants all three flavors of meter network not just for meters, but for devices in homes and businesses. Toshiba , Landies and Gyy's work on the technology needed to meet TEPCO's multi-model metering communications plans involves multiple meter manufacturers, all building to a modular design that can permit the swapping out of three flavors of communication.

TEPCO needs its smart meter network to scale big and scale both ways. TEPCO's 27 million smart meters are each meant to network with multiple in-premise devices with scalability from the individual components back to the head-end, to deal with those huge volumes of meter data.

E. India

India operates the world's largest synchronous grid covering an area of 3.28 million square kilometers with a connected capacity of 235 GW and about 200 million customers. Even though 79 million households in India do not have access to electricity, but it's per capita consumption is one fourth of world's average[10].

Smart grid vision for India is "Transform the Indian power sector into a secure, adaptive, sustainable and digitally enabled ecosystem that provides reliable and quality energy for all with active participation of stakeholders"

In 2013, Government of India (GoI) issued "Smart Grid Vision and Roadmap for India" which is a 15 year roadmap for transformation of Indian power system to smart grids. With the recent activities around 14 smart grid pilot projects in different states, India has emerged as the hot destination for smart grids. India Smart Grid Forum (ISGF) is a public private partnership initiative of Ministry of Power (MoP), for accelerated development of smart grid technologies in the Indian power sector. ISGF was setup in 2010 to provide a mechanism through which academia, industry, utilities and other stakeholders could participate in the development of Indian smart grid systems and provide relevant inputs to the government's decision-making.

ISGF has 10 Working groups. They are:

1. Advanced Transmission
2. Advanced Distribution
3. Communications
4. Metering
5. Load Control
6. Regulatory & Policy
7. Architecture & Design
8. Pilots and Business Models
9. Cyber Security: newly formed
10. Renewables & Micro grids: newly formed

The metering group aims are to assess the metering scenario in India and also to identify it's requirements and goals. The group 4 also focus on the available technologies and the best practices as well as identifying the gaps in existing solutions from an Indian perspective. It is worth mentioning that for Restructured Accelerated Power Development and Reforms Program (R-APDRP) metering applications the IEC 62056 It is worth mentioning that for Restructured Accelerated Power Development and Reforms Program (R-APDRP) metering applications the International Electrotechnical Commission (IEC) 62056 is chosen as the standard metering protocol. Central Power Research Institute (CPRI) has the test facility for carrying out conformance test for this protocol standard. The metering group can extend the additional design and standards required for smart meters. Metering group scope is such as:

- Study of country wide metering and billing practices. This includes Automatic Meter Reading (AMR) projects, merits & demerits, understanding of present technology, regulatory provisions, Electricity Act (EA) and requirements for AMI infrastructure.
- To design different smart meters for single-phase and three- phase customers.
- To analyze different communication technologies. Information requirements.
- To analyze different information and interface device requirements. .
- Meter Data Management Systems (MDMS).

India Smart Grid Task Force (ISGTF), launched along with ISGF is an inter-ministerial government task force. ISGTF mooted the idea of promoting 8 smart grid pilots in the country in different distribution utilities and it has 5 working groups, such as:

1. Pilots on New Technologies
2. Loss Reduction & Analysis
3. Power to Rural/Urban Areas
4. Distributed Generation & Renewables
5. Cyber Security

Smart Grid Vision and Road map for India has planned as, the 12th five year plan (2012-17) road map of smart grid will meet the expectations of customers, the 13th five year plan (2017-22) of smart grid vision for India will

meet the requirements of utilities and the 14th five year plan (2022-27) will hit government and regulators expectations.

IV. THE INFORMATION AND COMMUNICATION TECHNOLOGIES

The communication medium in an AMI system must ensure the communication between the smart meters and the central computer at the service provider. The communication structure can be wired like Power Line Carrier (PLC) or wireless like Global System Mobile (GSM), ZigBee, Radio Frequency (RF) and Wide Area Measurement System (WAMS). The chosen way must take into account the distance between the devices and existing infrastructure [11].

The following are the factors that impact the selection of communication technology [12]. :

- Evaluation of the existing infrastructure.
- Impact on legacy equipment, functionality, technical requirements as well as the economic impact to the utilities and consumers.

A. Power Line Carrier Communication (PLCC)

PLCC is an approach to utilize the existing power lines for the transmission of information. In today's world every house and building has properly installed electricity lines. By using the existing AC power lines as a medium to transfer the information, it becomes easy to connect the houses with a high speed network access point without installing new wings. The data collected by smart meter can be transmitted to utility central collection point by using the utility power lines. Then the delivered data is further processed and analyzed. [11]. PLCC technology has some advantages like, it can improve cost effectiveness for rural lines, and make it possible to work for the remote area or over long distances. This technology also has some drawbacks like, it has longer data transmitting time than wireless, higher cost in urban areas and less bandwidth.

Some research has been conducted in the PLC area . Rakesh Rao [13] presented a method for identifying outlines among a set of smart meters by measuring the PLC signal strength between the communication node (transmitter) and residential smart meters. The PLC signal is used as a proactively avert local power outages. Mojtaba Rafiei [14] propose a practical smart metering approach which can be used for both type of AMR and AMI by using combination of PLC and Wi-Fi protocols. Liang Dong [15] present the noise characteristic and transmission characteristic of the power line channel at first, then establish the basic power line channel model according to measured data.

B. Radio Frequency (RF)

The collected data from end users is transmitted to data collector through wireless radio frequency using smart meters. Then, the data is processed and delivered in several methods to utility data systems at a central collection location. The utility billing, outage management and other systems use these data for operational and business purposes. The RF technologies are classified in to two. They are:

Mesh Technology:

The smart meters talk to each other to form a Local Area Network (LAN) cloud at the collection point. The collector transmits the data using different Wide Area Network (WAN) methods to the utility central location [11].

1. The mesh RF technology has some advantages, such as large bandwidth, acceptable latency and a typical operational frequency of 915MHz.
2. The mesh RF technology also has some drawbacks, such as proprietary communication, the topography and long distance issues for the remote areas.

Point to Point Technology:

In this technology, smart meters talk directly to a collector, usually a tower. The tower collector transmits the data using various methods to the utility central location for processing [11].

1. Point to Point RF technology has some advantages, such as large bandwidth, little or no latency, direct communication with each endpoint, better throughput, and can cover longer distances.
2. Point to Point RF technology also has some disadvantages, such as the topography, long distance issues for remote areas, proprietary communications and less interface with Distribution Automation (DA) devices.

C. Cellular networks

Public cellular networks use in smart grid is slowly gaining a acceptance and acceleration across the world. Cellular network is now commonly seen as an additional connectivity option just like PLCC and RF mesh. Global System for Mobile communication (GSM) is a digital mobile telephony system that digitizes and compresses data before sending it. The main advantage of the GSM is its widespread use throughout the world and the use of Subscriber Identity Module (SIM) cards to send Short Message Service (SMS). [16].

D. ZigBee

ZigBee is a low-cost, low-power, wireless mesh networking standard. It is best suited for local coverage such as Home Area Networks (HANs). Smart grid considers ZigBee as a main communication as it controls the appliances automatically. ZigBee installation and upgrade cost is low, in addition it offers meter-to-meter communication and remote monitoring ability of whole home conditions [17].

Smart energy meters using both ZigBee and GSM technologies should have a transmitter and a receiver with both technologies. The meter can read the energy and send it to the receiver using GSM or ZigBee. The data management system collects and stores the data and uploads it to the internet. So, the consumer can check his information from the internet using a developed android program or through a website portal. The receiver can also send the consumption information to the user by an SMS message through the GSM network [16].

E. Web Access Management System (WAMS)

WAMS is a solution for obtaining accurately time synchronized measurements of electrical parameters of a power grid, spanning over wide geographical areas such as large regions and even entire nations. The analysis of WAMS data provides a real-time view of the grid condition, allows certain situations to be predicted and preventative action taken to avoid large scale outages or blackouts. WAMS enhances the the functionality of traditional operation technology such as Supervisory Control And Data Acquisition (SCADA) systems by collecting more data from devices called Phasor Measurement Units (PMU) situated at strategic positions with in the grid [10].

A typical SCADA system measures the magnitude of electrical parameters such as voltage, current, frequency and power at a rate of 1 sample per second but WAMS measures both the magnitude and phase angle of electrical parameters at about 30 to 120 samples per second with accurate synchronized time-stamping. This feature enables WAMS to provide a real-time view of grid conditions. More data, faster access to data and real-time analysis of data provides situational awareness to grid operators, enabling them to take intelligence based and timely control actions to preserve the grid's stability and efficiency.

The key is that WAMS provides much more information with higher resolution and clarity, as compared to traditional operational technology.

V. THE CHALLENGES OF SMART METER

Despite its widespread benefits, deploying smart meters presents three major challenges that include:

1. High Capital Cost: A full scale deployment of AMI requires expenditure on all hardware and software components, smart meters, network infrastructure and network management software along with cost assosiated with the installation and maintenance of meters and information technology systems.

2. integration: AMI is a complex system of technologies that must be integrated with utilitie's information technology system, including Customer Information Systems (CIS), Geographical Information Systems (GIS), Outage Management Systems (OMS), Work Management Systems (WMS), Mobile Workforce Managemet (MWM), SCADA sytem, Distribution Automation System (DAS) etc.

3. Standardization: Interoperability standards to be defined, which set uniform requirements for AMI technology, deployment and general oprations are the keys to successfully connecting and maintaining an AMI based grid system.

CONCLUSIONS

This paper reviews several important aspects of smart metering. It presents the advantages of a smart meter system from the point of view of consumers, utilities and governments respectively. In addition, it presents the current situation and future objectives of leading countries in terms of electricity generation. Moreover, research related to different communication technologies is presented in detail. Finally, the paper arises various challenges to be met by the smart meter.

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The Test Bench for FPGA-based QPSK and QAM Modulators in Software defined radio

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***Abstract*—In todays fast evolving mobile communications the requirements of higher data rates are continuously increasing, pushing operators to upgrade the back haul to support these speeds. A cost effective way of doing this is by using microwave links between base stations, but as the requirements of data rates increase, the capacity of the microwave links must be increased. The objective of the paper is the developing the next generation high speed microwave links for the E-band. In the research project there was a need for a testing system that was able to generate a series of test signals with selectable QAM modulations and adjustable properties to be able to measure and evaluate hardware within the project. The developed system was designed in a digital domain using an FPGA platform from Altera, and had the ability of selecting several types of modulations and changing the properties of the output signals as requested. By using simulation in several steps and measurements of the complete system the functionality was verified. The developed system can be used to test several different modulators in other projects as well and is easily extended to provide further properties.**

***Index Terms*—FPGA, Signal generation, Quadrature modulation, QPSK, Software defined radio, Testbench, Radio communication, High datarate.**

I. INTRODUCTION

As the demand from customers of Internet capacity within mobile networks increase, the operators need to improve the capacity of the entire network continuously. To connect sub networks and antennas to the backbone of the network, several linking methods exist to create a backhaul. The paper aims at developing a microwave link with increased data capacity to be used in a back haul. The application of the paper is to demonstrate a 10 Gbps radio system over E-band. The following text is cited from the project specification [1] and provides a general idea of the purpose of the application. A general knowledge in radio communications will ease the understanding. This paper work is aiming at solutions for spectrum efficient radio communication at the E-band 71-76, and 81-86 GHz, and the 120 GHz band. The E-band is now gaining an increased interest for telecom operators providing internet access over the mobile network where radio links are used for the backhaul. The driving force is the demand from customers to have mobile access to internet for streaming video etc. The E-band provide 2*5 GHz bandwidth, commercial radio links for the E-band often use the modulation format OOK, which is simple but not spectrum efficient. The goal of this work is to investigate solutions for spectrum efficient use of the E-band and higher frequencies like 120 and 220 GHz-band, and as a result increase the bit rate at least by a factor of four utilizing the same bandwidth. In this paper, several solutions will be implemented and tested. The first solution is based on D-QPSK modulation, which uses a precoder realized in FPGA. This solution is more complex than the OOK-based system but is more spectrum efficient, by a factor of two. Like the OOK, the D-QPSK is non-coherent i.e. the phase of the carrier is not needed to be retrieved. For higher spectrum efficiency, more complex modulation is required like QAM. In a QAM signal, the data is represented by both amplitude and phase of the modulated carrier, the carrier phase reference have to be retrieved in the receiver, and both the amplitude and phase have to be detected. Therefore D/A converters are needed in the modulator of the transmitter and A/D converters in the receiver. Some of the simpler modulation formats will be realized in hardware while QAM will be realized using software in FPGA's.

The relation between application and this paper work provides an understanding of the purpose. The project purpose is to investigate several different options and types of modulators and modulations, and the efficiency of these. To provide a flexible way of testing the transmission and modulation properties of products within the project, a proposal of developing a test bench
as a paper was laid out. This paper is the result of that proposal. The focus within paper was on implementation of a system to be used for testing products within the application. The system that was implemented provides a way of measuring properties of different options that are selectable in the project to be guidance in crossroads with focus on modulation type. Outside of the scope of the paper, the test bench will also be usable for other components in the project but this will not be considered during implementation due to time and resource limitations. Within the scope of the paper, all work that was done was based on information of existing technology although the actual implementation was very specific for the application. The existing technology includes the types of modulation and techniques for generation of test sequences.

A) Software defined radio

The general idea of constructing communication components in software by using FPGAs or MCUs has increased in popularity as prices decrease and performance

increase. The technology is referred to as SDR, Software Defined Radio. This technology provides a way of changing properties of a radio transmitter or receiver within reconfigurable blocks, such as modulation, frequencies, amplitudes and algorithms amongst others. SDR technology opens up new ways of adaptive communication and a higher spectral efficiency according to Tuttlebee [2]. Since the parameters can be controlled by software, a higher performance and greater spectral efficiency can be achieved since the communication channel can be adjusted dynamically depending on the environment, and properties such as modulation type can be adjusted to minimize the number of errors while keeping the data rate at a maximum. The interest in SDR continuously increases, but some problems exist that still require parts of the radio system to be in hardware and this is due to the limited performance of A/D and D/A converters and requirement of faster performance of the SDR [2], especially as frequencies increase. In the paper, a SDR block was used as a main component in the test bench that was developed.

B) QAM MODULATION

A commonly used modulation scheme is QAM, Quadrature amplitude modulation. According to Ergen [4], this is one of the most widely used modulation methods and is used in most of todays digital communications. As the name suggests, it is an implementation of amplitude modulation. By using two separate carriers phase shifted to each other the two carriers are amplitude modulated separately by different data, and then combined into a single carrier by simple addition. The two carriers are named I and Q, in-phase and quadrature, and are usually a cosine (I) and sine (Q) wave due to their 90^{o} phase shifted relation to each other. The finite number of amplitude steps that the I and Q can be adjusted to implements different types of QAM modulations. By having two selectable amplitudes for each carrier, a constellation diagram such as the leftmost in Figure 1 is obtained and as seen, where each point in the constellation diagram represents two bits of data. This comes from each of the two carriers having two selectable amplitude levels and can thus represent one bit each, and together two bits. If the number of amplitude steps are increased to four the data represented by each point is four bits. By increasing the number of selectable amplitude steps, and thus the number of constellation points, more data can be represented by each point and thus a higher transmission rate can be achieved and the loss of SNR. The number of constellation points dictates the modulation type, described as M-QAM where M is the number of points in the constellation.

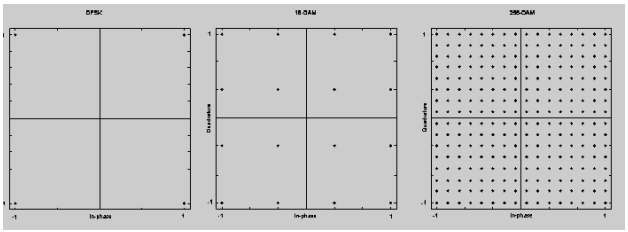

Figure 1: QPSK, 16-QAM and 256-QAM constellation diagrams

There are several different implementations of QAM modulation such as differential, circular and rectangular. In this paper only rectangular QAM was implemented. When transmitting a QAM signal as a radio wave, a modulator is used to apply the different amplitude levels on a carrier wave and thus modulating it. The method of directly applying amplitude levels on an input carrier wave is called direct conversion and due to the cost-effective implementation of this it is a common choice in today's digital communication systems. However, according to Schenk and Linnartz in RF imperfections in high-rate wireless systems [5].

II. IMPLEMENTATION

The main focus of the paper was in the implementation phase since the main objective of the paper was to produce a hardware unit usable in the MODEM project.To reach the goal of constructing a hardware unit with flexible attributes, the platform to be used in the project was chosen as an Field Programmable Gate Array (FPGA). This hardware component consists of logic elements with programmable paths in between, providing the possibility to create different hardware behavior by programming the FPGA. The programming is a result of code written in a hardware description language. In this paper System Verilog was used.The code used to describe the desired hardware behavior in an FPGA is written in a language type known as hardware description language. SystemVerilog, used in this project, is an extension to the widely used Verilog, providing additional data types and more flexible code construction than the original.

A) Development environment

The choice of environment when developing for FPGAs is tightly bound to the hardware used, since each hardware manufacturer provides the environment for their own product. In this paper, the hardware was supplied from Altera and thus the most convenient development environment was Quartus II which has features especially useful for development on Altera hardware. Several advanced hardware units can easily be generated by the program, providing means of utilizing several advanced hardware features such as Phase-Locked Loops (PLL) and Fast Fourier Transforms (FFT).

To get a better understanding of the algorithms and methods to be implemented, simulations in Mathworks Matlab were performed prior to each implementation task. By breaking down and dividing complex operations into smaller steps, a better understanding of how an implementation could be done was gained. As an example, dividing the cross correlation operation into basic mathematical operations such as multiplication and addition provided a way of understanding the needed components. The smaller steps were then combined to perform the original task, and compared with built-in functions of Matlab for verification. A major part of the development was simulation of the written code, as

examining the programmed FPGA simply would not provide enough information of internal states and is also a very cumbersome task due to compilation and programming times. Since Quartus II has a good integration with Modelsim, also provided by Altera, the choice of simulation software was obvious. With the help of Modelsim, the expected behavior of the written hardware descriptive code could be examined by simulation.

As an FPGA is only a chip, more hardware was necessary to utilize the chip. To load the compiled code into the FPGA, a programmer was needed and connections to the FPGA had to be established. Also input and output possibilities were required to make use of the system along with power supplies, reference clocks, buses and other peripherals. There were several boards equipped with these units, along with an FPGA, to make development easier.

To observe the analog output from the conversion board, an Agilent Infiniium 54854A oscilloscope with X/Y-plot was used. This provided the ability to observe the constellation points produced in the analog domain, which is explained more in detail in the following sections.

B) Project work flow

The different tools specified all have their part in the work flow, and to illustrate the dependencies of each other and to visualize the work flow Figure 2.illustrates when the different tools were used. As the work flow describes, a hardware design was the starting point of the work. As soon as a design had been made, it was implemented in Matlab and Quartus II in two separate trails. The Matlab implementation resulted in immediate simulation and could be used find errors and provide a better understanding of the design early in the work flow. The Verilog code implemented in Quartus II resulted in HDL code that could be simulated using Modelsim, and by comparison with the Matlab simulation a first verification could be made before going deeper into implementation and synthesis of actual hardware.

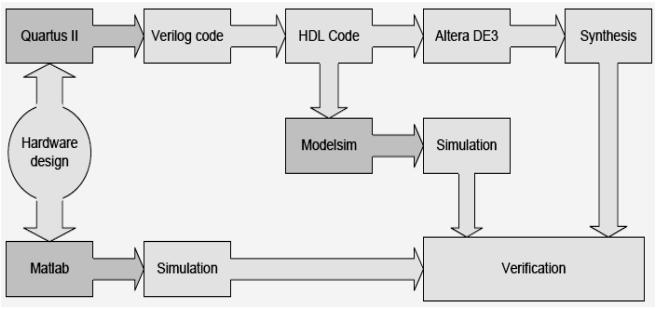

Figure 2: Project workflow.

When the Matlab simulation, Modelsim simulation and hardware synthesis all are completed, these can together perform a very genuine and reliable verification of the implemented hardware design.

C) Pseudo Random Bit Sequence (PRBS)generator and detector

The first hardware unit to implement was a Pseudo Random Bit Sequence generator and a detector for such a sequence. A PRBS can be seen as a sequence of bits with a specific length where the bits appear to be random, and the purpose of a PRBS generator is to produce such a sequence. Due to the random appearance, two rotated copies of the same PRBS does not have many bits in common except for when the two sequences match up exactly. This is useful when examining the input and output relation of a unit under test which is described more in detail later. The goal of this first step was to produce a PRBS generator along with a detector to be used in test transmissions.

The goal of a PRBS generator is to produce a sequence of a determined number of bits by using a generator polynomial implementation. There are several polynomials that can be used, and these polynomials generates sequences with the length 2^{n-1} where n is the degree of the polynomial. In this project, a decision was made that the length of 127 would be sufficient, thus the degree would be n=7. To implement a generator polynomial in hardware, n registers are used in combination with XNOR gates to produce a linear feedback shift register (LFSR).When put together, the degree of the polynomial decides the length of the bit sequence and the number of registers to be used. The polynomial provides information on where to place XNOR gates on the registers to create taps that implement a LFSR, whose output will be a PRBS. According to application note XAPP 052 [6, page 5] using XNOR from registers 6 and 7 will implement a maximum length LFSR. This implementation is derived from the generator polynomial:

$$y = x7 + x6 + 1$$

The hardware implementation with the XNOR taps is described by the circuit diagram in Figure 3.

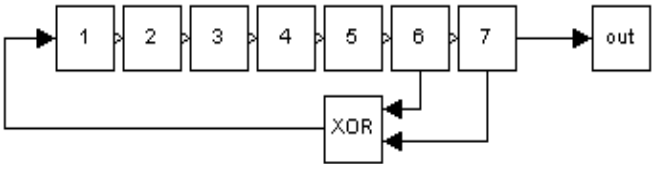

Figure 3: Linear feedback shift register

To utilize the PRBS generator in a test transmission, a tool for detecting the reception of the signal was necessary and this is where the PRBS detector was used. The purpose of the detector was to find a PRBS within a chosen bit stream and provide a way of measuring the integrity of the found sequence. A reference signal to be located in the bit stream was needed during the detection and therefore the detector had a PRBS generator built in with the same properties as of the transmitting generators. As cross correlation is an effective method for comparison of signals and thus detection, the method was used in this implementation. To perform the Fourier transform, a fast Fourier transform (FFT, which is a more efficient way of

calculating the transform) was used both for the transform and the inverse transform. The development environment Quartus II supplied tools.

The main task of the project was to produce a baseband signal in the FPGA and, by using the attached conversion board, convert these digital signals into an analog set of signals to be fed into a modulator for testing. The signals to be fed to the modulator was the In-phase signal and the Quadrature signal. The QPSK modulator was one of the first components to be implemented and therefore the signal design was revised when the unit was used in later stages. The main difference between this implementation and the one used later is the usage of an IF wave. This modulator was constructed to output I and Q signals as a 75 MHz modulated wave.

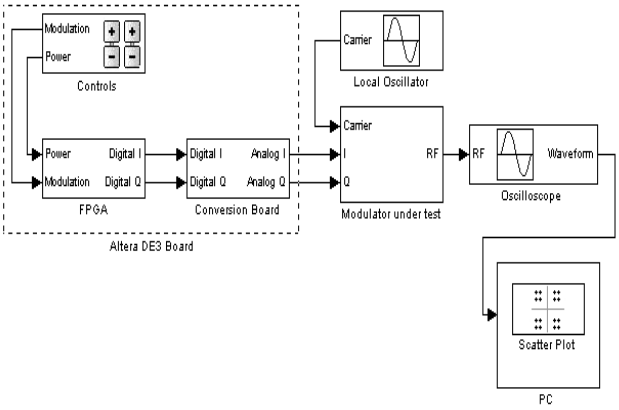

Figure 4: Measurement system overview

III. MEASUREMENT SYSTEM

The purpose of the measurement system was to provide a hardware unit with selectable modulations and signal properties to provide a way of measuring the performance of different modulations and the I/Q imbalance of these in a modulator. This was to be measured and be of assistance when deciding the modulation type to focus on in the research project. The different modulation units that were implemented previously in the thesis were used as building blocks for this system, but they were all modified to suit the purpose better. It is important to note that the hardware target to be measured upon is a modulator constructed within the MODEM-project, and internally inside the FPGA several modulators are implemented to produce the test signals for the hardware modulator.

These are two separate items which are not to be confused with each other although they are referred to by the same name. Since not all modulations were equally interesting from the research project point of view, a decision was made to only implement QPSK and 256-QAM. Along with this, an ability to adjust the voltage of the I and Q signals individually was also needed. An overview of the system and the environment is pictured in Figure 4.All of these functionalities had to be selectable and adjustable while the system was running, and the entire system also needed to be independent in a way that no computer would be needed during testing. Since an FPGA is a volatile device2 the system had to be reconfigured at each power-up. To avoid the need of a computer to do this, an on board ash memory served as the source for programming the FPGA upon startup.

The measurement system was constructed by using several building blocks previously written, along with a power control unit and a control system. The following sections describe the inner workings of these.

The system was built to test direct modulators and thus there was no need for an IF signal to be produced since only the amplitude levels of the I and Q signals were needed. The direct modulators internally produces a phase shift to be used on the Q signal from an input IF signal. Because of this, the VCO that resided in each of the modulators could be removed and instead the multiplication that previously was made with a sine or cosine wave could now be performed by multiplication with a constant factor. This constant was selected differently in each of the modulators to utilize the full range of the D/A converter and are described in table 2.4. The difference between the modulations were the number
of amplitude steps within the same output range. Since the signals from all different modulators later were to be adjusted in voltage, the conversion into unsigned signals had to be moved outside of the modulators and into the power control unit. Therefore the output was changed
from 14 bits unsigned info 14 bits signed within each of the modulators.

To avoid several clock domains, the PLL that each modulator was equipped with internally was also removed and instead the clock signal was fed into the modulator from a PLL that was global for the entire measurement system. The clocks for the D/A conversion board was also moved in the same way, reducing the complexity of each modulator unit.

A requested functionality was to be able to adjust the output voltage of the I and Q signals individually while the system was running. Since the available signals utilize the full range of the D/A conversion board, the voltage of the output signals could not be increased but only decreased, and this was performed by a power control unit that would attenuate the signals within a certain range. Since the signals should be scaled proportionally on each amplitude levels, a division with a voltage level variable had to be done. The desired division variable would be in the range of 0.5-1.0, but since division with decimal point numbers is a rather complex operation for an FPGA this was implemented using a different approach.By performing a multiplication with 214=x where x is the desired division variable and taking the high 14 bits of the 28 bit result, a much more effective division has been made since

multiplication between two numbers is a much simpler task than division for an FPGA. The maximum output from the D/A Conversion board was around 500 mV as measured previously, and without any attenuation the generated signals can at some stage reach this level. Eight stages of voltage levels were implemented since this was easily represented by the eight LEDs on the Altera DE3 board, and an estimate of the attenuation levels of these can be seen in table 2.5. As seen in table 2.5, the steps of maximum output amplitude are adjusted in steps of 15 mV. Another functionality of this unit was to convert the resulting signed 14 bit signals into unsigned 14 bits since this unit was removed from the modulators and the D/A Conversion board does not handle signed signals. This was simply done by adding 214=2 to the resulting signal, changing the range from -8192 to 8192 into 0 to 16383.

As this system was to be used stand-alone, the need for a computer had to be eliminated. The programmed FPGA looses all information once it is turned off and therefore the program had to be stored on a ash memory on the Altera DE3 which could reprogram the device every time it was powered up. To control the system and get information about applied settings, the on-board switches, pushbuttons, LEDs and HEX display was used. Using the switches, different modulations could be selected and displayed on the HEX display, see table 2.6. Pushbuttons were used to adjust the output voltage in eight stages, and to display the current setting the on-board LEDs were used. These were RGB LEDs therefore it was natural to use two separate colors for the different channels.

IV. RESULTS

All of the implemented systems were measured and verified. The results of these along with comments and discussions are provided in this section.Each of the hardware units implemented required different types of measurements for verification and thus different setup.

A) PRBS generator and detector

Since the PRBS units did not provide any output to be measured upon, all measurements were made by observing the internal states of the FPGA and comparing the output with simulations from Modelsim and Matlab. These produced enough information to prove the functionality of the system. To verify the design, observations of the internal states and registers were needed and for this task, a built-in program in Quartus II known as SignalTap was used. This program had the ability to observe a selected number of registers on the actual FPGA during runtime and download them to the development environment for verification. This method was used to observe the value of the cross correlation during runtime when correct or distorted PRBS were sent to the detector.

B) Modulator

All modulator implementations were tested during development to verify the functionality and signal behavior. The output waveforms were observed by using An oscilloscope and measured upon to determine the maximum output voltages. The first implementation, the QPSK modulator, was also compared with a Matlab simulation during development to provide knowledge on how the output waveforms should appear if fully functional. The following implementations did not include this step as the expected waveform simply had an increase in the number of attainable amplitude levels as seen in the oscilloscope measurements. The only reason the Matlab simulation was used was to determine that the mathematical operation of the modulator matched the hardware, and the same operation was used in all later implementations. Since each of the modulator implementations was a complete hardware block, the Altera DE3 had to be reprogrammed between each of the verifications. The waveforms were obtained using a 1 Gsps sample rate in the oscilloscope to properly sample the waveforms. The usage of SignalTap software was not possible due to hardware limitations when using the conversion board, therefore observations using an oscilloscope was the method of verification.

To obtain an eye diagram, the oscilloscope was set to keep the sampled waveforms for 500 ms while sampling new waveforms. This results in several samples being presented on the screen on top of each other, providing a possibility to see the amplitude levels at the same time in the shape of an eye.

i) QPSK

Since this was the first modulator to be implemented, initial simulations with Matlab and Modelsim was done to perform a verification of the output waveform correctness. As seen in Figure.5 the two different simulation results produce the same output, although the actual phase shift occurs slightly later in the Matlab simulation. the eye diagram of the qpsk is shown in Figure.6 .

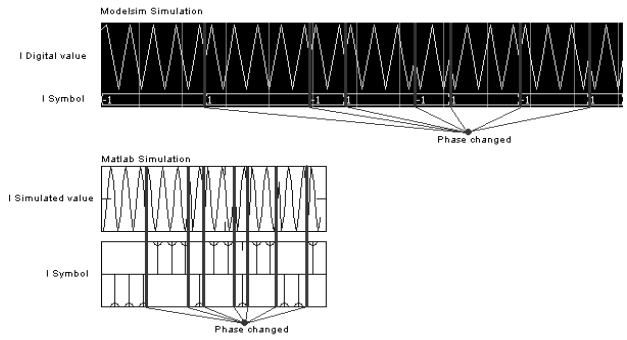

Figure 5: QPSK simulations in Modelsim and Matlab

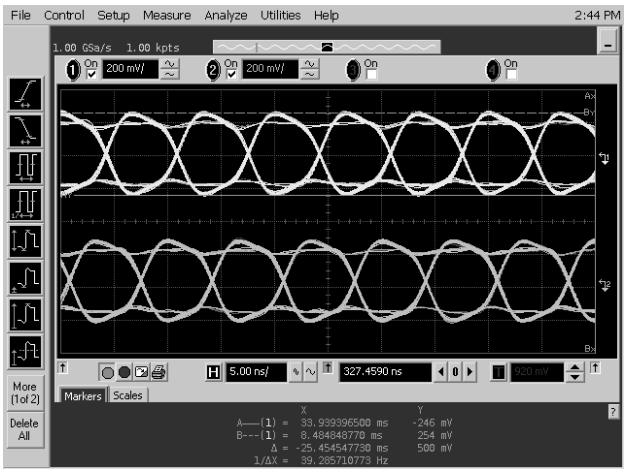

Figure 6: QPSK eye diagram

ii) 256-QAM

Increasing the number of amplitude levels to 32, this modulation puts high demands on the conversion board being able to provide a good enough resolution between the levels. Observing Figure.7 it is hard to tell how well the resolution is due to the actual resolution of the screen on the oscilloscope The utilization of the range on the conversion board was almost used at maximum in this modulator, using 15 as the maximum multiplication value and having a resolution of 10 bits on the sinus and cosine waves the expected maximum output voltage was 468.75mV.

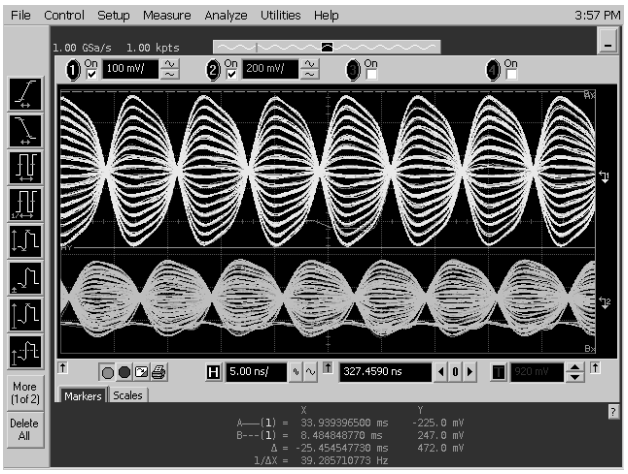

Figure 7: 256-QAM eye diagram

As the same range was used in all of the implemented modulators, the exact same maximum output value was expected in all cases. The Figures 8 and 9 prove that the same maximum out value was measured in all cases.

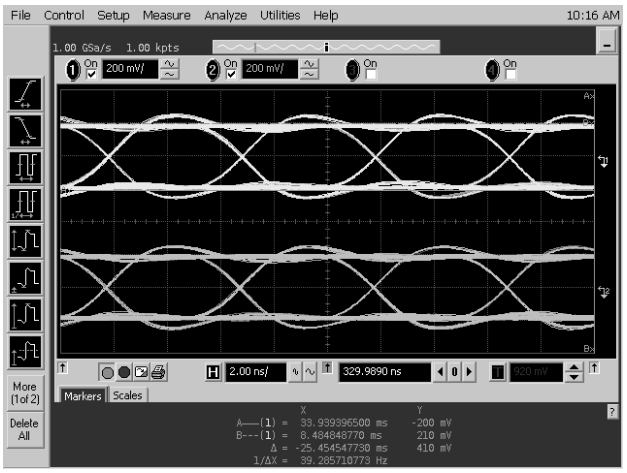

Figure 8: QPSK maximum output level

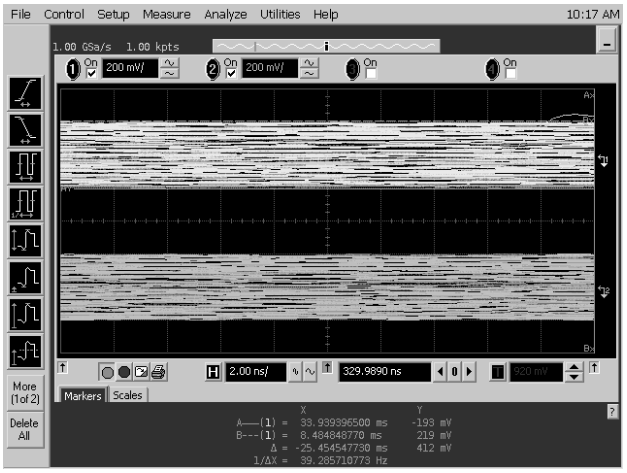

Figure 9: 256-QAM maximum output level

Since this constellation only consists of a total of four points, the distance between points is the same as the maximum and minimum amplitudes.

The Figure.10 provides information about the maximum and minimum output levels of QPSK : The maximum distance between points was 372 mV and The minimum distance between points was 291 mV. This constellation of256-QAM consists of 256 points, each theoretically representing 8 bits of data. The results were measured in Figure.11. The maximum distance between points was 25 mV and the minimum distance between points was 19 mV.

The maximum output voltage was measured to 500 mV at a 50ohm load which represents the maximum range of the bit digital value supplied to the conversion board ; the distance between the digital values 0 and 16383.

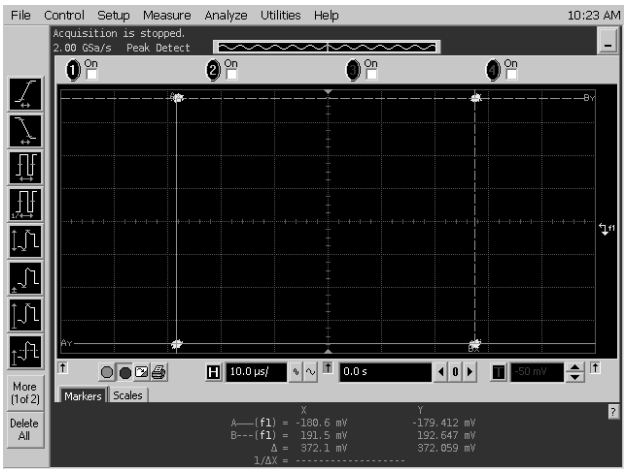

Figure 10: QPSK maximum distance between points 256-QAM.

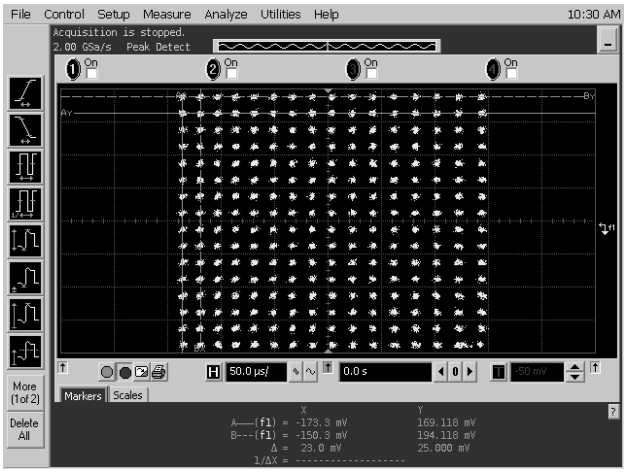

Figure 11: 256-QAM maximum distance between points

CONCLUSIONS

The work was set out to produce the following three tasks; 1. Generation of pseudo random data sequence. 2. Generation of I/Q symbol signals for an E-band I/Q modulator for QPSK and 256-QAM 3. Interfacing with existing modulator from Gotmic. The pseudo random data sequence was implemented first of all, with a detector accompanying it. All of the required modulators and several more have been implemented in a complete dynamic system to be used with any direct modulator. Interfacing with the existing modulator could not be performed due to hardware not being available, but the system is ready to be connected to any direct modulator that is required to be measured upon. The furnished system is delivered as a standalone system programmed onto the Altera DE3 board, as well as source code and programming files.

As stated earlier in the paper, there is room for extensions of the system to provide additional tools of evaluation. The two major tracks of extended functionality are Phase correction and Pre-distortion. Another track is to design the opposite module, the demodulator. In certain circumstances one might want to adjust the individual constellation points with different amplitude adjustments. One situation would be when there is an imbalance in the modulator which only affect certain constellation points and therefore are hard to adjust using the dynamic power or phase adjustments. With the help of a pre-distortion block, the individual constellation points can be adjusted before conversion into the analog domain. The individual adjustment could easily be implemented using two matrices with adjustment data for the I and Q signals respectively, and adjusting these matrices using a computer since there is limited abilities of user input on the Altera DE3 board.

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Auto Quality Testing and Filling Station by using NI LabVIEW and Specially Designed OFS

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Abstract— **Quality testing for various parameters of the final product of the miniature plant is performed by using various sensors. The sensors include LDR, PH meter, Thermo couple, Optical fiber sensor (OFS). pH, level, temperature, weight and turbidity are few parameters that are tested in this miniature industrial prototype. Miniature model of a bottle filling plant has been designed to implement various sensors and actuators.. OFS is an optical sensor that converts weight into electrical signal. It is based on the micro bending phenomenon. All the sensor signals are taken and actuator signals are given by the LabVIEW Data Acquisition through Compact Field Point. The automation, data logging and process controlling has been achieved by a Virtual Instrument (VI) designed on National Instrument's LabVIEW platform**.

Motivation for the project: **Any automated industrial plant or process needs to be monitored by sensors and controlled by a controller. The controllers to handle such sophisticated industrial processes need to be inevitably flexible and easier to program. Modular control is also a desirable tradeoff. All these requirements are satisfied by the graphical programming of LabVIEW VI.Iterative uniformity being the most important factor of output of any process, quality of the end products is tested for uniformity of various parameters. This quality testing helps in giving the system a feedback and a control input. The tested values are monitored by data logging in the form of graphs and charts.**

Index Terms: **OFS, LabVIEW, CFP, turbidity, LDR.**

I INTRODUCTION

The literature study of this project begins with the study of various sensors used in industries and a comparison between them in terms of flexibility, performance, environmental tolerance and other features. Also, the most suitable platform to work upon, in order to create a flexible program that is easy to design and handle i.e., LabVIEW is studied. The specifications and installation of NI CFP 2020, AI 100, AIO 610 and other NI modules are studied.

The project uses a prototype model of a miniature bottle filling plant where general instrumentation practices are observed and implemented. Right from sensors applications to controlling and actuation are dealt in the project. This involves physical setup of a process plant, devices, components, transducers, sensors, actuators, DAQ, CFP etc (Fig.1). An empty bottle is placed in the start of the process over a continuously running conveyor belt. An LDR sensor detects the presence of the bottle and the conveyor stops for a programmed time delay. During this delay, the DC solenoid valve is actuated to be opened and the liquid is filled. After filling the conveyor resumes for the bottle to be processed further towards quality testing end. The fluid in the filling tank is monitored for temperature pH and level. The filled bottle is monitored for weight within standards. A DAQ and CFP manufactured by National Instruments are used for data acquisition from field points to the software code. National Instruments Compact field point is used to interface the hardware with the virtual instrument code developed in LabVIEW [9]. LabVIEW is a graphical programming tool that enables the user to develop programs swiftly without even worrying about syntax. Various functions have been used modularly in order to run each independent process in parallel. The data obtained from the process is also recorded and stored in various formats directly from the virtual instrument.

The paper is organized as follows .Section I describes introduction to literature study, quality testing filling and techniques used for measurement of physical variables considered and controlling in our process.
Section II: Block diagram of the project considered
Section III: OFS and hardware setup.
Section IV: LabVIEW interfacing and VI code
Section V: results
Section VI: Conclusion

II BLOCK DIAGRAM OF THE APPLICATION

Industrial manufacturing has revolutionized with advances and developments in sensor technology and controller technology. Automation and process control has come into mainframe instrumentation as the follow up of industrial automation and control. Many tools have been developed as platforms for building automation programs. Customized microcontrollers, PLC, LabVIEW are few to name some. In any of these platforms, automation is achieved a network of information exchange if various parameters and a consequent instruction command embedded into the program code.

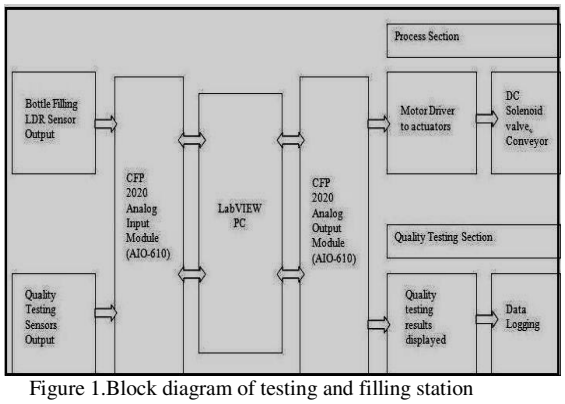

Figure 1.Block diagram of testing and filling station

The project uses a prototype model of a bottle filling plant where general instrumentation practices are observed and implemented. Right from sensors applications to controlling and actuation are dealt in the project. This involves physical setup of a process plant, devices, components, transducers, sensors, actuators, DAQ, CFP etc.

Quality testing: In any industrial process various process parameters are involved and they need to be measured, compared, modified and controlled for the output to meet the desired set points with a reasonable tolerance. Thus the output or product of the process is tested for various parameters to check for quality. The main objective of quality testing is to check for uniformity and precision of the outcome. Thus various transducers and sensors are used at various stages of the process like raw material testing, intermediate processes monitoring and end product testing. This measurement is also given as feedback to the process for process correction and adjustment. All the sensor signals are data-logged and plotted as graphs and charts by the LabVIEW VI. pH, level, temperature and weight are few parameters that are tested in this miniature industrial prototype.

In this paper we are using Virtual Instrumentation for data acquisition and control .Virtual Instrumentation is the use of customizable software and modular measurement hardware to create user-defined measurement systems, called virtual instruments. LabVIEW (Laboratory Virtual Instrumentation Engineering Workbench) is one such tool [7]. It is a highly productive development environment that engineers and scientists use for graphical programming and unprecedented hardware integration to rapidly design and deploy measurement and control systems. The graphical language is named "G" abbreviated as Graphical Programming is a Dataflow type Programming Language where the programmer connects different function-nodes by drawing wires. LabVIEW is commonly used for data acquisition, instrument control, and industrial automation on a variety of platforms.

DAQ Device (CFP2020): DAQ hardware acts as the interface between a computer and signals from the outside world. It primarily functions as a device that digitizes incoming analog signals so that a computer can interpret them [2]. The three key components of a DAQ device used for measuring a signal are the signal conditioning circuitry, analog-to-digital converter (ADC), and computer bus. Many DAQ devices include other functions for automating measurement systems and processes. For example, digital-to-analog converters (DACs) output analog signals, digital I/O lines input and output digital signals and counter/timers count and generate digital pulses.

Signal Conditioning: Signals from sensors or the outside world can be noisy or too dangerous to measure directly. Signal conditioning circuitry manipulates a signal into a form that is suitable for input into an ADC [3]. This circuitry can include amplification, attenuation, filtering, and isolation. Some DAQ devices include built-in signal conditioning designed for measuring specific types of sensors.

Driver software: Driver software provides application software the ability to interact with a DAQ device [9]. It simplifies communication with the DAQ device by abstracting low-level hardware commands and register-level programming. Typically, DAQ driver software exposes an application programming interface (API) that is used within a programming environment to build application software.

*Computer Bus***:** DAQ devices connect to a computer through a slot or port. The computer bus serves as the communication interface between the DAQ device and computer for passing instructions and measured data. DAQ devices are offered on the most common computer buses including USB, PCI, PCI Express, and Ethernet. Ethernet communication is employed in this project.

III OFS AND HARDWARE SETUP

Fiber optic weight sensors: A OFS (fiber optic sensor) is a sensor that uses optical fiber either as the sensing element ("intrinsic sensors"), or as a means of relaying signals from a remote sensor to the electronics that process the signals ("extrinsic sensors") shown in fig2. Fibers have many uses in remote sensing [3]. Depending on the application, fiber may be used because of its small size, or because no electrical power is needed at the remote location, or because many sensors can be multiplexed along the length of a fiber by using light wavelength shift for each sensor, or by sensing the time delay as light passes along the fiber through each sensor. Time delay can be determined using a device such as an optical time-domain reflects meter and wavelength shift can be calculated using an instrument implementing optical frequency domain reflectometry. Fiber Optic sensor system.

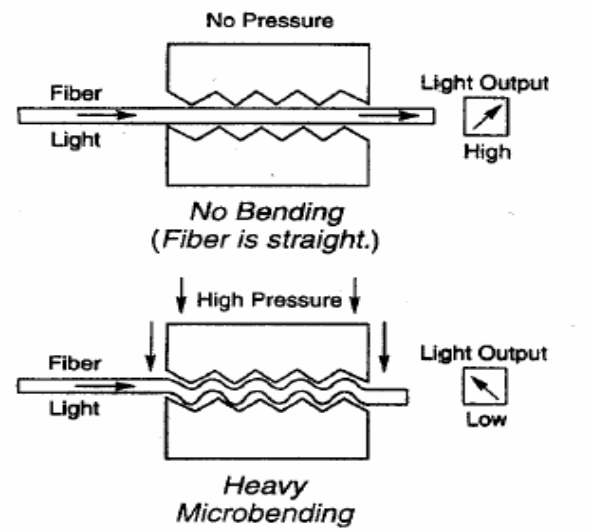

Figure 2. Microbend Sensor

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SETUP: Cylindrical sticks of 1mm of diameter are arranged in a pattern in order to create a corrugated pattern on both planes of the laid optical fiber is shown in fig.3. A LASER Source is incident continuously into the optical fiber as a simulation for the SSC at the other end of the fiber. An LDR circuit detects the amplitude of light passing through the fiber and then converts the non-electrical signal to an electrical signal. This voltage signal is given to the field point form where the VI takes the value for processing [4].

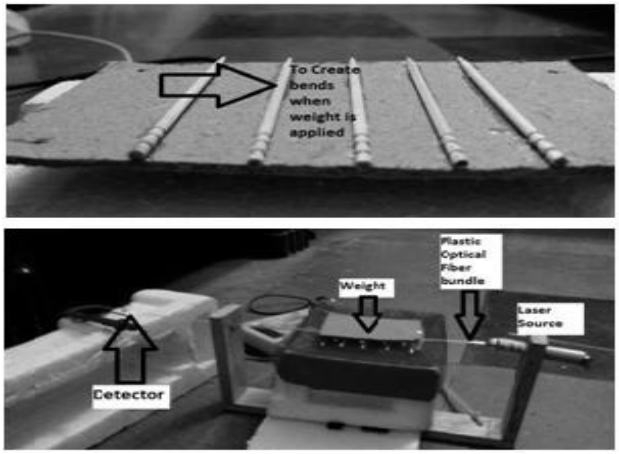

Figure.3. OFS sensor set up

Conveyor belt: A conveyor runs on two wheels fixed to shaft of 2 DC motors. The DC motors are used to drive the conveyor.

Motor driver- L293D: L293D is a dual H-bridge motor driver integrated circuit (IC) is shown in fig.4.Motor drivers act as current amplifiers since they take a low-current control signal and provide a higher-current signal. This higher current signal is used to drive the motors. L293D contains two inbuilt H-bridge driver circuits. In its common mode of operation, two DC motors can be driven simultaneously, both in forward and reverse direction. The motor operations of two motors can be controlled by input logic at pins 2 & 7 and 10 & 15. Input logic 00 or 11 will stop the corresponding motor. Logic 01 and 10 will rotate it in clockwise and anticlockwise directions, respectively.

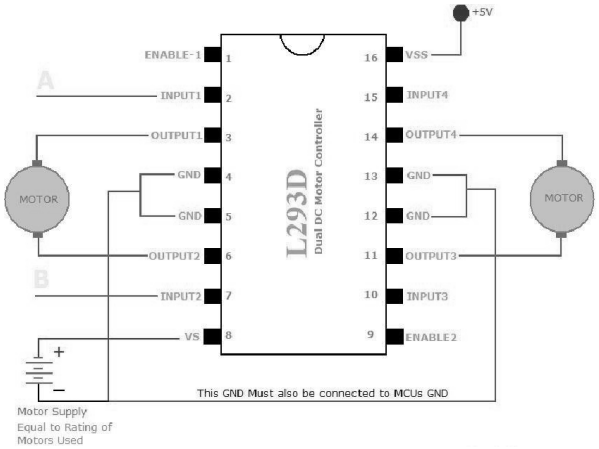

Figure. 4 Motor driver

CFP2020: In this paper by Using the NI LabVIEW Real-Time Module, powerful data-logging, control, and measurement systems on PC can be developed and application can be easily embedded on the NI CFP-2020 intelligent controller for reliable distributed or stand-alone deployment [9]. The cFP-2020 features an Ethernet port, four serial ports, removable Compact Flash storage, and extended DRAM memory for larger and more advanced applications. Engineers and scientists typically use cFP-20xx controllers in applications requiring industrial-grade reliability - such as stand-alone data-logging, analog process, and discrete control systems - to run PID control loops, actuate valves and motors, take measurements, perform real-time analysis and simulation, log data, and communicate over serial, phone, and Ethernet.

CFP-AIO-610 (analog input output module): The National Instruments cFP-AIO-610 is an 8-channel, single-ended, combination analog input/analog output module is shown in fig.5. It can measure four channels of voltage or mA current loops from industrial sensors and transmitters and can output four channels of 0 to 10 or ±10 V to control valves, gauges, and other industrial actuators. The NI cFP-AIO-610 has an internal update rate of 1.4 kHz, ideal for low-channel-count systems or PID control. The module includes over ranging and onboard diagnostics to ensure trouble-free installation and maintenance. The module also makes programming easier by automatically scaling and liberalizing input and output signals to avoid the step of converting binary numbers into engineering units in your control or monitoring software. The cFP-AIO-610 module is calibrated according to NIST-traceable calibration standards, ensuring accurate and reliable analog measurement and control.

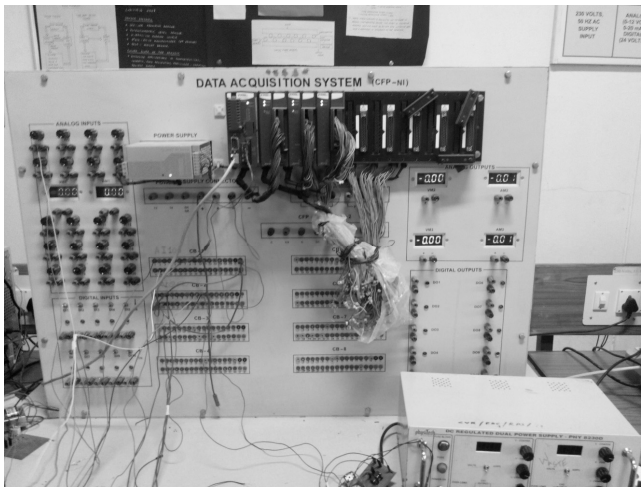

Figure.5.NI compact field point

The CFP-AIO-610 is a Compact Field Point analog input and output module with the following features:

1. Four analog voltage or current input channels with 11 input ranges up to ±30 V or ±20 mA (±36 V or ±24 mA with 20% over ranging)
2. Four analog voltage output channels with ±10 or 0–10 V ranges (±10.2 or 0–10.2 V with 2% over ranging)
3. 1.4 kHz hardware update rate
4. 12-bit resolution
5. –40 to 70 °C operation
6. Voltage outputs sink or source up to 10 mA per channel
7. On-board diagnostics including one out-of-range indicator for all inputs and one over current indicator for each output.
8. Current inputs protected up to ±10 V.

Wiring CFP- AI-100: Table 1 lists the terminal assignments for the signals associated with each channel. Each channel has separate input terminals for voltage (Vin) and current (Iin) input. Voltage and current inputs are referenced to the COM terminals. If an external supply is used to power field devices, power supply should be connected to the V and C terminals of the terminal base or connector block. The cFP-AI-100 has eight single-ended input channels. All eight channels share a common ground reference that is isolated from other modules in the Field Point system. Figure 5.8 shows the analog input circuitry on one channel

TABLE I
TERMINAL ASSIGNMENTS

Channel	Terminal Numbers			
	V_{in}	I_{in}	V_{sup}	COM
0	1	2	17	18
1	3	4	19	20
2	5	6	21	22
3	7	8	23	24
4	9	10	25	26
5	11	12	27	28
6	13	14	29	30
7	15	16	31	32

pH sensor- pH614:pH is the degree of acidity or alkalinity of a solution. pH measurement is very essential and crucial in any process plants where ever fluids are involved is shown in Fig.6. This inevitability is due to the metal fluid interaction during the processes [8]. Fluids involving process with boilers, pipelines, valves, stirrers, turbines, etc. need to be monitored for pH. In Fluid filling plants like food processing, pharmaceutical, cosmetic, chemical, fertilizer, etc. need to be checked for pH at the process end as part of quality testing.

Figure.6. pH Sensor electrode

LDR as proximity sensor: An LDR acts as a proximity sensor. The LDR is given a continuous 5V DC power supply with signal conditioning is shown in fig.7. The light from ambience falls on the LDR and keeps the circuit ON [8]. As and when a filled bottle passes between the pair, interrupting the ambient light, the circuit breaks and the count in the LabVIEW VI increments by one. The count form this sensor is used as a base count for other sensor's output analyzing to determine efficiency.

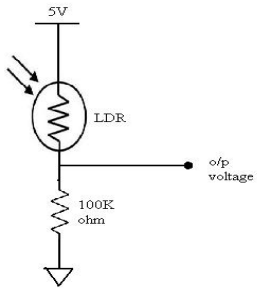

Figure.7. LDR Signal Conditioning

NI CFPTC 120: The National Instruments cFP-TC-120 is an 8-channel input module for direct measurement of temperature from standard J, K, T, N, R, S, E, and B thermocouple(Fig.8) types. With signal conditioning, double-insulated isolation, input noise filtering, and a high-accuracy delta-sigma 16-bit analog-to-digital converter, the NI cFP-TC-120 delivers reliable, accurate temperature or mill volt measurements. Designed from top to bottom for productivity and reliability, the cFP-TC-120 features Hot PnP (plug-and-play) operation, easy configuration, self-diagnostics, and automatic scaling to engineering units [7].

Figure.8 Thermocouple

IV LABVIEW INTERFACING AND VI CODE

This section deals with interfacing and locating- pins and icons for VI development is shown in (Fig.9 and Fig.11). It contains details to develop a VI and insight to various LabVIEW functions used. LabVIEW follows a dataflow model for running VIs. A block diagram node executes when it receives all required inputs. When a node executes, it produces output data and passes the data to the next node in the dataflow path. The movement of data through the nodes determines the execution order of the VIs and functions on the block diagram.

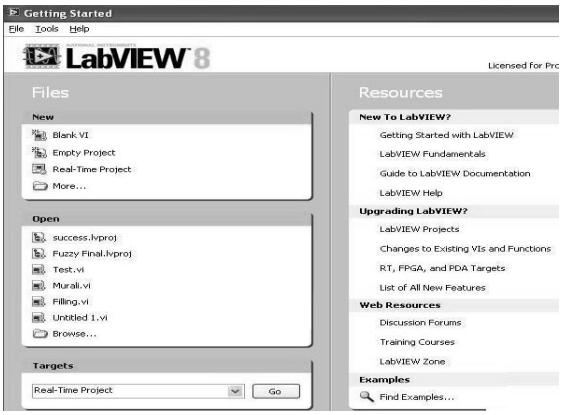

Figure.9. Getting started with LabVIEW

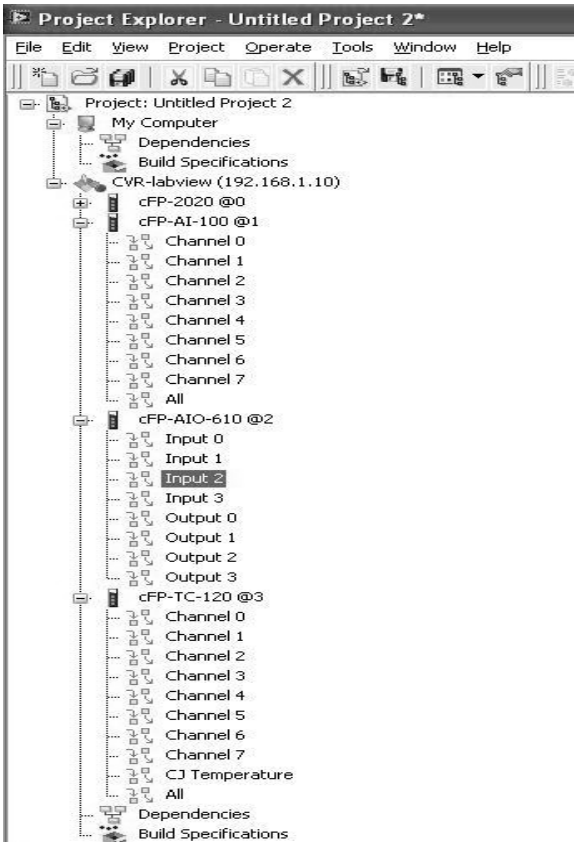

Figure. 10.Channels of NI modules

LabVIEW (Laboratory Virtual Instrumentation Engineering Workbench) is a highly productive development environment that engineers and scientists use for graphical programming and unprecedented hardware integration to rapidly design and deploy measurement and control systems. The graphical language is named "G" abbreviated as Graphical Programming is a Dataflow type Programming Language where the programmer connects different function-nodes by drawing wires. LabVIEW is commonly used for data acquisition, instrument control, and industrial automation on a variety of platforms.

Virtual Instrumentation is the use of customizable software and modular measurement hardware to create user-defined measurement systems, called virtual instruments Traditional' or 'natural' instrumentation systems are made up of pre-defined hardware components, such as digital multimeters and oscilloscopes that are completely specific to their stimulus, analysis, or measurement function. Because of their hard-coded function, these systems are more limited in their versatility than virtual instrumentation systems. The primary difference between 'natural' instrumentation and virtual instrumentation is the software component of a virtual instrument.

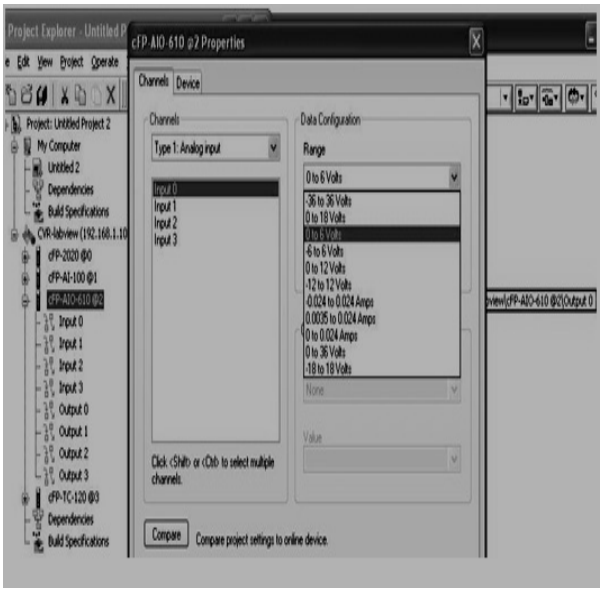

Figure. 11. Data configuration of pins

Working of the project

1. Empty bottles are placed on the conveyor.
2. When the empty bottle comes under the overhead tank for filling, LDR sensor detects the bottle.
3. The actuator stops the conveyor belt.
4. The Solenoid valve opens and the water from the overhead tank starts filling the bottle.
5. After the bottle is full (after a time delay) CFP signal changes and the bottle starts moving again.
6. In parallel, the tank is monitored for level, Ph and temperature.
7. Then, the bottle moves to the optical fiber strain gauge where the weight is measured and is logged to the spread sheet file with a time stamp.

V RESULTS

Results observed: The optical fiber sensor designed works linearly in the given range. The entire process has been automated and the quality test of the end product has been done. The data from the sensors and measuring devices has been logged by the VI and stored in various formats. The overhead tank level has been controlled by ON OFF control algorithm. Various process parameters like pH, temperature and other process parameters have been monitored. The result can be observed from fig.12 to fig.15.

Scope of the project: The scope of applying the sensors and controlling process used in this project is wide and huge. In the present project, the data acquisition is done using Ethernet protocol and communication. There is scope in LabVIEW that the VI can be used to control industrial field bus in controlling, monitoring and modifying through internet communication. In many industries like pharmaceutical, cosmetics, food processing, fertilizer, chemical, these processes are of inevitable use.

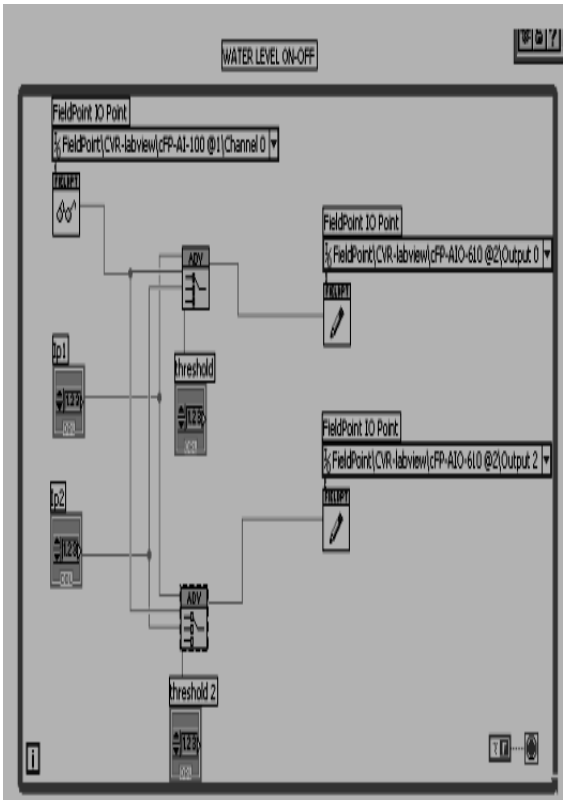

Figure.12. Water Level ON-OFF

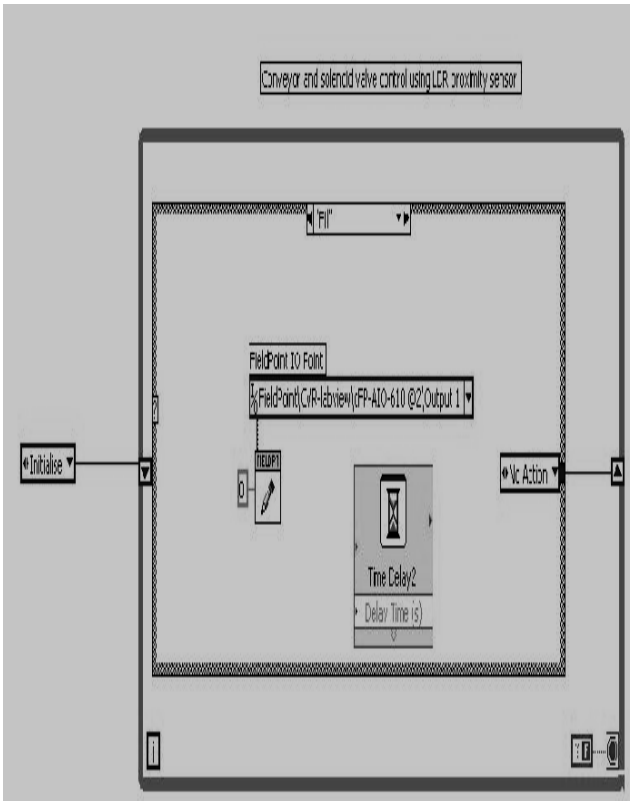

Figure.13. Fill case of case structure

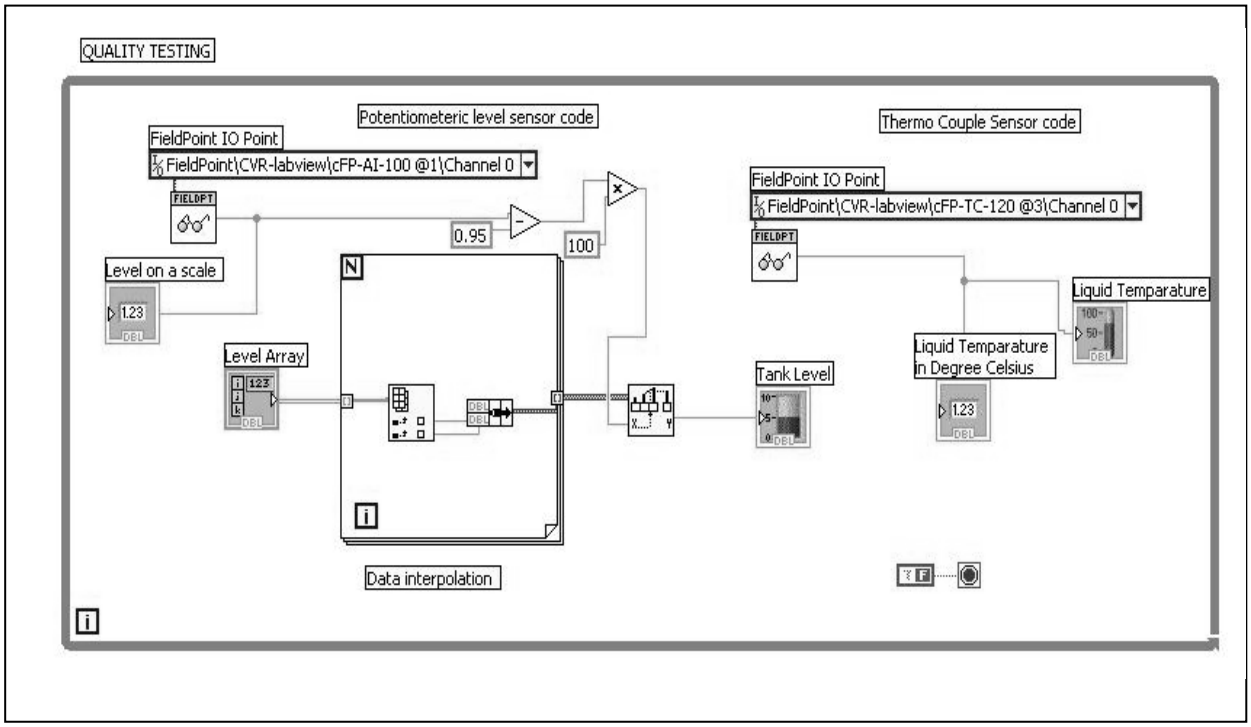

Figure.14.Blockdiagram of the application

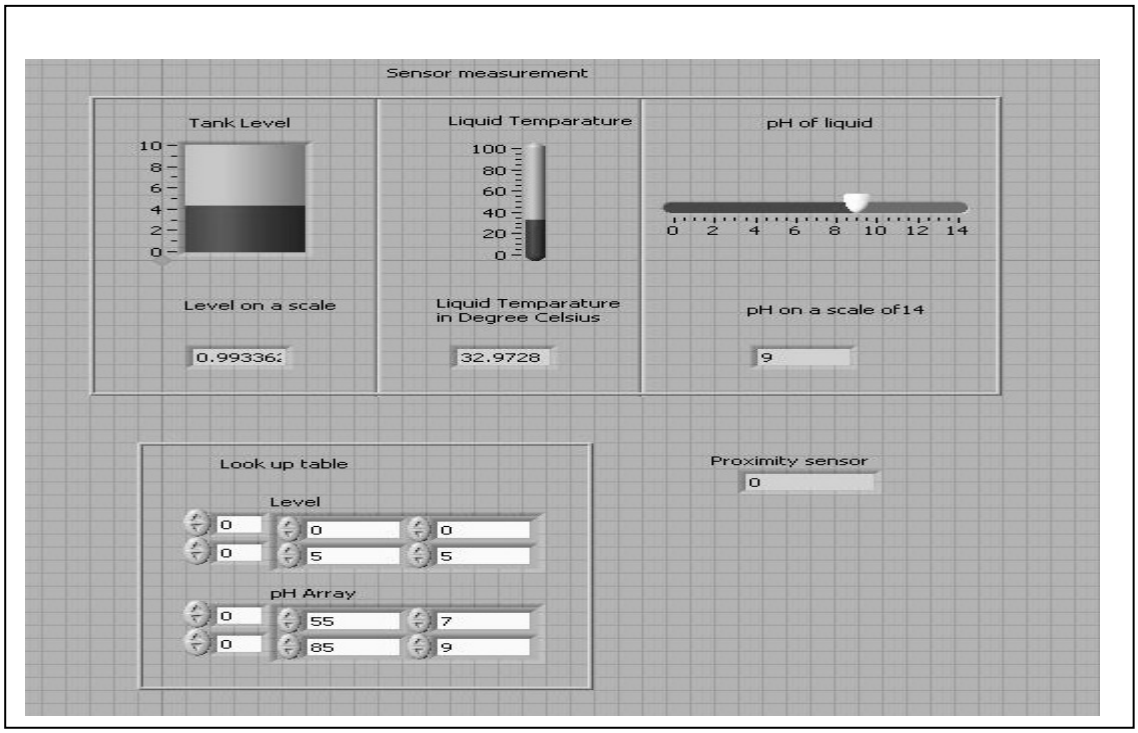

Figure.15.Front panel of the application

CONCLUSIONS

In this paper, the automatic bottle filling plant is implemented. The sensor applications are studied and operated to fully understand their characteristics and operation. This operational experience is used to implement the sensors appropriately. The automation, controlling, monitoring, data processing, of the bottle filling plant has been done by a Virtual Instrument developed on LabVIEW platform.

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Performance Assessment and Classification of Students using CAMP Model with Data Mining Approach

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Abstract - **With the advent of large number of professional colleges, especially with engineering colleges, the Quality of education is becoming compromised and unable to meet the demand vs. supply of Qualified and employable professionals in IT, ITES and other sectors. It needs lot of knowledge and skill based training programs to make the students employable and knowledgeable. In this paper the focus is on how best it can assess the students' performance and hence to provide the needful training and value added courses to bridge the gap to overcome the shortfalls. For this Assessment process CAMP (Conceptual, Analytical, Memory-Based, Practice-Based) model with data mining approach (EDM – Educational Data mining) is being utilized**

Index Terms—**Data Mining, Classification, Clustering, Rule based classification, Educational Data Mining (EDM).**

I. INTRODUCTION

The assessment process for evaluating the students' performance in the educational institutions for the past several years are based on the Quantitative rather than qualitative which is creating a gap between the supply vs. demand of employable graduates to the industries. This leads to a need for revising the assessment process and to train the graduates accordingly to make them employable. In this paper a mechanism is proposed to classify the students based on their performance using CAMP Model and hence to provide them additional support in the form of value added courses, refreshment courses and bridge courses etc.

II. RELATED WORK

A. Bloom's Taxonomy

During 1956, Benjamin Bloom headed a group of educational psychologists who developed classification of levels ofintell ectual behavior which is important in learning. This classification helps in an effective curriculum design and is presented as a pyramid [1]. This Taxonomy Originally developed as a method of classifying educational goals for student performance evaluation. By using Bloom's Taxonomy, can assess students on multiple learning outcomes. Bloom's Taxonomy is shown in Figure 1 and the subsequent of revisions made to this are show in Figure 2 and 3.

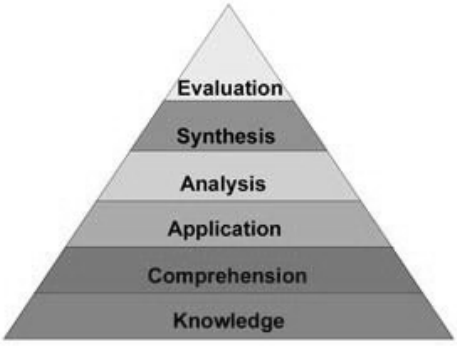

Figure 1: Bloom's Taxonomy (1956)

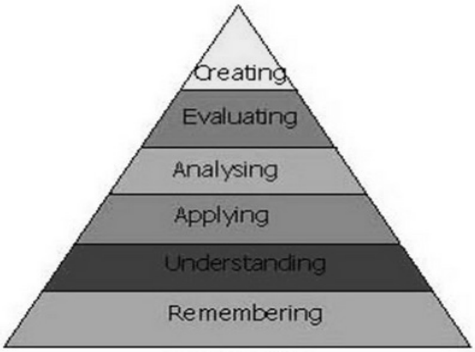

Figure 2: New version by Lorin Anderson (2001)

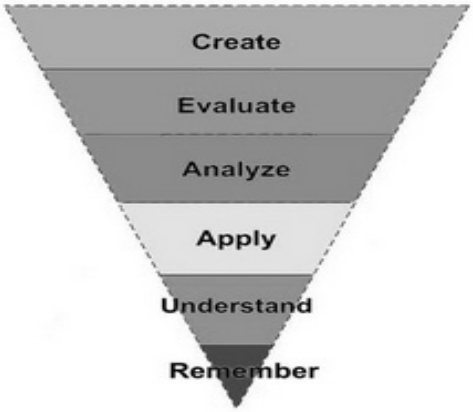

Figure 3: The Revised version by Lorin Anderson

The Taxonomy revised by the Lorin Anderson in figure 3 is the most adoptive taxonomy to the present need of the educational growth of the student in knowledge, creativity and employable dimension.

B. Graduate Aptitude Test in Engineering (GATE)

To assess the level students' competence at national level in core subjects, especially in engineering, GATE examination is being conducted in India. This test is becoming primary in screening the candidates in the process of recruitments in Government and PSU's .The pattern of evaluating the students' performance is in GATE is based the skills: Recall , Comprehension , application, analysis and synthesis. The following section represents what exactly these skills referring to.

Recall: Ability to memorize facts, principles, formulae or laws

Comprehension: Ability of understanding of the basics to draw simple conclusions from fundamental ideas.

Application: ability to apply knowledge either through computation or by logical reasoning.

Analysis and synthesis: ability to analyze the data, facts and ability to compare the information to draw valid conclusions

C. Infosys Campus Connect – FP TEST

Infosys Campus Connect – Foundation Program is an initiative by the Infosys to connect with the campuses (engineering colleges/professional colleges) to train and bridge the gap in the student competency levels at their fundamental /core subjects and hence to make them employable. They use the model called CAMP [2] (Conceptual, Analytical, Memory based, Practice-Based) model to train and asses the students on fundamental courses. They made the Examination pattern in evaluating the students' performance with the CAMP model such that the components should be as follows:

C+M = 20-30% and A+P = 70-80%

D. EDM: Educational Data Mining

EDM is an emerging discipline (as an application of Data Mining) deals with developing the methods and technique to explore the data coming from the educational Institutions to understand the students' performance and hence to setup the teaching and learning practice in an effective way to make the students competent and employable [3,4]. It was initiated during 2000 year. This EDM approach can helps in making the operations fine-tuned and can be used as tool to asses at various levels of administration of an educational institute. It also helps in designing effective curriculum, mode of teaching and evaluation methods

III. PROPOSED WORK

All the existing methods that are discussed above are evaluating the overall performance of the students and hence classifying them into a certain class/grade. But there is a need to understand the student performance at minute level of the ability skills on which the student is good at and lagging even though overall performance of the student is good and clearing the assessment tests. This type of evaluation helps in making the student competent at each and every core competence level [5, 6, 7, 8, 9, 10, 11]. In this proposed work, the process is to evaluate the performance of the students based on CAMP model and classifying them in order to provide the value added courses or additional training to make the student more competent and employable on core domains.

A. SAMPLING & DATA COLLECTION

The assessment is done based on the student performance in their core subjects with reference to their abilities (CAMP skills) are done. For this, Purposive sampling method is used to conducted a survey with a structured questionnaire (An objective multiple choice type Test) administered with the respondents (students). The design of Questionnaire to assess the students is as follows with respect to each skill component. The scheme of the questionnaire is shown in detailed in Table 1.

In each of the subjects, 30% of the weightage is given to (Concept + Memory) based Questions and 70% of the weightage is given to (Analytical + Practice) based questions. If a student gets 40% of marks in a subject then that students is considered to be passed in that subject. If the student scores 50 % of the marks on overall then that student is considered to be passed in the examination.

TABLE I
EXAMINATION PASSED VS PLACEMENT

Core Subject	C+M	A+P	SUBJECT WISE PASS	TEST PASS SCORE
Operating Systems	30%	70%	40%	50%
C Programming	30%	70%	40%	
Data Base Management Systems	30%	70%	40%	
Object Oriented Programming	30%	70%	40%	
IT Fundamentals	30%	70%	40%	

B. DATA ANALYSIS AND CLASSIFICATION

Data being collected through Questionnaire is loaded to the SPSS Software to analyze and process the data. SPSS Stands for Statistical Package for Social Sciences. This Software helps us to load various types of data stored in the formats like excel, text, csv etc. To carry out this study,

Descriptive statistics like frequencies, Cross tabulation etc using SPSS. This Software allows filtering the datasets, helps in writing our own coding/scripting (i.e. syntax) to process and analyzing the datasets. Segments (clusters) are defined using the association rules [12, 13, 14, 15] based on the subject wise scores, overall score and number of subjects passed by the students in the examination. The association rules for the segments (clusters) are defined as follows in Table 2.

TABLE II
CLUSTER VS CLUSTER DEFINITION

Cluster/Segment	Cluster Definition/ Association Rule
PERFORMERS	[ALL SUBJECTS PASS] & [GOT >=50% SCORE in the Test]
MODERATORS	[AT LEAST PASSED IN HALF OF THE SUBJECTS] & [GOT >=50% SCORE in The Test]
UNDER PERFORMERS	[NOT PASSED IN AT LEAST HALF OF THE SUBJECTS]

IV. RESULSTS AND DISCUSSION

Based on the sample of 48 respondents, the data is analyzed and the results are described below. The results are verified with their (students) respective placement status. This comparison helps us in whether the clusters are defined correctly and is aligning with the placement status. Based on the cluster and the placement status , can introspect the result of students on which they got failed in securing the placement (job). Whether they failed to secure the job due to lack of CAMP Skills or any other like interpersonal skills, presentation skills etc. this helps us to conduct value added and additional courses to make them employable and to enrich their skills.

A. RESULTS

The results which are obtained from the data being collected and analyzed are shown in the following Tables 3 and 4.

TABLE III
EXAMINATION PASSED VS PLACEMENT STATUS

	PLACED	NOT_PLACED	Total
EXAM PASSED	54.17%	35.42%	89.59%
EXAM NOT PASSED	0%	10.42%	10.42%
Total	54.17%	45.83%	100%

TABLE IV
CLUSTER VS EXAMINATION PASSED AND PLACED

	EXAM_PASSED		Total
	PLACED	NOT PLACED	
Performers	47.92%	22.92%	70.84%
Moderators	6.25%	14.58%	20.83%
Under performers	0%	8.33%	8.33%
Total	54.17%	45.83%	100%

B. DISCUSSION

- BASED ON OVERALL RESULTS

1. In “Performers” cluster, students are good at CAMP skills but some of them are unable to get the placements. This may be due to the lack of interpersonal and presentation skills. So these students who are not placed under “Performers” should be given some training on interpersonal and presentational skills (soft skills).

2. In "Moderators" cluster, students are moderate in CAMP skills. They need some additional training classes in the core subjects apart from soft skills.
3. In "Underperformers" cluster, students need to concentrate on the core subjects and special programs should be conducted to get the core domain knowledge apart from soft skills

- BASED ON SKILL LEVEL

1. Students that are not placed and have not answered 30% of Overall **C**oncept + Memory based questions should be given core subject knowledge by conducting the additional training programs on the core subjects along with the soft skills
2. Students that are not placed and have not answered 40% of Overall Analysis + Practice based Questions should be given practice based assignments, online tests and refresher courses apart from soft skills

CONCLUSIONS

In order to make the students employable, it is necessary to make the students more competent at the domain knowledge and also need to impart the soft skills and interpersonal skills to sustain in the competitive world. To make the students ready to compete, the curriculum and the teaching learning process should be fine-tuned in accordance with the industrial needs and the students' performance should be assessed and evaluated not only on the marks but also on their capability levels which helps in getting them placed in the industries

Since the study is purely empirical and on small size of data set, this study should be carried out on large size of data sets to know more insights of the data , though the results are on small data set resembles the reality. Secondly, the attributes that are considered for the classification under this study is among ability Skill set vs Placement status. This study further should be carried out with additional attributes like Academic background (rural/urban), Mode of instruction etc.

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Fourier Transform Infrared Spectroscopic Analysis of Medicinal Plant (Bhringaraj) from the Duvva Village West Godavari District, Andhra Pradesh, India.

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Abstract- **The main objective of the study is to determine the important features exhibited by FTIR. Dried leaves of Bhringaraj, a medicinal plant used in Ayurveda were selected for study. The vibrational assignments, intensities and wave numbers were obtained by absorption spectra. Various functional groups and chemical constituents were identified. This article gives an insight about the importance of herbal analysis and gives a platform for using these medicinal plants for developing wastewater treatment technology and for improving the quality of drinking water.**

Index terms- **Fourier Transform Infrared Spectroscopic (FTIR), Bhringaraj, water treatment technology.**

I. INTRODUCTION

Medicinal plants are a group of plants that can be used as a drug or therapeutic agent or active ingredient of a medical preparation. Plants form a basis of traditional medicine practices that have originated from historic times. Plants are used as drugs and they are found in arthava veda which is the basis of Ayurvedic medicine (dating back to 2000BCE) the clay tablets in Mesopotamia (1700BCE) and Eber Paprus in Egypt (1550BCE). The demand for plant-based medicines is increasing because they do not have adverse effects, and they are rich source of bioactive ingredients, which show Pharmacological activities. In the present study, FTIR is used to identify the different functional groups present in the leaf powder of Bhringaraj. FTIR has become a versatile tool for identification, characterization and detection of biomolecules [1, 2]. High sensitivity of vibrational spectra helps in identifying biological molecules such as water, proteins, nucleic acid, carbohydrates etc [3]. FTIR peaks are relatively narrow and in many cases can be associated with a vibration of a particular chemical bond (or a single functional group).

II. EXPERIMENTAL METHOD & MATERIALS

Selection of Bhringaraj leaves

The leaves of medicinal plant Bhringaraj were selected for the FTIR analysis were collected from the agriculture lands of Duvva Village, West Godavari District, Andhra Pradesh. The leaves were taxonomically authenticated.

Bhringraj in Ayurveda practitioners is commonly known as false daisy and it belongs to the family of Asteraceae, Botanical Name - Eclipta Alba. It is an erect, prostrate, branched roughly hairy herb grows commonly in moist places all over the world, as a weed. Phytochemical studies on Eclipta revealed the presence of Alkaloids like ecliptine and nicotine and bioactive steroidal alkaloids verazine dehydro verazine eclipatalbine [7]. Dried leaves have been reported to contain coumarins like wedelolactone and its derivatives [8], demethylwedelolactone, iso-demethylwedelolactone and strycholactone [9], many hydrocarbons like ecliptal [10] d-formyl terthienyl [11]. Six new Oleanane triterpene, Glycosides, Eclalbasaponins I-IV are reported [12]. Many types of sterols and flavonoids are present in the bhringraj [13].

FTIR is used for identification of biomolecules [4-6, 24] the chemical constituent's in bhringaraj are known for its anticancer, antileprotic, analgesic, antioxidant, antiviral, antihaemorrhagic, antibacterial, antimyotoxic, antihepatotoxic, spasmogenic, hypotensive and ovicidal properties.

Bhringaraj is used extensively by Ayurvedic practitioners, for treatment of Snakebites [14, 15], Scorpion stings [16]. It has anti-inflammatory [17] Bronchodilator activity [18,19] Nootropic activity [20] and it is used to treat Ranikhet disease [21], Salmonella epidermidis and salmonella typhimurium infections [22], used for hair growth [23, 24] treating skin diseases and eye infections. Due to its anti-inflammatory properties, anti oxidant activity, anti cancer activity [25] and anti hyper lipidemic activity [26] the herb is also used for treating hyperacidity. Bhringaraj is the main herb for the hair care and cirrhosis in Ayurveda. It is believed to maintain and rejuvenate hair, teeth, bones, memory, sight, hearing, kidneys and liver.

Healthy plants and fresh leaves were collected. These leaves were air dried and shade dried at room temperature in clean environment to avoid contamination and powdered in a domestic grinder. The powdered sample is stored in air tight glass bottle at room temperature for further analysis.

III. INSTRUMENTAION

Spectro-Chemical Analysis

The compact light weight Agilent Cary 630 FTIR connected to a sophisticated computer was used to record FTIR spectra of bhringaraj leaves in the spectral range of 4000-400cm^{-1}at room temperature.

IV. RESULTS AND DISCUSSION

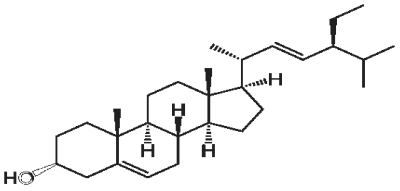
FTIR spectrum of Bhringaraj was used to identify the functional groups of active components based on the peak value in the region 4000-400cm^{-1} of infrared radiation. FTIR spectra of leaves of Bhringaraj were represented in Fig.1

This study has been undertaken with a view of identifying the functional groups present in the Bhringaraj leaves and to understand the significance of bioactive constituents present in it. The FTIR represented in Fig.1 is of complex nature and it indicates the various chemical constituents and chemical structures in the biomolecules given in Table -1, Scheme-1. The FTIR spectra show many absorption bands, the presence of hydroxyl groups in the biomolecule absorbed at 3852.93 cm^{-1}, 3447.12 cm^{-1} and 3107.03 cm^{-1}. The peak at 3852.93cm^{-1} represents OH stretching of hydroxyl groups in phenols [22]. The peak at 3447.10cm^{-1} is due to OH stretching. The absorption peaks at 2918cm^{-1} and 2850cm^{-1} represents asymmetric stretching of CH_2 groups and symmetric stretching of CH_3 groups indicating the presence of chlorophyll in biomolecule [24-29]. The peak at 2202cm^{-1} may be due chain containing carbon double bonded with nitrogen which is termed as nitrile group [30&31]. The band at 2096cm^{-1} represents azide group [31]. IR spectral peaks at 1445cm^{-1} and 1316.650cm^{-1} exhibits a high molecular coupling and this region is very complex [26] involving several modes of vibration of lignin and carbohydrates. A band around 1450cm^{-1} is reported to be deformation of lignin CH_2 and CH_3 which was reported previously. The absorption bands at 1100-1000cm^{-1} is the finger print region indicating several modes such as C-H deformations or C-O or C-C stretching pertaining to carbohydrates. Carbohydrates in the leaves are the major constituents of these absorption bands [32-35].

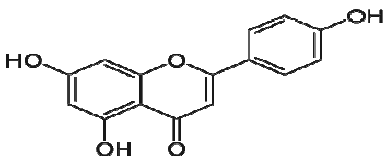
CONCLUSIONS

Water plays a vital role in the development and public health of population in every part of the world. The methodology for the purification of water remains expensive in developing countries. Many water treatment processes use alum and chlorine where Alum causes alizimers disease and pathogenic microbes are resistant to chlorine.

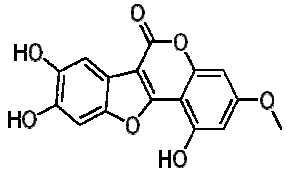
This study has been of preliminary nature with the objective of establishing the use of medicinal plants for water and waste water treatment. To improvise the water quality and to control the water pollution the medicinal plant bhringaraj can be used which contains many chemical components which are confirmed by FTIR in this paper. This bhringaraj medicinal plant has capacity to remove the suspended particles, heavy metals and fluoride from water and waste water by coagulation and adsorption thus increase the quality of water. The sludge which is produce during the treatment is less toxic. Further work and application of bhringaraj and other medicinal plants are in progress.



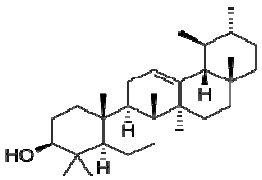
Stigmasterol



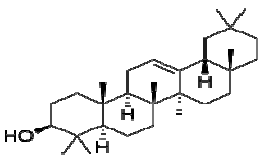
Apigenin



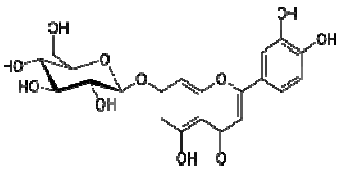
Wedelolactone



α –amyrin



β-amyrin



Luteolin 7-O-glucoside

Scheme - 1 Structures of Chemical Componetnts Present in Bhringaraj Medical Plant

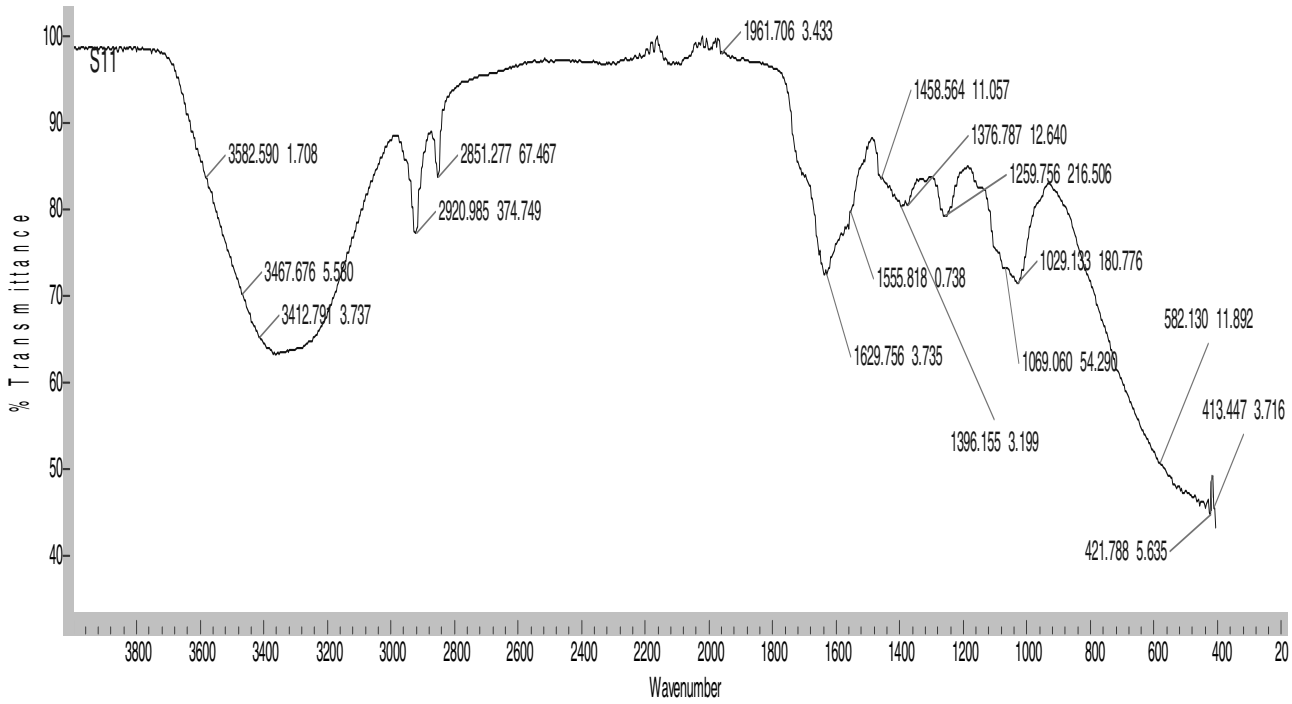


Figure 1. FTIR of Bhringaraj medicinal plant

TABLE -I
CHEMICAL COMPOSITION OF BHRINGARAJ PLANT LEAVES (ECLIPTA ALBA)

S.No	***Chemical constituents***	***Pharmacological acticity***	***Formula***	***Molecular weight (g/mol)***	***Iupac name***	***Other names***
1	Wedelolactone	Anti-hepatotoxic, Antibacterial, Trypsin inhibitor, Antivenom	$C_{16}H_{10}O_7$	314.24	1,8,9-trihydroxy-3-methoxy-6H-[1]benzofuro[3,2-c]chromen-6-one	
2	Demethyl wedelolactone	Antihepatotoxic, Antihaemorrhage, Antivenom, Dye (cosmetic)				
3	Apigenin	Anti-cancer, compound, Anti-inflammatory, flavonoids, Dye	$C_{15}H_{10}O_5$	270.24	5,7-Dihydroxy-2-(4-hydroxyphenyl)-4*H*-1-benzopyran-4-one	4',5,7-Trihydroxyflavone Apigenine, Chamomile, Apigenol,Spigenin,Versulin,
4	Leutolin7-O-gluoside	Antioxidant activity, Antimicrobial	$C_{21}H_{20}O_{11}$	448.37	2-(3,4-dihydroxyphenyl)-5-hydroxy-7 [(2*S*,3*R*,4*S*,5*S*,6*R*)-3,4,5-trihydroxy-6-(hydroxymethyl)oxan-2-yl]oxychromen-4-one	Glucoluteolin, Luteoloside, Cinaroside 7-Glucoluteolin 7-Glucosylluteolin Luteolin-7-glucoside Luteolin-7-O-glucoside
5	Stigmasterol	Antioxidant, Hypoglycemic	$C_{29}H_{48}O$	412.6908	(3*S*,8*S*,9*S*,10*R*,13*R*,14*S*,17*R*)-17-[(*E*,2*R*,5*S*)-5-ethyl-6-methylhept-3-en-2-yl]-10,13-dimethyl-2,3,4,7,8,9,11,12,14,15,16,17-dodecahydro-1*H*-cyclopenta[*a*]phenanthren-3-ol	Stigmasterin

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MHD Rivlin-Ericksen Free Convective Memory Flow through Porous Medium

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***Abstract* – Effects of free convective two dimensional unsteady Rivlin-Ericksen memory flow through porous medium of variable permeability, bounded by vertical porous plate with uniform suction and constant heat flux under the influence of uniform transverse magnetic field are studied. The permeability of porous medium fluctuates with time about a constant mean. Approximate solutions are found for mean velocity, transient velocity and temperature distribution. The temperature distribution and mean velocity are shown graphically and discussed.**

***Index Terms* – Magneto hydrodynamics, Free convection, Rivlin-Ericksen memory fluid, Porous medium.**

I. INTRODUCTION

In recent years, the problem of free convection flow through a porous medium of variable permeability has attracted the attention of many scholars. Sreekanth et al. [3] studied the fluctuating free convection through porous medium due to an infinite vertical plate with variable permeability. Rees and Pop [5] investigated free convective flow in porous medium of variable permeability effects. Singh et al. [6] have studied MHD free convective viscous flow past the vertical porous plate through non-homogenous porous media with radiation and temperature gradient dependent heat source in slip flow regime. Batarseh and Duwawri [7] have studied Isentropic sound propagation analysis and optimization over flat plate of saturated porous media of variable permeability. Noushima et al. [8] have studied Hydro Magnetic free convective Rivlin – Erickson flow through a porous medium of variable permeability. Uwanta et al. [9] analysed the heat and mass transfer flow through porous medium of variable permeability. Babu and Satya[10] have studied the influence of variable permeability and radiation absorption on heat and mass transfer in MHD micro-polar flow over a vertical moving porous plate. The variable permeability problem bounded by vertical plate has possible application in design of steam displacement process in oil recovery and geothermal systems.

Aim of the author is to extend the problem of [4] to Rivlin-Ericksen fluid [1] under the influence of transverse magnetic field.

II. FUNDAMENTAL EQUATIONS

The convective memory flow through a porous medium bounded by an infinite vertical porous plate with constant heat flux subject to uniform transverse magnetic field is considered. x- axis is taken along the plate in the upward direction and y–axis normal to it .

All the fluid properties are assumed to be constant, except the influence of density variations with temperature is considered only in the body force term. The magnetic field of small intensity H_0 is induced in the 'y 'direction since the fluid is slightly conducting, the magnetic Reynolds number is very much less than unity hence the induced magnetic field is omitted in comparison with the applied magnetic field. The viscous dissipation and Darcy's dissipation terms are omitted for small velocities. The flow in the medium is entirely due to buoyancy force. Under these conditions, the governing equations of flow are

$$\frac{\partial v}{\partial y} = 0 \qquad \text{i.e} \quad v = -v_0 \qquad (2.1)$$

$$\frac{\partial u}{\partial t} + v\frac{\partial u}{\partial y} = g\beta_1(T - T_\infty) + \vartheta\frac{\partial^2 u}{\partial y^2} + \frac{\beta}{\rho}\left[\frac{\partial^2 u}{\partial t \partial y^2} + v\frac{\partial^3 u}{\partial y^3}\right] - \frac{\vartheta u}{k(t)} - \left(\frac{\sigma\mu_e^2 H_0^2}{\rho}\right)u \qquad (2.2)$$

$$\frac{\partial T}{\partial t} + v\frac{\partial T}{\partial y} = \frac{\kappa}{\rho C_p}\frac{\partial^2 T}{\partial y^2} \qquad (2.3)$$

Where u and v are velocity components along x and y axes, and 'k' is the permeability of porous medium.

$$k(t) = k_0(1 + \varepsilon e^{i\omega t}) \qquad (2.4)$$

Where $'k_0'$is the mean permeability of the medium, $'\omega'$ the frequency of fluctuation, 't ' the time and $'\varepsilon'(<<1)$ is a constant quantity.

The boundary conditions are:

$$y = 0, \quad u = 0, \quad \frac{\partial T}{\partial y} = -\frac{q}{\kappa}$$

$$y \to \infty, \quad u = 0, \quad T = T_\infty \qquad (2.5)$$

Introducing the following non-dimensional quantities:

$$y' = \frac{yv_0}{\vartheta}, \quad t' = \frac{tv_0^2}{4\vartheta}, \quad \omega' = \frac{4\vartheta\omega}{v_0^2},$$

$$M = \frac{\sigma\vartheta H_0^2\mu_e^2}{\rho v_0^2}, \quad u' = \frac{u}{v_0}, \quad P = \frac{\mu C_p}{\kappa}$$

$$G = \frac{g\beta_1 q\vartheta^2}{\kappa v_0^4}, \quad k_0' = \frac{k_0 v_0^2}{\vartheta^2}, \quad R = \frac{\beta_1 v_0^2}{\vartheta^2},$$

$$\theta = \frac{(T - T_\infty)\kappa v_0}{q\vartheta} \qquad (2.6)$$

The equations (2.2) and (2.3), in view of (2.4) and (2.6) reduce to the following form.

$$\frac{1}{4}\frac{\partial u}{\partial t} - \frac{\partial u}{\partial y} = G\theta + \frac{\partial^2 u}{\partial y^2} + R\left(\frac{\partial^3 u}{4\,\partial t\,\partial y^2} - \frac{\partial^3 u}{\partial y^3}\right)$$

$$- \frac{u}{k_0(1 + \varepsilon e^{i\omega t})} - Mu \qquad (2.7)$$

$$\frac{1}{4}\frac{\partial\theta}{\partial t} - \frac{\partial\theta}{\partial y} = \frac{1}{P}\left(\frac{\partial^2\theta}{\partial y^2}\right) \qquad (2.8)$$

The corresponding boundary conditions become

$$y = 0, \quad u = 0, \quad \frac{\partial\theta}{\partial y} = -1$$

$$y \to \infty, \quad u = 0, \quad \theta = 0 \qquad (2.9)$$

III. SOLUTION OF THE PROBLEM

The partial differential equations (2.7) and (2.8) are reduced to ordinary ones by assuming the following series expressions for velocity and temperature fields.

$$u(y,t) = u_0(y) + \varepsilon e^{i\omega t}u_1(y) \qquad (3.1)$$

$$\theta(y,t) = \theta_0(y) + \varepsilon e^{i\omega t}\theta_1(y) \qquad (3.2)$$

Substituting equations (3.1) and (3.2) in equations (2.7) and (2.8) and equating the coefficients of like powers of ε to zero, the differential equations so obtained are

$$Ru_0''' - u_0'' - u_0' + \left(\frac{1}{k_0} + M\right)u_0 = G\theta_0 \qquad (3.3)$$

$$Ru_1''' - \left(1 + \frac{Ri\omega}{4}\right)u_1'' - u_1' + \left(\frac{1}{k_0} + M + \frac{i\omega}{4}\right)u_1$$

$$= G\theta_1 + \frac{u_0}{k_0} \qquad (3.4)$$

$$\left(\frac{1}{P}\right)\theta_0'' + \theta_0' = 0 \qquad (3.5)$$

$$\left(\frac{1}{P}\right)\theta_1'' + \theta_1' - \left(\frac{i\omega}{4}\right)\theta_1 = 0 \qquad (3.6)$$

The corresponding boundary conditions become

$$\theta_0' = -1, \theta_1' = u_0 = u_1 = 0 \text{ as } y = 0$$

$$\theta_0 = 0, \theta_1 = 0 = u_0 = u_1 = 0 \text{ as } y \to \infty \qquad (3.7)$$

The differential equations (3.3) and (3.4) are of third order when $R \neq 0$ and two boundary conditions are there. So Beard and Walters [2] rule gives rise to,

$$u_0 = u_{01} + Ru_{02} + o(R^2) \qquad (3.8)$$

$$u_1 = u_{11} + Ru_{12} + o(R^2) \qquad (3.9)$$

Substituting these equations (3.8) and (3.9) into (3.3) and (3.4) equating different powers of R and neglecting, $o(R^2)$, there by

$$u_{01}'' + u_{01}' - \left(\frac{1}{k_0} + M\right)u_{01} = -G\theta_0 \qquad (3.10)$$

$$u_{11}'' + u_{11}' - \left(\frac{1}{k_0} + M + \frac{i\omega}{4}\right)u_{11} = G\theta_1 - \frac{u_{01}}{k_0} \qquad (3.11)$$

$$u_{02}'' + u_{02}'\left(\frac{1}{k_0} + M\right)u_{02} = u_{01}''' \qquad (3.12)$$

$$u_{12}'' + u_{12}' + \left(\frac{1}{k_0} + M\right)u_{12} = u_{11}''' - \left(\frac{i\omega}{4}\right)u_{11}'' - \frac{u_{02}}{k_0} \qquad (3.13)$$

The boundary conditions are

$$u_{01} = u_{02} = u_{11} = u_{12} = 0 \text{ as } y \to 0$$

$$u_{01} = u_{02} = u_{11} = u_{12} = 0 \text{ as } y \to \infty \qquad (3.14)$$

The velocity and temperature fields are given by

$$u = u_0 + \varepsilon u_1$$

$$u = u_{01} + Ru_{02} + \varepsilon(u_{11} + Ru_{12})$$

$$= u_{01} + Ru_{02} + \varepsilon u_{11} \qquad (3.15)$$

$$\theta = \theta_0 + \varepsilon\theta_1 \qquad (3.16)$$

Solving (3.10 - 3.13) under boundary conditions (3.14), taking real part of the solution and can be put into form of fluctuating parts

$$u(y,t) = u_0(y) + \varepsilon[M_r \cos\omega t - M_i \sin\omega t] \quad (3.17)$$

The expression of transient velocity profiles for $\omega t = \pi/2$ is given by

$$u(y, \pi/2\omega) = u_0(y) - \varepsilon M_i \quad (3.18)$$

Where

$$u_0(y) = \frac{G}{P_2}[(e^{-r_1 y} - e^{-P_r y})(1 - RP_2) - Rr_2 e^{-r_1 y}] \quad (3.19)$$

$$\theta(y,t) = \left(\frac{1}{P_r}\right) e^{-P_r y} \quad (3.20)$$

For the sake of brevity constants and fluctuating parts are not given.

CONCLUSIONS

The temperature distribution decreases as Prandle number increases, is shown in fig 1. The mean velocity profiles are plotted in fig 2. Mean velocity increases with Grashoff number 'G_r' and Permeability parameter 'k_0' but decreases with Prandle number P_r and Hartmann number 'M'.

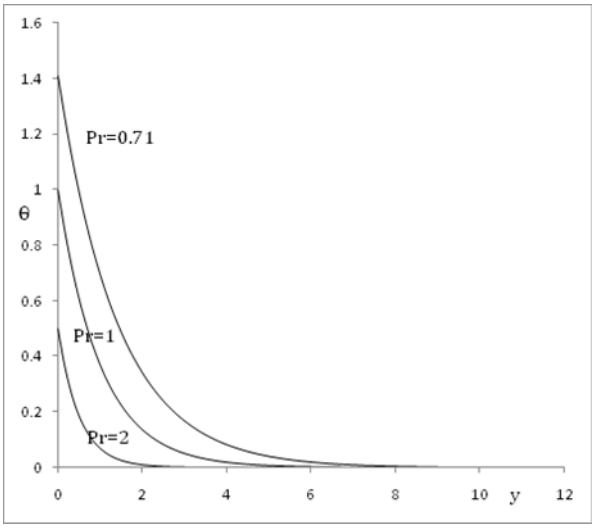

Figure 1. The temperature profiles for different values of Prandle number

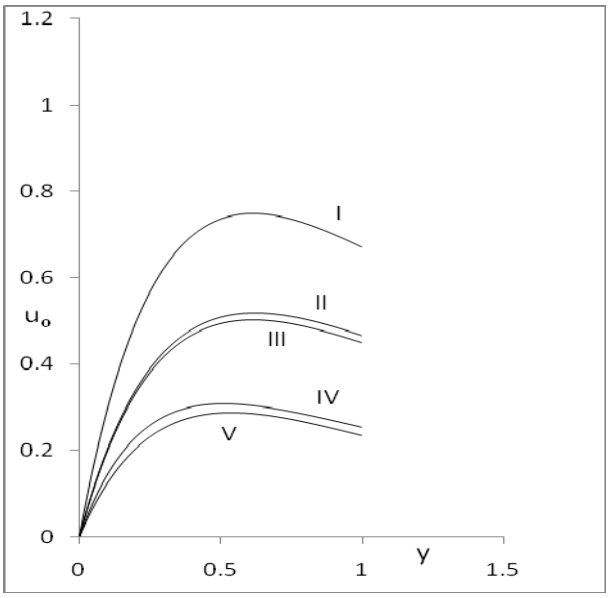

Figure . 2. Effects of k_o, M, G_r P_r on mean velocity u_o versus y for R = 0.05

	P_r	M	G_r	k_0
I	0.71	5	6	3
II	0.71	5	4	10
III	0.71	5	4	3
IV	0.71	10	4	3
V	1	5	4	3

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Social Marketing Strategies used for Fund Raising by NGOs Working in the Field of Disability Rehabilitation

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Abstract- **Fund raising is the process of inviting, mobilizing and collecting contributions in the form of money or other resources, by seeking donations from individuals, businesses, charitable foundations, or governmental agencies. Although fundraising typically refers to efforts to mobilize money for non-profit organizations, it is sometimes used to refer to the process of identification and tapping of prospective investors or other sources of capital for business enterprises. Many of the techniques and skills of fund raising can be or have been adapted from the domain of "marketing". Social marketing aims to achieve socially desirable goals, which benefits the society as a whole rather than for profit or other exclusive organizational goals. Social marketing includes the design, implementation and control of programs aimed to influence the acceptability of social ideas and involves considerations of product planning, pricing, communications and market research. In this sense, it has ingrained marketing principles. Social marketing strategy can be used for raising funds for the organizations, as the fund raising methods and social marketing strategies often move in tandem. This paper is aimed at studying the social marketing strategies used by NGOs working for disability rehabilitation to raise their funds. This study helps in revealing facts about the present scenario on social marketing among NGO sector. The sample size includes 15 NGOs located in and around Hyderabad working for rehabilitation of persons with disabilities It was observed that among the social marketing strategies, seeking individual donors and soliciting gift from major donors are most commonly used strategies by NGOs to raise their funds whereas the least used strategies include door to door solicitation, charitable games and street plays.**

Index Terms: **Social marketing, Fund raising, Disability rehabilitation.**

I. INTRODUCTION

In this competitive world everyone is eager or keen to establish themselves at international level. Everyone has serious concerns regarding the market share and their product offerings and their capacity and ability to reach consumer swiftly with less cost. All these objectives require the innovative applications of marketing strategies. 'Social marketing' approach has paid rich dividends in the service sector. Without doubt, it can be affirmed that social marketing can play a pivotal role for the success of Non Government Organizations working in the field of Disability Rehabilitation. The concept of social marketing implies planning and implementation of programs designed to bring about a social change using concepts from the sphere of business marketing. As defined by Kotler & Zaltman,(1971), "Social Marketing is the application of principles and techniques of marketing to achieve socially desirable goals, that is, benefits for society as a whole rather than for profit or other narrow organizational goals and includes the design, implementation and control of programs aimed to influence the acceptability of social ideas and involving considerations of product planning, pricing, communications and market research".

In basic terms, it is the effective promotion of ideas for bringing about discernible and perceptible change in society. Expressed more elaborately, it is creation, execution and control of programs designed to influence change in society. It uses many principles of business marketing - from assessing needs to identifying and focussing on audience, developing products and measuring outcome or results. Like business marketing, the primary focus is on the consumer--on learning what people need and want-- rather than trying to persuade them to buy what is produced. The planning process takes this consumer focus into account by addressing the elements of the "marketing mix." This refers to decisions about 1) the conception of a Product, 2) Price, 3) distribution (Place), and 4) Promotion. These are often called the "Four Ps" of marketing. Social marketing consists a few more 'P's as the elements of marketing mix apart from the Four 'P's mentioned already.

The social marketing "product" is not always a physical offering. A continuum of products exists, ranging from tangible, physical products (e.g., condoms, hearing aid, wheelchair etc.), to services (e.g., disability assessment, certification, medical exams etc.), and includes even practices (e.g., breastfeeding, physiotherapy, or eating a heart-healthy diet etc.). Finally, it also covers more intangible ideas such as environmental protection, rehabilitation models, policies etc. "Price" refers to what the consumer are willing and prepared to pay in order to obtain the product of social marketing. Social marketers balance these considerations, and often end up charging at least a nominal fee to enhance perceptions of quality and to provide a sense of "dignity" to the transaction. These perceptions of costs and benefits can be ascertained through the process of consumer survey research, and can be used in positioning the product. "Place" is all about the outlets or channels for the product to reach the consumer quickly at economical

costs. For a tangible product, this refers to the chain of distribution system--including the warehouse, trucks, sales force, retail outlets --where it is sold, or places where it is given out freely. For an intangible product, 'place' is less clear-cut, but refers to the decisions with regard to the marketing or distribution channels through which consumers are reached by means of information or training. This may include doctors' offices, shopping malls, mass media vehicles or in-home demonstrations. Finally, the last "P" is promotion. Promotion consists of the integrated use of marketing communications elements such as advertising, public relations, promotions, media advocacy, personal selling and entertainment vehicles. Additional social marketing "P's" are Publics, Partnership, Policy, Purse Strings etc.

II. EVOLUTION OF SOCIAL MARKETING

Social marketing was "born" as a discipline in the 1970s, when Philip Kotler and Gerald Zaltman realized that the marketing principles that were used to sell products to consumers can be equally potent to "sell" ideas, attitudes and behaviours. Kotler and Andreasen define social marketing as "Differing from other areas of marketing only with regard to the objectives of the marketer and his or her organization. Social marketing seeks to influence social behaviours not for the benefit of marketer, but for the benefit of the target audience and the society at large." This technique has been used extensively in international health programs, especially for contraceptives and Oral Re-hydration Therapy (ORT), and is being used with increased frequency in the United States of America in such diverse areas such as drug abuse, heart disease and organ donation. The sphere of health communications has witnessed rapid changes over the past two decades. It has fully evolved from the previously held one-dimensional reliance on public service announcements to blossom into a more sophisticated approach of comprehensive "social marketing." Rather than information being conveyed through 'top-down' approach, public health professionals are sensitised and trained to listen to the needs and desires of the target audience at the grass-root level, and build the program from there. This focus on consumer involves in-depth research and constant re-evaluation and reassessment of the program at every stage. In fact, research and evaluation together form the very cornerstone of the social marketing process.

Now, we know for sure, that the social marketing is for the cause of social change and its success hinges heavily on all segments of society. People with disabilities are one among the major stakeholders in the society and social marketing can be a catalyst for Disability Rehabilitation-centric social development and positive changes towards this end in society. Non Governmental Organizations or NGOs have multiple objectives and adopt distinct methods to achieve each of their objectives, each of them ultimately; resulting in development of the people and society they serve. They are non-profit voluntary groups organized at the local, national or international level. Non-governmental organizations are engaged in either campaigning or advocating sensitive issues, working on capacity building programs, concentrating on social research, or providing significant networking opportunities. Many NGOs work for the welfare of persons with disability and funds for the organization are needed to provide rehabilitation services. To meet the continuous requirement of funds for providing services, apart from the grants received from government, the organization resorts to specific fund raising methods.

III. FUNDRAISING AND SOCIAL MARKETING

Fundraising can be viewed as the process of inviting and mobilizing contributions as money or other resources, by seeking donations from individuals, businesses, charitable foundations, or governmental agencies. Although fundraising typically refers to efforts to mobilize money for non-profit organizations, it is sometimes used to refer to the identification and tapping of investors or other sources of capital for business enterprises. Many of the techniques and skills of fund raising (some of which are included here) can be or have been adapted from the profession of "marketing" (in fact, fund raising is referred to as "marketing" by many NGOs). While marketing and sales skills can be valuable, they must always be applied in an ethical manner.

Marketing is the process of ascertaining the needs and wants of customers by performing systematic market research, enabling the sale of products and/or services to customers through transaction and exchange and promoting them through integrated marketing communication to further enhance the sales. Marketing is the process through which companies build strong customer relationships and create value for their customers and for the organizations. Social marketing strategy can be used for raising funds for the institutions as the fund raising methods and social marketing strategies often move in tandem. By using these social marketing strategies, notable improvements in the fundraising effort could be seen. These strategies have, in effect, two dimensions, one raising the awareness of the people and sensitizing them to the basic cause and two in raising the fund for the specific cause.

IV. RESEARCH RELATED TO SOCIAL MARKETING AND FUND RAISING

While reviewing the literature for a period of two months, the researcher came across nearly 20 journals relating to different disciplines from various sources, e- journals like Social marketing quarterly, Books like Marketing Social Change: Changing Behaviour to Promote Health, Social Marketing: Improving the Quality of Life, etc. From the pool of literature surveyed, researcher has focused his attention on roughly 250 articles relating to different areas like health, road safety, nutrition, awareness on disability, non-profits, cancer prevention, etc. Around 153 articles among the ones reviewed belong to the domain of social marketing published in journals like "Journal of social work in disability & rehabilitation", "Journal of the royal institute of public health", "Journal of public transportation", "Health marketing quarterly", "American journal of infection

control", "Journal of business research", "Social marketing quarterly", etc. Upon classifying the articles according to the nature of study, it was found that 64% of the studies are related to the applications of social marketing in various settings, around 12% of the studies are related to theory and review, 6% on case study and the rest of 18 % can be grouped under other studies like training initiatives, resources, book review, etc. It was also noticed that around 68% of the studies are survey type research and 72% are descriptive in nature and only a small percentage i.e., 18% are experimental in nature.

From the review of literature, it can be concluded that in the area of "health", available studies are more in numbers (around 25%) followed by nutrition (13%), cancer prevention (12%), no-smoking (12%), HIV/AIDS prevention (8%), road safety (8%), awareness of non-profit (6%), behavioural change (5%), community development (5%), anti-drug campaign (4%) respectively. Only 2% of the literature surveyed focus on the topic of Disability Awareness.

The ultimate goal of fundraising for non-profit organizations is to draw in resources, which in turn enable the organizations serve their missions. Therefore, organizations consider and weigh both costs (investments) and savings (returns) before making their foray into online fundraising efforts. A study of United Kingdom charities found that online donations exceed both initial and regular maintenance costs of the organizations' websites (Sargeant et al., 2007). According to Sen & Swamy (2004), the example of an unique institution used by 19th century Indian guilds to raise funds is highlighted. On certain holidays only one shop was allowed to operate; an auction would be held to sell this right, and the winning bid would go to the guild fund. They compare this "taxation by auction" mechanism with more conventional tax schemes and show that under certain conditions, not only a majority of guild members prefer to be taxed via an auction, but also that this form of taxation is perceived to be more equitable.

There are various method adopted by NGOs in fund raising process, for the last several decades. Many NGOs used the traditional method of fund raising like fund for well being, donation for charity etc., whereas, only a few NGOs adopted new innovative ideas. It is a known fact that for NGO, to sustain itself in community for a long run, fund is the major requirement, and there are very few studies on the method of fund raising to make NGO self sustainable. The research work related to the use of social marketing strategies in fund raising is very limited.

V. PRESENT STUDY

In the course of review of literature, the researcher had identified various social marketing strategies used for fundraising across the world. The researcher has felt the need to study the social marketing strategies used for fundraising by Indian NGOs working in the field of disability rehabilitation. Hence, the major objective of this study was to find out the social marketing strategies used for fund raising by NGOs working in the field of Disability Rehabilitation. For this study, survey research design was used with a sample of 15 NGOs working in the field of disability rehabilitation, located in Secunderabad and Hyderabad. The study uses purposive sampling as a method to select the sample of the study. The samples were chosen by keeping following inclusive criteria into consideration:

1. NGOs working in the field of disability rehabilitation.
2. NGOs located in and around Hyderabad and Secunderabad.
3. NGOs that have at least 1-year experience in this field.

In order to collect data, a questionnaire was developed by the researcher to find out social marketing strategies used for fund raising by Indian NGOs working in the field of Disability Rehabilitation. The questionnaire was divided into three parts:

1. General information regarding organization, for example: name, address, and contact person's name and designation, year of establishment etc. It also includes the question regarding geographical areas of operations like urban, rural and both, information regarding service delivery model like IBR (institutional based rehabilitation), CBR (community based rehabilitation) or both and the annual expenditure,
2. Along with the general questions, the questionnaire also had a few close ended questions intended to elicit information specifically to the aspects related to funding of the organization, with options of choice of either "yes" or "no".
3. The third section of the questionnaire is devoted to elicit information regarding the use of 27 social marketing strategies, identified as 'social marketing strategies' for fund raising by many NGOs, across the world. These strategies include: 1.Attracting individual support and donations, 2.Soliciting gifts from major donors, 3.Promoting legacy gifts or planned giving, 4.Holding special events, 5.Raising money from business or sales, 6.Corporate sponsorship/ gifts, 7.Charitable gaming, 8.Auctions, 9.Door-to-door solicitation, 10.Holding a capital campaign, 11.Conducting private parties, 12.Conducting street plays, 13.Conducting cultural shows, 14. Through news paper, 15.Advertisement through T.V channels, 16.Advertisement through radio, 17.Banners, 18.Distributing pamphlets, 19.Coin/ fund boxes at public centers, 20.E-mail appeals, 21.E-news letter appeals, 22.Promotion on other sites, 23.Donated banner ads run on other sites, 24.Creating online fund transfer, 25.Home based services, 26.Institutional based services and 27.Community based services. The respondent was asked to mention whether the organization is using the particular strategy for fund raising or not.

Ten professionals working in the field of disability rehabilitation had validated the tool (questionnaire) for its content. Since, nine out of the ten professionals have approved 100% of the contents of the questionnaire; it was used, as it was framed, for the study, without any changes. The researcher had collected the data by visiting the respondents personally and seeking their responses by administering the questionnaire.

VI. MAJOR FINDINGS

The data obtained through the questionnaire was analyzed by using statistical mean and standard deviation. The results, and their interpretation and discussions on the findings in relation to the objective are presented as below:

Among the sample NGOs (n=15) chosen for the study, the oldest NGO was established in 1943 and the recent one in 2009. The annual budget of the NGOs ranged from a minimum of Rs.2 lakhs to a maximum of Rs.1700 lakhs. Out of 15 NGOs, 33.3% of the NGOs use Institution Based Rehabilitation (IBR) as their service delivery model, whereas, 13.3% of the NGOs use Community Base Rehabilitation (CBR) as their service delivery model. 53.3% of the NGOs working for the rehabilitation of persons with disabilities use both IBR & CBR as their model for service delivery. Out of the sample selected for the study, it is found that 66.7% of the NGOs are not using funds from government and only 33.3% of the NGOs use government funds. 33.3% of the NGOs are able to get grants from the government to run their services. Out of 66.7% the NGOs, who do not get grant from government, 13.3% of NGOs are able to get funds from international funding agencies, while the rest of the 86.7% are not.

Regarding social marketing strategies used for fund raising by NGOs in the field of disability rehabilitation, 14 out of the 15 NGOs were attracting individual support and donations whereas 10 NGOs are soliciting gifts from major donors. These two are the highly used strategies for fund raising by the NGOs selected for this study. The social marketing strategies that are not used by any NGOs within the sample group are; charitable gaming (e.g. raffles, bingo, golf, running), door-to-door solicitation, street plays, advertisement through radio and donation banners. The strategies like auctions, holding a capital campaign, conducting private parties and advertisement through T.V channels were used by only one NGO from the sample collected. Only two NGOs have used fund raising through social marketing strategies like; news paper, promotion on other sites, home based services, corporate sponsorship/ gifts, banners, coin/ fund boxes at public centres, e-news letter appeals. Creating an online fund transfer and community based services was used by 3 NGOs. Holding special events and cultural shows were used by 4 NGOs. Promoting legacy gifts or planned giving and raising money from business or sales were used by 5 NGOs. Distributing pamphlets and coin/ fund boxes at public centres were used by 6 NGOs.

As per the result of survey, the 27 Social Marketing Strategies (SMS) of fund raising can be grouped under five groups:

1. Group A - Never used SMS
2. Group B - Rarely used SMS
3. Group C - Sometime used SMS
4. Group D - Frequently used SMS
5. Group E - Most often used SMS

Strategies under Group A are "Never used SMS". These strategies are used by less than 1% of the disability rehabilitation organizations. These strategies (Fig. 01) are: 1).Charitable gaming, 2).Door-to-door solicitation, 3).Street plays, 4).Advertisement through radio and 5).Donated banner ads run on other sites. The reasons for not using these strategies could be the amount of time, energy and resources needed to utilize the strategies mentioned under Group A.

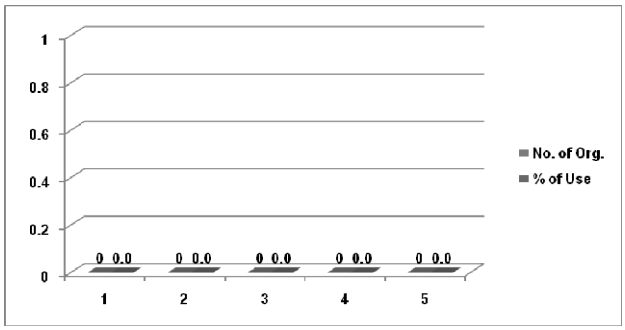

Figure.1 Group A - Never used SMS for Fund Raising by Disability Rehabilitation Organizations.

The fund raising strategies under Group B are "Rarely used SMS". These strategies are preferred by 01% to 10% of the NGOs. The strategies under Group B are presented in Fig. 02, these are: 1).Auctions, 2).Holding a capital campaign, 3).Conducting private parties and 4).Advertisement through T.V channels.

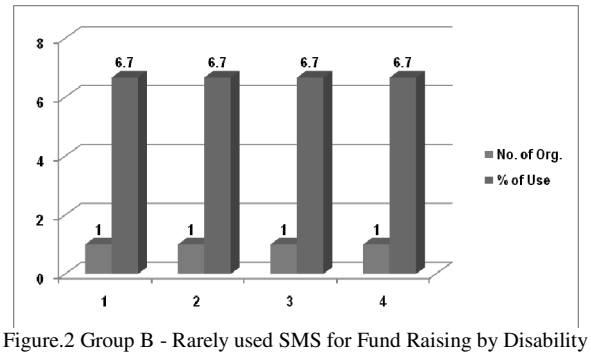

Figure.2 Group B - Rarely used SMS for Fund Raising by Disability Rehabilitation Organizations.

Strategies under Group C (Fig. 03) include 9 strategies categorized as "Sometime used SMS" and preferred by 11% to 25% of the NGOs working in the field of disability rehabilitation. These strategies are: 1).News paper, 2).Promotion on other sites, 3).Home based services, 4).Corporate sponsorship/gifts, 5).Banners, 6).Coin/fund boxes at public centres, 7).E-news letter appeals, 8).Creating an online fund transfer system and 9).Community based services.

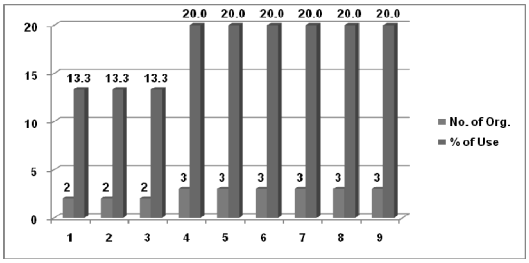

Figure.3 Group C - Sometime used SMS for Fund Raising by Disability Rehabilitation Organizations.

Even though the strategies mentioned in Group B & Group C need moderate amount of investment and have lesser probabilities of running into loss, the lack of skills required implementing these strategies restrict many NGOs to use strategies of Group B & Group C category.

Under Group D, 'Frequently used SMS" presented in Fig. 04, are used by 26% to 50% of the NGOs to raise their fund through: 1).Holding special events and 2).Cultural shows, 3).Promoting legacy gifts or planned giving, 4).Raising money from business or sales, 5).Distributing pamphlets and 6).E-mail appeals.

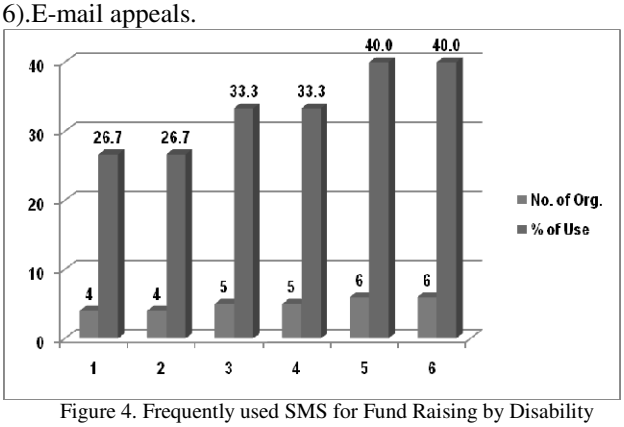

Figure 4. Frequently used SMS for Fund Raising by Disability Rehabilitation Organizations.

Fund raising strategies under Group E are presented in Fig. 05 and are categorized as "Most often used SMS" for fund raising in NGOs sector. The strategies under this category include: 1).Institutional based services, 2).Soliciting gifts from major donors and 3).Attracting individual support and donations. These strategies are used by more than 50% of the NGOs. In fact, the singular strategy of fundraising i.e., Attracting individual support and donations, is used by more than 93% of the NGOs.

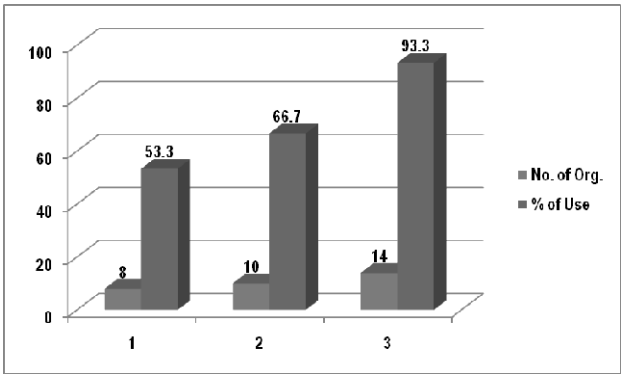

Figure.5 Most often used SMS for Fund Raising by Disability Rehabilitation Organizations.

This could be because of its cost effectiveness and easy approach. There are fewer chances of the strategy meeting with financial loss, as it hardly requires any investment and can generate huge amount.

CONCLUSIONS

The research was aimed at studying the social marketing strategies of fund raising used by NGOs working in Disability Rehabilitation sector. The pursuit of this objective helped in revealing facts which proved to be beneficial in gauging the present scenario on fund raising methods and social marketing strategies in NGOs. The study also gave rise to the inference that most of the NGOs are not focusing on social marketing as their prime strategy for fund raising. Further as mentioned in Para IV, the study on the topic was carried out based on the common thread of ideas found in the material from the following references.

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