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EDITORIAL

Volume 6 of the biannual journal of our college, CVR Journal of Science and Technology, is being brought out with 18 papers selected out of several papers received from the different branches of Engineering and Science.

Apart from the staff members of our college, the authors include a few from external institutions. It is gratifying to note the serious pursuit of research by our staff members. I am confident that the research activity will help in contributing to the quality of teaching apart from helping in providing valuable guidance to students in technical topics of current interest.

It is my earnest hope that the interest in contributing technical papers of high quality to our journal will grow further among the staff members of all the departments.

I wish to thank all the members of the Editorial Board for their support. Special thanks are due to Sri Deepak, Programmer in the Department of CSE for formatting the papers in camera ready form and for making the journal ready for final printing.

K.V. Chalapati Rao
Editor

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Object Tracking Using Computer Vision Techniques

N. Sushmitha[1], B. Meena[2], Mr.K.V Sriharsha[3], Dr N.V Rao[4]
[1]CVR College of Engg /CSE Dept, Hyderabad, India
Email:sushuma.shiri@gmail.com
[2]CVR College of Engg /CSE Dept, Hyderabad, India
Email:meenareddy38@gmail.com
[3]CVR College of Engg /I.T Dept, Hyderabad, India
Email: sriharsha.phd@gmail.com
[4]CVR College of Engg /CSE Dept, Hyderabad, India
Email:nvr@ieee.org

***Abstract*--Computer vision basically deals with different factors such as modeling of camera, lighting, color, texture, shape and motion that affect images and videos from visual inputs. Object detection and tracking are important components in many computer vision applications including activity recognition, traffic monitoring and automotive safety. This paper is about locating a moving object (or multiple objects) over a time using a stationary camera and associating the target object detections in consecutive video frames. In this perspective a video is captured by digital camera and is used for motion analysis. In the first stage of experiment frame differencing algorithm is chosen for object detection and its motion is estimated by associating the centroid of the moving object in each differenced frame. In the second stage of experiment same algorithm is chosen for object detection but motion of each, track is estimated by Kalman filter. However the best estimate is made by combining the knowledge of prediction and correction mechanisms that were incorporated as part of Kalman filter design. The tracking results obtained from two stages of experiment are presented for discussion.**

***Index Terms*- computer vision, object tracking, centroid, image filtering, grey thresholding, morphological, dilation, erosion, trajectory, point tracking, Kalman filter, dynamic model, observation model**

I. INTRODUCTION

Earlier computer vision systems [1] are only concern with scene analysis. The scene analysis is about recognizing the activities in a scene and to assimilate information from the sequence of images as a whole. There are two types of scene analysis one is static and the other is dynamic. Static scene analysis is about recognizing and understanding the activities of static objects from a stationary camera. There is a little scope of applying static scene analysis in the current day applications. Nowadays while observing a scene, the activities will never be static, they will be changing or moving rapidly with in a fraction of seconds. In such case there is a necessity to perform dynamic scene analysis. The changes in the scene may arise due to motion of camera or object. However system must be able to detect and track the changes that are going on rapidly over stationary or non stationary background. The dynamic scene analysis can be done in three cases stationary camera among moving objects (SCMO), Moving camera among stationary objects (MCSO), moving camera among moving objects (MCMO). As the researcher goal is to identify the objects of interest, track the motion, compute the characteristics of motion, SCMO gained much attention in this regard. In our paper the discussion is confined to stationary camera among moving objects. The analysis is about interpreting the activity of the scene by indentifying the objects of interest, classifying them and estimate the trajectory of object in the image plane as it moves around the scene. For tracking an object over a scene it is essential to represent [2] an object either using a shape or appearance. There are different ways in which an object can be represented by shape; one way is representing an object by a point (centroid), or a set of points. The other representations are primitive geometric shapes such as rectangle, ellipse are used for tracking rigid and non rigid objects. There are also other categories of representations like boundary of an object (contour) and region inside the object (Silhouette) which are used for tracking complex non rigid shapes. As point representations are much more suitable for

tracking objects that occupy small regions in a space, they are used for dynamic scene analysis in our experiment. Appearance based representation is also enormously used in many computer vision applications especially for tracking objects accurately in a scene. Template is one among which is formed using geometric shapes or silhouettes. The well and extensively used template matching for tracking objects in successive fames uses template representation. This approach works well for the cases where position and orientation simply called as pose; do not vary while tracking the objects in successive frames .The other is probability density based. These may be parametric or non parametric. Parametric take 1D Gaussian distribution, n-D Gaussian distribution or Gaussain Mixture Models (GMM). The objective parametric probabilities density based representation is to characterize an image region by its statistics. If the statistics differ from background, tracking should be enabled. Coming to Non parametric representations the most widely used for target representation is color histogram, which is mathematical equivalent to discrete probability density function of target region.

II. OBJECT DETECTION

Whenever objects appear in a video for tracking, they require object detection mechanism. It is the first step for dynamic scene analysis. It includes image segmentation process where foreground objects are separated from background objects by applying thresholding techniques. There is a possibility that foreground pixels may be affected with noise where image filtering is required for noise removal. The moment filtered foreground pixels are obtained; they are grouped into connected regions. The connected regions are further used to extract individual object features such as bounding box, area, perimeter etc.

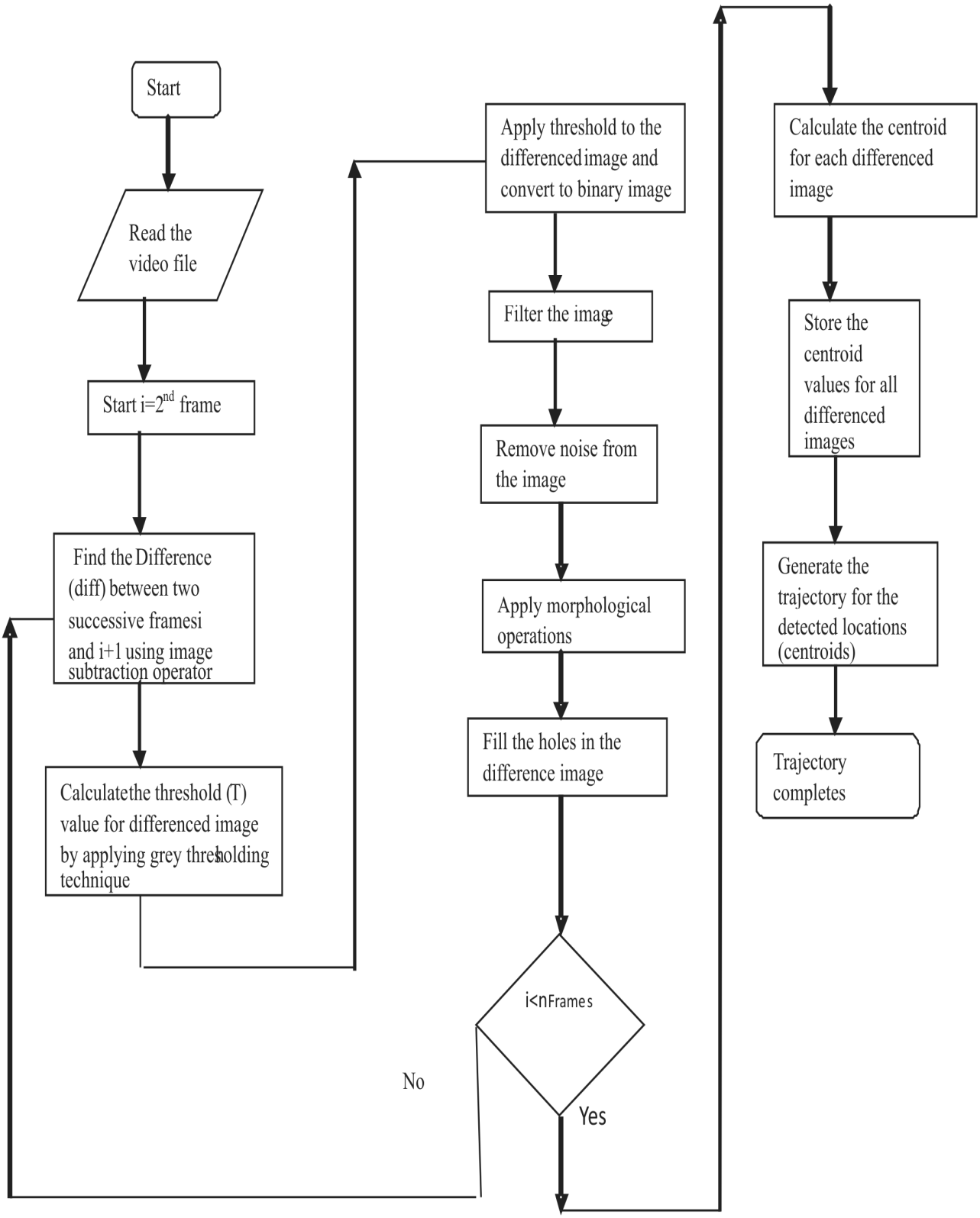
III. DIFFERENT TYPES OF OBJECT DETECTION MECHANISMS

Object detection [3] can be achieved by using a representation of a scene called background model and the comparing the model with each incoming frame. Any significant change observed in the image from the background model is considered as moving object and is processed further for analysis. This method is known as background subtraction .It is a popular pre processing step used in computer vision applications as it allows detections of objects of interest in stationary and non stationary background even when the camera is fixed. However the subtraction results in large number of false detections with the changes in illumination and fine scale motion in the scene. There are also statistical based detection methods like adaptive background mixture modeled by mixture of Gaussians. In order to know whether a pixel belong to foreground or background , Gaussian distribution of mixture model for that pixel is evaluated . The most simple one is temporal differencing (or frame differencing) takes pixel wise difference between two or more consecutive difference. This method is unable to detect the foreground object when texture is non uniform and when its speed is changing. However in our experiment We have chosen this method in order to avoid false detections.

IV. FIRST STAGE OF EXPERIMENT

A. Algorithm for object detection and tracking

In the first stage of experiment in order to identify the moving object in successive frames, frame differencing technique is applied. In this technique [4] a current frame is always subtracted from the previous frame by using image subtraction operator. The resulting differenced image is transformed to binary image as and when grey thresholding is applied. For removal of blur [5] (considered as Gaussian noise) in differenced image due to linear motion or unfocussed optics, filtering operation is applied. As it is known that Wiener filter is suitable for reconstruction of original from the noisy image and hence it is chosen for image filtering operation. Finally dilation and erosion operations are applied for removal of image imperfections. For each of the moving object that is identified in the preprocessed image, the centroid is computed. This centroid represents the moving object in each of the differenced image. Finally a trajectory is drawn by connecting the centroids of all differenced images [6]. The whole process is summarized in the following flowchart


Start
Read the video file
Start i=2nd frame
Find the Difference (diff) between two successive framesi and i+1 using image subtraction operator
Calculatethe threshold (T) value for differenced image by applying grey thresholding technique
Apply threshold to the differenced image and convert to binary image
Filter the image
Remove noise from the image
Apply morphological operations
Fill the holes in the difference image
i<nFrames
No
Yes
Calculate the centroid for each differenced image
Store the centroid values for all differenced images
Generate the trajectory for the detected locations (centroids)
Trajectory completes

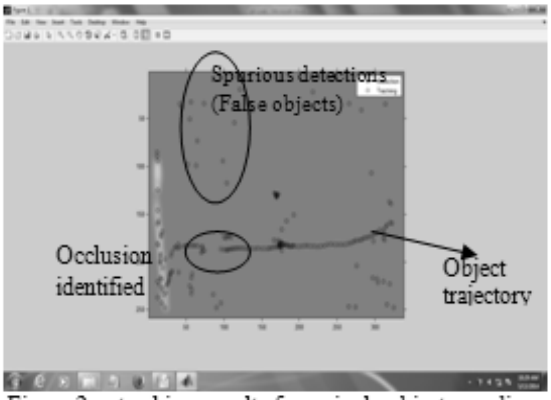


Figure.2.a: tracking results for a single object on adjacent Frames

The results obtained from fig 2.a plotted on the graph With frame number on X axis and number of objects on Y axis

Figure2.b: graph showing moving object along with spurious detection

The algorithm is again applied on odd number of frames and results obtained as follows.

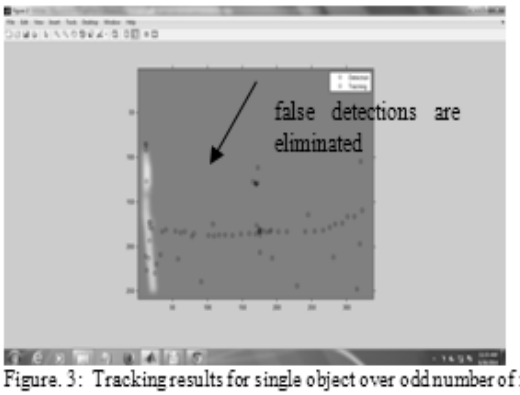


Figure. 3: Tracking results for single object over odd number of frame

V. CLASSIFICATION OF OBJECT TRACKING

Object tracking [7] can be categorized as point tracking, kernel based and silhouette based. Point tracking require object detection in every frame whereas kernel based and silhouette tracking only requires object detection when object first appear in the scene. In our paper the discussion is confined to point tracking .In this objects that are detected in successive or odd number of frames are represented by points. With an association of centroid of moving object over successive frames which includes object position and motion. Point tracking algorithms are either deterministic or statistical. Measurements obtained from video scene may be affected with noise and also object motion may undergo random perturbations. These are the challenges that are addressed in the deterministic methods. Statistical methods remove these uncertainties while estimating the state of an object in associated detections. Kalman filter falls under this category which can be applied to stationary and non stationary environments.

VI SECOND STAGE OF EXPERIMENT

A. Kalman filter for object tracking

Kalman filter [8] is s recursive predictive filter where each updated estimate of the state is computed from the previous estimate and the new input data. Hence only previous estimate requires storage. It eliminates the need for storing the entire past observed data. It is computationally more efficient than computing the estimate directly from the entire past observed data at each step of filtering process. In the previous case tracking results are not precise because of lack of prediction and correction mechanisms. Kalman filter make a good estimate by predicting the state of an object with dynamic model and correcting its state with observation model. Thus error covariance of the estimator is minimized by giving accurate tracking result.

B. Algorithm for frame differencing using Kalman filter

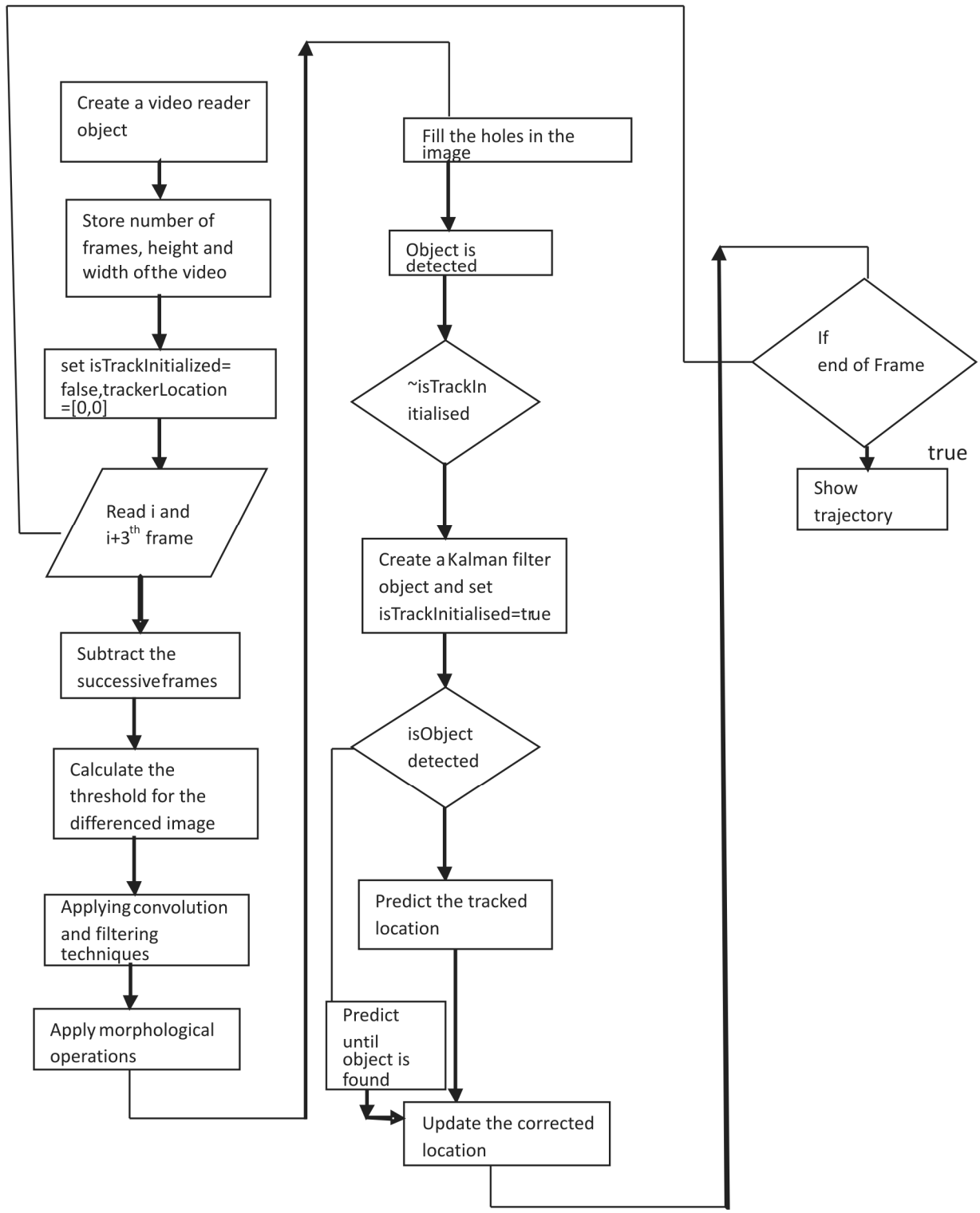


Figure.4: Object detection tracking using Kalman filter

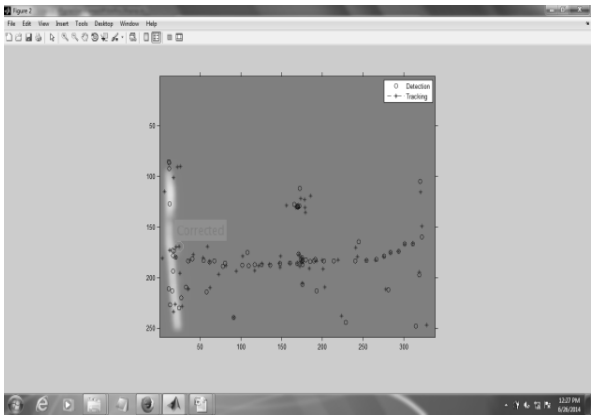


Figure.5: object detection and tracking using Kalman filter

From the fig. 5, it is observed that accurate tracking results were obtained with implementation of prediction and correction mechanism when compared to fig.2 & 3.

VII. CONCLUSION

In the first stage of experiment, moving object is detected and tracked successively by applying the algorithm on adjacent and odd number of frames. From the results obtained it is observed that comparatively less number of spurious detections were found by applying frame differencing algorithm on odd number of frames. As it was found that tracking results are not accurate in the first stage of experiment, Kalman filter is implemented and the path of the moving object is predicted and corrected.

VIII. FUTURE WORK

In this paper the discussion is confined to tracking single objects from a stationary camera, so the work is to be extended further on tracking multiple objects. The experiment is to be continued on moving object when camera is stationary and moving and at the same time it should possess the ability to cope up with complexities such as moving and changing objects, changing illumination and changing view points.

IX. REFERENCES

[1] Ramesh Jain , Rangachar Kasturi, Brian G.Schunck , Machine Viraw-Hill , Inc., ISBN 0-07-032018-7,1995

[2] A.Yilmaz, O . Javed , and M.Shah ,"object tracking: A srvey", ACM Computing Surveys,Vol. 38,No-4, Article - 13, December 2006.

[3] N Prabhakar , V . Vaithiyanathan, Akshaya Prakash Sharma , Anurag Singh and Pulkit Singhal ,"Object Tracking using Frame Differencing and Template matching", Research Journal of Applied Sciences , Engineeering and Technology 4(24):5497- 5501, Decemeber 15,2012.

[4] Macros martin-Fernandez, Emma Mnoz-Moreno, Carlos alberola-Lopez, "A Speckle Removal Filter Based on Anisotropic Wiener Filtering and the Rice Distribution" , IEEE Ultrasonics Symposim,2006.

[5] Rasit Koker , Serap Cakar , Cemil Oz , "Moving Object detection and Target Prediction in Video Image Using Computer Vision " ,proceedings of International Conference on Signal Processing , IJCI ,2003.

[6] Himani S.Parekh ,Darshak G.Thakore ,Udesang K. Jaliya ,"A survey on Object Detection and Tracking Methods", International Journal of Innovative research in Computer and Communication Engineering ,Vol.2,Issue 2,Febrary 2014.

[7] Ramsey Faragher, "Understanding the Basis of the Kalman Filter via a Simple and Intuitive Derivation", IEEE Signal Processing Magazine, September 2012

Managing Semantics of Graphic Components Through Remodeling Traditional Display Files

Dr. Hari Ramakrishna,
CBIT/ Computer Science and Engineering, Hyderabad, India
Email: dr.hariramakrishna@rediffmail.com

***Abstract*—Management, reuse and customization of semantics of graphic components through remodeling traditional display file models and graphic frameworks is presented. All these models are well tested in several graphic applications. A model debug driver tool application is adopted for the presentation of these models. Typical C++ code segments and Microsoft based visual studio application outputs are presented. These models are more generic and they can be used in any application domain using any language and development environment that support basic graphic primitives. The traditional ways of handling display files are also presented.**

***Index Terms*—Display files, Semantic graphic behavior, graphic components, graphic frameworks, debug driver tool, Microsoft graphic applications, object oriented models and frameworks. Dynamic display files.**

I. INTRODUCTION

Software industry is looking for rapid application development mechanisms with client orientation and short time span delivery, increasing quality and with-standing rapid changes in technology and requirements.

In this connection exporting third party tools plays a major role. Using third party tools decreases testing time. Development of frameworks for increasing degree of reuse has become an important focus. Customization of such frameworks as per client requirements increases importance of frameworks. Frameworks are different from libraries; client code is embedded in frameworks whereas client code includes and calls libraries. [1]

Display file concepts are traditionally used in several graphic models. Geometry of a graphic system is stored as a set of graphic instructions in display file. Display file interpreter recognizes these commands and generates graphics as per the client requirements.

Present day graphic and CAD systems are used at advanced levels. Present graphic systems demand implementation, and simulation of graphic components such that they mimic original real time components. Such requirements demand managing semantics of graphic components. These components should be in a position to implement their behavior, communicate with other components of the system and generate required graphics dynamically. These requirements demand remodeling of traditionally used graphic display file concepts.

II. TRADITIONAL DISPLAY FILE CONCEPTS

Display files store graphic behavior of elements of any graphic or GIS systems in a specific defined structure. The display file for general purpose interactive graphics software is divided into a set of segments such that each segment corresponds to a component of the overall display file. For example, in a building graphics information system, each civil engineering building element is treated as a segment. In other words, windows, doors, racks etc, which are known as civil engineering building elements, are stored in the display file as graphics segment. Sets of attributes are associated with each segment. All these attributes of segments are stored in segment-table.

The information that must be associated with each segment and how the information might be organized are important in understanding display file concepts. Each segment has its own unique name, and it can be referred with that name. For performing some segment operations like changing the visibility of segment, distinguishing the segment from other segments is required. When referring to a display file segment, set of display file instructions that belong to that segment are required. This may be determined by knowing where the display file instructions for that segment begin, and how many of them are there in its specific display file. For each segment, we need some way of associating its display file position information and its attribute information with its name. Sample display file attributes are listed in table 1.

Segmentation can be managed through a set of procedures to create, open, close and transform a segment. Sample user-routines needed to manage segments are listed in table 2.

The object-oriented dynamic display file models presented in this paper do not need implementation of segmentation requirements. The objects take care of

segmentation requirements as each graphic segment is defined as an object.

III. DISPLAY STRUCTURE MODELS

In the structure of the traditional display file, each display file command contains two parts: operation code (opcode), and operands. Opcode indicates what kind of command it is. Operands refer to required coordinates and other arguments required for executing the opcode. The display file is made up of a series of these instructions. The Display file stores all this information forming a huge storage. In the new concepts, this problem is solved as the display file for each component is generated dynamically. Only domain specific component state, and behavior identity are stored in the object itself. This information is helpful in the generation of display file content required for rendering that object.

In the traditional model, the display file must be large enough to hold all the commands needed to create the image. One must assign meaning to the possible operation code before proceeding to interpret them. For example, in a building graphical information system, various geometrical elements such as point, line, circle, arc and polygon may be considered. The general attributes of any simple display file instruction are -- the type of the geometrical element and its color, required coordinates and other geomantic information specific to that element.

The instruction is interpreted by invoking the required vector generator. The vector generators of special geometrical elements may need more information than that available in the main display file. This information is also in the form of graphics commands, which are stored in a separate display file. For example, all the instructions for plotting a polygon are in the polygon display file. Each vector generator of this type has its own interpreter for the interpretation of these commands. The starting-address and size of these instructions also are the needed attributes which are stored in the main display file. Figure 1 shows model sample storage of this type.

The information of the display file is useful to model the object and create the required image. The reason behind this is two-fold: some measure of device-independence is achieved, and it is easy to perform image transformation by changing the position and orientation of the required image. The display file contains the information necessary to construct the required image. The information can be in the form of instructions such as “move the pen”, “draw a line”, and “plot the required polygon”.

Saving instructions such as these usually takes much less storage than saving the picture itself. Each instruction indicates an action for the display device. A display file interpreter is used to convert these instructions into actual images. The display file interpreter serves as an interface between graphics program and the display device. The display file instruction may be actually stored in a file either for a display layer or for transfer to another machine. Such files of imaging instruction are sometimes called ”metafiles”. Table 3 presents sample vector-generating algorithms.

The vector generation algorithms used for dynamic display file based graphic framework presented are supported as a set of function libraries developed using Microsoft MFC classes. These algorithms are portable to any development environment that supports basic graphic primitives.

These functions are used by the display file interpreter while converting the display file instructions into the required picture on the display device. This process of generating image makes our graphics software independent of the nature of the display device and upon its software.

Whatever may be the way of storing and plotting the required images we require some tools for interaction with the graphics system. Table 4 presents various sample user-routines for building-graphics information system. Figures 1 and 2 present display file models for graphic framework. [2-6]

III. DYNAMIC DISPLAY FILE CONCEPTS

Dynamic display files are modeled to enable computation of graphic geometry online as per the behavior of the components. Such models enable graphic components to mimic real time components.

For example a printed circuit board (PCB) contains several electrical and electronic components. Each component has its own behavior. Similar components repeat several times in the same PCB but with different name, location and connections. They are exhibiting behavior as per the connected components.

Consider simulation of a logic circuit with electronic lids and electronic switches on a PCB. The lids get on and off as per the state of switches and logic circuit output. The dynamic display files enable the geometry of such components to get computed dynamically for each event of the model.

The display file in this model will be filled with display file instructions dynamically. Same display file can be reused for several components decreasing the object and class number in an application. This will enable complex applications to run on light weight systems with low configuration.

The debug driver tool is an application used for testing faulty components of a PCB board. As per the board structure the geometry is automatically computed. The required information is name of the board, board

type and structure of components on the board and their relations.

IV. GRPHIC APPLICATION USING DYNAMIC DISPLAY FILES

Implementation of graphic frameworks and applications using dynamic display files has several layers. Sample code segments and output screens along with advantages of such models are presented.

As a first step, display file and graphic primitive generation function libraries shown in table 2,3,4 need to be implemented. Function class frameworks are used for reuse and exporting such libraries as third party tools [1].

Graphic frameworks along with some graphic foundation classes are required in the next phase. Client component definition library and graphical user interface are required to build graphic applications.

Figure 3 presents a class diagram of the application developed in Visual studio Net 2010 that uses graphic framework developed using dynamic display file concepts. These concepts are more generic and they can be implemented in any application which supports basic graphic primitives. The class diagram presents MFC document view architecture used for providing GUI for the application. CView, CDocument, CDialog etc are MFC classes. Other classes are graphic framework classes that implement dynamic display file model.

V. CLIENT PROCEDURES FOR CONFIGURING GRAPHIC COMPONENTS

Some of the code segments that explain the implementation of dynamic display file are presented in this section. The domain client defines the component semantics for the generation of display file that compute the geometry required for display. Table 7 presents a sample code for component definition.

This procedure is not a member of CLogicCom class. It is a library function of a logic system for defining logic components. It is invoked from CLogicCom class Design method. This Design method is virtual function invoked whenever there is a need to re-compute the geometry of a component as per its behavior and status in the system. For example, in the LID device display the lights become on or off as per the data available in the system. The display file instructions are generated dynamically through invoking the procedure listed in table 9.

Figure 4 presents Logic Switch and Logic Display as per the user interface and logic circuit output. The green and white represent 1 and 0 (on and off). The red and black represent error and invalid data. The positions 4 and 7 represent error in red as the pins 4 and 8 are carrying invalid data. The first display is shown in green as the gate is AND gate and switches 2 and 3 are representing one. Depending on connections the component changes geometric behavior as per the requirement of simulation like components.

CONCLUSIONS

The traditional display file models and a model graphic framework based on traditional display files are presented. The dynamic display file concept and class diagrams along with sample code segments to demonstrate dynamic display file functioning concepts are presented. Output of a graphic application using dynamic display file concepts is presented. These concepts are applicable to any similar applications irrespective of application domain, object oriented development environment and development language with basic graphic support. The relation subsystem and other inherent concepts used are not covered in this paper.

REFERENCES

[1] Dr.Hari Ramakrishna, “A pattern language and traditional programming practices for exporting functionality” CVR Journal of Science & Technology, released in December 2013 ISSN 2277-3916

[2] Dr.Hari Ramakrishna, ”Pattern Approach to Build Traditional Graphic Frame works”, International 1 Journal of Computer Applications Volume 59– No.15, p35-42, December 2012. Published by Foundation of Computer Science ISSN :(0975 – 8887), New York, USA

[3] Dr. Hari Ramakrishna, “Design Pattern for Graphic/CAD Frameworks”, Ph.D thesis submitted to Faculty of Engineering Osmania University March 2003,

[4] Christopher Alexander, “An Introduction for Objectoriented Design”, A lecture Note at Alexander Personal web site www.patternlanguage.com

[5] Pattern Languages of Program Design. Edited by James O. Coplien and Douglas C. Schmidt. Addison-Wesley, 1995

[6] Erich Gamma, Richard Helm, Ralph Johnson, and John Vlissides, "Design Patterns: Elements of Reusable Software Architecture", Addison-Wesley, 1995

[7] Hari RamaKrishna “COM Applications for Real time Electrical Engineering Applications” IEEE sponsored International Conference at Bangalore - 2000.

[8] Hari RamaKrishna “Generation of flooring and wallpaper patterns using computer graphics” Proceedings of the First National Conference on Computer Aided Structural Analysis and Design, Jan 3-5,1996, Engineering Staff College of India and University College of Engineering, Osmania University, Hyderabad.

[9] Newman, W. S and Sproul, R.S (1981),Principles of interactive computer graphics McGraw-Hill International, second edition.

TABLE I
SEGMENT TABLE ATTRIBUTES

(1)	Segment name
(2)	Segment's starting address of the display file
(3)	Segment size i.e. number of instruction of segment
(4)	Segment visibility i.e. on or off
(5)	Segment transformation parameters i.e. scaling, translation, rotation around x,y,z axes
(6)	Segment reference point that is useful for transformations
(7)	Segment transparency (on or off) useful for hidden line and surface elimination Etc.

TABLE II
GRAPHIC SEGMENT TABLE INSTRUCTIONS

(1) Create-segment (n)
(2) close-segment (n)
(3) Append-segment (n)
(4) set-segment-visibility (n,I)
(5) Rotate-segment (n,ax,ay,az)
(6) translate-segment(n,tx,ty,tz)
(7) Set-segment-reference-point (n,x,y,z)
(8) scale-segment(n,sx,sy,sz)
(9) Show-segment (n)
(10) delete-segment (n)

TABLE III
DISPLAY ALGORITHMS

do-line3d (lc,bc,z,y,z),
do-point3d(lc,x,y,z),
do-circle3d(lc, cx,cy,cz,r,ax,ay,az),
doarc3d(lc,cx,cy,cz,r,sa,ea,ax,ay,az),
do-spehere)lc,cx,cy,cz,r) and
do-poly(lc,sadd,size:

where lc is the line foreground color, cz,cy,cz are the coordinates, sa, ea are the starting and the ending angles, ax, ay, az are the angles of inclination along x,y, and z axes respectively, and r is the radius.

TABLE IV
SAMPLE TRADITIONAL DISPLAY FILE USER ROUTINES FOR MANAGING GRAPHS

Move3d (x, y, z)
Line3d(x,y,z)
Line3d(lc,x,y,z)
Point3d(lc,x,y,z)
Arc3d(lc,x,y,z,r,sa,ea,ax,ay,az)
Circle3d(lc,x,y,z,r,ax,ay,az)

TABLE V
SAMPLE COMPONENT CLASS

```
class CLogicCmp :public Component
{
public:  -------
       BOOL   virtual IsLocated(CPoint);
       void virtual Design(void);
       ----------
};
```

TABLE VI
SAMPLE DISPLAY FILE INSTRUCTION ALGORITHM

```
void Component::LineTo(int x,int y)
{
         m_iNoOfInst++;
         DF[1][m_iNoOfInst] = 2;
         iPen_X = x;
         iPen_Y = y;
         DF[2][m_iNoOfInst] = iPen_X;
         DF[3][m_iNoOfInst] = iPen_Y;
}
```

TABLE VII
CLASSES OF DYNAMIC DISPLAY FILE FRAMEWORK

1) CDocument, CView, CLogicSystemView , CLogicsystemDoc are Microsoft based classes in Document view architecture.
2) CLogicCmp is inherited from Component and defines the behavior of domain specific components. In the above application components of a Degug driver tools which are defined. The function in table 6 will be invoked from design method of this class for loading behavior of a electronic LID component.
3) The Component class implement all the Display file procedures as per the definition of IDisplayFile Interface and other implicit procedures required.
4) The Graphic Element class implements all the procedures required for implementation of a graphic framework.
5) IGraphic Component is used to address all the graphic elements from Microsoft Document class. This can implement a generic persistence system which can be used to any graphic domain application using this framework.
6) The view class is inherited from Clogic Component for the purpose of creating a logic component. Even the GUI design can be reused for any domain similar to that of debugger driver tool.

TABLE VIII
COMPONENT CLASS MODEL

```
class Component : public CGraphElement
{
        < <Display file data definition >>
       << Display file implementation >>
<< virtual functions like >>
// For designing component at derived class
         void virtual Design(void);
// for rendering the component INTERPRETER
        void virtual Display(CDC* dc);
……
}
```

TABLE IX
COMPONENT SEMANTIC DEFINITION FOR A ELECTRONIC DISPLAY LID COMPONENT

```
void VRLogicLID(Component* ge)
{// Component color
        ge->SetLineColor(ge->GetBkColor());
        ge->RectSolidAt(0,0,100,100);
//  Inside Area
        ge->SetLineColor(LIGHTGRAY1);
        ge->RectSolidAt(0,0,96,96);
        ge->SetLineColor(DARKGRAY1);
        ge->RectAt(0,0,94,94);
        ge->RectAt(0,0,96,96);
        ge->SetLineColor(DARKGRAY1);
        ge->RectAt(12,0,24,85);
        ge->RectAt(12,0,18,80);
// Designing light on/off status
int k=1;
for (int i=-35;i<=35;i+=10)
{
  if (ge->GetData(k)==1)
        ge->SetLineColor(RGB(0,255,0));
  else if (ge->GetData(k)==0)
    ge->SetLineColor(RGB(255,255,255));
        else if (ge->GetData(k)==2)
        ge->SetLineColor(RGB(255,0,0));
        else
        ge->SetLineColor(RGB(0,0,0));
// 255,255,255 is white(0 or OFF)
// all zeros black (junk data)
// 255 ,0,0 is red(error in output)
//0,255,0 is green(1 or ON)
  ge->RectSolidAt(12,i,15,8);
  ge->SetLineColor(RGB(0,0,0));
  ge->RectAt(12,i,-15,8);
  k=k+1;
}
ge->SetLineColor(DARKGRAY1);
for(int  i= -35; i<= 35; i+=10)
{
        ge->MoveTo(-45,i);
        ge->LineRel(-15,0);
}// displaying pins of the component
// displaying text of the components
 ge->TextBkColor(LIGHTGRAY1);
 ge->TextColor(RGB(255,0,0));
 ge->TextAt(-40,25);
 ge->Text11At(-40,-25);
} // end of the procedure
```

TABLE X
DESIGN PROCEDURE

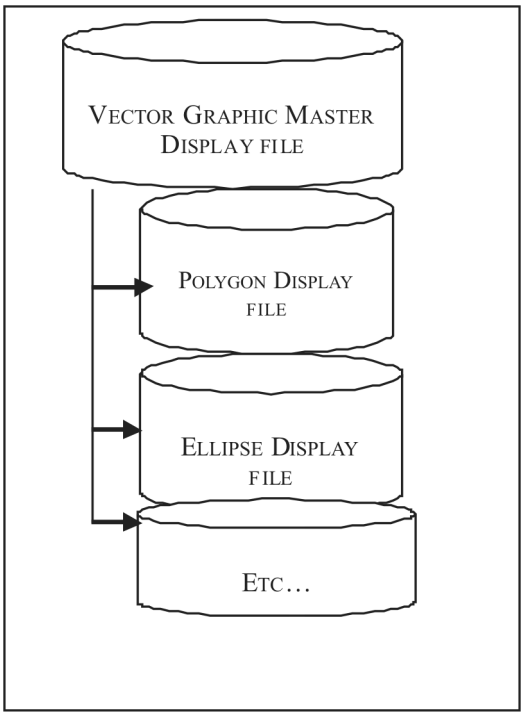
```
void CLogicCmp::Design(void)
{       switch(GetComponentType())
        { case 1: VRLogicLID (this);
                break;  …. }
}
```

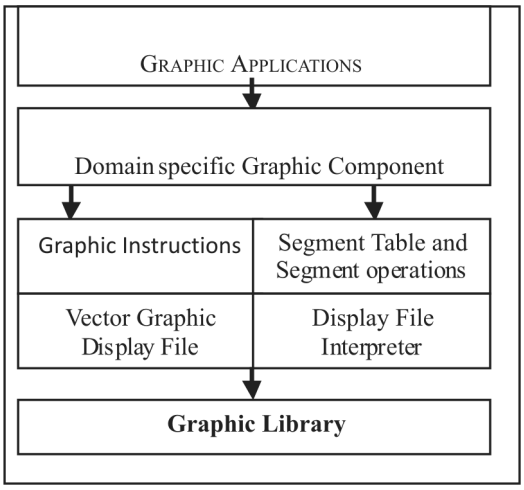
TABLE XI
INTERFACE IDISPLAYFILEINSTRUCTIONS

```
class IDisplayFileInstructions
{
public:
        // Display File Functions
        void virtual  MoveTo(int x,int y) = 0; // 1
        void virtual  LineTo(int x,int y) = 0; // 2
void virtual  TextAt(int x,int y) = 0; // 3  horizontal
void virtual  MoveRel(int x,int y) = 0;  // logical 1
void virtual  LineRel(int x,int y) = 0;  // logical 2
void virtual  TextRel(int x,int y) = 0;  // logical 3

void virtual  VerticalTextAt(int x,int y) = 0; // 4 Vertical
void virtual  VerticalTextRel(int x,int y) = 0; // logical 4
// 5 Rectangle
void virtual  RectAt(int x,int y,int a,int b) = 0;
// 6 used even for circles ellipses
void virtual  ArcAt(int x,int y,int sa,int ea,int r1, r2) = 0;
// 7 Filled Solid Ellise
void virtual  EllipseSolid(int x, y, a, b) = 0;
// 8 Solid Rectangle
void virtual  RectSolidAt(int x,int y,int a,int b) = 0;
// 9 Set color of line
void virtual  SetLineColor(COLORREF i) = 0;
// 10 Set FillColor
void virtual  SetFillColor(COLORREF i) = 0;
void virtual  Text1At(int x,int y) = 0; // 11
void virtual  Text2At(int x,int y) = 0; // 12
// 13 sets Text BkColor
void virtual  TextBkColor(COLORREF r) = 0;
// 14 Set TextColor
void virtual  TextColor(COLORREF col) = 0;
void virtual  Text11At( int x,int y) = 0; // 15 Text
void virtual  Text12At( int x,int y) = 0; // 16 Text
void virtual  Text21At( int x,int y) = 0; // 17 Text
void virtual  Text22At( int x,int y) = 0; // 18 Text

};
```

TABLE XII
GRAPHIC COMPONENT INTERFACE

```
class IGraphicComponent  :public
IDisplayFile, public IGraphicElement
{

 << Graphic Element interface contains
Graphic Framework user interface
Procedures >>
<< I Display file has
IDisplayFileInstructions and other related
interfaces >>

};
```





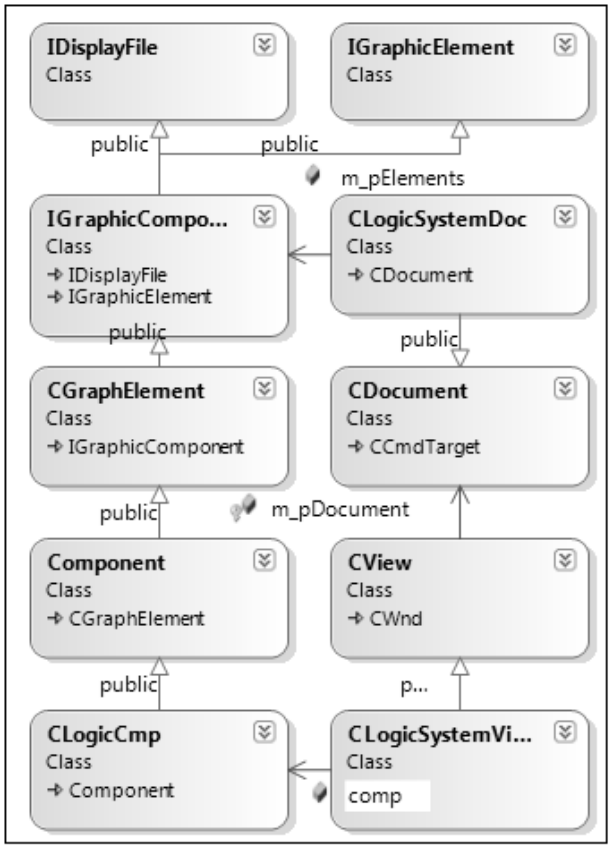


Figure: 3 Class diagram of a graphic application in Visual studio .NET 2010 using dynamic display files

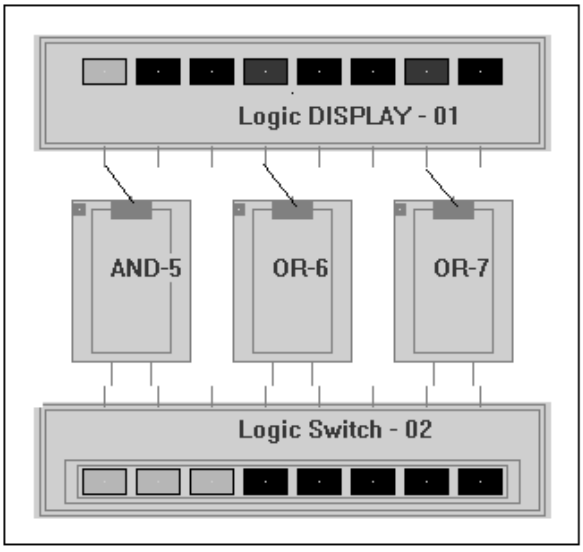


Figure: 4 A logic circuit designed with and OR gate, AND gate and logic switch components on a PCB.

Big Data Mining: Problems and Prospects

Nayani Sateesh
CVR College of Engineering/ Information Technology, Hyderabad, India
Email: nayanisateesh@gmail.com

***Abstract* - Nowadays decision making is going towards data centric and the data is becoming crucial in understanding the user needs and behavior so as to enhance the services. As the communication is going over the internet, lots and lots of data is being generated like in social networks, blogs etc., which is to be managed and analyzed properly. Big Data is becoming more prominent nowadays in the data management and processing. Big data deals with huge amount of data which is large in size, heterogeneous in nature, complex to process. In this paper I would like to review various problems in mining the Big Data and its applications in various sectors etc.**

***Index Terms*— Big Data, Data Mining, KDD.**

I. INTRODUCTION

From the recent past, we are hearing the most prominent topic or area is the big data in the information and communication technology (ICT) world. Because of data centric computing in understanding the user's behavior and their trend in the usage of services, Big Data is playing a vital role to gain the competitive edge in the market and to reach and increase the global customer base. In Big Data Analysis understanding the nature, significance of data and data visualization [1, 2] is more important. "Big Data" describes data sets so large and complex they are impractical to manage with traditional software tools. It relates to data generation, data storage, data retrieval and analysis of data that is remarkable in terms of size, type, and rate in which data being generated or stored.

II. BIG DATA: TREND AND CHARACTERISTICS

As per NESSI forum big data is defined [3] as "Big Data" is a term encompassing the use of techniques to capture, process, analyze and visualize potentially large datasets in a reasonable timeframe not accessible to standard IT technologies. By extension, the platform, tools and software used for this purpose are collectively called "Big Data technologies".

A. Data Trend

As per Oracle's review, data is being growing at 40% annual rate from the last few years and reaching by 45 ZB by 2020. The trend shows that the volume of business data significantly grows every year which emphasis the need for analysis of the data being generated to know the insights of the data to get the competitive edge in the market to showcase their products and service in an effective way to the users and hence to stand in the top place in the competitive global market.

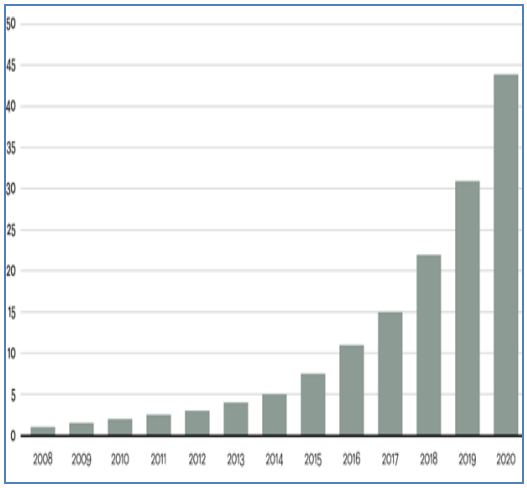


Figure 1: Data Growth (2008-2020)
Source : Oracle 2012 (Data in Zetta Bytes)

A. Characteristics

Characteristics of BIG Data can be usually called as 5 V's [4, 5]. They can be classified as Primary and Secondary characteristics based on their significance in Data Analytics.

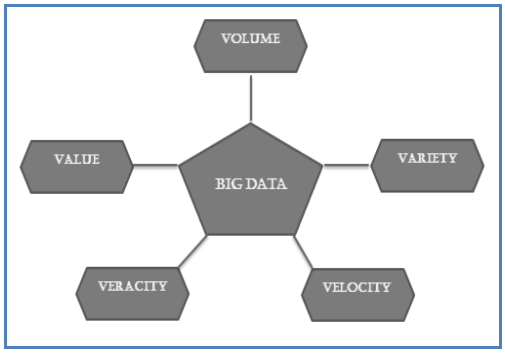


Figure 2: Characeristics of Big Data (5V's)

Primary Characteristics – 3V's (Volume, Variety, Velocity)
Secondary Characteristics – 2V's (Veracity, Value)
Volume: It reference to the size of the data being stored. The data size can be terabytes or petabytes or even more.

Variety: it refers to the structure or type of the data being stored. They include unstructured, semi-structured and structured. Examples of such variety are audio, video, xml, sensor data, text files etc.
Velocity: it refers to data rate at which data is being generated and stored into the databases.
Veracity: It refers to trustworthiness of the data being stored
Value: It refers to insight of the data being extracted from the stored data is useful and which will extend the business in terms of returns and market share [6].

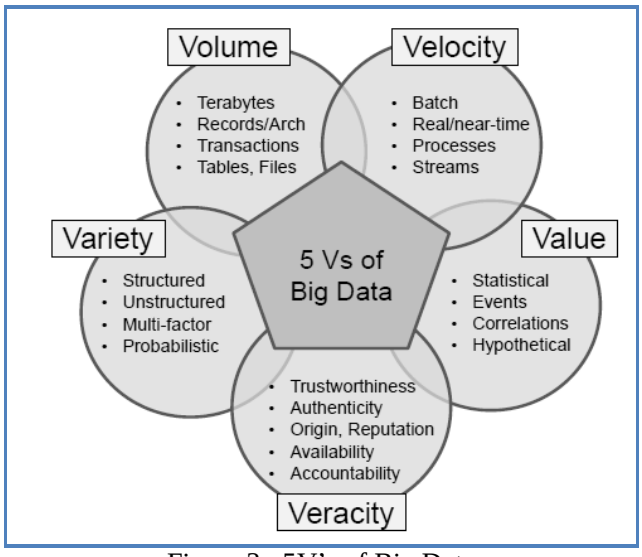


Figure 3: 5V's of Big Data

III – DATA MINING vs. BIG DATA MINING

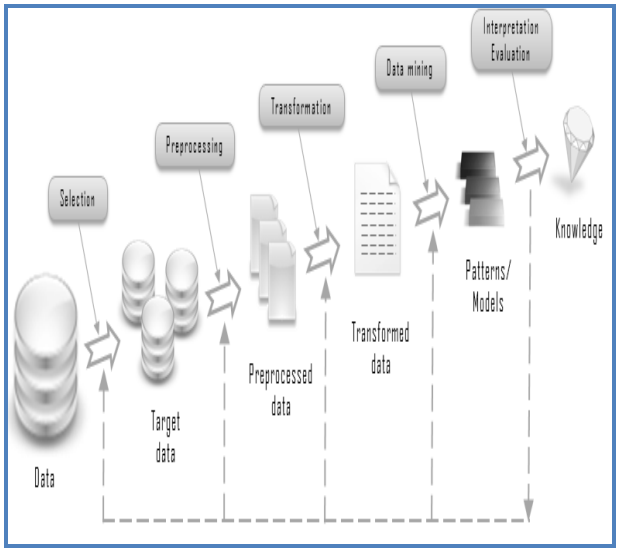
*Big Data for the Enterprise:*With Big Data databases, in any vertical enterprises can save money, achieve many other business objectives, grow revenue.

Using Big Data organizations can do the following:

Build new applications: Helps the organization to optimize the real data and build new applications to analyze and reuse the data
Improve effectiveness and lower the cost of existing applications: Many big data technologies are open source technology based; they can be implemented at low cost than proprietary technologies.
Realize competitive advantage: Big data can help businesses to act quickly to adapt to changes faster than their competitors.
Increase customer loyalty: Increasing the amount of data shared within the organization – and the speed with which it is updated – allows businesses and other organizations to more rapidly and accurately respond to customer demand.

A. *Data Mining*

According to Simoudis (1996) - Data mining can be defined as process of extracting previously unknown, comprehensible and actionable information from large databases and using it to make crucial business decisions. Data from various sources is integrated and then data is transformed to standard format after preprocessing. Using Data mining Algorithms interesting patterns and rules are extracted. The patterns and rules that are extracted are interpreted into the useful information which increases the knowledge of the end users.



A. *Mining Big Data – Problems*

Whatever the knowledge discovery process that we discussed above is also applicable for the Big Data also. Here in this section we will look on the possible problems [4, 7, 8, 9, 10, 11] that we face during the Big Data mining process with reference to knowledge discovery process.

a. *Data integration:* Since we are integrating the data from various sources, there exists a possibility of integrating unstructured, semi-structured and structured data. Data to be mined in big data will be huge in terms of terabytes, petabytes etc. This is one problem for the integration tools to integrate high volume and variety of data. Reliable and High quality data should be integrated and transformed to standard form.
b. *Preprocessing:* Since large data to be pre-processed due to Velocity of Big Data, the pre-processing tools or applications should be able to process the data in minimal time and to convert into standard form. Data scaling should be handled properly. Since large data is being stored and taken for the pre-processing, reliable and accurate data only to be taken.
c. *Data mining:* data mining algorithms should be able to process the huge amount of data and Variety of the data should be handled appropriately to extract the interesting patterns in minimal time. Here

sophisticated data mining algorithms are needed which will process the data at faster rate. Also people working on this domain should be highly skilled in processing and extracting interesting patterns.

d. *Evaluation and Interpretation:* The patterns should be evaluated effectively and should be presented visually which will increase the end user knowledge. Presenting the data in visual way in an effective manner and the people involved in the processing and presentation of the visualized data is an important factor in mining big data. Appropriately visualized data will provide the value to the data being mined and helps in increasing the business market. Visualization tools are more important in presenting the data patterns. Visualization tools that we are using should be appropriate and capable of handling and processing high loads of data.

B. Mining Big Data – Prospects & Applications

With the invent of internet, services nowadays are provided over the internet and with the social networking activities on day to day , large amount of data is being generated and stored in in the data bases in various formats. Integrating such data to understand the insights of the data and hence to understand the needs of the user and the trends in usage, Big data mining is playing a vital role.

Nowadays various organizations investing huge amounts in storing and processing of historical and real-time data as the decision making process is going towards the data centric and accurate decisions need to be taken based on the historical and real time data which is available. Lot of research work is going on towards data integration and effective visualization of qualitative patterns to be extracted.

Since Big data mining is an interdisciplinary, it has significance in various sectors in decision making process. It is generating huge amount of business returns [12].

The following figure illustrate the trend in Big Data market forecast

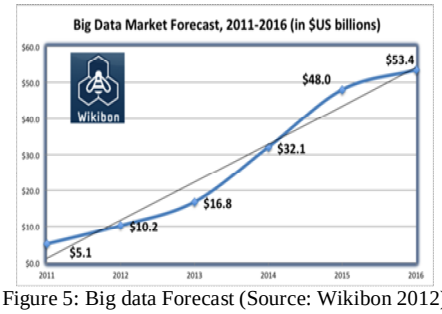


Figure 5: Big data Forecast (Source: Wikibon 2012)

Some of the applications [7, 8, 13, 14] of big data mining are:

1. *Social networking* – Based on user access patterns and data being used and generated, User Profiles can be analyzed effectively and the web pages can be personalized.
2. *Manufacturing*–Product modeling, quality and performance of the products can be analyzed and hence to customize the product to meet the customer needs.
3. *Weather forecasting* – Time series data can be analyzed effectively which helps in weather forecasting so as to alert the people and governments in case of natural disasters and other calamities.
4. *Marketing Research* – Product Reviews by the customers can be analyzed which helps in Sales Promotion, pricing and increasing the sales. It also, helps in understanding user buying behavior and sentiment analysis
5. *Advertising & Brand Promotion* – Designing the advertisements based on perspective of product performance and promoting the brands to retain the customers and also to create new customer base.
6. *BioInformatics*–Biological and genetic data like DNA sequence, protein sequence etc. can be analyzed in classification of species.
7. *Financial Data Analysis* – To detect the uncertainty and fraud in the financial data
8. *Healthcare* – To understand various vital statistics to classify the patients and disease level. Also helps in understanding the effectiveness of the drugs being given to the patients in curing the disease.
9. *Government & Political* - Evaluate the policies being implemented and the trend of the resources and budget being utilized can be analyzed.
10. *Retailing* – Managing the customer relationships and understating the user's needs and pricing modeling can be done.
11. *Energy* – Operation modeling can be done.
12. *Media & Telecommunications* – Network Optimization and fraud detection can be done.

CONCLUSIONS

During the next few years also Big Data is going to grow and continue since the need of the historical data and the management of real-time data which is generating in huge volume, which helps to understand the insights of the data and the user requirements to enhance the products and services so as to retain their space by the organizations in the global market since decision making is becoming data centric. Efficient Analytical Architecture is needed to handle the various problems that we discussed in this paper and the proper management of the variety of data being stored and the efficient visualization tools are also needed to improve

the visual appeal of the data insights which will improve the knowledge being mined. Big Data is becoming the new Final Frontier for scientific data research and for business applications and contributing to data science research.

FUTURE DIRECTIONS

Business Analytics and Big Data Tools need to be reviewed to get further insight into the research areas of Mining and visualizing Big Data.

REFERENCES

[1] Big Data Visualization: Turning Big Data Into Big Insights - A White Paper, Intel IT Center, Intel, March 2013

[2] Dennis McCafferty,"Data Visualization: Making Sense of Big Data", Baseline Magazine, April 2014.

[3] Big Data: A New World of Opportunities, NESSI White Paper, December 2012.

[4] Mrs. Deepali Kishor Jadhav, "Big Data: The New Challenges in Data Mining", International Journal of Innovative Research in Computer Science & Technology, Vol 1, Issue 2, Sept 2013, pp. 39-42.

[5] Yuri Demchenko, "Defining the Big Data Architecture Framework", University of Amsterdam, July 2013.

[6] Zhong Li, "Harness Big Data Value and Empower Customer Experience Transformation", Infosys Labs Briefings, Vol. 11, 2013, pp. 27-34.

[7] Katina Michael, Keith W. Miller , "Big Data: New Opportunities and New Challenges", IEEE Computer Society, Vol. 46, Issue No. 6, June 2013, pp. 22-24.

[8] Alexandros Labrinidis, H. V. Jagadish," Challenges and Opportunities with Big Data", Proceedings of the VLDB Endowment, Vol. 5, No. 12, pp. 2032- 2033.

[9] Big Data Strategy — Issues Paper, © Commonwealth of Australia, 2013.

[10] Divyakant Agrawal, et.al "Challenges and Opportunities with Big Data" – A community white paper, United States, March 2012.
http://cra.org/ccc/docs/init/bigdatawhitepaper.pdf

[11] E. Letouzé ,"Big Data for Development: Opportunities & Challenges", May 2011.

[12] The Emerging Big Returns on Big Data - A TCS Global Trend Study, 2013.

[13] Wei Fan, Albert Bifet, "Mining Big Data: Current Status, and Forecast to the Future", SIGKDD Explorations, Volume 14, Issue 2, pp. 1-5.

[14] J. Manyika, M. Chui, B. Brown, J. Bughin, R.Dobbs, C. Roxburgh, and A. H. Byers. "Big data: The next frontier for innovation, competition, and productivity",McKinsey Global Institute,May 2011.

[15] Chris Snijders, Uwe Matzat, Ulf-Dietrich Reips, "Big Data: Big Gaps of Knowledge in the Field of Internet Science", International Journal of Internet Science, Vol. 7, 2012, pp. 1-5.

Design And Implementation Of A Cyclic ADC For CMOS Image Sensors

O. Venkata Krishna[1], B. Janardhana Rao[2]
[1]CVR College of Engineering/EIE, Hyderabad, India
Email: venkatakrishna.odugu@gmail.com
[2]CVR College of Engineering, Hyderabad, India
Email: janardhan.bitra@gmail.com

Abstract— **The constant strive for improvement of digital video capturing speeds together with power efficiency increase, has lead to tremendous research activities in the image sensor readout field during the past decade. The improvement of lithography and solid-state technologies provide the possibility of manufacturing higher resolution image sensors, as they provide possibilities for reduced power consumption and integration of complete on-chip cameras. With the increase of image sensors' resolution and frame rate, traditional serial readout schemes become more laborious to design and in many cases simply unachievable for certain required readout speeds. This transfer however imposes additional demands to parallel ADC designs, mainly related to achievable accuracy, area and power.**

In this paper a 12-bit Cyclic ADC (CADC) is designed and implemented in 180nm CMOS technology aimed for column-parallel readout implementation in CMOS image sensors. The multiple CADC sub-component architectures and few various Multiplying DAC (MDAC) structures have been re-examined and implemented. Three comparator architectures have been explored and a dynamic interpolative Sub-ADC is presented. Finally, some weak spots degrading the performance of the carried-out design have been analyzed. As an architectural improvement possibility two MDAC capacitor mismatch error reduction techniques have been presented.

Index Terms—**ADC, DAC, Sensor, CMOS, Low power, Switched Capacitor, Comparator.**

I. INTRODUCTION

The target of this paper is to design an algorithmic, also commonly known as cyclic, ADC architecture for the purpose of its implementation in a column-parallel readout CMOS image sensor. With the increase of image sensor's resolution and frame rate, traditional serial readout schemes become more laborious to design and in many cases simply unachievable for certain required readout speeds.

A possible solution to this problem is the usage of multiple parallel working ADCs, in order to relax the speed requirements of the otherwise standalone data converter. This solution to the problem however, as in any technological problem has its advantages, challenges and disadvantages. One of the challenge points in column-parallel ADCs appear to be the tight silicon area and power consumption requirements. As various ADC architectures exist, among the compact ones strike to be the algorithmic (cyclic) ADC. The most relevant reasoning about the conduction of this study on cyclic ADCs is the low area requirements as well as the reasonably high resolutions and conversion rates achievable with this type of converters.

Historically the first trials of image sensor developments date back to 1969, when Willard Boyle and George Smith at Bell Labs invented the first charge-coupled device (CCD), which a few years later was implemented in the Hubble Space Telescope [2]. In the same decade range a non-charge-transfer imaging device, as we know it nowadays as CMOS image sensor, was introduced. Even though that both technologies are based on converting photons to electrical charges, CCD based image sensors gained higher velocity due to the fact that they provided much better imaging qualities with the existent semiconductor technology. In the later years, starting late 1980s, with the development of high precision lithography and silicon purification technologies, CMOS image sensors gained popularity, as they provide possibilities for reduced power consumption and integration of complete on-chip cameras. The most important pixel parameters of the image sensors required as input data for the ADC design, Output range, Integration (exposure) time, Reset time and Noise boundary.

The Table 1. lists the main imposed ADC requirements for this work. The provided specifications have been kept in mind during the design. The required sampling speed has been set to comply with a readout speed of 60 frames per second on a 1080p vertical resolution sensor utilizing digital correlated double sampling.

TABLE I
SPECIFICATIONS OF ADC

Parameter	Value	Unit
Resolution	12	bits
Sampling Rate	>130	KSps
Integral Non-Linearity	<10	LSB
Differential Non-Linearity	<0.5	LSB
Power Consumption	300	µW
Supply Voltage	3.3	V
Technology	180	nm
Area		µm

II. Design and Implementation of Cyclic ADC

A broad seek for simple architectures incorporating digital correlated double sampling (Digital CDS) and no need for the pixel's signal pre-conditioning was performed. A few attractive architectures in literature were found [5] ,[4] & [7], in a sense that all of them incorporated the fore-mentioned basic functionality, combined with simple choice of circuitry, namely single-ended MDAC designs. The reasons for the hunt after simplified circuits employing single-ended schematics, stood behind the main design limit, which is the narrow column pitch in high resolution image sensors 2 to 6 μm, demanding very low area designs. To achieve high frame rate and high resolution from a sensor, could practically only be achieved with the column-parallel readout architecture.

This section aims to give an overview of the proposed ADC. The block diagram of the cyclic converter shown on Figure 1. The converter utilizes an almost similar single-ended MDAC structure but, in this split of the sampling capacitor into two sub-capacitors allowing the generation of the mid-reference locally. The converter utilizes the popular 1.5 bit redundant signed digit conversion, thus allowing for relaxed comparator offset requirements by utilizing a digital error correction.

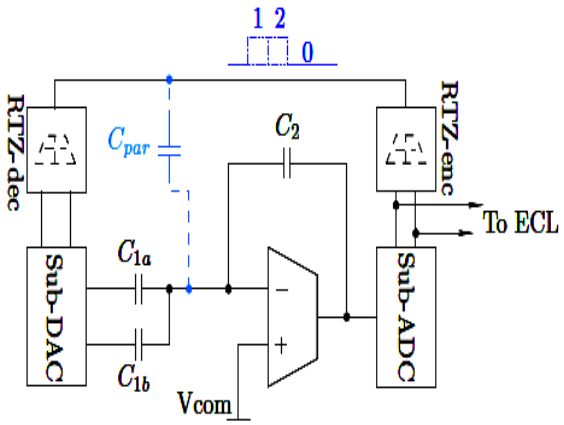


Figure 1. The Principal diagram of Cyclic ADC architecture.

One major disadvantage with respect to the circuit's performance of the proposed MDAC architecture is its single-ended nature. A differential structure would typically be more insensitive to common-mode noise and provide a more stable readout and parasitic insensitiveness. However due to the additional circuit complexity and two extra sampling capacitors as well as switches required, it appeared to tilt the scales towards a single-ended architecture. While in an isolated case a single-ended structure would give much worse performance results, in a mutual aid with Digital CDS as well as the RTZ coding technique, could potentially provide enough noise independence and accuracy to suit for a 12-bit column-parallel ADC.

A In-DAC mid-reference generation scheme

The in-DAC reference generation Figure 2. proposed by [5], practically utilizes the MDAC sampling capacitor as a capacitive divider during the feedback phase to generate the third mid-reference locally from the fed-in *VrefH* and *VrefL*.

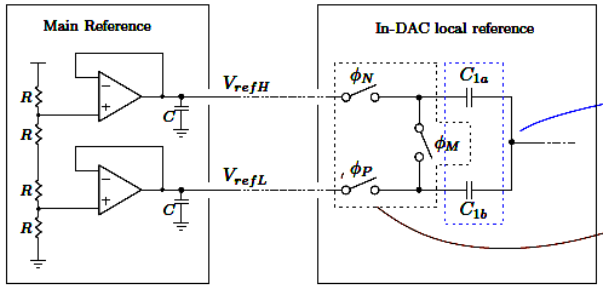


Figure 2. Local in-DAC mid-reference generation.

Apart from the obvious silicon area improvement advantage, by relaxing the requirements of the external voltage reference block or in other words removing one extra required reference voltage to be routed, this internal generation scheme allows for a more accurate mid-reference generation, regardless of the absolute values of the *VrefH* and *VrefL* references. Of course all these statements imply that such resulting converter linearity improvements with this scheme would be possible only by having highly matched sampling capacitors.

B RTZ coding scheme for parasitic sensitivity relaxation

While a fully differential configuration is less sensitive to parasitic coupling of the feedback signals from the sub-ADC, a single-ended structure can not boast with such an advantage. Theoretically the differential MDAC should be 4/6 times less sensitive to parasitic or to formulate it, the error voltage due to parasitic coupling to the summation node will be equal for a single-ended case to:

$$V_{err} = \left(\frac{C_{par1}}{C_2} andD_0 + \frac{C_{par1}}{C_2} andD_1 \right) V_{data-line}$$

Although it might be possible to guard the data lines with an extra metal for wider-pitched columns, the authors proposed a return to zero (RTZ) encoding scheme for an effective reduction of the parasitic coupling to the charge summation node. The principal diagram of the ADC architecture on Figure 1. gives an outline of the RTZ coding scheme. The thermometer code from the Sub-ADC is encoded into a pulse width modulated signal, which is quickly transmitted before the very end of the feedback phase. In this way the effect of the parasitic couplings to the charge summation nodes is reduced practically to almost zero. The parasitic effect from these nodes will only be dependent on the transmission speed of the pulse-width encoded signal.

C The MDAC in details

This section aims to provide a detailed analysis of the re-examined MDAC implemented by [5] and comment on its advantages and disadvantages. As a start Figure 3. shows a principal schematic of the MDAC, built-up around an operational transconductance amplifier. An OTA is a common choice for applications with small capacitive loads, as the case of the MDAC is, due to a row of reasons, standing behind the circuit simplicity of an OTA, or mainly the lack of an output buffer stage in comparison with most OPs.

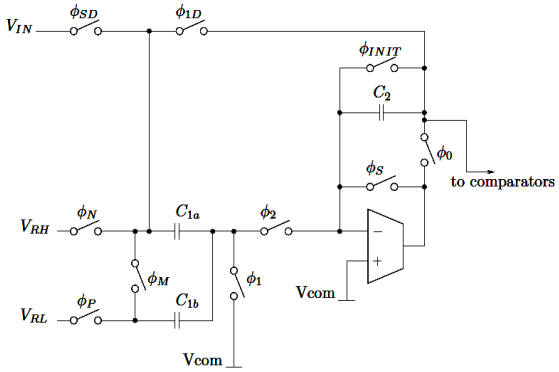


Figure 3. Principal schematic diagram of the MDAC.

The MDAC structure differs slightly from the "Modified Flip-Around" structure, apart from the split sampling capacitor allowing for internal mid-reference generation, the structure halves the accommodated OTA offset. This results in a global ADC offset, which should not be troublesome and in addition the DCDS technique should fully cancel-out such offset. To go through the functionality of the MDAC we can look at the separate sub-phases and perform a charge redistribution analysis. Figure 4. shows the 4 basic modes of operation of the MDAC.

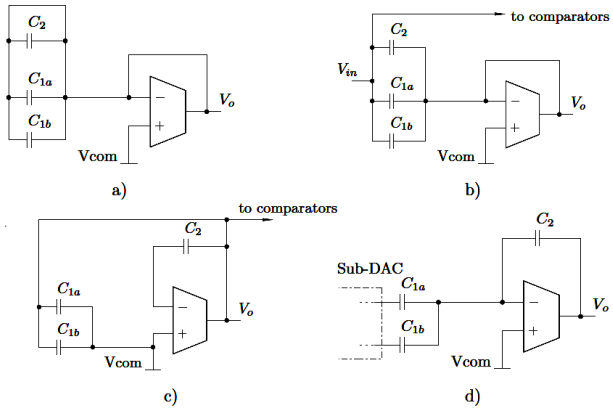


Figure 4. Detailed MDAC configurations for the four phases.

D Functional analysis

Before performing signal sampling, in order to make sure that there is no residual charge from previous conversions and make sure all conditions are the same for every CDS step, all capacitors are reset for a short period of time, Figure 4 a). After completion of this phase, signal sampling can start, Figure 4 b). This implies that the charge stored in the capacitors would be:

$$q_{1a}(t) = (V_{in} - V_{com} + V_{os})C_{1a}$$
$$q_{1b}(t) = (V_{in} - V_{com} + V_{os})C_{1b}$$
$$q_2(t) = (V_{in} - V_{com} + V_{os})C_2$$

During the next - feedback phase, Figure 4. c) the sampled signal is amplified by two. Here is the place to mention again that the accumulated offset during sampling will appear as a global ADC offset with half the magnitude of the OTA offset, as capacitor *C*2 had stored the offset in the previous phase and during the present phase is connected in the feedback loop, thus the amplifier would have added half the OTA offset. The fourth phase performs the analogue subtraction. Depending on the decisions taken during the feedback phase by the Sub-ADC, the top plates of *C*1*a* and *C*1*b* are connected to the reference voltages.

III. COMPARATOR IMPLEMENTATIONS

A Static latched comparator.

To begin with a simple static latched comparator is shown on Figure 5 as proposed by [3]. Transistors *M*1, *M*2, *M*3 and *M*4 are forming a differential amplifier, which controls the current flow through the latch composed of transistors *M*5 and *M*6 via the control transistors *M*7 and *M*8. The decision is taken when the reset transistors' *Vgs* is pulled down, thus releasing the latch from reset state, depending on the currents flowing through the differential pair, thus the two latch

branches, one of the transistors *M*5 or *M*6 switch on first and trigger the regeneration.

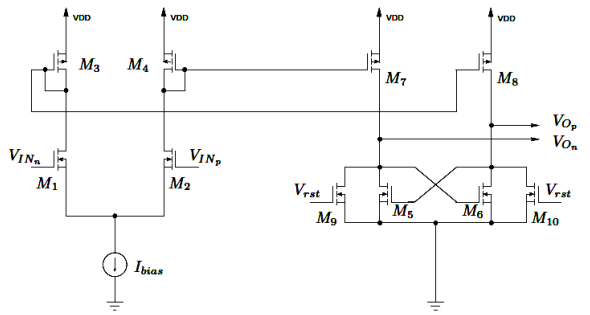


Figure 5. A principle schematic diagram of a simple static latched comparator.

The simple static implementation candidate shown on Figure 5 has some advantages and disadvantages as compared to dynamic comparator implementations. As the currents flowing through the latch transistors are well defined by the biasing current, the comparator's speed can be very easily controlled, however the connection between speed and static power consumption is very closely tight. As it is crucial to keep low power consumption in a column parallel ADC, this architecture does not allure a great interest due to its low efficiency. The architecture provides a somewhat more adequate kickback noise performance, in comparison with some dynamic implementations as we shall see further. The differential amplifier and the current mirroring transistors provide a very good isolation between the latch pair. These however may have a speed reduction effect due to the additional capacitive load overhead i.e. an additional pole added at the drains of the differential pair diode loads.

B Class AB comparator.

An architecture, very similar in a functional point of view to the first static candidate is shown on Figure 6.

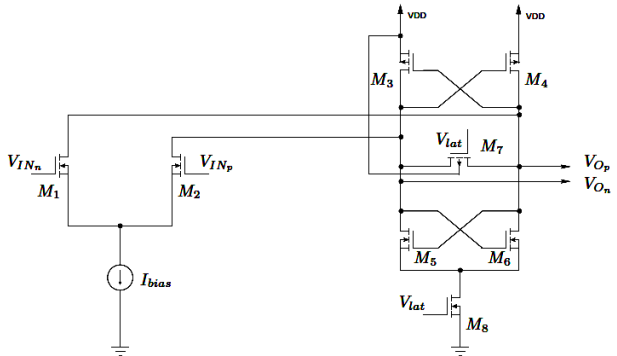


Figure 6. A semi-static often referred to as Class AB comparator.

In order to increase the comparator's speed the semi-static or often referred to as Class AB comparators, do not rely on keeping the latch in reset by holding the reset transistors on, as was the previous case with the static comparator in Figure 5. Instead to reduce the static current drawn by the latch a complementary latch pair is utilized (transistors *M*3, *M*4, *M*5 and *M*6) together with a switchoff transistor *M*8. Shortly, when *Vlat* is low, the only current path flows through the differential pair, transistor *M*7 is on, which keeps the upper latch (transistors *M*3 and *M*4) in reset. When *Vlat* is triggered high, *M*7 turns off, meaning that the upper latch's regeneration is triggered. At the very same moment *M*8 turns on and the bottom pair's drain currents start increasing depending on the upper latch's tilt. This implies that the output should be driven much faster, as there is no intentional current limitation. A major drawback of this architecture as also described by [5] appears to be the increased kickback noise at the inputs, since the differential pair's drains are capacitive coupled directly to the output nodes, which jump back and over from rail to rail. In addition, a hidden effect, decreasing comparator's accuracy, potentially introducing higher metastability issues is the reset transistor *M*7. When turned off, its residual channel charge will flow to both output branches, which may not be with equal impedance nor voltage level, therefore setting unequal starting conditions for the regeneration latch. This would imply that the Class AB stage would potentially have higher offset dependency, as if the regeneration latch transistors *M*5 and *M*6 are mismatched, the effect of charge injection from *M*7 will be amplified.

C A dynamic implementation

A major drawback in the static implementations described in the previous section is the poor power efficiency as well as relatively low speeds. A solution to the power efficiency problem appear to be the dynamic implementations. Figure 7. shows a dynamic comparator implementation using two inverter gates as a regeneration
latch.

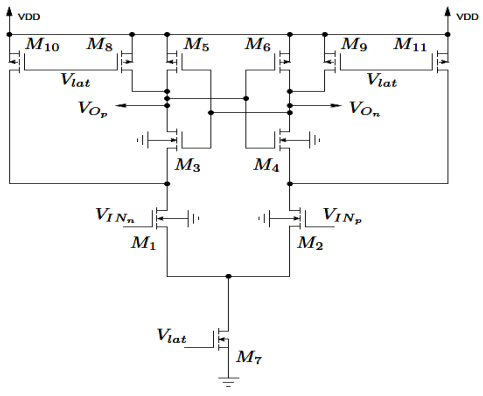


Figure 7. A dynamic comparator implementation.

It could be noted that transistor *M*7 when *Vlat* is kept low, completely turns off the whole circuit and only the leakage currents through *M*7 contribute to the

total power consumption at this phase. Transistors *M*8, *M*9, *M*10 and *M*11 keep the inverters consisting of *M*3, *M*5, *M*4 and *M*6 reset and ensure equal starting conditions for both of them. When *Vlat* is triggered high, *M*7 starts conducting, the reset transistors *M*8, *M*9, *M*10 and *M*11 switch off and the regeneration process starts. When the inverters settle, there is no current flowing through the system, besides the DS leakage currents flowing though the inverters. The output voltage range of this dynamic implementation is however limited in the lower end by the DS drops over the differential pair transistors *M*1, *M*2 and the tail switch
*M*7, thus the architecture does not ensure full rail-rail output range. This implies that if full swing is required some level restoration circuits must be used, in its simplest example this could be an inverter stage. The kickback noise generated from this architecture seems to be comparable with the AB stage. The differential pair is closely coupled with the output nodes, only *M*3 and *M*4 provide insignificant insulation, as their *VD* is also expected to jump up-down. The dynamic implementation
besides the static offset from the differential pair, will also be susceptible to larger dynamic offset due to the charge injection (CI) and clock feed-through of the switches. The particular structure on Figure 7. would possibly have somewhat relaxed CI effect, as the reset transistors *M*8, *M*9, *M*10 and *M*11 would, to a large extent, cancel-out the charge influence on the inverters. *M*10 and *M*11 would inject charge on the source nodes of *M*3 and *M*4, while *M*8 and *M*9 would do on the drains of *M*5 and *M*6. This however is a very idealistic and difficult to define effect, as in reality there would be a clock skew and respectively turn-off time between all reset transistors, which makes the analysis difficult to follow.

D The Sub-AD comparator implementation

Due to its power efficiency the fore mentioned dynamic implementation was chosen as the basic building block of the Sub-AD module. In addition a voltage reference interpolation technique has been used to ensure higher reliability for the cost of a few additional elements and a small increase in power consumption.

As the dynamic implementation offers lowest power consumption and moderately high offset, which is acceptable, it appeared to be the most attractive architecture among the above-described. As an additional improvement possibility, implementing an interpolative Sub-AD was also possible with the chosen dynamic architecture, for the only cost of an additional latch stage as proposed by [23].

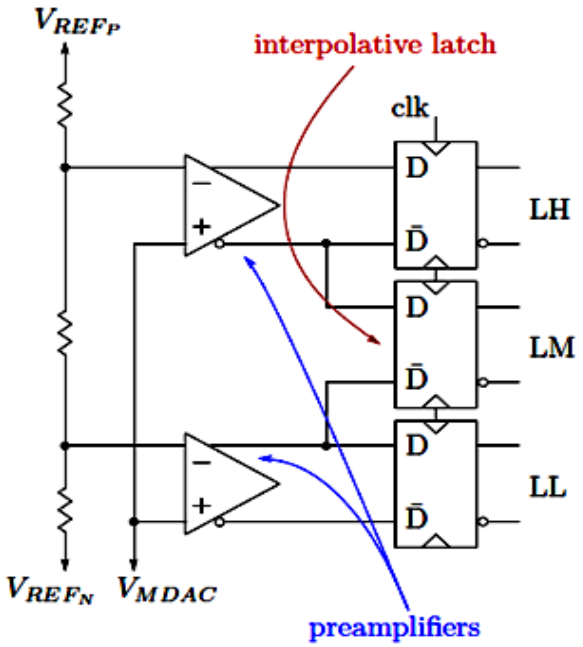


Figure 8. Sub Flash AD Comparator Interpolation Technique

To start with, the basic interpolation idea is clarified on Figure 8. The preamplifiers amplify the difference between the fed-in voltage from the MDAC and the generated sub-references, for further decision from the latches. We can clearly see that the two neighboring shoulders of the differential amplifiers could be used for generating an additional decision level for the cost of an extra latch. Figure 9. shows the outputs of two differential amplifiers hooked-up in a configuration as shown on Figure 8. with a swept input node close to the two reference voltage levels. Practically the interpolative latch, will be triggering on the mid-reference which should be equal to:

$$V_{REF_M ID} = \frac{V_{REF_H} + V_{REF_L}}{2}$$

The main drawbacks of this implementation stand behind the required balancing of the unequal loading of the differential pairs, as this may create a static design-inherited offset and also create a higher linearity requirement. The extra preamp loads also add additional poles and in general such interpolative structures are slower. In the case with the current application, requirements on the comparator's speed are somewhat relaxed and utilizing interpolation does not cause additional issues with respect to speed. The principle schematic on Figure 8. aims to present the interpolation technique in the voltage domain, this however in the case of the chosen fully dynamic comparator would be transferred into the current domain, as all the current flows through the differential pairs.

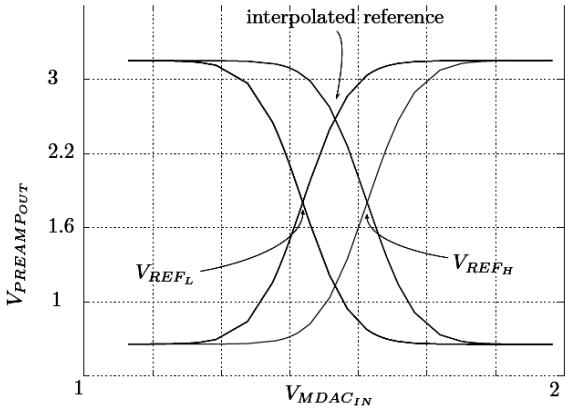


Figure 9. Mid-reference interpolation output voltages of two differential amplifier stages in a function of a linearly swept input voltage, hooked-up following the configuration on Figure 8.

To give a final summary of the designed dynamic comparator's performance for the Sub-AD module, Table 2. shows the main measured parameters. It should be noted that the comparator's design would most probably require modifications after parasitic extraction estimations and/or layout. A design of a comparator fulfilling the requirements in all corners, including parasitic sensitiveness prediction could be a very time-consuming task. As the scope of this thesis is to explore the proposed architecture and possibly improve it, full corner and parasitic optimizations are to be further explored.

TABLE II
SUMMARY OF THE MAIN MEASURED COMPARATOR PERFORMANCE PARAMETERS

Symbol	Parameter	Min	Typical	Max	Unit
ΔV_{os}	Input Offset Voltage Drift	-58	3	+61	mV
T_d	Response Time	-	118	-	ns
σ_n	Noise variance	-	0.48	-	mV
δ_{min}	Resolution	-	0.317	-	mV
V_{supp}	Supply Voltage	-	3.3	-	V
P_{dyn}	Dynamic Power	-	6	-	µW
P_{stat}	Static Power	-	0.224	-	µW

IV. SUB-AD CONTROL LOGIC

As the code provided by the comparators is thermometer-encoded and an RSD representation output is required, certain encoding logic had to be introduced. In addition the Sub-AD logic has the task to control the MDAC and determine the In-DAC switch states during the next feedback phase. In the previous subsection an interpolation technique for the comparators was introduced, thus effectively forming a 2 bit Sub-AD. As this extra half bit was introduced for reduction of an error probability, it is the Sub-AD logic that needs to convert the three thermometer encoded comparator levels to binary 1.5 bit RSD. Table 3. shows a truth-table of the implemented Sub-AD logic.

TABLE III
A TRUTH TABLE OF THE IMPLEMENTED SSB-AD LOGIC

vCODEIN<0:2>	BINOUT<0:1>	P_HP	P_HM	P_HN
000	00	1	1	0
001	01	1	0	1
011	01	1	0	1
111	10	0	1	1
100	00	1	1	0
010	01	1	0	1
110	10	0	1	1
101	00	1	1	0

As a reference, the hardware implementation of the encoding logic is shown on Figure 10.

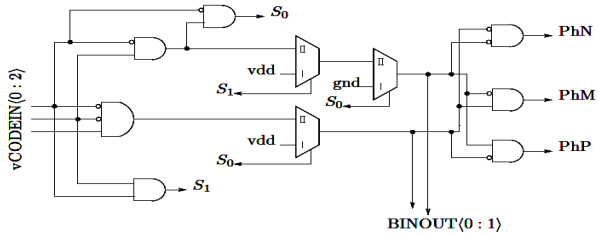


Figure 10: A principal logic diagram of the implemented Sub-AD encoding control logic.

V. RESULTS

In this section of the paper, The main ADC performance parameters concerning image sensors were introduced. In order to estimate the converter's performance from linearity point of view, transient noise simulations based on multiple samples per code were performed, following the IEEE 1241 standard [1]. Figure11. And figure 12. shows distribution histograms of the differential and integral non-linearity simulations.

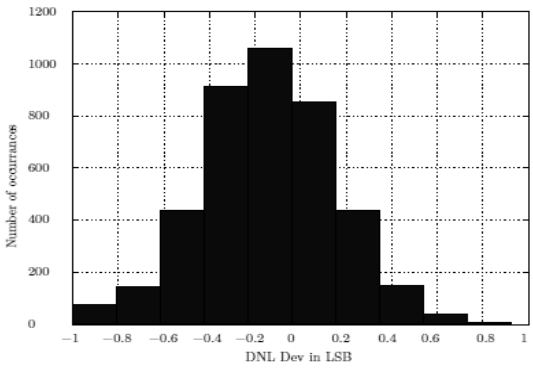


Figure 11. Differential Non-Linearity deviation distribution.

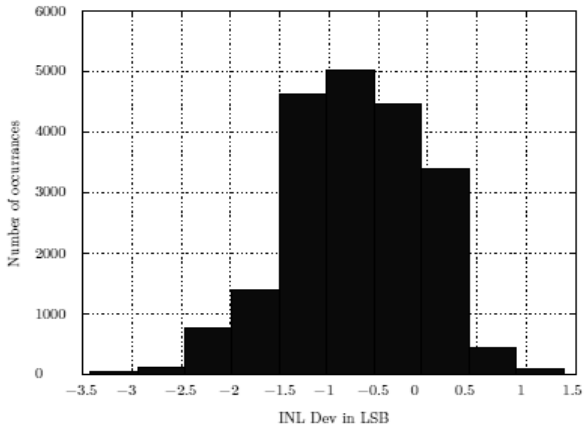


Figure 12. Integral Non-Linearity deviation distribution.

The random noise of an ADC is the excursive fluctuation of its converted digital code word, when an ideal noise-free signal is applied at its input. In the case with the current application, the random ADC noise would appear as a spatial image noise and is thus an important degradation index. The currently performed random noise tests were performed following the IEEE1241 Method 4.5.3.1 standard [1]. Practically following that standard the noise variance was estimated. Figure 13. shows a histogram of the acquired logic level differences from sample to sample. An evaluation script was developed using the IEEE1241 Method 4.5.3.1 and Method 4.5.3.2.

To provide an overview of the current state of the converter Table. 4 provides summarized results for the designed converter. These must be only taken as indicative results, as the current design state does not include device mismatch, external reference voltage and Sub-AD reference generation non-idealities.

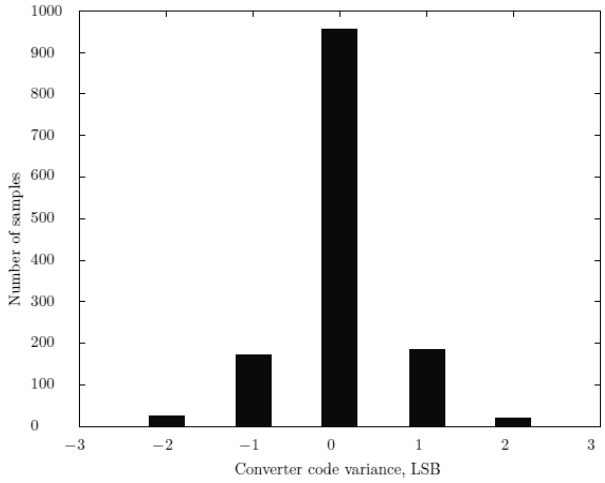


Figure 13: Simulated random noise variance, estimated by 1500 samples, worst case corner.

TABLE IV
SUMMARIZED PERFORMANCE RESULTS OF THE DESIGNED CONVERTER

Parameter	Value	Unit
Technology	180	nm
Resolution	12	bits
Sampling Rate	<150	Ksps
Input Voltage Range	1.35	V
Integral non- Linearity	+1.5/-3.5	LSB
Differential Non-Linearity	±0.8	LSB
Random Noise	367	µV
Power Supply	3.3	V
Power core	72	µW
Power cor+logic	193	µW
Energy per conversion Cycle	15.4	µJ
Reference Voltage H	2.35	V
Reference Voltage L	1.00	V

VI. CONCLUSION

For the Image sensors the single-ended MDAC architecture appeared to be of particular interest due to its design simplicity and was chosen as a re-exploration basis for the conducted design work.

An analysis on the architectural choice was performed and all basic ADC core component requirements were identified. A few MDAC OTA architectures have been listed and a choice, design and validation of a current mirror OTA with output cascodes had been conducted. The interpolative dynamic Sub-AD comparator module was developed, along with all digital control and feedback logic to the MDAC. Finally a few capacitor flipping mismatch reduction techniques had been proposed as possible ADC core improvement.

While all ADC sub-blocks have been implemented, wired-up and synchronized to achieve certain linearity and sampling speed performance measures. The Process corner simulations have been performed, however process variations and mismatch has not been taken into account.

The achieved results show that the major ADC speed limitation component is the MDAC's OTA. Following the converter's direct accuracy parameters as integral and differential linearity, the most critical influence components appear to be the MDAC's sampling and feedback capacitors. Capacitor mismatch reduction techniques appear to be of high relevance to the converter's linearity and further investigation on possible capacitor flipping techniques is left as a future task.

REFERENCES

[1] Ieee standard for terminology and test methods for analog-to-digital converters. IEEE Std 1241-2000, pages i–, 2001.

[2] W. S. Boyle and G. E. Smith. Charge coupled semiconductor devices, 1970.

[3] P.M. Figueiredo and J.C. Vital. Kickback noise reduction techniques for cmos latched comparators. Circuits and Systems II: Express Briefs, IEEE Transactions on, 53(7):541–545, 2006.

[4] Jin-Fu Lin, Soon-Jyh Chang, Chin-Fong Chiu, Hann-Huei Tsai, and Jiann- Jong Wang. Low-power and wide-bandwidth cyclic adc with capacitor and opamp reuse techniques for cmos image sensor application. Sensors Journal, IEEE, 9(12):2044–2054, 2009.

[5] Jong-Ho Park, S. Aoyama, T. Watanabe, K. Isobe, and S. Kawahito. A highspeed low-noise cmos image sensor with 13-b column-parallel single-ended cyclic adcs. Electron Devices, IEEE Transactions on, 56(11):2414 –2422, nov. 2009.

[6] Clemenz Lenard Portmann. Characterization and reduction of metastability errors in cmos interface circuits. Technical Report CSL-TR-95-671, ARPA, June 1995.

[7] Min-Woong Seo, Sung-Ho Suh, T. Iida, T. Takasawa, K. Isobe, T. Watanabe, S. Itoh, K. Yasutomi, and Shoji Kawahito. A low-noise high intrascene dynamic range cmos image sensor with a 13 to 19b variable-resolution columnparallel folding-integration/cyclic adc. Solid-State Circuits, IEEE Journal of, 47(1):272–283, 2012.

[8] F. Silveira, D. Flandre, and P. G A Jespers. A gm/id based methodology for the design of cmos analog circuits and its application to the synthesis of a silicon-on-insulator micropower ota. Solid-State Circuits, IEEE Journal of, 31(9):1314–1319, 1996.

[9] M.F. Snoeij, A.J.P. Theuwissen, K.A.A. Makinwa, and J.H. Huijsing. A cmos imager with column-level adc using dynamic column fixed-pattern noise reduction. Solid-State Circuits, IEEE Journal of, 41(12):3007 –3015, dec. 2006.

Stochastic Modeling and Availability Evaluation of Computer Systems

Wg Cdr Varghese Thattil[1] and Swetha Akula[2]
[1] CVR College of Engineering/Electronics and Communication, Hyderabad, India
Email: mailthattil@cvr.ac.in
[2] CVR College of Engineering/Electronics and Communication, Hyderabad, India
Email: swethaakula9@cvr.ac.in

***Abstract*—There are many applications of the computer systems where in the system availability has to be ensured. The evaluation of the availability is very vital before a computer system is being put into operation in such critical applications. In the case of hardware faults, high degree of reliability can be achieved by hardware redundancy. For microprocessor systems good additional feature is fault tolerance. By the use of dedicated customized hardware, fault tolerance can be achieved which is cost effective. A stochastic modeling of the microprocessor based computer system has been carried out and the lifetime availability is estimated. This evaluation is always being during the entire process of system design. The modeling framework used for the Multiprocessor system is based on an extension of Petri nets called Stochastic Activity Networks (SAN). A major contribution of this paper is that a SAN based comprehensive model for computer system using Mobius simulation tool has been developed which can be extensively used for the lifetime evaluation of systems of various architectures and hardware designs.**

***Index Terms*—Fault tolerance, Stochastic Activity Networks, Multiprocessor Systems, Simulation.**

I. INTRODUCTION

In our everyday life computers play a prominent role. There are computers used is mission-critical applications, life support applications, homeland security, battlefield situations, where the availability of the computer system is considered to be vital. A system with 99.99% availability over 30 days is unavailable for 4.32 minutes in 30 days.

The microprocessors are regarded as one of the most paramount contrivance in computer systems. Usually a microprocessor will have a silicon chip having millions of transistors & other devices that will be in processing millions of operations per second [1, 2]. It is a multipurpose, programmable microchip that utilizes digital data as an input. Once it processes the input according to the instructions stored in its memory, it provides results as an output. As microprocessor has internal memory, it became an example of sequential digital logic. Operation of microprocessors is based on the numbers and symbols represented in the binary numeral system. Main purpose of designing microprocessors is to perform arithmetic and logic operations. Application of microprocessors in PCs is for computation and text editing`[3].

Computational control is provided by the microprocessor which functions as a central processing unit (CPU) of a computer. Along with the arithmetic and logic functional units, control logic, instruction processing circuitry, and some part of the memory hierarchy are incorporated in characteristic microprocessors. Sanctioning more frugal overall systems, some parts of the interface logic for the input/output and memory subsystems are saturated. To provide multiple functional units and relatively sizably voluminous caches, microprocessors and single-chip designs depend on a small number of chips.

The system availability is greatly influenced by the way the system architecture is designed, the quality of the components of the system, the design of major data structures, files, and databases and the specifications of the interfaces between components.

Microprocessors are fabricated utilizing techniques homogeneous to those utilized for other integrated circuits, such as memory chips. Microprocessors generally have a more intricate structure than do other chips, and their manufacture requires immensely precise techniques [4].

The working of the microprocessor is done in three steps i.e, fetching, decoding and processing. In the first step it gets an instruction from the computer memory and decodes the instruction in second step. In the last step, the processor carries out the decoded set of instructions. A microprocessor carry out three step process, millions of times per second.

In designing process of computer and communication systems, performance modeling is incorporated. Issues aroused during modeling process is addressed by the new techniques .Better design and manufacturing process ensures high quality components being manufactured however performance of these

components when integrated into a system offers much poorer performance. Therefore it is very essential to estimate the mean life time and reliability of any system before being put into operational use.

Challenging problem faced in many engineering applications is the estimation of mean lifetime and reliability of sophisticated systems. In such cases, obtaining the results for the lifetime and reliability of complex systems; by theoretical development is tedious. Systems have become so complex that the study of their reliability requires extensive modeling and simulation. Modeling is a complex process which can be attained by experience and continuous improvement. The paper discusses method of modeling a disk storage system through stochastic process.

A. Reliability and Availability

Reliability and expected lifetime are very important issues in modern complex systems. Systems have become so complex that the study of their reliability / availability requires extensive modeling and simulation. Reliability can be defined as the conditional probability at a given confidence level that a system will perform its operation properly without failure at specified performance requirements during a given time interval [0, t]. Whereas availability is the probability that a system will be operational at any given time taking into consideration the failure time and time to repair. Availability is concerned with repairable systems.

B. Petri Nets

Place/transition Petri nets (p/t-nets, for short); Petri nets is a graphical and mathematical tool which have been used to describe a wide range of systems since their invention by Carl Adam Petri in 1962. High-level Petri Nets were developed to overcome the problem of the explosion of the number of elements of their graphical form for complex systems in Petri nets. As techniques for solving models advanced, formalisms (formal languages for expressing models) were also developed.

C. Stochastic Petri Nets

For the description of Discrete Event Dynamic Systems (DEDS) Stochastic Petri Nets (SPNs) were introduced in 1980 [5],[6]. SPNs represent the dynamic behavior of DEDS with continuous-time homogeneous Markov chains for their performance and reliability evaluation.

D. Models

It's difficult to understand the behavior of real time systems because their organization is complex and the interaction among their components is difficult. The possibility of computing results from the analysis of a model is the key for closing a loop that starts from the abstraction of the relevant features of the system during modeling construction and that ends with the interpretation of the results provided by the model and reflected on the real system. Designer has to decide on the relevant performance parameters which have to be studied for each model.

It should be noted that a key element in the development of a model is the selection of the level of abstraction (also called level of detail). This amounts to selecting the system features to be included in the model. No precise rule exists for this selection, which rests mainly on the experience and ingenuity of the performance analyst and the knowledge of the system being modeled.

E. Discrete Event Dynamic Systems

Discrete Event Dynamic Systems (DEDS) are systems with a discrete state space and whose evolution is not directly due to the passage of time, but to the occurrence of events. The systems are views as DEDS not because the system itself is discrete in nature but the aspects of their behavior mainly outcomes of a system that we want to study are discrete in nature.

II. PERFORMANCE EVALUATION OF DEDS

Time-related performance indices such as availability, resource consumption, reliability and system response time accounting for system failure are computed using mathematical and simulation models which come under performance evaluation. To solve problem multiple models are evolving and databases are maintained.

A. Stochastic Activity Networks (SAN)

Probabilistic extensions of activity networks are stochastic activity networks. Stochastic Petri Nets are less powerful and inflexible compared to Stochastic activity networks [7]. SAN model is a particular kind of directed graph composed of primitives like places, activities and gates. Timed activities and instantaneous activities are two kinds of activities.

1. Place:

Places are used to represent the "state" of a system. A state of a Petri net is determined by a distribution of tokens (a nonnegative integer) on its places. This mapping is usually called a *marking*. A place is depicted as ○.

2. Timed Activity:

Marked as ▌ timed activities represent activities of the modeled system whose durations impact the system's ability to perform? An activity distribution

function, an enabling rate function, and an *n*-array computable predicate called the reactivation predicate is associated with timed activity.

3. Instantaneous Activity:

Marked as | **.** Instantaneous activities are completed in a negligible amount of time. An instantaneous activity has m inputs and n outputs. Case probability function is associated with each instantaneous activity. Realization of spatial uncertainty is permitted by the case probabilities.

4. Input Gate:

Marked as◄. To permit greater flexibility in defining, enabling and completion rules gates are introduced. An input gate is confined to one output and finite set of inputs. An n-array computable predicate called the enabling predicate is associated with each input gate called input function.

5. Output Gate:

Marked as ⊣∑. An output gate is confined to one input and finite set of outputs. A computable function is associated with each output gate called the output function.

B. Basic Approach for Building SAN Model

Modeling complex systems with stochastic processes requires a good knowledge of the system to be modeled along with knowledge of probability theory, advanced calculus, matrix algebra and a general level of mathematical maturity [8]. The process of system modeling using SAN involves building up the individual atomic models and forming the composed model using them. Within the atomic model input / output gates, place markings and activities have to be properly programmed.

The composed model is built precisely interconnecting the atomic models. A Join is used to compose two or more sub models using equivalence sharing. A Replicate is used to construct a model consisting of a number of identical copies of its single child. Each child node of a Replicate or Join node can be a Replicate, a Join, or a single atomic or composed model. The desired performance measures are specified on the composed model. Reward models are built upon atomic and composed models, equipping them with the specification of a performance measure PV **[**9].

III. APPLICATION: FAULT TOLERANT MULTIPROCESSOR SYSTEM

Fault tolerant is defined as the ability to perform execution correctly in spite of the presence of faults. Much importance has been given to fault tolerance because of the critical applications of multi processor systems [10]. System failure is modelled based on the failures of the components in the system. The two possible states often allowed for components in the system is either in working state or failed state [11]. The system we consider is highly redundant fault-tolerant multiprocessor as shown in fig 1. This system is modelled in hierarchically, such that the system at highest level consists of multiple computers. Series system is considered not functional, if one component fails total system fails. Whereas, parallel system is considered functional, if at least one component functions. To overcome the disadvantage of series system, for failure recovery purpose a spare unit is also included. Fault tolerance can be achieved by the dedicated hardware [12]. Each computer is composed of 3 CPU units, of which 1 is spare unit; 3 memory modules, of which 1 is a spare unit; 2 I/O ports, of which one is spare port and 2 non-redundant error-handling chips. If we look internally, each unit is made up of chips. Like, memory module consists of 41 RAM chips out of which 2 are spare chips and 2 interface chips. Each CPU unit and I/O port consists of 6 non-redundant chips. We consider the system is operational only when at least one computer is operational. If at least 2 CPU units, at least 1 I/O port, at least 2 memory modules and 2 error-handling chips are functioning then computer is classified as operational. At least 39 of its 41 RAM chips, and its 2 interface chips, are to be working for memory module is to be operational [13].

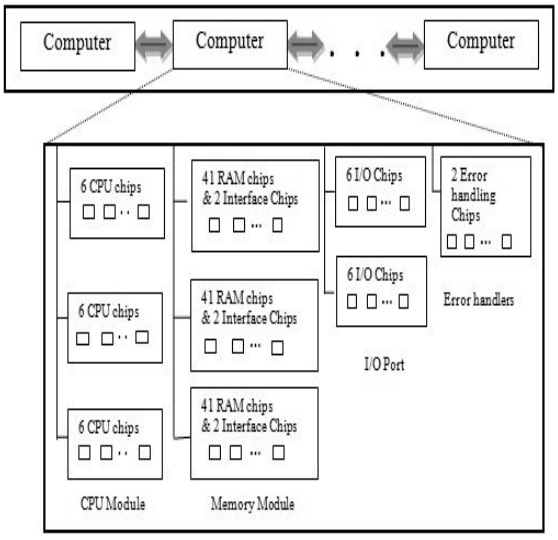


Figure 1. Fault Tolerant Microprocessor System

Redundant units are included in this hierarchy; so that, even when there is a failure of any unit it is replaced with the spare. If the probability of failure of one CPU unit is 0.995 then the failed one is replaced with the spare unit and the computer will be operational. Also, there is a probability of 0.005 (CPU coverage) that fault recovery fails and the computer operation will get ceased. Finally, it is assumed that the failure rate of

every chip is 0.0008766 in the system (1 failure per 1141 years). Coverage probabilities of each unit are given in Table I.

TABLE I
COVERAGE PROBABILITIES

Redundant Component	Fault Coverage Probability
CPU Unit	0.995
I/O Port	0.99
Memory Module	0.95
RAM Chip	0.998
Computer	0.95

IV. MODELING OF A FAULT TOLERANT SYSTEM USING MOBIUS

Mobius tool is used to model the fault tolerant multi processor system. In Mobius atomic models are built for each module. These atomic models are either replicated or joined to form a composed model. Performance variable is retrieved in the reward model. The study model is used to give values of the parameters for simulating various experiments. This composed model is simulated using a solver.

A. SAN Submodels (Atomic Models)

SAN sub model of CPU module is created and then places, input gates, timed activities and output gates are included in the model. Sub model of the CPU module is shown in Fig 2.

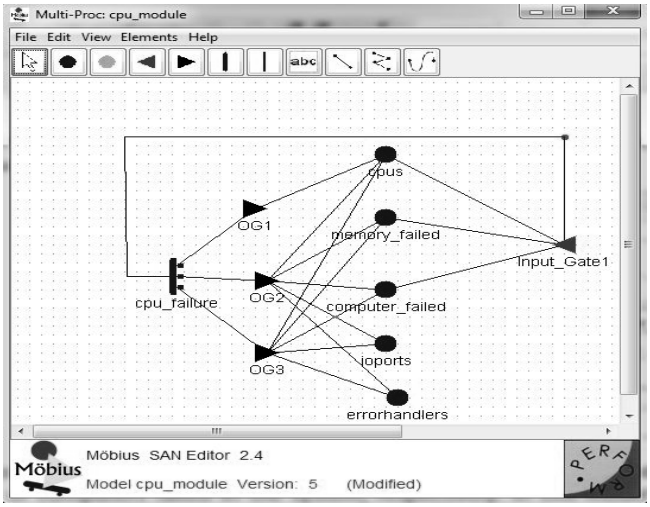


Figure 2. SAN Sub model of cpu_module

Number of tokens in the places cpus and computer_failed represents number of operational CPUs in a computer and the number of computers failed in the system, respectively. In this model the places io ports, errorhandlers and memory_failed are also labelled. Additional lumping of states is done to reduce complexity because; if a computer fails no need to track the component failure which leads to computer failure. According to the assumption that all internal components are failing for the computer that have failed. CPU unit, a memory module, an I/O port, or an error-handling chip is combined to form a single state which represents the failure of a computer. Combined state marking is achieved by setting the number of tokens in each of the places CPUs, I/O ports, and error handlers to zero, setting the number of tokens in memory failed to 2, and incrementing the number of tokens in computer failed. cpu_failure is the timed activity and it takes place only when the condition in input gate is satisfied. If the timed activity CPU_failure is completed then it corresponds to cpu failure. If a spare CPU unit is available (i.e., CPUs->Mark() == 3), three cases are associated with the activity completion, as designated in the Case quantity field. First case represents that spare CPU is replaced with the failed CPU and the computer operates normally. Second case represents the situation in which the spare unit CPU is not available to replace failed CPU such that, spare computer is replaced with the failed computer. Third case arises when there is no spare CPU and no spare computer is available leading to total system failure.CPU module activity distribution is given in (1).

cpu failure = exp(0.0052596*cpus->Mark( )) (1)

We consider 3 cases in timed activity of cpu_module. Probabilities of those 3 cases are mentioned in Table II.

TABLE II
CPU_MODULE CASE PROBABILITIES OF ACTIVITY

Case	Probability
	cpu_failure

1	if (cpus->Mark() == 3)
	return(0.995);
	else
	return(0.0);

2	if (cpus->Mark() == 3)
	return(0.00475);
	else
	return(0.95);

3	if (cpus->Mark() == 3)
	return(0.00025);
	else
	return(0.05);

Functions of Input Gate and Output Gates are given in Tables III & IV.

TABLE III
CPU_MODULE INPUT GATE FUNCTION

Gate	Function
Input_Gate1	(cpus->Mark()>1)&&(memory failed->Mark()<2)&&(computerfailed->Mark()<num comp)

TABLE IV
CPU_MODULE OUTPUT GATE FUNCTIONS

Gate	Function
OG1	if (cpus->Mark() == 3) cpus->Mark()--;

OG2	cpus->Mark() = 0;
	ioports->Mark() = 0;
	errorhandlers->Mark() = 0;
	memory failed->Mark() = 2;
	computer failed->Mark()++;

OG3	cpus->Mark() = 0;
	ioports->Mark() = 0;
	errorhandlers->Mark() = 0;
	memory failed->Mark() = 2;
	computer failed->Mark() = num comp;

Modelling the other sub models is similar to the cpu_module sub model.

B. Composed Model

To form a composed model from the atomic models replicate and join operations are used. Figure 3 shows the multi_proc composed model for the fault tolerant multiprocessor system. Atomic models are represented as leaf nodes. Variables included in the respective atomic models can be shared in all sub models of the system; this sharing is done in the composed model.

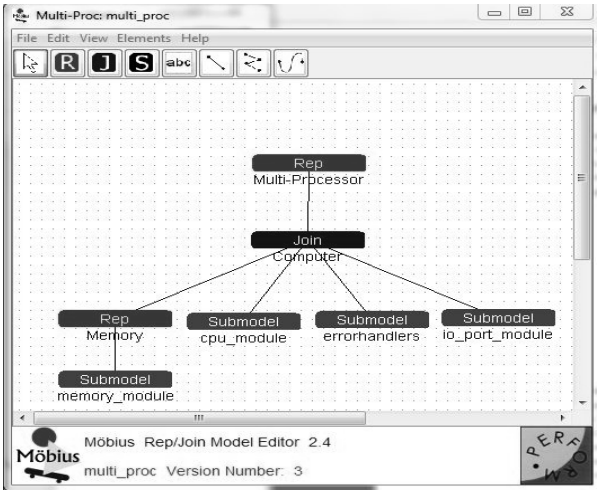


Figure 3. Multi_proc composed model

C. Reward Model

The reward model specifies the performance variable which has to be evaluated. The reward model can be used to measure many performance measures. Reward model is as shown in Fig 4.

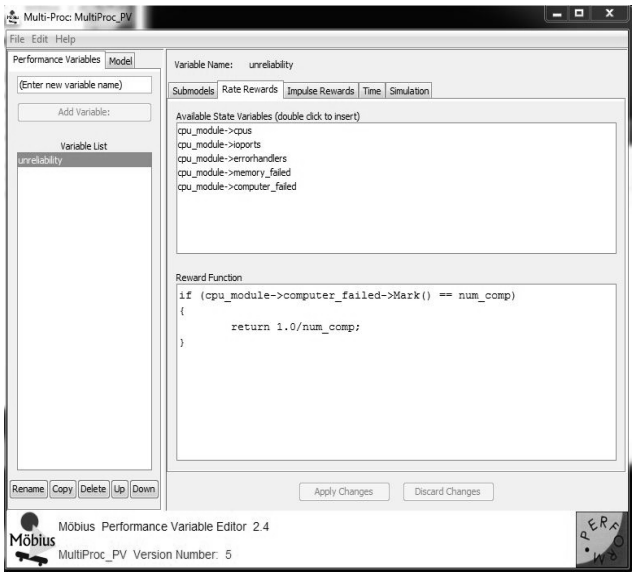


Figure 4. Multiproc_pv reward model

D. Study Model

Global variables of each of the atomic and composed models define the experimental parameters. Different experiments on the system model are defined by giving suitable values in the study model. Study model is shown in Fig 5.

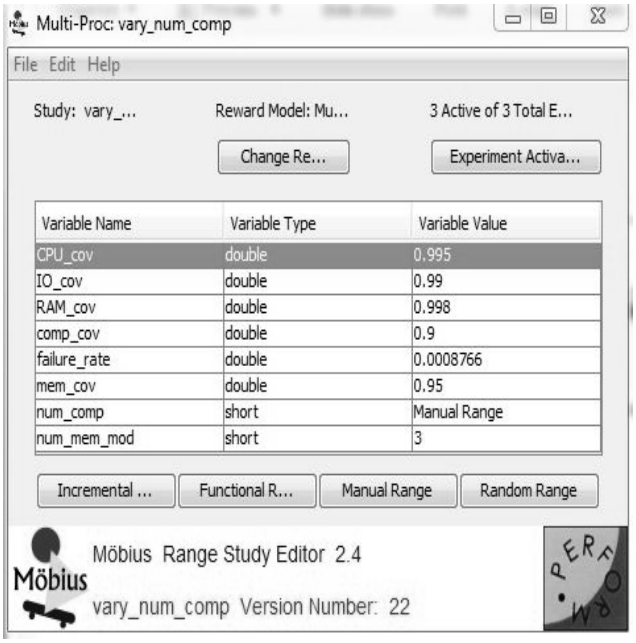


Figure 5. Multi_proc study model

Case I: Number of computers vary in study model. If the number of spare computers is more than 1, then the system reliability lasts longer compared to the system with a single computer. System reliability with varying number of computers is shown in Fig 6.

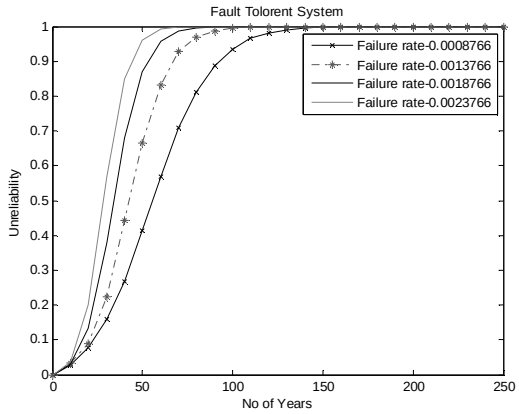


Figure 6. Probability of achieving system lifetime for Variation No of computers

Case II. To represent the operating characteristics of a unit that tends to frequency as it ages, failure rate is a good measure [14]. Failure rates vary in study model. As the failure rate falls, the lifetime of the system increases. The result obtained after varying failure rates is shown in Fig7.

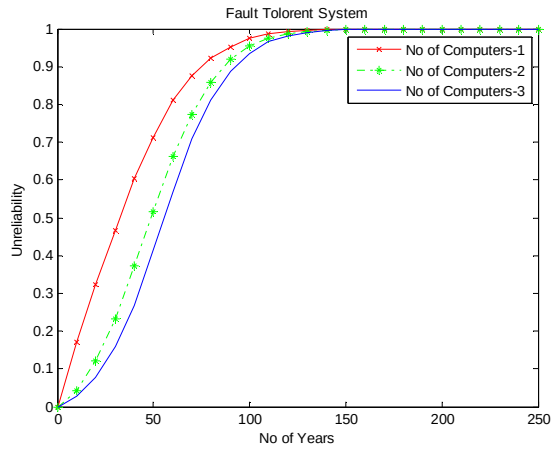


Figure 7. System lifetime for varying failure rates

CONCLUSION

As reliability is a major issue in real time applications, the reliability of a fault tolerant microprocessor system is obtained by modeling it using Mobius. The probability of achieving system lifetime for various spare computers and failure rates is shown in Fig 6 & 7. The proposed system gives the lifetime of the reliable system per number of years.

REFERENCES

[1] Basset Ross (2003). "When is a Microprocessor not a Microprocessor? The Industrial Construction of SemiconductorInnovation".In Finn, Bernard. Exposing Electronics. Michigan State University Press.p. 121. ISBN 0-87013-658-5.

[2] Borkar; Shekhar; Chien; Andrew A(2011); The Future of Microprocessor, Communications of the ACM, Vol. 54 Issue 5,May2011,pp67-77, 11p

[3] The Uses of Microprocessors (2012); an online material downloadable at http://web.engr.oregonstate.edu/~qassim /index_files/FinalECE570_ASP_2012_Project_Report.pdf Aldosari: "Microprocessors".

[4] F. J. W. Symons. "Introduction to numerical Petri nets, a general graphical model of concurrent processing systems". Australian Telecommunications Research, 14(1):28– 33, January 1980.

[5] Gianfranco Balbo "Introduction to Stochastic Petri Nets" Universit`a di Torino, Torino, Italy, Dipartimento di Informatica.

[6] A. Movaghar, "Stochastic Activity Networks: A New Definition," Proc. of the IASTED Int. Conf. on Modeling and Simulation (MS'97), Pittsburgh, PA, May 1997, pp. 27-30.M.

[7] M. Abdollahi Azgomi And A. Movagh Ar "A Modeling Tool For A New Definition Of stochastic Activity Networks" Dept. of Computer Engineering, Sharif University of Technology, Tehran, I. R. of Iran Iranian Journal of Science & Technology, Transaction B, Engineering, Vol. 29, No. B1 Printed in the Islamic Republic of Iran, 2005 © Shiraz University

[8] W. H. Sanders and J. F. Meyer. A unified approach for specifying measures of performance, dependability, and performability. In A. Avizienis, J. Kopetz, and J. Laprie, editors, Dependable Computing for Critical Applications, volume 4 of Dependable Computing and Fault-Tolerant Systems, pages 215– 237. Heidelberg: Springer-Verlag, 1991.

[9] "Fault tolerance in Multiprocessor systems".sadhana, vol 11,parts 1&2, October 1987,pp.93-110.

[10] Rong-Tsorng Wang. "Reliability Evaluation Techniques".

[11] Hussain Al-Asaad and Alireza Sarvi. "Fault tolerance for multi processor systems via time redundant task scheduling".

[12] "MobiusManual"(http://www.mobius.illinois.edu/docs/MobiusManual.pdf).

[13] T. Nakagawa, Maintenance Theory of Reliability (Springer, London, 2005)

Design of On-Chip Testing Memory for High Speed Circuits

M.V. Sushumna
CVR College of Engineering/ECE, Hyderabad, India
Email: sushumna451@gmail.com

***Abstract*— Mixed-signal processing systems especially data converters can be reliably tested at high frequencies using on-chip testing schemes based on memory. In this thesis, an on-chip testing strategy based on shift registers/memory (2 k bits) has been proposed for digital-to-analog converters (DACs) operating at 5 GHz. The proposed design uses word length of 8 bits in order to test DAC at high speed of 5 GHz. The proposed testing strategy has been designed in standard 90 nm CMOS technology with additional requirement of 1-V supply. This design has been implemented using Cadence IC design environment.**

The additional advantage of the proposed testing strategy is that it requires lower number of I/O pins and avoids the large number of high speed I/O pads. It therefore also solves the problem of the bandwidth limitation that is associated with I/O transmission paths. The design of the on-chip tester based on memory contains no analog block and is implemented entirely in digital domain. In the proposed design, low frequency of 1 MHz has been used outside the chip to load the data into the memory during the write mode. During the read mode, the frequency of 600 MHz is used to read the data from the memory. A multiplexing system is used to reuse the stored data during read mode to test the intended functionality and performance.

In order to convert the parallel data into serial data at high frequency at the memory output, serial converter has been used. By using the frequencies of 1.25 GHz and 2.5 GHz, the serial converter speeds up the data from the lower frequency of 600 MHz to the highest frequency of 5 GHz in order to test DAC at 5 GHz.

***Index Terms*— CMOS, on-chip memory, Testing of high-speed MSPS circuits, Shift register, Clock divider, Clock multiplexing, Serializer, Multiplexer, Synchronous sequential circuits.**

I. INTRODUCTION

The Complementary metal-oxide semiconductor (CMOS) technology has been considered as the dominant technology for the very large scale integration (VLSI) chip design [1],[2] because CMOS technology has become the basis of the modern digital integrated circuits because of the increased performance in terms of high speed due to continuous scaling. Moreover, it provides high speed with low cost transistors on the same chip.

As digital circuits cost is very low or almost free in ultra-deep submicron CMOS technologies, therefore nowadays the interest in on-chip testing is increasing by increasing the complexity of the VLSI digital circuits. The on-chip testing is less costly than the testing based on external instrumentation because of the increased performance requirement of the chip in terms of high speed operation. Moreover, it is becoming less practical that the tester be manufactured on other semiconductor chip when the device and the tester can easily be manufactured on the same single chip, especially in ultra-deep submicron technologies where the transistor has been largely scaled down. Furthermore, system-on-chip (SoC) allows designing and fabricating digital, analog, and mixed-signal integrated circuits on the same chip.

As the complexity of the mixed-signal processing systems (MSPSs) is increasing, the challenges of testing are emerging. It is difficult to connect the external test instrument to the chip without loss or distortion in high speed testing. So, the testing of integrated circuits (ICs) by using external instruments has become very complicated due to the high performance requirements.

The measurement of very high frequency suffers from degradation of core circuit performance because of the bandwidth limitations. The bandwidth limitations are caused by the physical nature of the I/O pads and physical length of the transmission path [3].

The on-chip memory tester overcomes these problems. The high frequency is generated from another on-chip circuit. The proposed design provides clock divider to divide this clock frequency into four frequencies which can perform high frequency tests. In such case, the bandwidth limitation problem imposed by I/O transmission paths is solved. Hence, the on-chip memory (2 k bits) is included in the proposed design in order to avoid a large number of very high speed I/O pads and the proposed design can use the lower number

of possible pins [4]. The low frequency during write operation can be driven from outside the chip to write the data into memory. This reduces the cost and complexity of the design. In addition, the serializer is included in the design in order to test the intended device at high frequency.

When choosing the word length and depth of the memory, many aspects have been taken into account, such as total area consumption, power consumption and design complexity. These aspects are affected by the memory, serializer and clock distribution network needed in the design. In order to choose the optimum design parameters a tradeoff between the frequency of the first stage of the serializer and the word length of the memory should also be taken into account. The higher the frequency of the first stage of the serializer, less bits are needed to be taken out from the memory unit (lower word length). But at the same time, increasing the frequency of the first stage of the serializer increases the overall area and power consumption of the design. It will also increase the design complexity. Therefore, lower frequency of 625 MHz and higher word length of 64 bits with depth of 32 have been chosen.

II. Overview of the Design

The proposed design is composed of six main units: serial to parallel conversion, memory, serializer, clock divider, control, and clock distribution network as shown in Figure 1. Serial to parallel conversion unit consists of 64 memory elements. The memory unit consists of 2048 memory elements. The multiplexing system is also presented in the memory unit design. The memory unit stores the data at low frequency and reuses the stored data at high frequency (625 MHz). The serializer unit uses different frequencies 625 MHz, 1.25 GHz, 2.5 GHz, and 5 GHz in order to speed up the stored data from 625 MHz to the 5 GHz to test at high frequency. The clock divider unit is responsible for dividing the frequency (5 GHz) into four frequencies (clocks) in order to use them in the different parts of the design. The control unit is responsible for generating all the control signals that the design needs. The clock distribution network consists of multiple stages of buffer in order to drive the signal from its source to the terminal port.

The word length of the memory (64 bits) can be considered as 8 groups of 8 bits. Therefore, the output of each group is connected to one of 8:1 serializer unit. So, the entire serializer design consists of 8 pages of 8:1 serializer unit.

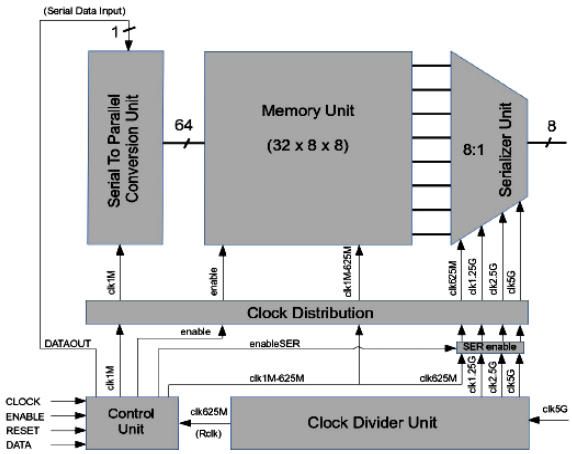


Figure 1: Block diagram of proposed design

A Serial to Parallel Conversion Unit

The serial to parallel conversion technique is needed to convert the serial input data into parallel output data. Thereby, the output data of the serial to parallel conversion unit are the input data of the memory unit. This technique is active during the write mode. The conversion from the serial format to the parallel format is done by using serial-in/parallel-out (SIPO) shift registers. These registers work at the frequency of 1 MHz (clk1M signal). According to the proposed design, the memory unit has 64 bits as a word length with depth of 32. Thus, 64 registers are needed to convert the data into parallel format. Each data bit is shifted during one clock cycle of clk1M signal. After 64 clock cycles, the 64 bits of data are stored into these registers. It is important to ensure that each new set of 64 bits data should be stored first into these registers and afterwards, the data are shifted into the memory.

The advantage of this operation is that each set of 64 bits data is going to be valid at the output of the memory at the same time. After the memory is filled, the clock signal (clk1M) of the serial to parallel conversion unit is turned off. This means that the serial to parallel conversion unit is off and thus no more data enter into the memory.

B Memory Design

The memory unit is one of the most important units in the proposed design. From the specification requirement of the design, 2k bits memory should be designed to store the data at low frequency and read these data at high frequency in order to test the intended device. Integrated circuit design, involves tradeoffs among many factors, such as speed, power consumption, chip area, and cost. In this paper, the main objective is to generate the on-chip input data at 5 GHz for testing of high-speed mixed-signal circuits.

Therefore, in this particular case, the most important design requirements on the memory are the speed and operational robustness. As will be explained in the following, robust and low-power shift registers are utilized as memory cells, and the high-speed memory readout is enabled with a 3-step successive multiplexing of 64 bits at 625 MHz to 8 bits at 5 GHz.

The proposed memory (2k bits) has two dimensional array of shift registers (64x32 cells). One register denotes one cell memory (one bit). The transistor size of the register can be small. The proposed memory operation concept is very simple. The data transfer from one DFF to the adjacent DFF during single clock cycle and so on. Thus, the first data bit entered into the memory, is the first output data bit from the memory. To perform write and read operations this memory requires two clocks. The clock port of the memory passes the write clock (low frequency) during the write mode. After the memory is filled, the clock port passes the read clock (high frequency) in order to read the stored data during the read mode. Therefore, clock multiplexer should be designed in order to perform the multiplexing from the write clock to the read clock. When the whole memory is filled, multiplexing system should be provided in the memory unit in order to reuse the stored data for testing during the read mode. So, 64 multiplexers should be designed. Moreover, control unit to manage the multiplexers for writing and reading operations should be also designed. The whole memory unit with the serial to parallel conversion unit is shown in Figure 2. The memory unit and serial to parallel conversion unit use static traditional master-slave positive edge-triggered registers using multiplexers. They are distributed as shown in Figure 2. Note that there is a buffer stage after each register in order to fulfill the timing requirements between two adjacent registers. In contrast to the serial to parallel conversion unit, the memory has two modes of operation, write and read modes.

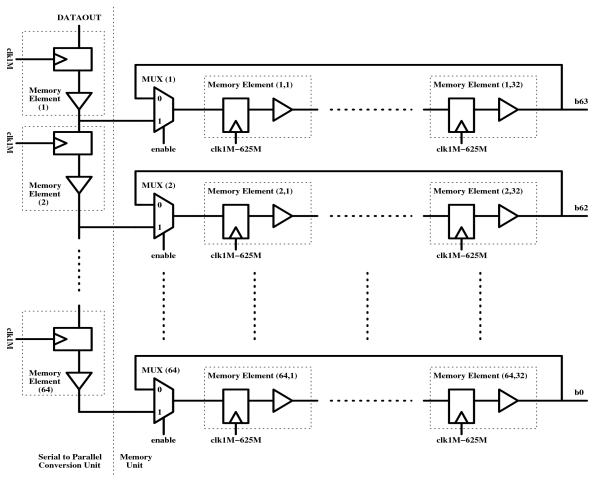


Figure 2: The whole memory unit with the serial to parallel conversion unit.

When the memory works at write mode, clk1M-625M signal is high all the time (64 clock cycles of clk1M) except the last half clock cycle (low). This means that after each set of 64 bits data has been converted from serial to parallel, these data are shifted simultaneously into the memory. Note that the stored data inside the memory will not be shifted to the next column until the new set of 64 bits data is stored again after the serial to parallel converter. The memory is filled after 32x64 times the clock cycles of clk1M. The write mode is ended and the serial to parallel conversion unit is deactivated while the read mode is started by activating the multiplexing system.

The multiplexer consists of two pass transistors forming transmission gate, inverters, and buffers. In order to overcome the charge-sharing problems, inverters are added before and after the transmission gates. Besides, the output signal of the multiplexer is going to be more robust because the transmission gates produce degraded signal. The buffers can be needed to satisfy the timing requirements for the circuit. This type of multiplexer consumes very low power and offers high speed performance [5]. So, it is faster than the multiplexer based on gate level approach because of the slower charging and discharging operations in the later approach. Thereby, the use of the proposed multiplexer in a high speed circuit design will be very helpful than the other. In addition, the proposed multiplexer has less number of transistors than the other. This schematic is not used only in the memory unit; it is also used in other different units in the proposed design, such as control unit and serializer.

C Clock Divider Unit

The clock divider is needed to generate the required clocks from the original frequency (EXclock signal) which is 5 GHz. The output signals (clocks) of the clock divider are clk5G, clk2.5G, clk1.25G, and clk625M, respectively.

There are two design topologies for the clock divider unit; asynchronous counter and synchronous counter. Using the asynchronous ripple counter, presented in [6],[7] reduces the power consumption due to the small capacitance at high frequency node. However, the jitter problems are increased because the jitter will be accumulated stage by stage. On the other hand, using the synchronous counter increases the power consumption due to the large capacitance at high frequency node, but the advantage is that the jitter accumulation problems are reduced [7]. In addition, the clock synchronous divider topology eliminates any cumulative time delay because all the DFFs are connected together to the same single clock. Therefore, all output clocks change simultaneously at the rising edge of clock, and the maximum frequency of the synchronous counter will be significantly higher than

the asynchronous ripple counter. The proposed clock divider schematic is based on a synchronous 3-bit counter as shown in Figure 3.

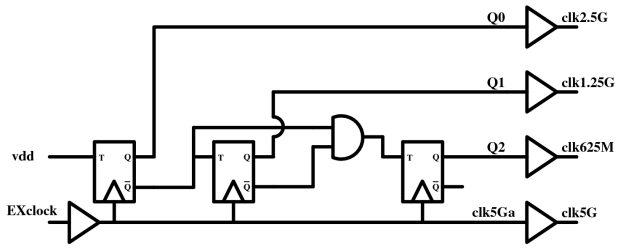


Figure 3: Clock divider unit based on a synchronous 3-bit counter.

The clock divider schematic consists of three T flip-flops (TFFs), one AND gate, and buffers. The TFF consists of one DFF and one non-inverting buffered 2:1 multiplexer unit, as shown in Figure 4.

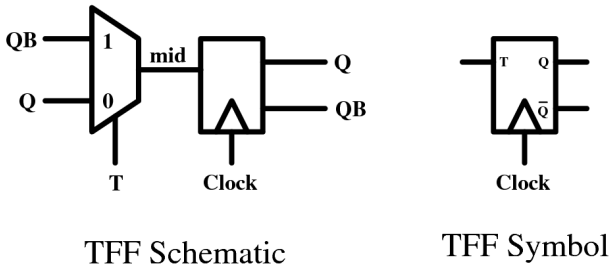


Figure 4: T flip-flop.

The DFFs are operating at the high frequency (5 GHz). The buffer before (clk5Ga) node is used to drive the gates after this node and makes the signal more robust, especially when the rise time and fall time of the output signal (clk5G) should be less than 20 ps across different process corners. In addition, the rise time and fall time of the output signals (clk625M, clk1.25G, and clk2.5G) should be less than 100 ps, 80 ps, and 20 ps, respectively, across different process corners. The rising edge of all signals (clocks) should happen at the same time. To achieve this condition, the $\bar{Q}$ node of the first TFF is connected to the input of the second TFF, and the $\bar{Q}$ node of the second TFF is connected to the input of the AND gate. The output signals of the clock divider unit are shown in Figure 5.

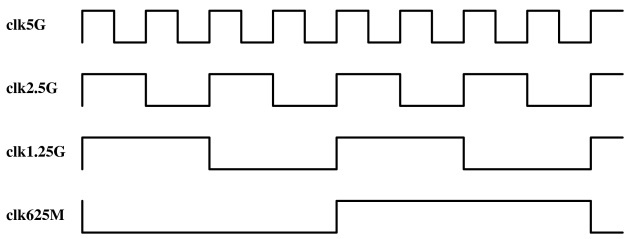


Figure 5: Output signals of the clock divider unit.

In order to achieve proper synchronization between the clocks, additional buffers are introduced. The synchronous buffers of the different clocks are very useful to use them in this phase of designing to facilitate minimization of the skew effect after the clock distribution. Thereby, four different clock signals (clk5G, clk2.5G, clk1.25G, and clk625M) have been generated, and the required performances have been achieved. The clk5G, clk2.5G, and clk1.25G are connected directly to the serializer unit while clk625M (Rclk signal) is connected to the clock multiplexing unit inside the control unit.

D Control Unit

The control unit is one of the most important units in the design because it is responsible for fetching the CLOCK, ENABLE, RESET, and DATA signals (from outside chip) and uses them with the clock divider unit to generate all the control signals that are needed in the design. All the input signals of the control unit are fetched from the outside chip except the Rclk signal (read clock) which is fetched from the clock divider unit.

The proposed control unit design consists of the following units: interface, clock multiplexing, non-inverting buffered 2:1 multiplexers, pulse generation, and enable element units. The overview of the control unit is shown in Figure 6.

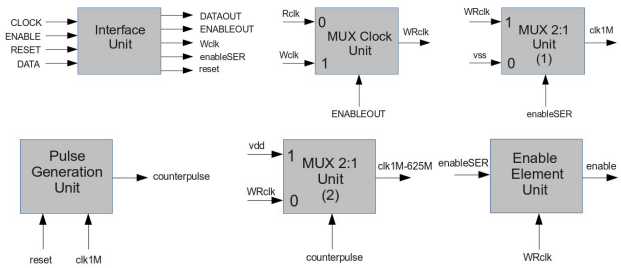


Figure 6: Control unit components.

i) Interface Unit

The interface unit consists of master-slave negative edge-triggered registers using multiplexers, drivers, and buffers. It is responsible for fetching the CLOCK, DATA, ENABLE, and RESET signals (from outside chip) to the proposed design. The interface unit schematic is shown in Figure 7. The Wclk signal is derived from the CLOCK signal by using driver, and it is used to synchronize the other control signals. Thus, the output signals of the interface unit are synchronized at the falling edge of the Wclk signal. The driver before the reset signal is used to increase the fan-out of the reset signal and to drive the gates in the pulse generation unit. All the timing regions of the interface unit have also been shown in the same Figure.

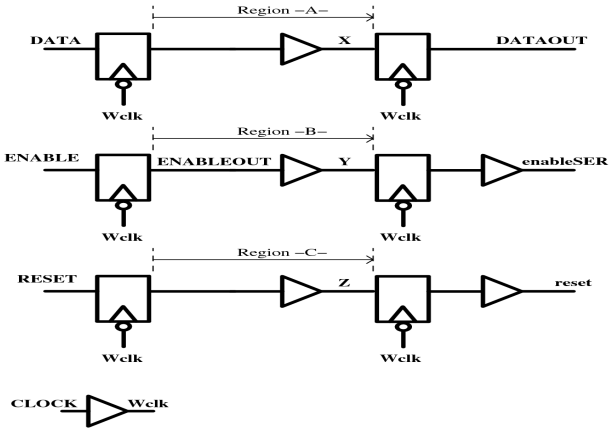


Figure 7: Interface unit schematic.

ii) Clock Multiplexing Unit

The memory has two operation modes, write and read mode. During write mode, WRclk signal is considered as the Wclk signal (1 MHz), while during read mode, WRclk signal switches to the (Rclk) read clock signal (625 MHz). Thus, the clock multiplexing unit is needed to generate the write-read clock signal (WRclk). The advantage of generating the WRclk signal is to generate the memory clock signal (clk1M-625M). During the clock multiplexing operation, the clock multiplexer should be switched from clock to another without introducing any glitch at the output of the multiplexer.

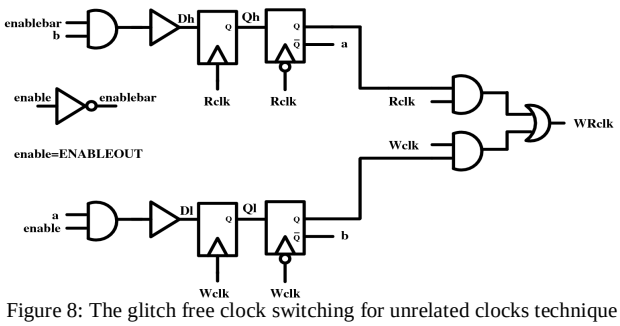


Figure 8: The glitch free clock switching for unrelated clocks technique

The clocks may be multiples of each other, or totally unrelated to each other. These two different methods of implementing a glitch free clock multiplexing are presented and discussed in detail in [8]. The write and read clocks may not be related, because they are generated from different sources. So, the glitch free clock Switching for unrelated clocks is used as shown in Figure 8. Hence, no data are missed during the clock switching operation.

The glitch may happen at the output of the multiplexer in case that the output signal switches from the current clock to the next clock directly when the select signal changes. The two negative edge-triggered DFFs are added first in the selection path in order to prevent any kind of glitch at the output of the clock multiplexer where the clocks are multiples of each other by using the feedback from the selection of one clock to the other forward clock. This operation disables the current clock to propagate directly to the output and waits for the next clock before the propagation. Thereby, any glitches are avoided when the clocks are multiples of each other. In order to use this criterion to avoid the glitches when the clocks are completely unrelated, two positive edge-triggered DFFs are added in the selection path. The selection signal or the feedback selection signal may be applied in asynchronous manner. The meta-stability caused by these signals is avoided after adding these DFFs [8].

The read mode is activated after the memory is filled. This means, after (64x32xTWclk), the ENABLEOUT signal goes low. Then, the output clock (WRclk) is switched to the read clock after a certain time. In order to avoid missing data, during clock multiplexing operation caused by the waiting state, the ENABLEOUT signal should be taken from the node. The output clock (WRclk) is considered as a write-read clock. In other words, the WRclk signal is equal to Wclk signal during the write mode, while the WRclk signal is equal to Rclk signal during the read mode.

iii) Pulse Generation Unit

After each 64 clock cycles of clk1M signal, the 64 bits data are stored first into the serial to parallel conversion unit before shifting these data into the memory.

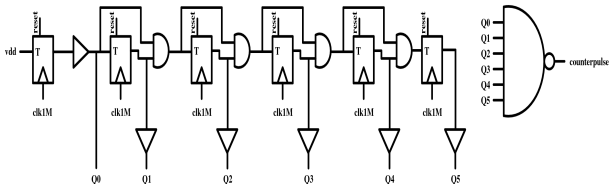


Figure 9: Schematic of the pulse generation unit

In order to create single pulse signal in each 64 clock cycles of clk1M, pulse generation unit is presented. The pulse generation unit is based on the 6-bit counter with synchronous reset in order to reset the counter. In addition, 6-input NAND gate is used to generate the needed (counter pulse) signal from the output of the 6-bit counter. The schematic of the pulse generation unit is shown in Figure 9.

iv) Enable Element Unit

The enable circuit element is used in order to generate the enable signal of the memory unit. It consists of one DFF and buffer as shown in Figure 10. The enable signal is derived from the enable SER signal in each clock cycle of the WRclk signal. The enable signal is responsible for activating the multiplexing system in the memory unit during the read mode. During the write mode, the enable signal is high, so the multiplexing system of the memory unit is deactivated

until all the data are stored into the memory. While during the read mode, the enable signal is low, so the multiplexing system in the memory unit is activated and allows the memory to reuse the stored data to test the intended device after the serializer unit.

The most important issue is that, before the multiplexing system is activated, the data should be completely stored into the memory. The multiplexing system may loose one bit data in each row of the memory when enable selection goes from high to low. This happens if the enable signal goes low before the clk1M-625M signal goes high (after the distribution circuits). Thus, the unwanted data are entered into the memory from the multiplexing system. This may happen because of the propagation delay of the enable signal is much less than the propagation delay of the clk1M-625M signal. In order to solve this problem, buffers are introduced before the enable distribution in order to be sure that the enable signal goes low after the rising edge of the clk1M-625M (after the distribution circuits).

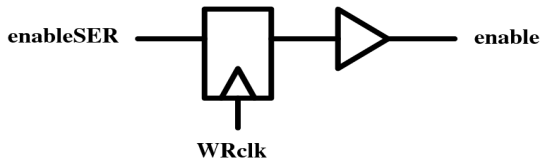


Figure 10: Schematic of the enable element.

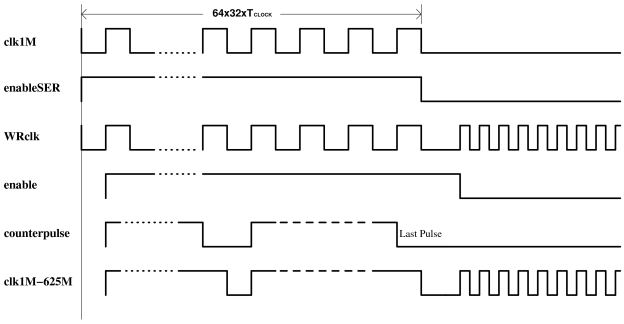


Figure 11: Output signals of the control unit.

The control unit is used to generate the control signals of the proposed design. The design of control unit is successfully implemented, and the functionality of the control unit is achieved. The input signals of the control unit are CLOCK, ENABLE, RESET, DATA & Rclk. The output signals of the control unit are DATAOUT, clk1M, clk1M-625M, enable & enable SER. Finally the control signals of the control unit are shown in Figure 11.

E Serializer Unit

The serializer unit is used to convert the parallel data at low frequency into serial data at high frequency. In other words, it is responsible for speeding up the data from low frequencies to high frequencies. Thereby, the high speed issues and the robustness are considered as the most important keys of designing the serializer unit.

The proposed architecture of the serializer unit is based on the traditional tree structure technique and was implemented as an arrangement of 2:1 serializer units [9],[10]-[12]. In order to convert 64 bits parallel data at low frequency to 8 bits data streams at high frequency, 8 pages of 8:1 serializer with 5 GHz serial data at the output are presented. Each 8:1 serializer consists of seven 2:1 serializer units (four Unit625M, two Unit1.25G, and one Unit2.5G). Each set of 8 bits data is separated into even and odd data. At the output of the serializer unit, these data are serialized separately into 1 bit streams at 2.5 GHz. Then, the data are resynchronized at 5 GHz at the output. So, each 8 bits stream is interleaved into one bit streams at 5 GHz. In order to get the correct sequence as [b7, b6, b5, b4, b3, b2, b1, b0] at the output, the input data sequence should be as b0, b4, b2, b6, b1, b5, b3, and b7, respectively. The proposed 8:1 serializer unit is shown in Figure 12.

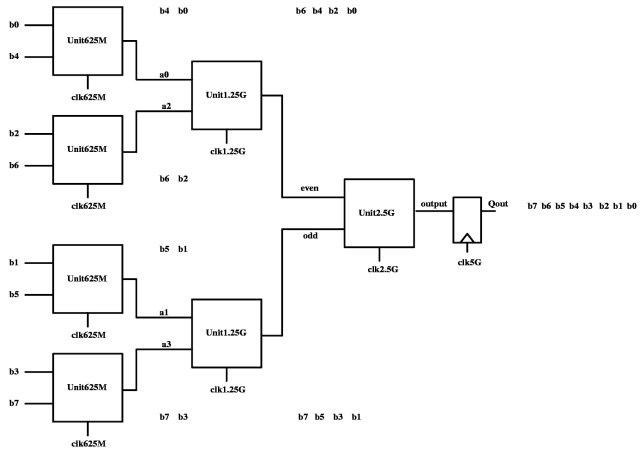


Figure 12: Proposed 8:1 serializer unit.

III. RESULTS

In the proposed design (implemented in 90 nm process), the transistors were set to the minimum channel length, and the used width ratios of NMOS: PMOS were 1:2.5 and 1:2 ratio for the inverter and the transmission gate, respectively. This results in equalization between the rise time and fall time as much as possible at the output node. The simulation results satisfy the process corners TT @ 50 °C, SS @ 100 °C, and FF @ 0 °C temperatures, respectively. For simulation purposes, write frequency used is equal to 156.25 MHz instead of 1 MHz in order to reduce the simulation time of the design. The parameters of the testbench are the following: TEXclock = 200 ps, tr = tf = 100 ps, TCLOCK = 6.4 ns, TDATA = 12.8 ns, TRESET = 6.4 ns, TENABLE = 64x32xTCLOCK = 13107.2 ns.

The test-bench of the complete system is shown in Figure 13. The parameters are the following: TEXclock

= 200 ps, tr = tf = 100 ps, TCLOCK = 6.4 ns, TDATA = 12.8 ns, TRESET = 6.4 ns, TENABLE = 64x32xTCLOCK = 13107.2 ns. The data input sequence is the following: [0 1 0 1 0 1 0 1 0 .....]. The functionality of the output data is shown in Figure 14.

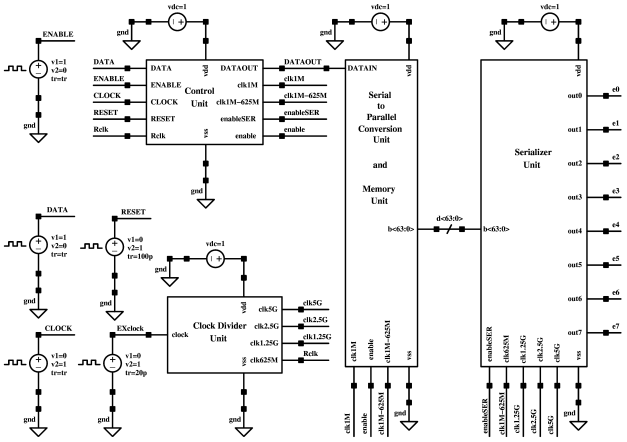


Figure 13: Test-bench of the complete system.

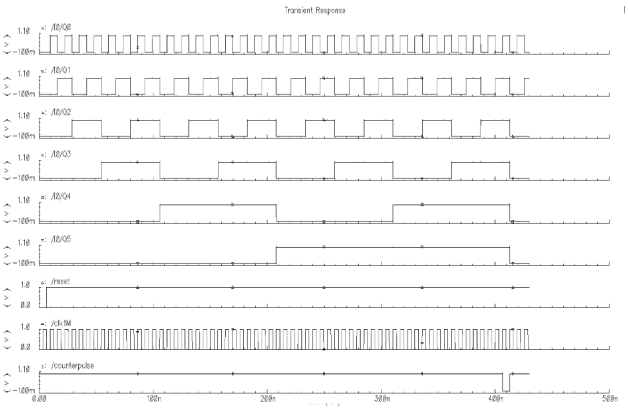


Figure 14: Simulation results of the complete system.

According to the different δ calculations Tables for different clocks in the design, the acceptable range of positive and negative δW is shown in Table 1.

TABLE I
ACCEPTABLE RANGE OF POSITIVE AND NEGATIVE ΔW FOR DIFFERENT CLOCKS

Between Different Clocks	Positive δW (ps)	Negative δW (ps)
Low clock = (clk1M)	(clk1M	625M)
High clock = (clk1M	625M)	(clk625M)
(clk625M)	(clk1.25G)	663.5 35
(clk1.25G)	(clk2.5G)	265.5 33.5
(clk2.5G)	(clk5G)	115 34

TABLE II
POWER DISSIPATION OF THE PROPOSED DESIGN ACROSS DIFFERENT PROCESS CORNERS

Power Dissipation of the main parts of the design Iav => Pdissipation = Iav · vdd = Iav (mW)	Different Process Corners		
	TT,50oC	SS,100oC	FF,0oC
Control unit	0.10	0.08	0.16
Clock Divider Unit	1.13	1.07	1.15
Serial to Parallel Conversion Unit + Memory Unit	3.65	2.93	6.59
Serializer Unit	0.50	0.39	1.04
Total power Dissipation	5.38	4.47	8.94

CONCLUSION

The on-chip memory based tester can be considered as a new circuit builder for testing devices of MSPSs at high frequency in SoC environment. The enormous technology evolution of CMOS has largely improved the performance of digital ICs in terms of low cost, high speed operation, and area consumption. Moreover, during high speed operation, the new on-chip tester methodology overcomes the bandwidth limitations problem imposed by I/O transmission paths due to the old instrumentation tester methodology. In order to avoid a large number of very high speed I/O pads, the on-chip memory is implemented in the tester [4].

Thereby, the on-chip tester has become the dominant choice in deep submicron technologies as compared to the old instrumentation tester. But there exists a tradeoff between many factors, such as area, power consumption, timing requirements, robustness, and simplicity for tester design in 90 nm CMOS process. In addition, there are big challenges facing digital circuit's designers, such as fetching the data from the outside chip into the on-chip memory, designing the on-chip memory with low area consumption, speeding up the data from low frequencies to high frequencies without losing any data, and designing the serializer with low power consumption.

To overcome these challenges, the serial to parallel conversion unit based on shift register has been designed in order to fetch the data into the on-chip memory at low frequency, shift registers based on master-slave DFF are used as a memory elements in the on-chip memory design, an arrangement of 2:1 serializer units based on a traditional tree structure [9],[10]-[12] is designed in order to speed up the data, and different clocks are generated from the clock divider unit to use them in the different parts of the

design. This thesis has addressed the implementation of on-chip memory design in order to test MSPS devices with a word length of 8 bits at a rate of 5 GS/s. The simulation result in schematic level design shows that the on-chip tester design has been successfully implemented, and the specification requirements of the design have been achieved.

REFERENCES

[1] P. Larsson-Edefors, "High-Speed CMOS Design – Bit-Serial Arithmetic Applications and Technology Mapping of Combinational Boolean Equations," Ph.D. dissertation, Physics and Measurement Technology Dept., Linkoping Univ., Linkoping, Sweden, 1995.

[2] N. H. E. Weste and K. Eshraghian, *Principles of CMOS VLSI Design: A Systems Perspective*, MA: Addison-Wesley, Second Edition, 1993.

[3] R. Rashidzadeh, "An Embedded Tester Core for Mixed-Signal System-on-Chip Circuits," Ph.D. dissertation, Electrical and Computer Engineering Dept., Windsor Univ., Windsor, Canada, 2007.

[4] J. Muller, B. Stefanelli, A. Frappe, L. Ye, A. Cathelin, A. Niknejad, and A. Kaiser, "A 7-Bit 18th Order 9.6 GS/s FIR Up-Sampling Filter for High Data Rate 60-GHz Wireless Transmitters," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, pp. 1743-1756, July 2012.

[5] K. Runge and P. B. Thomas, "5Gbit/s 2:l multiplexer fabricated in 0.35µm CMOS and 3Gbit/s 1:2 demultiplexer fabricated in 0.5µm CMOS technology," *IEEE Electronic Letters*, vol. 35, no. 19, pp. 1631-1633, September 1999.

[6] F. Tobajas, R. Esper-Chaín, R. Regidor, O. Santana, and R. Sarmiento. *A Low Power 2.5 Gbps 32:1 Serializer in SiGe BiCMOS Technology* [Online]. Available: http://www.iuma.ulpgc.es/publicaciones/2005.html

[7] M. Wong, "A 2.5Gbps CMOS Serial Link Transceiver Design," M.S. thesis, Electrical Engineering Dept., National Central Univ., Taiwan, China, 2002.

[8] R. Mahmud. (2003, June 26). *Techniques to make clock switching glitch free* [Online]. Available: http://www.eetimes.com/document.asp?doc_id=1202359.

[9] D. F. Tondo, and R. R. López, "A Low-Power, High-Speed CMOS/CML 16:1 Serializer," *Proceedings of the Argentine School of Micro-Nanoelectronics, Technology and Applications*, San Carlos de Bariloche, pp. 81-86, October 2009.

[10] J. H. Shim, S. Byun, J. C. Lee, K. Kim, and C. S. Kim, "A low-power 10-Gb/s 0.13-µm CMOS Transmitter for OC-192/STM-64 Applications," *50th Midwest Symposium on Circuits and Systems*, Montreal, Que., pp. 1165-1168, August 2007.

[11] K. Ishii, H. Nakajima, H. Nosaka, M. Ida, K. urishima, S. Yamahata, T. Enoki, and T. Shibata "Over 40 Gbit/s 16:1 multiplexer IC using InP/InGaAs HBT technology," *IEEE Electronic Letters*,vol. 39, no. 12, June 2003.

[12] F. Znidarsic, E. Mullner, and R. Strunz "16:1 retiming multiplexer for 10 Gbit/s in Si production technology," *IEEE Electronic Letters*,vol. 32, no. 3, pp. 207-209, February 1996.

Implementation of Wireless Remote Control for Bore-well Motor

Shakeel Ahmed[1] and N.Nitin Kumar[2]
[1] CVR College of Engineering/ECE Department, Ibrahimpatan, R.R.District, Telangana., India
Email: Shakeel_be@yahoo.com
[2] CVR College of Engineering/ECE Department, Ibrahimpatan, R.R.District, Telangana., India
Email: nitin.nagamalla@gmail.com

***Abstract*— The world around is technically advancing in every speck of human life. With the growth in VLSI technology and advent of microcontrollers, man has made his way of leading life simpler. Many a times, certain situations are encountered wherein a device has to be controlled from a remote distance, which is likely to be seen in industries, colleges etc., In such cases, the proposed system "Wireless Remote Control for Bore-well Motor" serves as a suitable solution, thus saving time and energy. In this paper, the design and implementation of the proposed system is described. The status of a bore-well is controlled using a mobile phone, rather than going to the actual place and manually controlling it. The circuit of the proposed system involves the essential components like AVR microcontroller and DTMF (Dual Tone Multi-Frequency) decoder. This circuit can also be implemented for controlling home appliances like fans, bulbs etc. The advantage of the circuit is that any device can be controlled from any distance until and unless the system runs out of coverage area of the network.**

***Index Terms*—Embedded system, DTMF & wireless network.**

I. INTRODUCTION

The technical advancement of the world around is evident from the fact that there is rapid growth in industrialization today and also marketing demands are continuously increasing. The advancements in technology have made human's way of leading life simpler. Many electronic circuits are being designed to satisfy human needs. Technology has made possible the automation of manual work thus saving time and money. In such situations, electronic circuits provide a flexibility of controlling the associated devices/machines from a remote distance.

The proposed work is to control a device/machine from a remote distance and achieve automation. There are instances where it is desired to operate a device located at a distance without actually going to the place, i.e., automatic control of the device. To control a machine like bore well that is situated outside the college, it is required that a person goes and operates it manually, which consumes petrol, human effort and more important time. Hence a system is designed to ease the human work and thus save time and energy. Moreover, it is often found that many students feel lazy to switch off their lights after their preparation for their exam or preparation of their project report over night. And same is the case with elders after the completion of their office work over late night. In such circumstances, a device or system that enables controlling of light from a remote distance is always appreciated. There are many more situations wherein this circuit is seriously needed. For example, switching off a large machine directly can be too dangerous sometimes. So, even in those situations controlling of the machines remotely can serve the purpose.

The rest of the paper is organized as follows:

- Section II gives a brief introduction of the proposed system.
- Section III gives the block diagram of the proposed system and a brief description of each of the components used in the system.
- Section IV explains the working of the proposed system.
- Section V gives the results followed with advantages & limitations of the proposed system.
- Section VI Concludes the paper with its future scope.

II. PROPOSED SYSTEM

The proposed system is designed to achieve automation which makes possible to control a device/machine without even being present at the actual site. A device can be made ON/OFF by just making a call to the receiver mobile and press the specified keys. To accomplish this, two mobile phones are required, one at the transmitter and other at the receiver section. The prerequisites of this system include good signal strength at the site and the mobile at the receiver section must have an auto answer option.

The other essential components include microcontroller (ATMEGA8515L), DTMF decoder/receiver (CM8870), relay, relay driver

(ULN2003A), AC contactor. The microcontroller is the heart of the project. Suitable program is dumped into the microcontroller which actually controls the whole system. When a user makes a call to the receiver mobile and presses a key, it is sent as an input to microcontroller via DTMF decoder. DTMF decoder performs the task of decoding the output from transmitter phone to determine the actual key pressed by the user. The microcontroller now performs the actual job of controlling the device based on the input from DTMF decoder and feedback input from buzzer.

The output from buzzer indicates the change of the state of the device. The possible states are ON, OFF. If the user presses a valid key, an interrupt is generated which causes the microcontroller to run and from the output of buzzer, it complements the previous state of the device. Buzzer beeps to indicate if the user has pressed an invalid key. If the device is previously OFF, the user presses '1' to make it ON and '3' to perform the opposite action. The buzzer beeps once to indicate that the device is ON, twice to indicate that it is OFF and thrice to indicate the user has pressed the wrong key. This circuit works with regulated 5V supply.

III. DESIGN AND IMPLEMENTATION

The block diagram of the proposed system is as shown below:

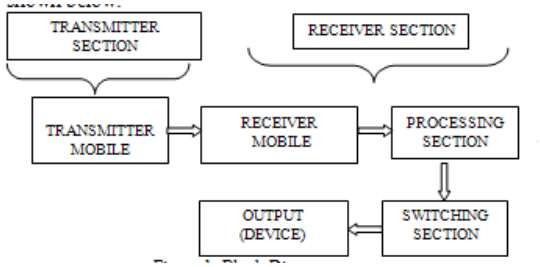


Figure 1: Block Diagram

The schematic diagram for this circuit is as shown in the figure below:

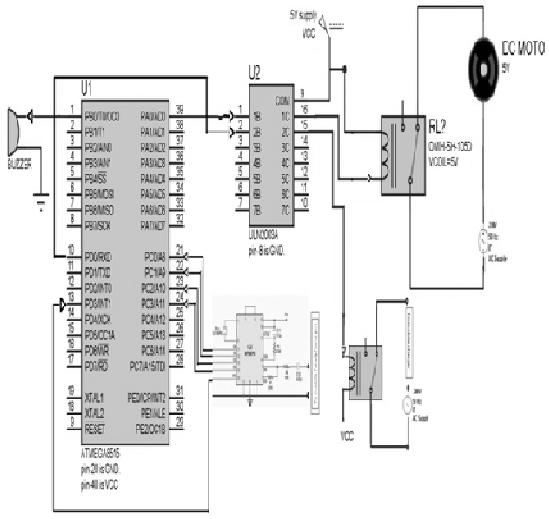


Figure 2: Schematic Diagram

The major components that are required for building the circuit are

1. Microcontroller: ATMEGA8515L
2. DTMF Decoder/Receiver : CM8870
3. Relay switch
4. Relay driver: ULN2003A
5. AC Contactor

Apart from these components, Buzzer, Oscillator, Resistors, and Capacitors are used in the circuit. The description of major component is given below

1. Microcontroller: ATMEGA8515L

The ATMEGA8515L is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega8515 provides the following features: 8K bytes of In-System Programmable Flash with Read-While-Write capabilities, 512 bytes EEPROM, 512 bytes SRAM, an External memory interface, 35 general purpose I/O lines, 32 general purpose working registers, two flexible Timer/Counters with compare modes, Internal and External interrupts, a Serial Programmable USART, a programmable Watchdog Timer with internal Oscillator, a SPI serial port, and three software selectable power saving modes. The Power-down mode saves the Register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption.

The ATmega8515 is supported with a full suite of program and system development tools including: C Compilers, macro assemblers, program debugger, in-circuit emulators, and evaluation kits.

2. DTMF Decoder/Receiver : CM8870

Dual-tone multi-frequency signaling (DTMF) is used for telecommunication signaling over analog telephone lines in the voice-frequency band between telephone handsets and other communications devices and the switching center. The version of DTMF that is used in push-button telephones for tone dialing is known as Touch-Tone. Introduced by AT&T in 1963, the Touch-Tone system using the telephone keypad gradually replaced the use of rotary dial and has become the industry standard for landline service.

Multi-frequency signaling is a group of signaling methods that use a mixture of two pure tone (pure sine wave) sounds i.e., each key in the keypad has two

frequencies (low and high) associated with it. Whenever a key is pressed, a composite sine wave formed by superimposing of one wave (low frequency) with the other (high frequency) is generated. Various MF signaling protocols were devised by the Bell System and CCITT. The earliest of these were for in-band signaling between switching centers, where long-distance telephone operators used a 16-digit keypad to input the next portion of the destination telephone number in order to contact the next downstream long-distance telephone operator. This semi-automated signaling and switching proved successful in both speed and cost effectiveness. Based on this prior success with using MF by specialists to establish long-distance telephone calls, Dual-tone multi-frequency (DTMF) signaling was developed for the consumer to signal their own telephone-call's destination telephone number instead of talking to a telephone operator. Typical 16 digit keypad is shown below.

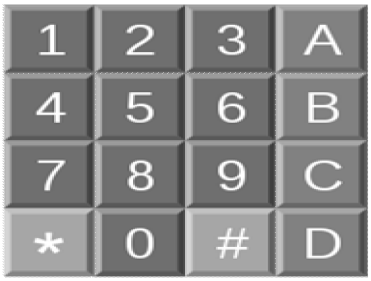


Figure 3: DTMF Keypad Layout

CM8870 provides full DTMF receiver capability by integrating both the band split filter and digital decoder functions into a single 18-pin DIP, SOIC, or 20-pin PLCC package. The CM8870 is manufactured using state-of-the-art CMOS process technology for low power consumption (35mW, max.) and precise data handling. The filter section uses a switched capacitor technique for both high and low group filters and dial tone rejection. The CM8870 decoder uses digital counting techniques for the detection and decoding of all 16 DTMF tone pairs into a 4-bit code. This DTMF receiver minimizes external component count by providing an on-chip differential input amplifier, clock generator, and a latched three-state interface bus.

Separation of the low-group and high-group tones is achieved by applying the dual-tone signal to the inputs of two 9th-order switched capacitor band pass filters. The filter section also incorporates notches at 350 Hz and 440 Hz which provides excellent dial tone rejection. The decoder section uses a digital counting technique to determine the frequencies of the limited tones and to verify that these tones correspond to standard DTMF frequencies. A complex averaging algorithm is used to protect against tone simulation by extraneous signals (such as voice) while providing tolerance to small frequency variations.

3. Relay switch

A relay is an electrically operated switch. Many relays use an electromagnet to operate a switching mechanism mechanically, but other operating principles are also used. Relays are used where it is necessary to control a circuit by a low-power signal (with complete electrical isolation between control and controlled circuits), or where several circuits must be controlled by one signal. The first relays were used in long distance telegraph circuits, repeating the signal coming in from one circuit and re-transmitting it to another. Relays were used extensively in telephone exchanges and early computers to perform logical operations.

Generally speaking, a relay circuit is a circuit that uses a small mechanical switch or a semiconductor device (with associated circuitry) to energize a relay, which will then close a contact set to complete another circuit.

The four parts of a relay are:

- Electromagnet
- Armature
- Spring

Set of electrical contacts

Figure 4 shows various outlooks of a Relay switch

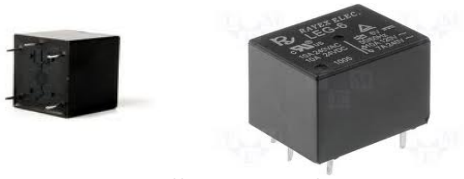


Figure 4: Two different views of a relay switch

4. Relay driver: ULN2003A

The output current from the microcontroller is not sufficient to drive a relay that electrically operates the device. ULN2003A, relay driver, acts as an intermediary component for microcontroller and relay in providing sufficient current that could energize the relay.

The ULN2003 is a high voltage, high current Darlington array each containing seven open collector Darlington pairs with common emitters. Each channel rated at 500mA, can withstand peak currents of 600mA and produces an output voltage of about 50V. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout. It is a 5V TTL, CMOS logic device.

This versatile device is useful for driving a wide range of loads including solenoids, relays DC motors, LED displays filament lamps, thermal print heads and high power buffers. The ULN2003A is supplied in 16 pin plastic DIP packages with a copper lead frame to reduce thermal resistance. It is also available in small outline package.

5. AC Contactor

A contactor is an electrically controlled switch used for switching a power circuit, similar to a relay except with higher current ratings. A contactor is controlled by a circuit which has a much lower power level than the switched circuit.

Contactors come in many forms with varying capacities and features. Unlike a circuit breaker, a contactor is not intended to interrupt a short circuit current. Contactors range from those having a breaking current of several amperes to thousands of amperes and 24V DC to many kilovolts. The physical size of contactors ranges from a device small enough to pick up with one hand, to large devices approximately a meter (yard) on a side.

Contactors are used to control electric motors, lighting, heating, capacitor banks, thermal evaporators and other electrical loads.

A contactor has three components. The contacts are the current carrying part of the contactor. This includes power contacts, auxiliary contacts, and contact springs. The electromagnet (or "coil") provides the driving force to close the contacts. The enclosure is a frame housing the contact and the electromagnet. Enclosures are made of insulating materials like Bakelite, Nylon 6, and thermosetting plastics to protect and insulate the contacts and to provide some measure of protection against personnel touching the contacts. Open-frame contactors may have a further enclosure to protect against dust, oil, explosion hazards and weather.

A basic contactor will have a coil input (which may be driven by either an AC or DC supply depending on the contactor design). The coil may be energized at the same voltage as a motor the contactor is controlling, or may be separately controlled with a lower coil voltage better suited to control by programmable and lower-voltage pilot devices. Certain contactors have series coils connected in the motor circuit; these are used, for example, for automatic acceleration control, where the next stage of resistance is not cut out until the motor current has dropped.

Unlike general-purpose relays, contactors are designed to be directly connected to high-current load devices. Relays tend to be of lower capacity and are usually designed for both normally closed and normally open applications. Devices switching more than 15 amperes or in circuits rated more than a few kilowatts are usually called contactors. Apart from optional auxiliary low current contacts, contactors are almost exclusively fitted with normally open ("form A") contacts. Unlike relays, contactors are designed with features to control and suppress the arc produced when interrupting heavy motor currents.

When current passes through the electromagnet, a magnetic field is produced, which attracts the moving core of the contactor. The electromagnet coil draws more current initially, until its inductance increases when the metal core enters the coil. The moving contact is propelled by the moving core; the force developed by the electromagnet holds the moving and fixed contacts together. When the contactor coil is de-energized, gravity or a spring returns the electromagnet core to its initial position and opens the contacts.

For contactors energized with alternating current, a small part of the core is surrounded with a shading coil, which slightly delays the magnetic flux in the core. The effect is to average out the alternating pull of the magnetic field and so prevent the core from buzzing at twice line frequency. Rapid closing can, however, lead to increase contact bounce which causes additional unwanted open-close cycles. One solution is to have bifurcated contacts to minimize contact bounce; two contacts designed to close simultaneously, but bounce at different times so the circuit will not be briefly disconnected and cause an arc.

A slight variant has multiple contacts designed to engage in rapid succession. The first to make contact and last to break will experience the greatest contact wear and will form a high-resistance connection that would cause excessive heating inside the contactor. However, in doing so, it will protect the primary contact from arcing, so a low contact resistance will be established a millisecond later. Another technique for improving the life of contactors is contact wipe; the contacts move past each other after initial contact on order to wipe off any contamination.

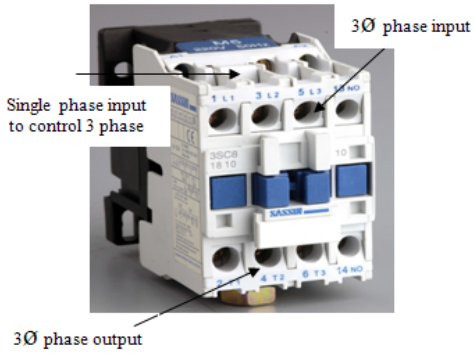


Figure 5: AC Contactor

IV. WORKING OF THE PROPOSED SYSTEM

The system consists of the following three sections.

1. Transmitter section
2. Receiver section
3. Processing section

Transmitter Section: consists of mobile having facility to SMS. The transmitter side should know the receiver mobile SIM number.

Receiver Section: the receiver mobile is set in auto answer mode. When a user makes a call to the receiver mobile, it is automatically answered. When a key is pressed, its corresponding dual tone multi-frequency is generated and the actual key pressed by the user is determined by DTMF decoder/receiver.

Processing Section: a specific key is pressed in the mobile at transmitter section, its 4-bit binary equivalent is generated and an impulse ESt signal as an output from CM8870. This binary output is fed as an input and ESt signal as interrupt input to the microcontroller, which is programmed such that the status of the device is controlled by pressing the specified keys inside interrupt service routine. Buzzer is provided so as to produce an acknowledgement or feedback on the status of the device when a key is pressed.

When '1' is pressed from the mobile, the status of the device changes from OFF to ON and the buzzer beeps once indicating that the device has been switched ON. When the key '3' is pressed, the status of the device changes from ON to OFF and the buzzer beeps twice indicating that the device has been switched OFF. Depending on the buzzer beeps, the current status of the device can be known. When the user presses a key other than those specified, buzzer beeps thrice indicating that the user has pressed an unspecified key.

The processing section is shown in the figure 3.

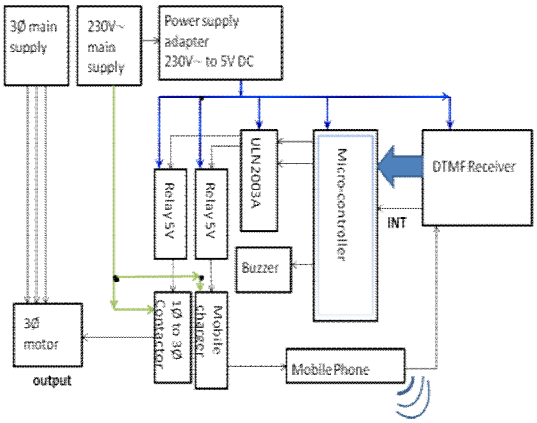


Figure 3: Processing Section

V. RESULTS

The proposed system was implemented successfully and the result obtained is in very much accordance with our requirement of controlling of a device with the mobile. By pressing '1' or '3', the status of the device changes accordingly. The present and next state of the motor is given in table 1.

TABLE I

Key pressed	Present state of motor	next state of motor
1	ON or OFF	ON
3	ON or OFF	OFF
Other than 1 and 3	ON OFF	ON OFF

Thus proposed system can be used to control any device from a remote distance.

A. *Advantages*

- As mentioned earlier, this circuit saves time and energy because it enables the remote controlling of the device instead of going to the site and operating it directly.
- It is economical as the components used are available at low cost.
- The construction of circuit is so simple.
- Also, automatic mobile charging facility has been provided.
- Moreover, upgradation of such circuits eases the work of humans especially those working in big industries and operating on very large machines.
- This circuit makes home and industrial automation feasible.

B. *Limitations*

- The main disadvantage of this circuit is if there is no proper signal strength at the receiver side, making calls wouldn't be possible and hence the circuit doesn't work.
- Only mobiles having the auto answer option can be used at the receiver.

VI. CONCLUSION AND FUTURE SCOPE

A. *Conclusion*

The basic level of device control using cell phone had been implemented successfully. It was tested many times and found to be successfully working all the times. The circuit is very simple to implement, easy to handle and very economical.

B. *Future Scope*

- Automation has become more powerful and will take over the present system of device control in near future.
- The application of this circuit can be extended up to controlling of seven devices at a time using ULN2003A and multiple relays.

It is basis for many complex circuits that can be employed in industries where remote access of a machine is required thereby reducing the human effort.

REFERENCES

[1] Avigyan Datta Gupta, Savan Samanta, Avishek Acharjee, "Cellphone Based Device Control With Voice Acknowledgement," IJETAE, Vol 2, Issue 10, October 2012

[2] Steven F. Barrett and Daniel J. Pack, *'Atmel AVR Microcontroller Primer: Programming and Interfacing'*

[3] http://en.wikipedia.org/wiki/Contactor

[4] http://en.wikipedia.org/wiki/Microcontroller

[5] http://www.atmel.com/images/doc2512.pdf

Improving the Bit Error Rate of OFDM using Convolutional codes

R. Prakash Kumar
CVR College of Engineering/E.C.E Department, Hyderabad, India
Email: prakash.rachmagdu@gmail.com

***Abstract*— In wireless applications high throughput and better transmission quality can be achieved by parallel transmission of data, one of such technique is Orthogonal Frequency Division Multiplexing (OFDM) by adding channel coding to the uncoded OFDM ,the performance can be improved. In this paper, the system throughput of a working OFDM system has been enhanced by adding convolution coding. Convolution codes are used extensively in numerous applications in order to achieve reliable data transfer, including digital audio and video, mobile, radio communication, satellite deep space network communication. They can correct even burst and random errors. Simulation is done over Additive white Gaussian Noise (AWGN) channel has 64- sub carriers each is individually modulated by 16-QAM (Quadrature Amplitude Modulation). The performance parameter used for evaluation of BER(Bit Error Rate) with AWGN channel.**

***Index Terms*— OFDM, BER, Convolution codes.**

I. INTRODUCTION

The FEC (Forward Error Correction) have become a vital part of modern digital wireless communication systems enabling reliable transmission to be achieved by over noisy channel by adding the redundancy to the transmitted data. These additional bits (redundancy), while conveying no new information themselves, make it possible for channel decoder to detect and correct information bearing bits. Error detection and correction lowers the overall probability of error. Over the past years convolutional codes have been widely considered to be most practical importance. Convolutional code maps information blocks of length 'k' to code blocks of length 'n'. This linear mapping contains memory, because the encode block depends on 'm' previous information blocks. In IEEE 802.11a/g transmitters, convolution codes are used for FEC at the physical layer.

II. SYSTEM MODELING

The block diagram of convolution coded OFDM shown in Fig. 1. It consists of transmitter, AWGN channel and receiver. The transmitter consists of Convolution encoder and OFDM modulator. The information bits are encoded by convolution encoder, converts serial data into parallel data. This information is modulated by a 16-QAM modulator mapping onto the sub carrier amplitude and phase, and then transforms this spectral representation of the data into the time domain using an Inverse Fast Fourier Transform (IFFT). During modulation, OFDM symbols are divided into frames such that data will be modulated by frame in order to receive signal be in SYNC with the receiver. In order to eliminate ISI (Inter Symbol Interference) and ICI (Inter Carrier Interference) a guard time (cyclic prefix) is inserted between the OFDM symbols. This allows the receiver to capture the starting point of a symbol period, such that FFT (Fast Fourier Transform) has corrected the information bits.

This signal is passed through an AWGN channel. The important property of this channel is ,it is a universal channel and linear in all frequencies of amplitude and phase, so 16- QAM modulated signal passes through it without any loss of amplitude and phase. Apart from this fading doesn't exit. There by received signal is the summation of original signal and white Gaussian noise.

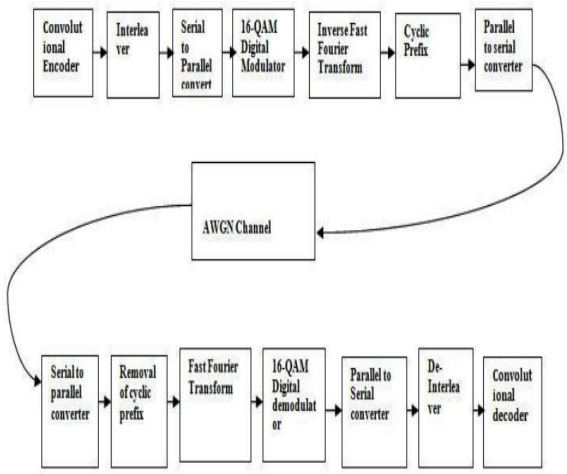


Figure 1 Block diagram of convolution coded OFDM

The receiver performs the inverse operation of transmitter. First, the CCOFDM (convolution coded OFDM) data are split from a serial stream into parallel sets. The Fast Fourier Transform (FFT) converts the time domain samples back into a frequency domain

representation. The magnitudes of the frequency components correspond to the original data demodulated by 16-QAM demodulator. Finally, the parallel to serial block converts this parallel data into a serial stream to recover the original input data is decoded by viterbi algorithm.

III. CONVOLUTION ENCODER

An (n, k, m) convolutional code can be implemented with a k-input, n-output linear sequential circuit with input memory m .it encodes the data by passing through a linear finite state-shift register. Depends on the shift register connection encoders are two types, one is feed forward and other is feedback systematic and Nonsystematic. In this paper the Encoding process begins with the generation of 600000 random binary bits. For text data type, the first step is decimal to binary conversion. Then it is encoded by convolutional code of rate ½. With the constraint length of 7 and feedback connections are (133) and (171) with generator upper polynomial matrix, [1 1 1] and under polynomial matrix, [1 0 1]. The output of this block is codeword with length 1200000 bits. Through 16- QAM block codeword is mapped into signal with the possibility of phase and amplitude formed. 16-QAM modulator produces symbols in which each symbol represents 4 bits.

IV. OFDM MODULATOR

The main principle of OFDM is the high-speed distribution of a data stream into a number of low-speed data streams, then, sent through subcarrier simultaneously. Row of data is converted into information in the form of parallel. The original bit rate R is transmitted into a parallel path R/N, where N refers to number of 64-subcarriers (equal to the number of parallel paths) of which each datum is modulated by subcarrier with FFT size 64 using the IFFT to form OFDM symbols. Equation (1) [5] shows the IFFT process that allows the allocation of OFDM symbols in the form of time. The output of the IFFT OFDM symbols forms a mutually orthogonal in time domain.

$$x(n) = \sum_{n=0}^{N-1} x(k) \sin\left(\frac{2\pi kn}{N}\right) - j\sum_{n=0}^{N-1} x(k) \cos\left(\frac{2\pi kn}{N}\right) \quad (1)$$

Where x(n) is the IFFT output signal, x(k) is the transmitted signal at the k^{th} and N is the number of subcarriers. OFDM symbol is formed after the next process is added with cyclic prefix 25% of the total subcarrier channel that serves as a guard to avoid ISI. After the addition of the cyclic prefix represented in Equation 2, the data are converted back to serial form that can be transmitted from the channel parallel to serial converter.

$$T_{total} = T + T`_g \quad (2)$$

Where T is the OFDM symbol length without cyclic prefix, T_g is the length of cyclic prefix and the OFDM symbol T_{total} is the overall length.

V. OFDM DEMODULATOR

OFDM decomposes a signal using Fast Fourier Transform (FFT). Its function is convert time domain signal into frequency domain. The FFT process can be represented by (3) [5]. This process is also done in the disposal of cyclic prefix.

$$x(k) = \sum_{n=0}^{N-1} x(n) \sin\left(\frac{2\pi kn}{N}\right) + j\sum_{n=0}^{N-1} x(n) \cos\left(\frac{2\pi kn}{N}\right) \quad (3)$$

Where x (n) is the signal at time n; N is the number of subcarriers (subcarrier = 64), k is the frequency index of N; n is the index of time that produces x (k) that is the value of the frequency spectrum at k.

VI. CONVOLUTION DECODER

There are two basic categories to decoding convolutional codes. They are sequential decoding and maximum likelihood decoding based on Fano algorithm and Viterbi algorithm respectively. In this paper we are using the Viterbi decoding is an efficient and practical decoding for short constraint lengths. The following procedure used to trellis encoded data decoded by viterbi algorithm. Decoder is start with initialization of resetting all registers to 0's hamming distance has been calculated The Vitrerbi Decoder is a "maximum likelihood" decoder; this means that every time an input symbol is identified as "invalid" (i.e. it cannot be the direct output of a specified counvolutional encoder, no matter what sequence has been fed into the encoder), the decoder will try to assume the most likely symbol to have been transmitted by the encoder. The likelihood criteria are established based on a number of assumptions on the characteristics of the transmission channel. The Viterbi Decoder assumes that the transmission channel is memory less (i.e. its characteristics at a given moment do not depend on the previous channel state), the transfer function of the channel is linear (a non-linear function would produce cross-modulation effects), the transfer function is time-invariant, and a Gaussian additive noise is present on the channel.

VII. SIMULATION RESULTS

The main goal of this paper was to simulate OFDM system by utilizing convolution coding in Matlab. The CCOFDM simulated parameter and their values are shown in Table 1.in this paper CCOFDM generates total number of frames are 100, each frame consists of 96-bits. Each frame is modulated by 16-QAMand 64-subcarrier OFDM system with convolution code rate ½ and feedback connections are (133) and (171) is

simulated. Simulation algorithm steps and parameters as shown in Table 1.

TABLE I
THE CCOFDM SIMULATION PARAMETERS

Simulation parameter	value
Number of subcarriers	64
Convolution code	½(133,171)
IFFT size	64
Modulation scheme	16-QAM
SNR	(0-16)dB
Single Frame Size	96-bits
Total number of Frames	100
Number of pilots	4
Cyclic extension	25%(16)
Channel	AWGN

Simulation of Algorithm steps:

Here, we measured the performance of the CCOFDM through MATLAB simulation. The simulation follows the procedure listed below:

Step 1: 9600 information bits are randomly generated by built in command is randint (9600, 1).

Step 2: Encode the information bits using a convolutional encoder with the specified (133,171) poly2trellis matrix.

Step 3: 16-QAM modulation convert the binary bits, 0 and 1, into complex signals (before these modulations use zero padding) .each signal is 4-bits.

Step 4: Performed serial to parallel conversion.

Step 5: Use IFFT to generate OFDM signals, total 100 frames are generated each frame size of 96-bits.

Step 6: Use parallel to serial convertor to transmit signal serially.

Step 7: Introduce noise to simulate channel errors. We assume that the signals are transmitted over an AWGN channel. The noise is modeled as a Gaussian random variable with zero mean and variance the variance of the noise is obtained by a probability function as

$$f(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{\frac{(x-m)^2}{2\sigma^2}}$$

Step 8: At the receiver side, perform reverse operations to decode the received sequence.

Step 9: Count the number of erroneous bits by comparing the decoded bit sequence with the original one.

Step 10: Calculate the BER and plot it.

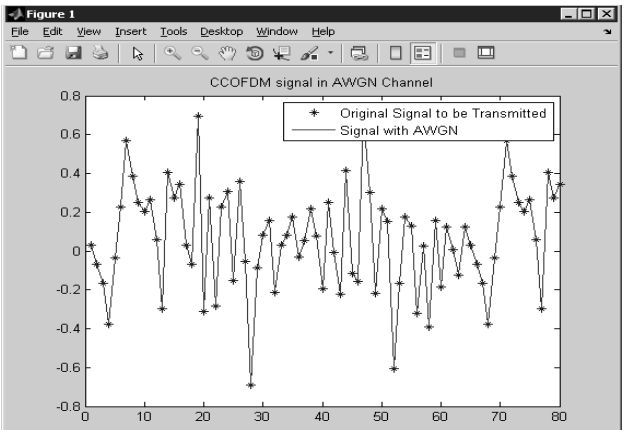


Figure 2. CCOFDM signal in the AWGN channel

Three methods are used to describe convolution encoders in graphically, they are tree, state and trellis. In this paper we are using the feed forward trellis convolution encoder. Encoded data is transfer to OFDM system. It generates the 100 frames. Each frame is modulated by 16-QAM adding the cyclic prefix of 16-bits. 4-pilot carriers are inserted in each frame. The total size if each frame is 96-bits. These are transmitted into the AWGN channel. This will aid the noise in the range of (0-20) dB. **Fig.2** shows the CCOFDM is transmitted through an AWGN channel, in this * symbols are representing the noise add the signal and – represents original signal. At the receiving end extract the information bits by viterbi decoding.

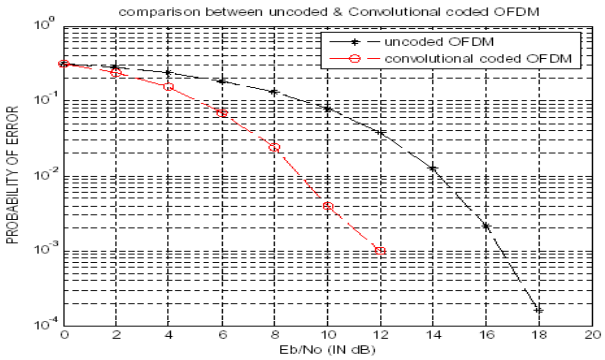


Figure 3. Performance analysis between uncoded and convolution coded OFDM system

According to the study [15] it is known that bursty errors can deteriorate the performance of any communication system. The burst errors can happen either by deep frequency fades or by impulsive noise. Power line channel suffers from both of these deficiencies. To improve the performance of OFDM system we can use FEC code. convolution code is good example of FEC code this result is shown below **Fig.3** Convolution coding in OFDM can give performance improvement of some 4 db on AWGN channel over the uncoded OFDM system at required BER .figure 1 shows convolutional codes with QPSK modulation give performance improvement of some 8dB over AWGN

channel gain at 10^{-2} for uncoded ofdm is 8dB and convolutional coded OFDM is 4.8dB.

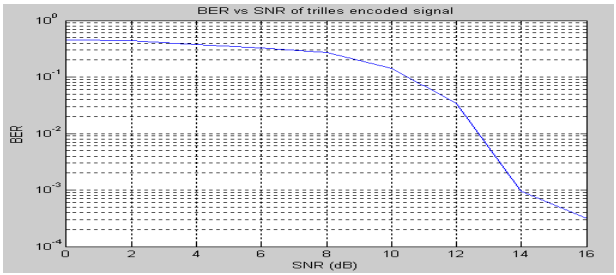


Figure 4. performance of CCOFDM over AWGN channel.

The Fig.4 the show the convolution coded OFDM system with total number frames are 100 each frame is generated by modulating 16-QAM, FFT size using 64-FFTand convolution code rate ½ .each frame consists of 96-bits and 4 pilots are used .the OFDM requires SNR of 8dB to achieve a BER of 10-2 , SNR of 10 db to achieve a BER o 10-3 .so by adding convolution code , the CCOFDM improves the system performance by 4dB.A comparison of uncoded and coded OFDM performance can be improved by 4dB. But coded OFDM requires memory .so that system complexity and computation is increases.

CONCLUSIONS

The performance analysis of the convolutional coded OFDM system is evaluated by simulations in AWGN channel. The advantages of using convolutional codes and OFDM are studied separately. It is shown that binary convolutional coded -OFDM can provide a better performance than single carrier Binary convolutional coded ofdm system in fading channels. On the other hand, convolutional codes can eliminate the residual inter symbol interference (ISI) and inter channel interference (ICI) and therefore reduce the length of the required Cyclic prefix in an OFDM system. This decreases the overhead associated with the Cyclic Prefix. The use of convolutional codes in OFDM system for high data rate transmission in wireless LANs, results in a considerable improvement in terms of bit error rate performance and bandwidth efficiency.

REFERENCES

[1] B.Balaji Naik ―Performance Of Turbo Coded OFDM In Wireless Application‖ in partial fulfillment of the requirements for the award of Master of Technology degree in Electronics and Communication Engineering with specialization in ―VLSI Design & Embedded system‖ during session 2007-2008 at National Institute Of Technology, Rourkela (Deemed University).

[2] I Gede Puja Astawa, Yoedy Moegiharto, Ahmad Zainudin, Imam Dui Agus Salim, Nur Annisa Anggraeni- Performance Analysis of MIMO-OFDM Using Convolution Codes with QAM Modulation in- International Journal of Electrical, Electronic Science and Engineering Vol:7 No:12, 2013 .

[3] Xu Zhang-QAM-based COFDM System in partial fulfillment of the requirements for the award of Master of Technology degree in Master of Science Degree in Electrical Engineering at University of Toledo in August 2011.

[4] Error Control Coding (2nd Edition) [Hardcover] by Shu Lin , Daniel J. Costell.

[5] Analog and Digital communication by sham shanmugam.

[6] contempory communication systems by – proiakis.

[7] Payaswini Pand Manjaiah D.H -ANALYSIS OF EFFECT OF CYCLIC PREFIX ON DATA RATES IN OFDM MODULATION TECHNIQUES International Journal of Advanced Computer and Mathematical Sciences ISSN 2230-9624. Vol 3, Issue 4, 2012.

[8] J.Faezah, and K.Sabira, "Adaptive Modulation for OFDM Systems" International Journal of Communication Ne tworks and Information Security (IJCNIS) Vol. 1, No. 2, August 2009 .

[9] Peters, S.W., Heath, R.W. "The future of WiMAX:Multihop relaying with IEEE 802.16j" IEEE Communication magazine vol. 47 issue 1, pp. 104-111. Jan 2009

[10] P. Van Eetvelt, G. Wade, and M. Tomlinson, "Peak to average power reduction for OFDM schemes by selective scrambling," Elect. Letter, October 1996, pp. 1963-1964.

[11] Ramjee Prasad, "OFDM for wireless communications systems" (2004), Artech House Inc. ISBN 1-58053-796-0

[12] T.Tsugi, M. Itami, "A study on adaptive modulation of OFDM under impulsive power line channel," IEEE International Symposium on Power Line Communications and Its Applications, ISPLC, pp. 304-309, 2-4 April 2008

[13] U. K. Kwon, G. H. Im, and E. S. Kim, "An iteration technique for recovering insufficient cyclic prefix and clipped OFDM signals," IEEE Signal Process. vol. 14, no. 5, pp. 317- 320, May 2007.

[14] Werner Henkel, George Taubock, Per Odling,Per Ola Borjesson, Niklas Petersson, Albin Johansson, "The Cyclic Prefix of OFDM/DMT – An Analysis", International Zurich Seminar on Broadband Communications access – transmission – Networking.

[15] Ms Neetu Sharma, Prof. Rajeshwar Lal Dua-" To improve Bit error Rate OFDM Transmission Using turbo codes."- International Journal of Advanced Research in Computer Engineering & Technology Volume 1, Issue 4, June 2012.

[16] Block Turbo Code And Its Application to OFDM For Wireless Local Area Network‖ Phd thesis submitted by Hrudananda Pradhan.

[17] C. Berrou, A. Glavieux, and P. Thitimajshima, ―Near Shannon Limit Error-Correcting Coding: Turbo Codes‖, Proceedings of the IEEE International Conference on Communications, ICC '93, Geneva., pp. 1064-1070, May 1993.

[18] D. Rajaveerappa, Abdelsalam Almarimi ―RSA/Shift Secured IFFT/FFT Based OFDM Wireless System‖ in 2009 Fifth International Conference on Information Assurance and Security.

Implementation of Digital Filters for the Removal of Artifacts from Electrocardiogram

P. Naga Malleswari
CVR College of Engineering /ECE, Hyderabad, India
Email: pinjalamalleswari@gmail.com.

Abstract— **In this paper various digital filters based algorithms that can be applied to ECG signal in order to remove artifacts from them are presented. Noises that commonly disturb the basic electrocardiogram are power line interference, instrumentation noise, external electromagnetic field interference, noise due to random body movements and respirational movements. These noises can be classified according to their frequency content. It is essential to reduce these disturbances in ECG signal to improve accuracy and reliability. Different types of adaptive and non-adaptive digital filters have been proposed to remove these noises. In this paper, window based FIR filters, adaptive filters and wavelet filter banks are applied to remove the artifacts. Performances of the filters are compared based on PSNR values.**

Index Terms— **ECG denoising, FIR filter, Adaptive filter, Wavelet Decomposition, PSNR.**

I. INTRODUCTION

The electrocardiogram (ECG) is a graphical representa-tion of the cardiac activity and it is widely used for the diagnosis of heart diseases [1]. In clinical environment during acquisition, the ECG signal encounters various types of artifacts. The predominant artifacts present in the ECG signal are Power-line Interference (PLI), Baseline Wander (BW), Muscle Artifacts (MA) and Motion Artifacts (EM). In this paper Power-line Interference is considered for PSNR simulations.

Power-line interference (PLI) is a significant source of noise during bio-potential measurements. It degrades the signal quality. In most existing PLI suppression methods, it is assumed that 1) the PLI is already present in the input ECG signal, 2) the number of harmonics is known (usually a single sinusoid), and 3) the frequencies of the narrow band harmonics or the statistics of them are known. But these assumptions are often unrealistic in real-world applications.It is essential to reduce disturbances in ECG signal and improve the accuracy and reliability for better diagnosis[1].

Different methods have been implemented to remove the artifacts from noisy ECG signal. The basic method is to pass the signal through static filters such as IIR, FIR and notch filters. In some cases these static filters also remove some important frequency components in the vicinity of cut off frequency. The static filters have fixed filter coefficients and it is very difficult to reduce the instrumentation noise with fixed filter coefficients, because the time varying behavior of this noise is not exactly known. To overcome the limitations of static filters, different adaptive filtering techniques have been developed. Adaptive filtering techniques are used for the processing and analysis of the ECG signals. Adaptive filters permit to detect time varying potentials and to track the dynamic variations of the signals. Some examples of dynamic filters are adaptive Kalman filter, wiener filter, modified extended Kalman filter etc. In this paper, various filters have been implemented for removal of artifacts in ECG. Their performances are also compared based on the PSNR values.

This paper is organized as follow: Section I gives the introduction of the ECG signal and power-line interference noise that affects the ECG. Section II explains ECG Denoising using non adaptive filter algorithms. Section III describes Denoising using adaptive filter algorithms with their equations of the related work. This section also explains the basic adaptive filter structure used for primitive LMS algorithm, which forms a base for all the other improved algorithms. Section IV explains the Wavelet based Denoising algorithms. Section V shows the simulation results and performance of the proposed techniques and at last section VI concludes the paper and followed by the references.

II. ECG DENOISING ALGORITHMS

For denoising purpose, the window based FIR filtering, adaptive filtering and wavelet filter bank based denoising are used.

A. FIR FILTERING

Digital filters are classified either as Finite Impulse Response (FIR) filters or Infinite Impulse response (IIR) filters, depending on the impulse response of the system. In the FIR system, the impulse response is of finite duration where as in the IIR system, the impulse response is of infinite duration. IIR filter structures are having feedback, that's why the present response of IIR

filter is a function of present and past values of the excitation as well as the past value of the output [5]. But the response of the FIR filter structures having no feedback so the response depends only on the present and past values of the input only.FIR filters are always stable, Exact linear phase, Can be realized efficiently in hardware. Due to the above advantages the design of FIR filters is preferred .

B. The Window Based FIR Filter Design

In this method, we start with the desired frequency response $H_d(\omega)$ and the corresponding unit sample response $h_d(n)$ is determined using inverse Fourier transform. The relation between $H_d(\omega)$ and $h_d(n)$ is as follows[7] :

$$H_d(\omega) = \sum_{n=0}^{\infty} h_d(n) e^{-j\omega n} \quad (1)$$

Where $h_d(n) = \int_{-\pi}^{\pi} H_d(\omega) e^{j\omega n}\, d\omega$ (2)

The impulse response $h_d(n)$ obtained from the Eq.(2) is of infinite duration. So, it is truncated at some point, say n = N - 1 to yield an FIR filter of length N (i.e. 0 to N-1). This truncation of $h_d(n)$ to length N - 1 is done by multiplying $h_d(n)$ with an window . Here the design is explained by considering the "rectangular window", defined as

$$w(n) = \begin{cases} 1 & n = 0,1,2.....N-1 \\ 0 & otherwise \end{cases} \quad (3)$$

Thus, the impulse response of the FIR filter becomes

$$h(n) = h_d(n)\, w(n) \quad (4)$$

$$h(n) = \begin{cases} h_d(n) & n = 0,1,2.....N-1 \\ 0 & otherwise \end{cases} \quad (5)$$

Design flexibility is very less and window method is basically useful for design of prototype filters like low pass, high pass, band pass, etc. This makes its applications very limited. Due to these reasons Adaptive filters are proposed.

III ADAPTIVE FILTERING AND ALGORITHMS

In this chapter we investigate performance of Adaptive filter and adaptive noise cancellation, system identification, frequency tracking and channel equalization[8]. Adaptive filtering involves the change of filter filter coefficients over time. It adapts to the change in signal characteristics in order to minimize the error. The general structure of an adaptive filter is shown in figure1.

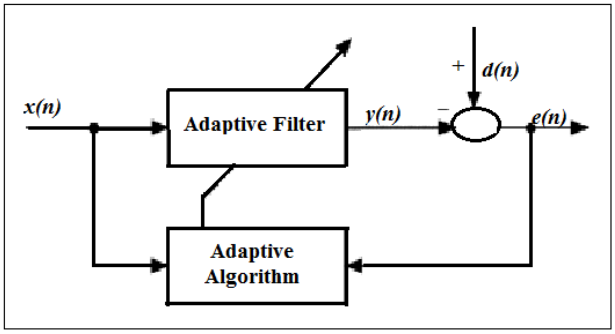


Figure 1: Adaptive filter structure

In figure1. $x(n)$ denotes the input signal. The vector representation of $x(n)$ is given by

$$x(n) = \left[x(n), x(n-1),.....x(n-N-1)\right]^T \quad (6)$$

This input signal is corrupted with noises. In other words, it is the sum of desired signal $d(n)$ and noise $v(n)$ i.e.

$$x(n) = d(n) + v(n) \quad (7)$$

The adaptive filter has a Finite Impulse Response (FIR) structure. For such structures, the impulse response is equal to the filter coefficients. The coefficients for a filter of order N are defined as

$$w(n) = \left[w_n(0), w_n(1),.....w_n(N-1)\right]^T \quad (8)$$

The output of the adaptive filter $y(n)$ is given by

$$y(n) = w(n)^T x(n) \quad (9)$$

The error signal is the difference between the desired and the estimated signal

$$e(n) = d(n) - y(n) \quad (10)$$

Moreover, the variable filter updates the filter coefficients at every time instant

$$w(n+1) = w(n) + \Delta w(n) \quad (11)$$

Where $\Delta w(n)$ is a correction factor for the filter coefficients. The adaptive algorithm generates this correction factor based on the input and error signals.

In adaptive filters, the weight vectors are updated by an adaptive algorithm to minimize the error function. The algorithms used for noise reduction in ECG in this thesis are least mean square (LMS), Normalized least mean square (NLMS), Sign data least mean square (SDLMS),Sign error least mean square (SELMS) and Sign-Sign least mean square (SSLMS) algorithms.

A. LMS algorithm

According to this LMS algorithm the updated weight is given by

$$w(n+1) = w(n) + 2.\mu.x(n).e(n) \quad (12)$$

Where μ is the step size.

B. NLMS algorithm

The NLMS algorithm is a modified form of the standard LMS algorithm. The NLMS algorithm updates the coefficients of an adaptive filter by using the equation

$$w(n+1) = w(n) + 2.\mu.\frac{x(n)}{\|x(n)\|^2}.e(n) \quad (13)$$

Eq. (13) can be rewritten as

$$w(n+1) = w(n) + 2.\mu(n).x(n).e(n) \quad (14)$$

Where $\mu(n) = \frac{\mu}{\|x(n)\|^2}$

From Eq. (12) and Eq.(14) the NLMS algorithm becomes the same as the standard LMS algorithm except that the NLMS algorithm has a time-varying step size $\mu(n)$. This step size improves the convergence speed of the adaptive filter.

C. SDLMS algorithm

In SDLMS algorithm, the sign function is applied to the input signal vector $x(n)$. This algorithm updates the coefficients of an adaptive filter using the equation.

$$w(n+1) = w(n) + 2.\mu.x(n).\text{sgn}(x(n)).e(n) \quad (15)$$

D. SELMS algorithm

In SELMS, the sign function is applied to the error signal *e(n)*. This algorithm updates the coefficients of an adaptive filter using the equation.

$$w(n+1) = w(n) + 2.\mu.x(n).\text{sgn}(e(n)) \quad (16)$$

E. SSLMS algorithm

Here, the sign function is applied to both *e*(*n*) and *x(n)*. This algorithm updates the coefficients of an adaptive filter using the equation

$$w(n+1) = w(n) + 2.\mu.\text{sgn}(x(n)).\text{sgn}(e(n)) \quad (17)$$

VI WAVELET DENOISING

The wavelet transform is similar to the Fourier transform. For the FFT, the basis functions are sines and cosines. For the wavelet transform, the basis functions are more complicated called wavelets, mother wavelets or analyzing wavelets and scaling function. In wavelet analysis, the signal is broken into shifted and scaled versions of the original (or *mother*) wavelet. Wavelet transform is suitable for multiresolution used for the analysis of non-stationary signals such as the ECG signal.

A. Wavelet Transform

If we take the Fourier transform over the whole time axis, we cannot tell at what instant a particular frequency rises. Short-time Fourier transform (STFT) uses a sliding window to find spectrogram, which gives the information of both time and frequency. But the length of window limits the resolution in frequency. To avoid this problem Wavelet transform is a good choice. Wavelet transforms (WT) are based on small wavelets with limited duration. In WT both the time and frequency resolutions vary in time-frequency plane in order to obtain a multiresolution analysis[9].

In wavelet transform, a signal x(t) can be written as

$$x(t) = \sum_k a_{j0,k}\varphi_{j0,k}(t) + \sum_{j=j0}^{\infty}\sum_k b_{j,k}\psi_{j,k}(t) \quad (18)$$

where *a*, *b* are the coefficients associated with $\varphi_{j,k}(t)$ and $\psi_{j,k}(t)$ respectively, and x(t) belongs to the square integrable subspace $L^2(R)$ is expressed in terms of scaling function $\varphi_{j,k}(t)$ and mother wavelet function $\psi_{j,k}(t)$.Here *j* is the parameter of dilation or the visibility in frequency and *k* is the parameter of the position.The coefficients *a*, *b* can be using the following equations (19) and (20).

$$a_{j0,k} = \int_{-\infty}^{\infty} x(t)\,\varphi_{j0,k}(t)\,dt \quad (19)$$

$$b_{j,k} = \int_{-\infty}^{\infty} x(t)\,\psi_{j,k}(t)\,dt \quad (20)$$

The scaling function $\varphi_{j,k}(t)$ can be expressed in equation (21)

$$\varphi_{j,k}(t) = 2^{j/2}\varphi(2^j t - k) \quad (21)$$

$\psi_{j,k}(t)$ can also be derived from its shifted version i.e. $\psi_{j,k}(2t)$. The expression of $\varphi_{j,k}(t)$ in terms of $\varphi_{j,k}(2t)$ will be

$$\varphi(t) = \sum_n h_\varphi(n)\sqrt{2}\,\varphi(2t-n) \quad (22)$$

In Eq. (22) *n* is the shifting parameter and $h_\varphi(n)$ are the coefficients.

The mother wavelet function $\psi_{j,k}(t)$ is expressed in equation (23) i.e.

$$\psi_{j,k}(t) = 2^{j/2}\psi(2^j t - k) \quad (23)$$

$\psi_{j,k}(t)$ can also be written using shifted version $\varphi_{j,k}(t)$ i.e. $\varphi_{j,k}(2t)$. The expression of $\psi_{j,k}(t)$ will be

$$\psi(t) = \sum_n h_\psi(n)\sqrt{2}\varphi(2t-n) \quad (24)$$

In Eq. (24) n is the shifting parameter and $h_\psi(n)$ are the coefficients.

B. Discrete Wavelet Transform

Discrete wavelet transform (DWT) decomposes the signal into mutually orthogonal set of wavelets. The scaling function $\varphi_{j,k}(n)$ and the mother wavelet function $\psi_{j,k}(n)$ in discrete domain are represented in equations (25) and (26).

$$\varphi_{j,n}(n) = 2^{j/2}\varphi(2^j n - k) \quad (25)$$

$$\psi_{j,n}(n) = 2^{j/2}\psi(2^j n - k) \quad (26)$$

The DWT of an discrete signal *x(n)* of length N-1 is given by

$$x(n) = \sum_k W_\varphi(j_0,k)\,\varphi_{j0,k}(n) + \sum_{j=j0}^{\infty}\sum_k W_\psi(j_0,k)\psi_{j,k}(n)$$

Here $W_\varphi(j_0,k)$ and $W_\psi(j_0,k)$ are called the wavelet coefficients.

$\varphi_{j,k}(n)$ and $\psi_{j,k}(n)$ are orthogonal to each other. Hence we can simply take the inner product to obtain the wavelet coefficients.

$$W_\varphi(j_0,k) = \frac{1}{\sqrt{M}}\sum_n x(n)\varphi_{j0,k}[n] \quad (27)$$

$$W_\psi(j,k) = \frac{1}{\sqrt{M}}\sum_n x(n)\psi_{j0,k}[n] \qquad j \geq j_0 \quad (28)$$

The coefficients $W_\varphi(j_0,k)$ in equation (27) are called the approximation coefficients and the coefficients $W_\psi(j_0,k)$ in equation (28)are called the detailed coefficient.The DWT can be realized in terms of high pass and low pass filters. The output of the low pass filter gives the approximation coefficients and the output of the high pass filter gives the detailed coefficients.

To get the filter coefficients $W_\varphi(j_0,k)$ and $W_\psi(j_0,k)$ can be rewritten as

$$W_\varphi(j,k) = \sum_n h_\varphi(n-2k)W_\varphi(j+1,m) \quad (29)$$

$$W_\psi(j,k) = \sum_m h_\psi(m-2k)W_\psi(j+1,m) \quad (30)$$

h_φ and h_ψ are the low pass filter and high pass filter coefficients in equations (29)and (30).

C. Wavelet Decomposition

The DWT decomposes the signal into approximate and detail information. Thus, it helps in analyzing the signal at different frequency bands with different resolutions[10].

1. Single stage wavelet filtering

Single stage wavelet filtering process is the most basic level. In this the original signal *x(n)* is passed through two complementary filters and emerges as two signals as shown in figure 2.

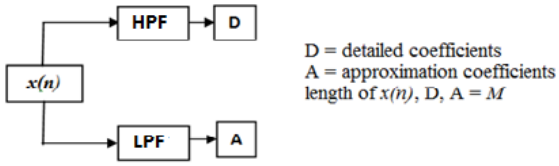


Figure 2: Single stage wavelet filtering

The original signal *x(n)* consists of *M* samples of data. If we apply single stage wavelet filter the resulting approximation and detail coefficients are each of length *M*, for a total of *2M*. There exists an alternative method to perform the decomposition using wavelets. By down sampling A and D to half of their lengths i.e. *M/2*, the total length of resulting signal can be maintained. The final output signals after down sampling are denoted as cA and cD. It is shown in figure 3.

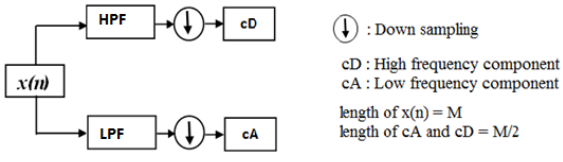


Figure3: Single stage wavelet filtering with down sampling

2 . Multistage wavelet filtering

In this wavelet decomposition process one signal is broken down into many lower resolution components. This is called the wavelet decomposition tree.

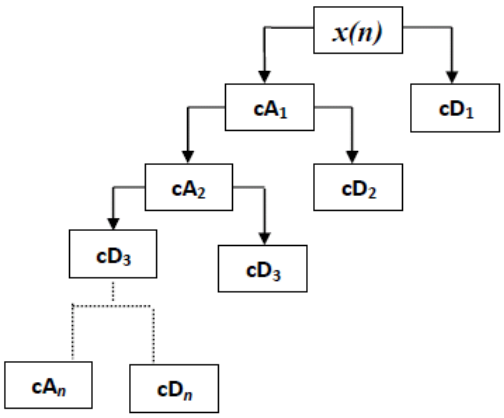


Figure 4:.Multistage Wavelet Decomposition tree.

Multistage wavelet filtering analysis process is iterative, theoretically it can be continued till infinite levels. Ideally the decomposition can be done only until the individual details consist of a single sample. In practice, a suitable number of decomposition levels based on the nature and frequency component of the signal.

3. Wavelet Reconstruction

After decomposition, the task is to again reconstruct the original signal without loss of important information. This process is called *reconstruction*, or *synthesis*. The synthesis is done mathematically by using the inverse discrete wavelet transform (IDWT).

In wavelet analysis, filtering and followed by down sampling are involved. But the wavelet reconstruction process consists of up sampling followed by filtering. Up sampling is the process of lengthening a signal component by inserting zeros between samples.

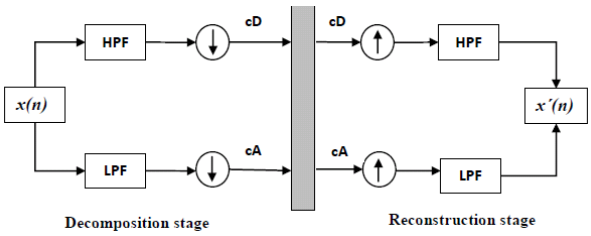


Figure 5: Single stage decomposition and reconstruction.

We combine cA and cD by IDWT to get the reconstructed original signal. For multiple level reconstruction, the single stage reconstruction technique is iterated to reassemble the original signal.

D. ECG Denoising Using Wavelet Transform

In this method, the corrupted ECG signal *x(n)* is denoised by taking the DWT of raw and noisy ECG signal. A family of the mother wavelet is available having the energy spectrum concentrated around the low frequencies like the ECG signal as well as better resembling the QRS complex of the ECG signal. We have used *symlet* wavelet, which resembles the ECG wave.

In discrete wavelet transform (DWT), the low and high frequency components in *x(n)* is analyzed by passing it through a series of low-pass and high-pass filters with different cut-off frequencies. This process results in a set of approximate coefficients (cA) and detail coefficients (cD). To remove the power line interference and the high frequency noise, the DWT is computed to level 4 using *symlet8* mother wavelet function and scaling function. Then the approximate coefficients at level 4 (cA4) are set to zero. After that, inverse wavelet transform (IDWT) of the modified coefficients are taken to obtain the approximate noise of the ECG signal. The residue of the raw signal and the approximate noise is obtained to get noise free ECG signal.

V. Simulation Results

All the simulation results are obtained by using MATLAB.The ECG waveform taken from MIT-BIH database, generated noises and the corrupted ECG signal are also shown.

A. ECG WAVEFORM

All the simulations shown in the later parts are carried out with data no. 100 of MIT-BIH arrhythmia database. The ECG waveform is shown in figure 6.

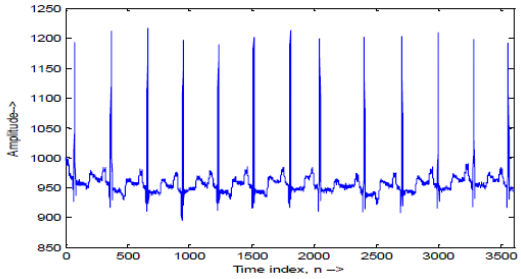


Figure 6: ECG signal

B. GENERATION OF NOISES

The artifacts in ECG can be categorized according to their frequency content. The low frequency noise (electrode contact noise and motion artifact) has frequency less than 1 Hz, high frequency noise (EMG noise) whose frequency is more than 100 Hz and power line interference of frequency 50 Hz or 60 Hz (depending on the supply). These noises are generated in MATLAB based on their frequency content.

1. Generation of Low Frequency Noise (Base Line Wander)

We generated the baseline drift by adding two sine waves of frequency 0.1 Hz and 0.02 Hz and Triangular wave of 0.05Hz which is shown in figure 7.

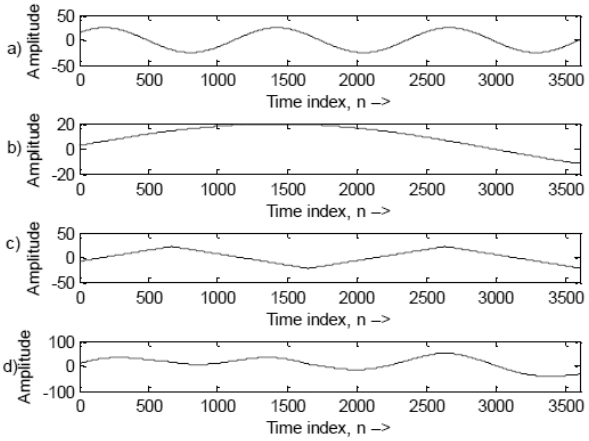


Figure 7: (a) Sine wave of frequency 0.1Hz (b)Sine wave of frequency 0.02Hz (c) Triangular wave of frequency 0.05Hz (d) base line wander.

2. *Generation of High Frequency Noise*

High frequency noise is generated by multiplying sine wave of 150 Hz frequency with a random signal. The generated high frequency noise is shown in figure 8.

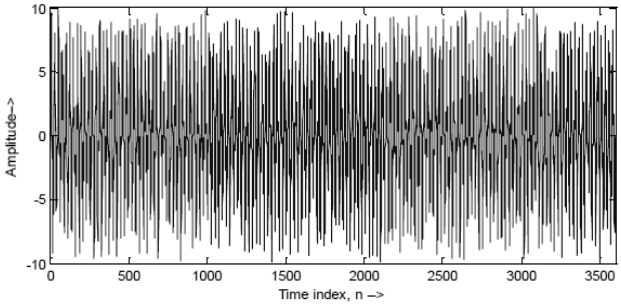


Figure 8: High Frequency Noise.

3. Generation of Power Line Interference

Here the 50 Hz power supply is considered. So, a sine wave of 50 Hz amplitude was taken to represent the power line interference. The resulted power line interference is shown in figure 9.

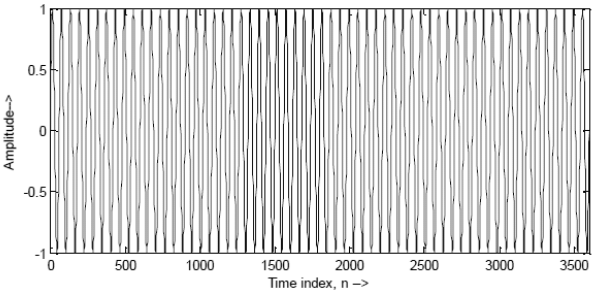


Figure 9: Power line interference

4. ADDITION OF NOISES TO ECG

The noise signals generated are added with the ECG signal to get the corrupted ECG. figure. 10 shows the corrupted ECG.

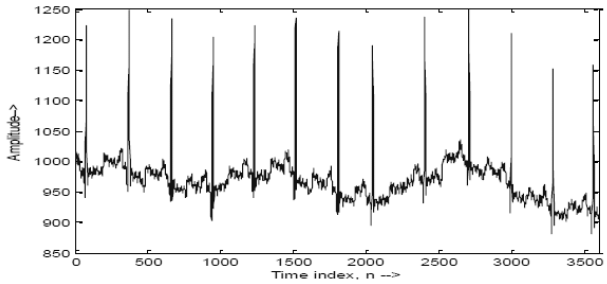


Figure 10: Corrupted ECG Signal

C. RESULTS OF WINDOW BASED FIR FILTERING

We designed FIR filters of order 100.Rectangular window based FIR filter gives the response with sharp attenuation and pulsation in the stop band. In the pass band, the filter was found to be stable. The Hamming, Hanning and the Blackman windows do not have a sharp cut-off like the Rectangular window. Using these windows, we designed the high pass filter of cut-off frequency 3 Hz and the low pass filter of cut-off frequency 100Hz. figure. 11, 12, 13, 14 show the filtered ECG signal by passing through the FIR filter based on Rectangular window, Hamming window, Hanning window and Blackman window respectively.

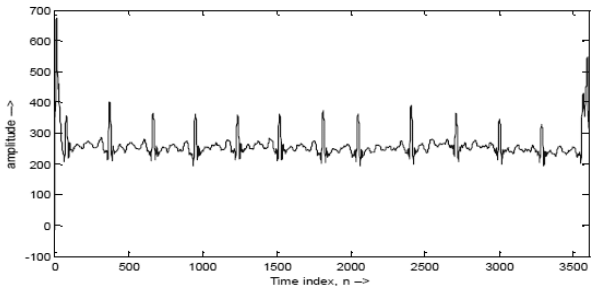


Figure 11: ECG signal after passing through FIR filter with Rectangular Window.

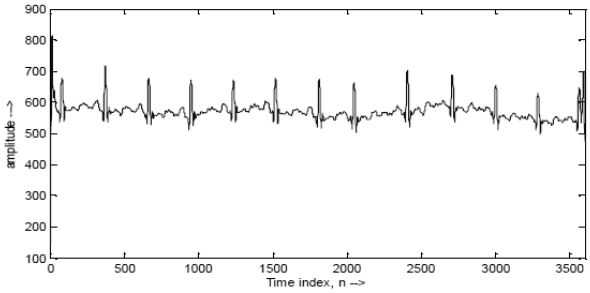


Figure 12: ECG signal after passing through FIR filter with Hamming window

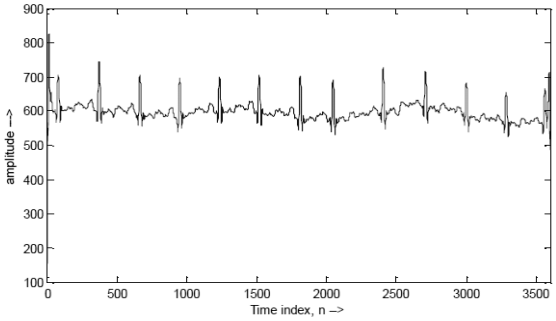


Figure 13: ECG signal after passing through FIR filter with Hanning window

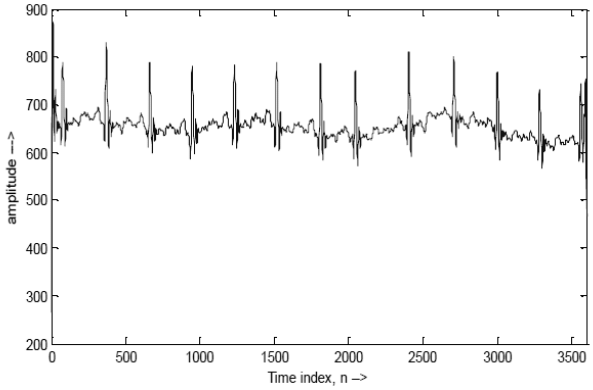


Figure 14: ECG signal after passing through FIR filter with Blackman window.

To evaluate the performance of all these filters PSNR values are calculated which is listed in the Table 1.

TABLE I
PSNR COMPARISION OF WINDOW BASED FIR FILTERS

Window Type	PSNR(dB)
Rectangular	21.13
Hanning	18.65
Hamming	18.90
Blackman	18.00

The Table1. shows the performance of rectangular window based filter is better than the rest window based filters because the rectangular filter has sharp attenuation and pulsation present in the stop band. The phase response of rectangular window based filter is linear and the filter is also stable.

D. RESULTS OF ADAPTIVE FILTERING

The corrupted ECG signal shown in Figure10. is passed through the adaptive filters. Figure. 15, 16, 17,18 and 19 show the filtered output and the error plot of the adaptive filters using LMS, NLMS, SDLMS, SELMS, SSLMS algorithms respectively.

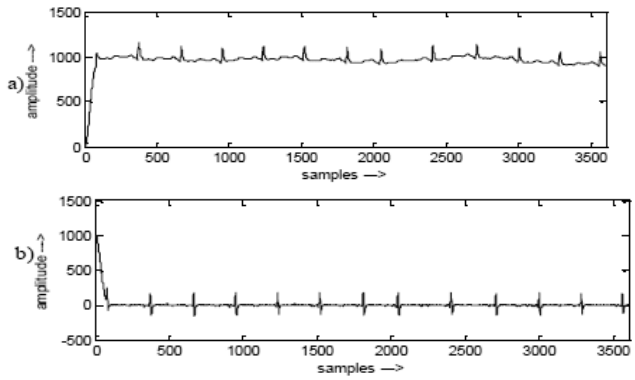


Figure 15: (a) ECG signal after passing through LMS based filter (b) Error plot after passing through LMS based adaptive filter

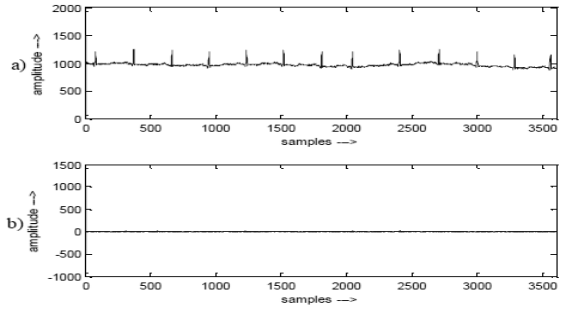


Figure 16: (a) ECG signal after passing through NLMS based filter (b) Error plot after passing through NLMS based adaptive filter

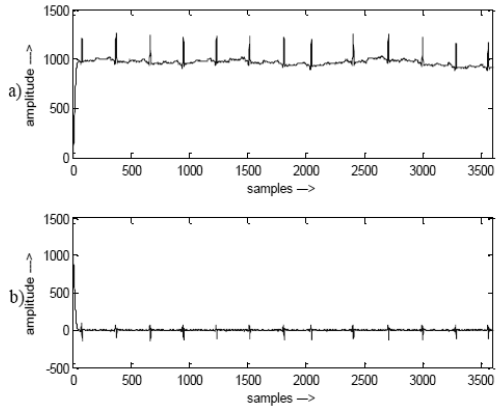


Figure 17: (a) ECG signal after passing through SDLMS based filter (b) Error plot after passing through SDLMS based adaptive filter

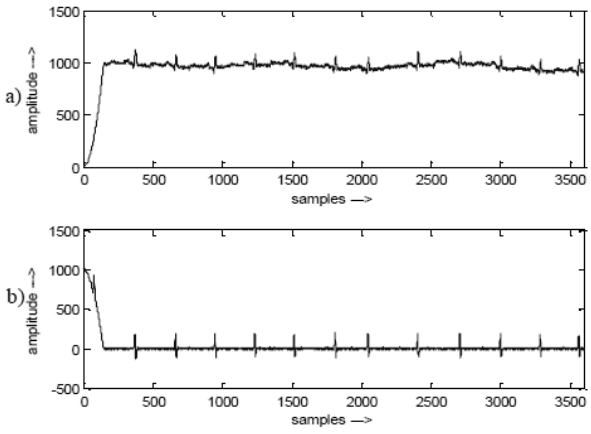


Figure18: a) ECG signal after passing through SELMS based filter (b) Error plot after passing through SELMS based adaptive filter

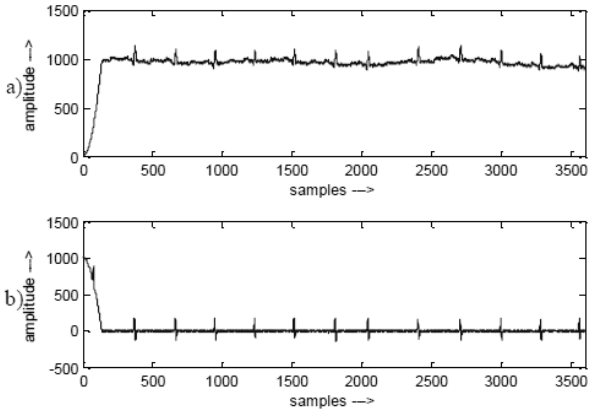


Figure 19: (a) ECG signal after passing through SSLMS based filter (b) Error plot after passing through SSLMS based adaptive filter

All the simulations shown in the above figures are carried out with data no. 100 of MIT-BIH arrhythmia database[3]. To have a comparison of these adaptive filters, the PSNR values are calculated with ECG data 105 and 108 of the database. PSNR values of different adaptive filters are shown in Table 2.

TABLE II
PSNR VALUES OF VARIOUS ADAPTIVE FILTERS

Data No.	LMS	NLMS	SDLMS	SELMS	SSLMS
100	35.58	38.24	37.29	34.63	31.34
105	35.10	37.46	35.22	34.16	32.54
108	32.42	35.36	31.82	31.85	32.53
average	34.37	37.01	34.78	33.54	32.12

The Table 2. Shows the comparative analysis of the PSNR values, The NLMS based adaptive filter gives the better result among all . In case of SDLMS, SELMS and SSLMS based adaptive filters, the computational complexity is decreased at the cost of lower PSNR values. So, NLMS algorithm is preferred when better performance is required. Sign based adaptive algorithms are chosen when faster performance is needed.

E. RESULTS OF WAVELET FILTER BANK BASED DENOISING

For wavelet filter bank based denoising, we have only considered the high frequency noise and the power line interference shown in Figure. 8 and figure 9. These noises are added to the ECG signal shown in Figure.6. After adding the noises, the corrupted ECG signal is shown in figure 20.

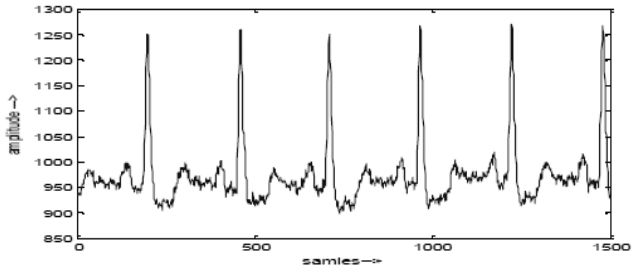


Figure 20:Noisy ECG signal used in wavelet filter bank based denoising

The noisy signal shown in figure 19. is denoised by using discrete wavelet transform. For this, we have chosen *symlet8* wavelet because it has energy spectrum concentrated around the low frequencies like the ECG signal. The *symlet8* wavelet also resembles the QRS complex of the ECG signal. The scaling function φ and wavelet function ψ are shown in figure 21. and figure 22.

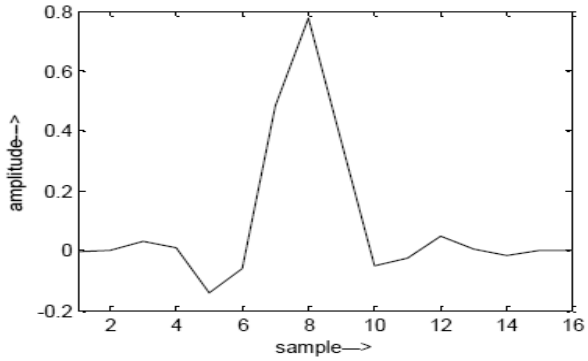


Figure 21:Symlet scaling function φ

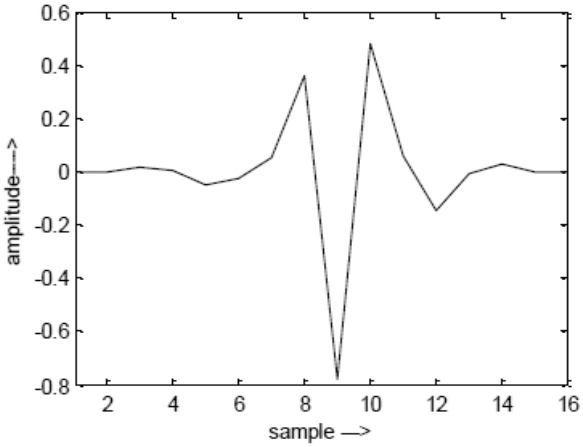


Figure 22:Symlet wavelet function ψ

To remove the power line interference and the high frequency noise, the DWT is computed to level 4 using *symlet8* mother wavelet function and scaling function. The approximate coefficients cAn and cDn at each decomposition level are shown in figure 23. and figure 24. respectively.

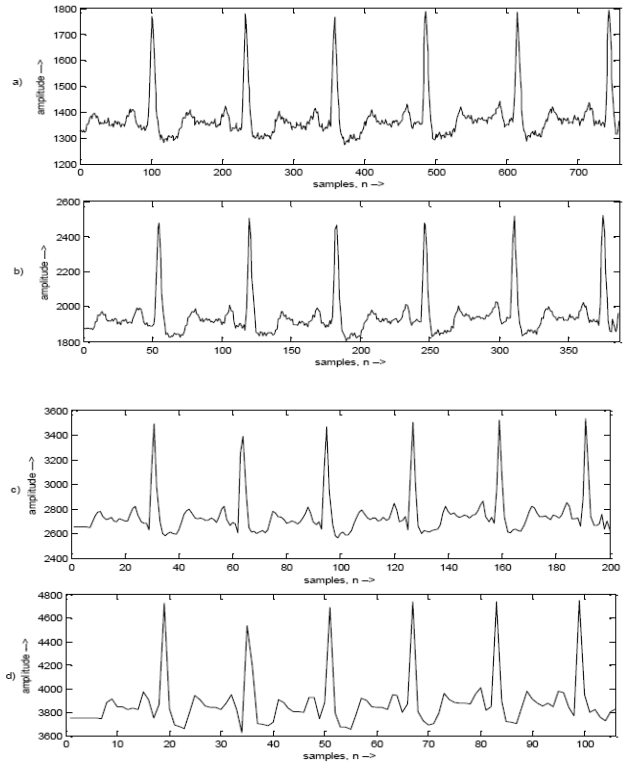


Figure 23:Approximation coefficients at level 1,2,3and 4

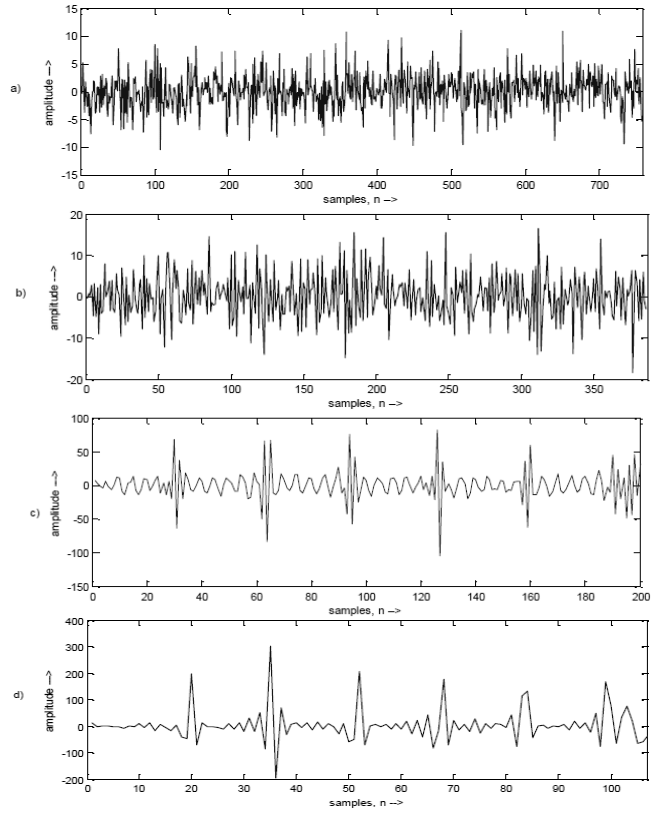


Figure 24:Detailed coefficients at level 1,2,3 and 4.

Then the approximate coefficients at level 4 (cA4) are set to zero. After that, inverse wavelet transform (IDWT) of the modified coefficients are taken to obtain the approximate noise of the ECG signal. The approximated noise signal is shown in figure 25. The residue of the raw signal and the approximate noise is obtained to get noise free ECG signal. The denoised ECG signal is given in figure 26.

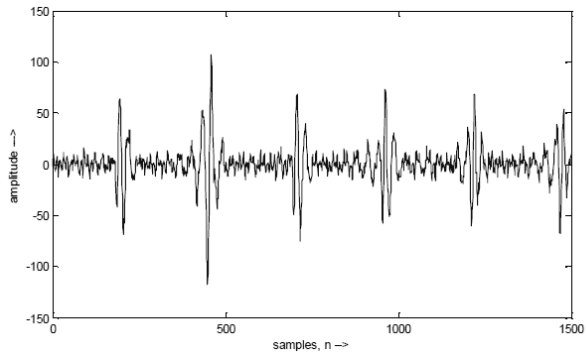


Figure 25: Approximated noise

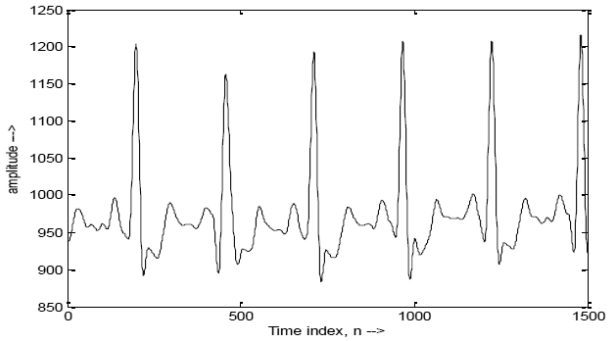


Figure 26:Denoised ECG using wavelet filter bank

CONCLUSIONS

In this thesis we designed and investigated the performance of various Adaptive and Non adaptive filters to remove the artifacts from ECG signal. All the filters are compared with the PSNR values. For the simulations, the ECG signals are taken from the MIT-BIH data base. The later part of the thesis deals with all the filtering algorithms that are used and the simulation results. The filtering algorithms used in this thesis are window based FIR filtering, adaptive filtering and wavelet filter bank technique.

In first algorithm the Rectangular window based FIR filter gives sharp attenuation and pulsation present in the stop band. The phase response of Rectangular window based filter is linear and the filter is also stable. The second algorithm analyses the performance of different adaptive filters for ECG denoising. In NLMS based adaptive filter, the step size is greater than LMS algorithm and hence the convergence is faster. NLMS based adaptive filter offers better performance than the LMS counterpart. The computational complexity of NLMS is slightly higher. In all the sign LMS algorithms, the computation is faster. So,NLMS algorithm is preferred when better performance is required.

To remove the power line interference and the high frequency noise, the DWT is computed to level 4 using

symlet8 mother wavelet function and scaling function. Then the approximate coefficients at level 4 (cA4) are set to zero. After that, inverse wavelet transform (IDWT) of the modified coefficients are taken to obtain the approximate noise of the ECG signal. The residue of the raw signal and the approximate noise is obtained to get noise free ECG signal. This method removes noise from the ECG signal without any distortion of the ECG signal features.

FUTURE WORK

In this thesis , the window based FIR and LMS algorithm based adaptive filters remove the high frequency, power line interference and low frequency noises. In wavelet filter bank based denoising, only high frequency noise and power line interference are removed. The future developments to this work can be made as follows : 1) Use of other adaptive methods like FT-RLS, QRD-RLS algorithms for ECG denoising. 2) Implementation of wavelet based denoising for the removal of base line wander.

REFERENCES

[1] Syed AteequrRehman,R.Ranjith Kumar "Performance Comparison of Adaptive Filter Algorithms for ECG Signal Enhancement", *International Journal of Advanced Research in Computer and Communication Engineering Vol. 1, Issue 2, April 2012*

[2] M. Popescu, P. Cristea and A. Bezerianos, "High resolution ECG filtering using adaptive BSayesian wavelet shrinkage", *Proceedings of International conference on Computers in Cardiology*, pp. 401–404, Cleveland, OH, September 1998.

[3] http://www.physionet.org/physiobank/database/mitdb/ MIT-BIH Database distribution, Massachusetts Institute of Technology, 77 Massachusetts Avenue, Cambridge.

[4] R.G. Mark, P.S. Schluter, G.B. Moody, P.H. Devlin and D. Chernoff, "An annotated ECG database for evaluating arrhythmia detectors", *IEEE Transactions on Biomedical Engineering*, vol. 29, no. 8, pp. 600,1982.

[5] Carson K. S. Pun, S. C. Chan, K. S. Yeung, and K. L. Ho, On the design and implementation of FIR and IIR digital filters with variable frequency characteristics, *IEEE transactions on circuits and systems-II: analog and digital signal processing*, vol. 49, no. 11, pp. 689 – 703, November 2002.

[6] John G. Proakis and Dimitris G. Manolakis, "Digital signal processing: Principles, algorithms, and applications" , 4th edition, 2007, *Pearson education*, ISBN: 978-81-317-1000-5.

[7] Kangshun Li and Yuan Liu, "The FIR window function design based on evolutionary algorithm", *Proceedings of International Conference on Mechatronic Science, Electric Engineering and Computer (MEC)*, pp. 1797 – 1800, Jilin, China , August 2011

[8] Paulo S.R. Diniz, "Adaptive Filtering Algorithms and Practical Implementation", Springer ,3rd edition, 2008, ISBN 978-0-387-31274-3

[9] Mahmoodabadi and S. Ahmadian, "ECG feature extraction based on multiresolution wavelet transform", *Proceedings of the IEEE 27th Annual Conference on Engineering in Medicine and Biology*, pp. 3902–3905, Shanghai, China, January 2005.

[10] O. Rioul and M. Vetterli, "Wavelets and signal processing" , *IEEE Signal Processing Magazine*, vol. 8, no. 4, pp. 14–38, August 1991.

Simplified LS and Modified MMSE Estimators for Channel Estimation of OFDM

B. Janardhana Rao[1] and O. Venkata Krishna [2]
[1] CVR College of Engineering/ECE, Hyderabad, India
Email: janardhan.bitra@gmail.com
[2] CVR College of Engineering/EIE, Hyderabad, India
Email: venkatakrishna.odugu@gmail.com

***Abstract*— In this paper we investigate the block-type pilot channel estimation for orthogonal frequency division multiplexing (OFDM) systems. The estimation is based on the minimum mean square error (MMSE) estimator and the least square (LS) estimator. We derive the MMSE and LS estimators' architecture and investigate their performances. We prove that the MMSE estimator performance is better but computational complexity is high, contrary the LS estimator has low complexity but poor performance. For reducing complexity we proposed two different solutions which are the Simplified Least Square (SLS) estimator and the modified MMSE estimator. In the SLS estimator, we apply an auto-correlation function with the LS estimator to remove the noise. In the modified MMSE estimator, we consider only the significant energy samples and ignore the remaining noisy samples. Based on this idea we introduce the modified MMSE estimator. We evaluate estimator's performance on basis of mean square error and symbol error rate for 16 QAM systems using MATLAB.**

***Index Terms*— Channel Estimation, OFDM, LS Estimator, MMSE Estimator, SLS estimator**

I. INTRODUCTION

Orthogonal Frequency Division Multiplexing (OFDM) is one of the most widely used modulation technique for high-bit-rate wireless communication. Especially the wireless local area network systems such as WiMax, WiBro, WiFi and the emerging fourth-generation mobile systems are used OFDM as the core modulation technique. Wireless communication systems use two different signaling schemes which are: coherent and general signaling schemes. Quadrature Amplitude Modulation (QAM) which is Coherent signaling scheme requires channel estimation and tracking of the fading channel.

In OFDM system, the channel is usually assumed to have a finite impulse response. To avoid the inter-symbol interference, a cyclic extension is put between the consecutive blocks, where the cyclic extension length is longer than the channel impulse response. Decision-directed and pilot–symbol-aided methods are two different ways for channel estimation. Pilot-symbol-aided channel estimation can be further divided in two types: block type-pilot channel estimation and comb-type-pilot channel estimation. All sub-carriers are reserved for the pilot within a specific period in block-type-pilot method. The estimation of the channel can be based on Least Square (LS) or on Minimum Mean Square Error (MMSE)
in this method. In the comb-type-pilot method, one sub-carrier is reserved as a pilot for each symbol. The estimation of the channel for the comb-type-pilot arrangement can be based on linear interpolation, second order interpolation, low-pass interpolation or on time domain interpolation.

The MMSE estimator performance is good but its complexity is high. Contrary the LS estimator complexity is low but its performance is poor [1]. For reducing complexity of the both estimators we proposed two different algorithms which reduce complexity without compromise in performance or with slightly lower performance.

II. OFDM SYSTEM DESCRIPTION

The basic idea underlying OFDM systems is the division of the available frequency spectrum into several subcarriers, converting a frequency-selective channel into a parallel collection of frequency at sub channels [2]. To obtain a high spectral efficiency, the signal spectra corresponding to the different subcarriers overlap in frequency, and yet they have the minimum frequency separation to maintain orthogonality of their corresponding time domain waveforms [3]. To preserve the orthogonality of the tones and eliminates ISI between consecutive OFDM symbols here we use Cyclic Prefix (CP). A block diagram of a baseband OFDM system is shown in Figure 1.

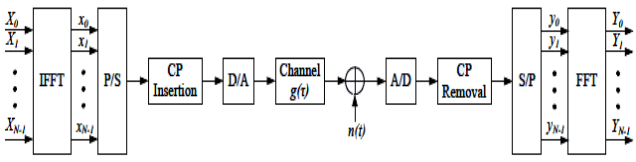


Figure 1: Baseband OFDM

After the information bits are grouped, coded and modulated, they are fed into N-point inverse fast Fourier transform (IFFT) to obtain the time domain OFDM symbols, i.e.,

$$x_n = IFFT_N\{X_K\} = \sum_{K=0}^{N-1} X_K e^{j2\pi Kn/N}, 0 \le n, K \le N-1 \quad \text{--- (1)}$$

, where n is the time domain sampling index, X_K is the data at kth subcarrier, and N is the total number of subcarriers. Following IFFT block, a cyclic extension of time length, T_G, chosen to be larger than the expected maximum delay spread of the channel [5], is inserted to avoid intersymbol and intercarrier interferences. The digital-to-analog (D/A) converter contains low-pass filters with bandwidth $1/T_S$, where T_S is the sampling interval or an OFDM symbol period. The channel is modeled as an impulse response, g(τ), followed by the complex additive white Gaussian noise (AWGN), n(t) [6].

$$g(\tau) = \sum_{m=0}^{M-1} \alpha_m \delta(\tau - \tau_m T_s) \quad \text{---------- (2)}$$

, where M is the number of multipaths, α_m is the m th path gain in complex, and τ_m is the corresponding path delay. The N-point FFT is used to transform the data back to frequency domain At the receiver, after passing through the analog-to-digital (A/D) and removing CP. Finally, the information bits are obtained after the channel equalization/decoding, and demodulation.

Under the assumption that the use of a CP preserves the orthogonality of the tones and the entire impulse response lies inside the guard interval, i.e., $0 \le \tau_m Ts \le T_G$ [7, 9], we can describe the received signals as

$$Y = FFT_N\{IFFT_N\{X\} \otimes g + \tilde{n}\} \quad \text{---------- (3)}$$

, where $Y = [Y_0\ Y_1 \ldots\ldots Y_{N-1}]^T$ is the received vector, $X = [X_0\ X_1 \ldots\ldots X_{N-1}]^T$ is a vector of the transmitted signal, and $g = [g_0\ g_1\ \ldots..g_{N-1}]^T$ and $\tilde{n} = [\tilde{n}_0\ \tilde{n}_1\ \ldots.\ \tilde{n}_{N-1}]^T$ are the sampled frequency response of g(τ) and AWGN, respectively. Note that both Y and X are frequency domain data. In fact, the expression in equation (3) is equivalent to a transmission of data over a set of parallel Gaussian channels [8], as shown in Figure 2.

Therefore, the system described by equation (3) can be written as

$$Y = XF_g + F\tilde{n} \quad \text{---------- (4)}$$

, where X is a diagonal matrix containing the elements of X in equation (3), and

$$\boldsymbol{F} = \begin{bmatrix} W_N^{00} & \cdots & W_N^{0(N-1)} \\ \vdots & \ddots & \vdots \\ W_N^{(N-1)0} & \cdots & W_N^{(N-1)(N-1)} \end{bmatrix}$$

is the FFT matrix with

$$W_N^{nk} = \frac{1}{\sqrt{N}} e^{-j2\pi \frac{nk}{N}}$$

Also, let $h = FFT_N\{g\} = Fg$ and $n = FFT_N\{\tilde{n}\} = F\tilde{n}$. Thus, equation (4) now becomes

$$Y = Xh + n \quad \text{--------- (5)}$$

we assume that the noise n is a vector of independent identically distributed complex zero-mean Gaussian noise with variance σ_n^2. We also assume that n is uncorrelated with the channel h.

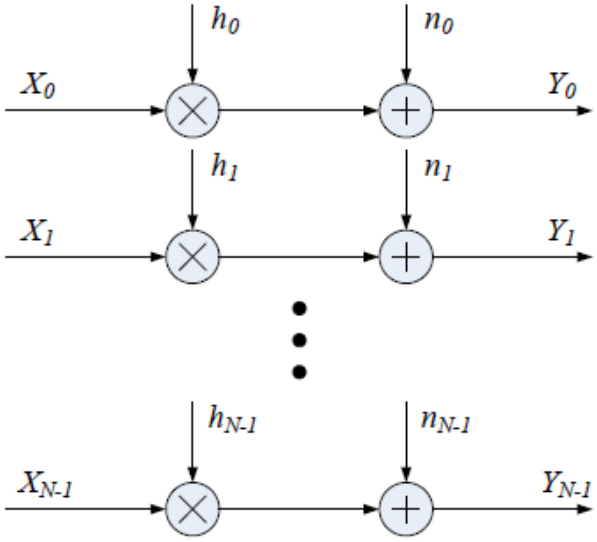


Figure 2: The OFDM system, modeled as parallel Gaussian channels

III. CHANNEL ESTIMATION TECHNIQUES

A. MMSE Estimator

The major rule of MMSE estimator is to efficiently estimate the channel to minimize the MSE or SER of the channel. In equation (5), R_{gg} and R_{yy} denote as the auto-covariance matrix of $\boldsymbol{g}$ and $\boldsymbol{y}$ respectively, where $\boldsymbol{g}$ is the channel energy and $\boldsymbol{y}$ is the received signal. Moreover, the cross covariance of $\boldsymbol{g}$ and $\boldsymbol{y}$ is denoted by R_{gy} and the noise variance $E\{|n|^2\}$ is denoted by δ_n^2. The channel estimation by using MMSE estimator g_{MMSE} can be derived as follows:

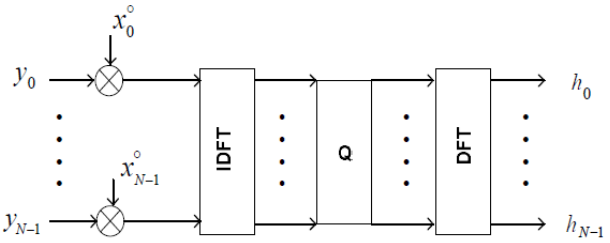


Figure 3: Block diagram of channel estimator

$$g_{MMSE} = R_{gy} R_{yy}^{-1} y \quad \text{--------- (6)}$$

Where,

$$R_{gy} = E\{gy^H\} = R_{gg} F^H x^H \quad \text{------- (7)}$$

$$R_{yy} = E\{yy^H\} = xFR_{gg} F^H x^H + \delta_n^2 I_n \quad \text{------- (8)}$$

The columns in ***F*** are orthogonal and ***I*** is the identity matrix. From Figure 3, the channel impulse response h_{MMSE} is as fallows

$$h_{MMSE} = Fg_{MMSE} = FQ_{MMSE} F^H x^H y \quad \text{-------} \quad (9)$$

Where,

$$Q_{MMSE} = R_{gg}[(F^H x^H xF)\delta_n^2 + R]^{-1}(F^H x^H Fx)^{-1} \text{- (10)}$$

h_{MMSE} is the channel attenuation for MMSE estimator, g_{MMSE} is the channel energy, ***y*** is received signal, ***x*** is the transmitted signal and ***F*** is the DFT matrix [2].

B. LS Estimator

The LS estimator has lower computational complexity than MMSE. The LS estimator for the cyclic impulse response ***g*** minimizes $(yxFg)(y - xFg)^H$ and generates the channel attenuation as bellow

$$h_{LS} = FQ_{LS} F^H x^H y \quad \text{----------} \quad (11)$$

Here,

$$Q_{LS} = (F^H x^H Fx)^{-1} \quad \text{----------} \quad (12)$$

and $(y - xFg)^H$ are the conjugate transpose operations. So, the lest square h_{LS} can be written as

$$h_{LS} = x^{-1} y \quad \text{----------} \quad (13)$$

Where, the least square h_{LS} is the channel attenuation for LS. Equations (9) and (13) are the general expressions for MMSE and LS estimators respectively. The performances of the estimators are evaluated using Mean square error and symbol error rate.

C. Mean Square Error (MSE)

The mean square error or MSE of an estimator is one of many ways to quantify the difference between the theoretical values of an estimator and the true value of the quantity being estimated. MSE measures the average of the square of the error. The error is the amount by which the estimator differs from the quantity to be estimated. We define the mean square error as [10]

$$meansquarerror = mean\{abs(H) - abs(h_{estimator})\}^2$$

---------- (14)

Where, ***H*** is theoretical transfer function and $h_{estimator}$ is the calculated transfer function for each estimator.

D. Symbol Error Rate (SER)

Symbol rate is the number of symbol changes made to the transmission medium per second using a digitally modulated signal. Symbol error rate for 16-QAM system is [11]

$$P_{S,16-QAM} = \frac{3}{2} erfc\left(\sqrt{\frac{E_S}{10N_0}}\right) \quad \text{----------} \quad (15)$$

Where, $erfc$ denoted complementary error function, E_S denoted signal energy and N_0 denoted bit rate.

Both estimators have some drawbacks. However the MMSE estimator performance is better but computational complexity is high, contrary the LS estimator has high mean-square error means least performance but its computational complexity is very low [2]. For reducing computational complexity and improve performance, we proposed two channel estimation approaches.

IV. MODEL OF THE PROPOSED ESTIMATOR

A. System Structure for SLS Estimator

The LS estimator has least performance with high mean square error. For improving the performance and to reduce the computation complexity, we proposed the following SLS estimator.

Equation (12) can be rewrite like this

$$h_{LS} = h + n \quad \text{----------} \quad (16)$$

Here

$$h = Fg \quad \text{----------} \quad (17)$$

h is the transfer function, n is the Gaussian noise, ***F*** is the DFT matrix, g is the channel impulse response in time domain. From equation (16), the LS estimator consists of channel transfer function plus some noise. Due to noise part the LS estimator gives the poor performance. The noise from the original signal has to remove to improve the performance. The LS estimation is noisy observation of the channel attenuation which can be smoother using some auto-correlation operation with the channel attenuation h_{LS}. If the channel transfer function is h, the received signal y and the transmitted symbol x, then the SLS channel estimator will be:

$$h_{SLS} = W_x h_{LS} \quad \text{----------} \quad (18)$$

where, W_x is weighted matrix and

$$W_x = R_{hh}(R_{hh} + \sigma_n^2 (xx^H)^{-1})^{-1} \quad \text{----------} \quad (19)$$

$$R_{hh} = E\{hh^H\} \quad \text{----------} \quad (20)$$

where, R_{hh} is the auto-covariance matrix of h. The weighting matrix W_x of size $N \times N$ depends on the transmitted signal $\boldsymbol{x}$. As a step towards the low-complexity estimators we want to find a weighting matrix which does not depend on the transmitted signal x. The weighting matrix can be obtained from the auto-covariance matrix of h and auto-correlation of transmitted signal x. Consider that the transmitted signal x to be stochastic with independent and uniformly distributed constellation points. In that case the auto-covariance matrix of noise becomes

$$R_{nn} = \frac{\alpha}{SNR} I \quad \text{----------} \quad (21)$$

where, α is constellation factor and $E\{|X_i|^2\}E\{1/|X_i|^2\}$ is the mathematical expression of α. The value of α is $\frac{17}{6}$ for 16-QAM. SNR is a per-symbol signal-to-noise ratio equal to $E\{|X_i|^2\}/\delta_n^2$. Then the SLS estimator becomes

$$h_{SLS} = W_{\mathrm{mod}\,ified} h_{LS} \quad \text{----------} \quad (22)$$

where the modified weighting matrix is give by

$$W_{\mathrm{mod}\,ified} = R_{hh}(R_{hh} + R_{nn})^{-1} \quad \text{----------} \quad (23)$$

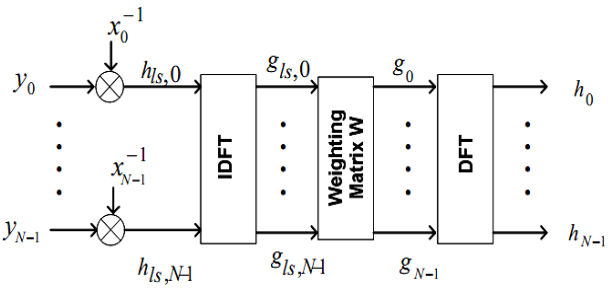


Figure 4: Block diagram for SLS estimator

Figure 4 shows the block diagram of h_{SLS} estimator. x_n represents the input signal start from 0 to N, y_n is the output from 0 to N sample, g_n is the channel impulse response in the time domain from 0 to N samples and h_n is the channel transfer function in the frequency domain.

B. System Structure for Modified MMSE

The modified estimator is based on MMSE estimator. According to equation (2), most of the channel energy $\boldsymbol{g}$ is contained in or near to the first (L+1) samples, where L is $\left\lceil \frac{T_G}{T_S} \right\rceil N$, where T_G is the cyclic extension of time length, T_S is sampling interval and N is the DFT size. Therefore to modify the estimator we consider only the significant energy samples that are the upper left corner of auto-covariance matrix R_{gg}. From the IEEE std. 802.11 and IEEE std 802.16, $\left\lceil \frac{T_G}{T_S} \right\rceil$ should be chosen among $\{1/32, 1/16, 1/8\}$. Considering the significant energy level is 8. So $\frac{T_G}{T_S} = 1/8$ and $L = \frac{1}{8} \times 64 = 8$. So, the significant energy consists of 1 to 8 sample and remaining samples are noise of low SNR. To reduce the complexity we consider only the significant energy samples.

Figure 5, shows the general structure of Modified MMSE estimator. where x_n is the input signal, y_n is output signal, $\boldsymbol{Q}$ is frequency response in time domain and h_n is the transfer function, all these variables are range from 0 to *N-th* sample.

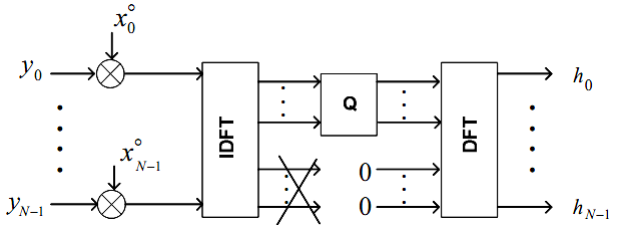


Figure 5: Block diagram for modified MMSE channel estimator

We consider only the significant energy samples that samples are transmit the data signal and remaining samples transmit null signal. In MMSE-3 estimator, first three samples send data signal and remaining samples send null signal. By implement the same approach- , MMSE-5, MMSE-8, MMSE-14 and MMSE-20 estimators' data signal are consists of five, eight, fourteen and twenty samples respectively and the rest of data bit information is set to null signal.

V. SIMULATION AND RESULT ANALYSIS

The goal of the simulation is efficiently estimate the channel and then validation of the proposed method. The simulation scenarios enable analysis of different channel estimator performance to find the optimal

channel estimator with low complexity. The significant energy level is one of the major factors to determine estimator performance. In our simulation, the significant energy level is concentrated in the first nine samples. The mean square error and symbol error rate are the major parameters to evaluate the estimators' performance. Our main emphasis is to minimize the mean square error and symbol error rate for each estimator. In our simulation scenario we consider a system with 500 kHz bandwidth which is divided into 64 carriers. The total symbol period is 64×2+10 = 138 µs where the symbol period for sender is 64+5=69 and for receiver 64+5= 69, the system used 64 subcarriers, 10 µs is for the cyclic prefix and the sampling is performed with 500 kHz rate. A symbol consists of 64+5=69 samples where five of them belong to cyclic prefix. Our simulation scenarios are on based the following system parameters are shown in Table 1.

TABLE I
SYSTEM PARAMETERS

parameters	Specification
FFT size	64
Number of carriers *N*	64
Pilot Ratio	1/10
Guard Length	10
Guard Type	Cyclic Prefix
Bandwidth	500KHz
Signal Constellation	16 QAM

Numbers of sample in each channel estimator used in our simulation are given in Table 2.

TABLE II
DIFFERENT CHANNEL ESTIMATORS AND THEIR SIZE

Estimator	Notation	Number of sample
MMSE	MMSE	0.....63
LS	LS	0.....63
SLS estimator	SLS	0.....63
Modified MMSE estimator	MMSE-3	0...2
	MMSE-5	0.....4
	MMSE-8	0.....7
	MMSE-14	0.....13
	MMSE-20	0.....19

All the programs are executed in Matlab simulator and the models validations are done on the basis of two parameter analysis are Mean Square Error and Symbol Error Rate.

A. Analysis of simulation result - Mean Square Error approach

We analyze the different channel estimators' performance based on mean square error criteria according to equation (14).

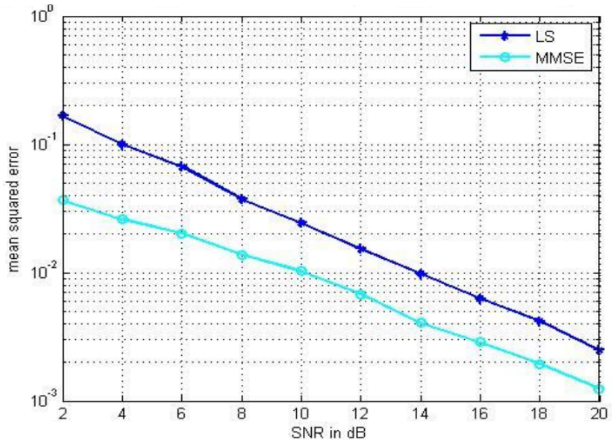


Figure 6: MMSE and LS estimator performance comparison based on characteristics of MSE versus SNR

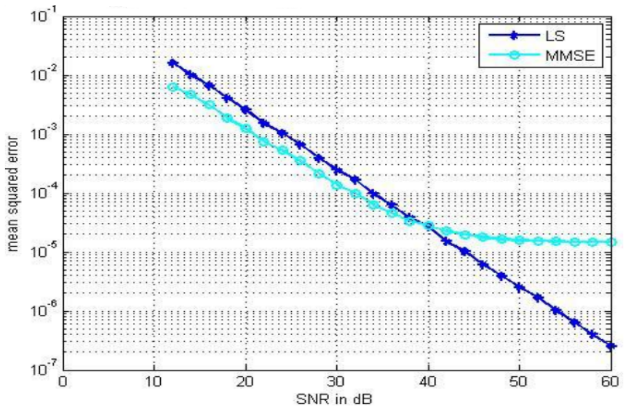


Figure 7: MMSE and LS estimator performance comparison based on characteristics of MSE versus SNR (for higher range of SNR)

Figures 6 and 7 show the mean square error versus SNR curve for LS and MMSE. For SNR range from 2 dB to 20 dB, the MMSE estimator mean square error range is 10^{-3} to 10^{-1} whereas the LS estimator mean square error range is 10^{-3} to 10. While SNR range increases from 12 dB to 60 dB, the MMSE estimator mean square error range is 10^{-5} to 10^{-1}, whereas the LS estimator mean square error range is 10^{-7} to 10^{-1}. LS and MMSE, the both of estimators give lower square error for higher range of SNR. Figures 8 and 9 shows the characteristics of MSE versus SNR for the MMSE, LS and SLS estimators respectively. The SLS estimator performance is better than LS for less than 16 dB SNR.

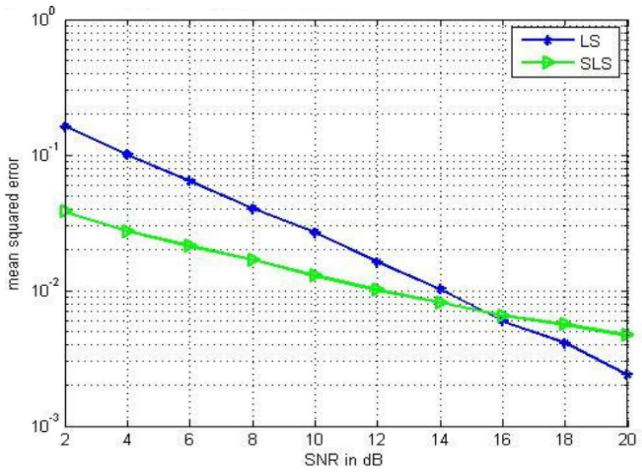


Figure 8: SLS and LS estimator performance comparison based on MSE versus SNR parameters

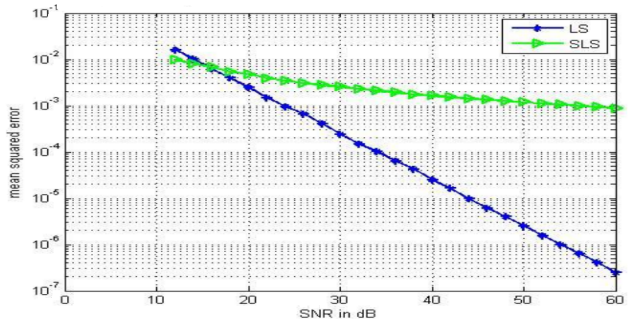


Figure 9: SLS and LS estimator performance comparison based on MSE versus SNR parameters (for higher range of SNR)

Figures 10 and 11 show comparisons of the MSE performance of the estimation schemes with original MMSE and modified MMSE. In Figure 10, the MMSE-20 estimator MSE is lower than others modified MMSE and for higher number of power samples estimator gives lower MSE values. In Figure 11, we compare all of modified MMSE estimators with original MMSE estimator where we can observe for higher SNR range, all modified estimators' gives the lower MSE. The original MMSE estimator MSE range is 10^{-5} to 10^{-2} whereas the modified MMSE estimator MSE range is 10^{-1} to 10^{0}.

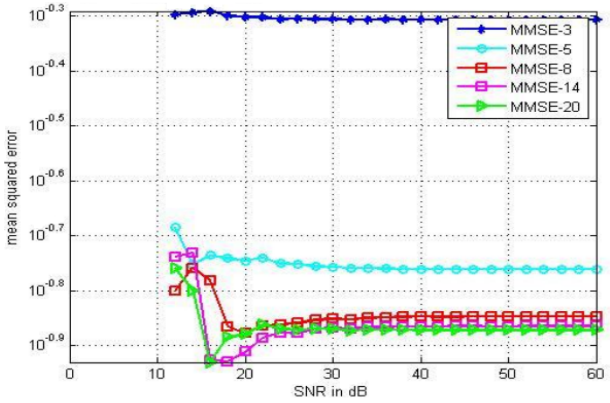


Figure 10: Performance analysis for modified MMSE based on MSE versus SNR

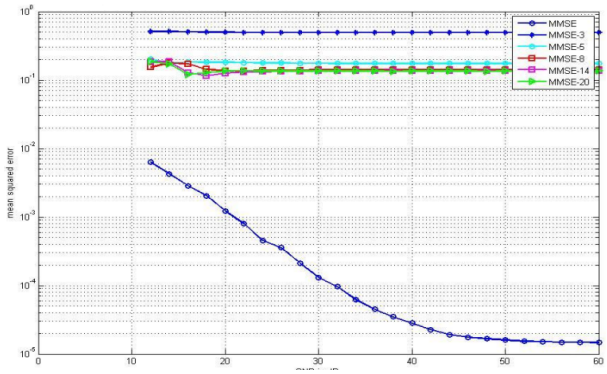


Figure 11: Comparison between Original MMSE and modified MMSE

B. Analysis of simulation result - Symbol Error Rate approach

In this section, we analysis the different channel estimators' performance based on symbol error rate approach based on equation (15).

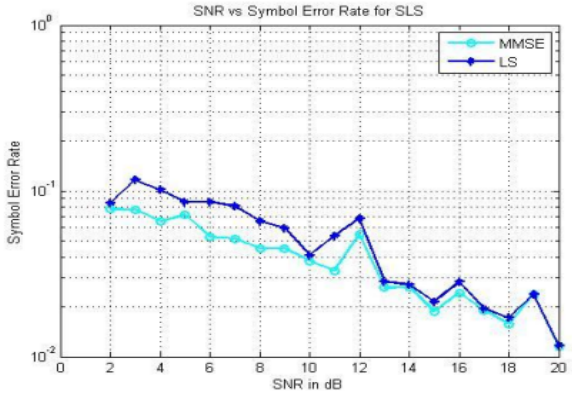


Figure 12: Performance analysis for MMSE and LS based on SER versus SNR

Figures 12 and 13 show the comparison between the LS and MMSE estimator based on SER versus SNR. In the SNR range from 2 dB to 20 dB, the MMSE estimator SER is lower than the LS estimator. SERs of LS and MMSE are almost the same from 25 dB SNR range.

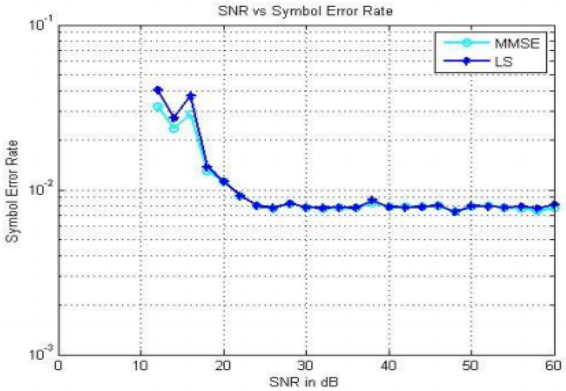


Figure 13: MMSE and LS estimator performance comparison based on characteristics of SERversus SNR (For higher SNR range)

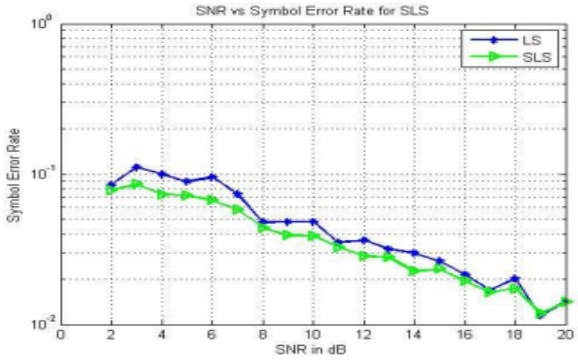


Figure 14: Performance comparison for SLS and LS based on SER versus SNR

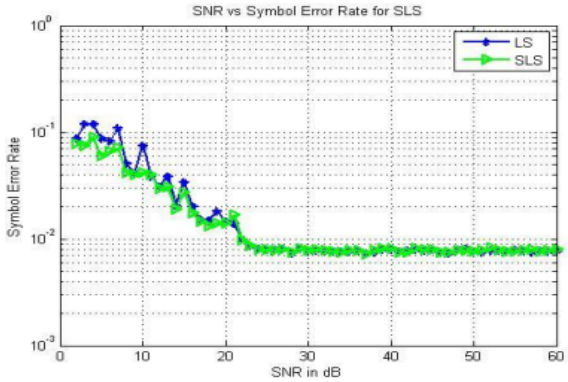


Figure 15: Performance comparison for SLS and LS based on SER versus SNR (for higher SNR range).

Figure 14 and 15 show the performance characteristics of LS and SLS estimator. The SNR range from 2 dB to 20 dB, the SLS and LS estimator SER are in the range from 10^{-2} to 10^{0}. The same for the SNR range from 2 dB to 60 dB, the SLS and LS estimator SERs are in the same range from 10^{-2} to 10^{-1}. For higher range of SNR the SER is almost same for the LS and SLS estimator.

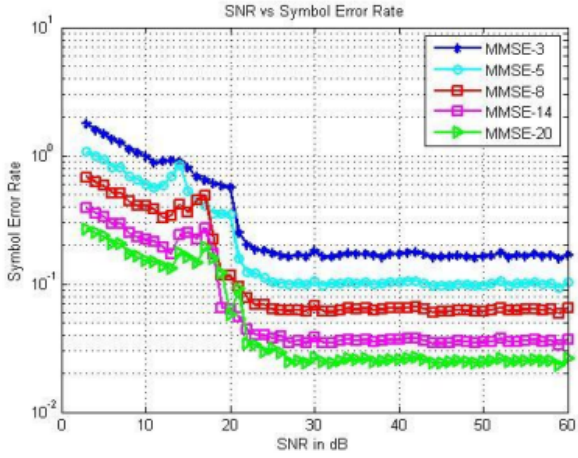


Figure 16: Performance comparison of modified MMSE based on SER versus SNR

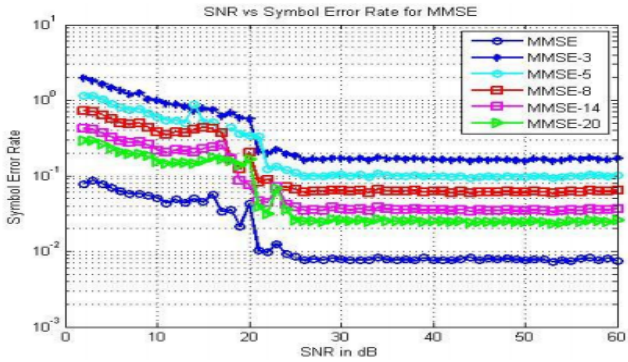


Figure 17: Performance comparison of MMSE and modified MMSE based on SER versus SNR

The Figures 16 and 17 illustrate the SER performance of the estimation schemes with original MMSE and modified MMSE. In Figure 16, we can conclude that MMSE-20 estimator SER is lower than all others modified MMSE. When the number of significant energy samples increases, then the SER decreases. So, for larger number of significant energy sample, the performance can be improved. In figure 17, we compare all of modified MMSE estimators' with original MMSE estimator. For higher range of SNR, all of estimator gives lower SER. All of modified MMSE estimators' are in the SER range from 10^{-2} to 10^{1} whereas the original MMSE estimator SER ranges 10^{-2} to 10^{-1}. It can be concluded that modified MMSE estimator slightly compromises with the performances.

CONCLUSION

In this paper, first, we show the general structure of all estimators. Then we investigate the LS and the MMSE estimator performances using the mean square error and symbol error rate. Based on the performance analysis the MMSE estimator is recognized as better than LS estimator, but the MMSE estimator suffers from high computational complexity. To reduce its computational complexity we proposed two different channel estimation methods: The SLS estimator and the modified MMSE estimator. The significant energy samples and noisy observation of the LS estimator are the key points to implement our ideas. In the SLS estimator, we apply an auto-correlation function with the LS estimator to remove the noise. In the modified MMSE estimator, we consider only the significant energy samples and ignore the remaining noisy samples. Based on this we introduce the modified MMSE estimator.

By using the Matlab simulator, we validated our models. The comparison of all estimators' performances on basis of mean square error and symbol error rate is shown. The simulation result shows that the MMSE estimator performances better than the LS estimator, especially in higher SNR range. From the performance analysis of each estimator, the SLS estimator MSE is

10^{-1} to 10^{-7} and SER is 10^{-1} to 10^{-2} for 10 dB to 60 dB SNR range. However the modified MMSE estimator MSE is 10^{0} to 10^{-1} and SER is 10^{1} to 10^{-1} on the same SNR range. The SLS estimator MSE is lower than the modified MMSE estimator. In modified MMSE estimator, the MMSE-20 estimator gives the lower MSE than the others modified MMSE estimator. In future work, the proposed channel estimation method can be applied for 4G LTE to achieve high data rate.

REFERENCES

[1] Yi Gong and K.B Lataief, "Low rank channel estimation for space-time coded wide band OFDM systems", *IEEE Vehicular Technology Conference*, vol. 2, pp. 772-776, 2001.

[2] Y. Shen and E. Martinez. Channel estimation in ofdm systems. Technical Report AN3059, Freescale Semiconductor, Inc., 2006.

[3] S. W. McLanughln Y. Li M. A. Ingram G. L. Stuber, J. R. Barry and T. G. Pratt. Broadband mimo-ofdm wireless communications. Proceedings of the IEEE, 92(2), Feb. 2004.

[4] Coleri,S; Ergen,M; Puri,A; Bahai,A. "Channel estimation techniques based on pilot arrangement in OFDM systems", *IEEE Transactions on Broadcasting*, vol. 48, Issue 3, pp. 223229, Sept.2002.

[5] C. Li and S. Roy. Subspace-based blind channel estimation for ofdm by exploiting virtual carriers. IEEE Trans. Wireless Commun., 2(1), Jan. 2003.

[6] R. Steele. Mobile Radio Communications. New York: Wiley, 1974.

[7] S. W. McLanughln Y. Li M. A. Ingram G. L. Stuber, J. R. Barry and T. G. Pratt.Broadband mimo-ofdm wireless communications. Proceedings of the IEEE, 92(2), Feb.2004.

[8] J. J. van de Beek S. K. Wilson O. Edfors, M. Sandell and P. O. Borjesson. Ofdm channel estimation by singular value decomposition. IEEE Trans. Commun., 46(7), July 1998.

[9] M. Sandell S. K. Wilson J. J. van de Beek, O. Edfors and P. O. Borjesson. On channel estimation in OFDM systems. In Proc. IEEE Vehicular Technology Conf., volume 2,pages 815{819, Chicago, IL., July 1995.

[10] "Mean Squared Error", July 23, 2010. [online] Available: http://en.wikipedia.org/wiki/Mean_squared_error [Accessed: August 2010].

[11] "Symbol Error Rate" for 16-QAM. October 18, 2008. [Online]. Available: http://www.dsplog.com/2007/12/09/symbol-error-rate-for-16qam/ [Accessed: August 2010].

Design Of High Performance Configurable Radix-4 Booth Multiplier Using Cadence Tools

Dr.T. Esther Rani
CVR College of Engineering, Dept of ECE, Hyderabad, India
estherlawrenc@gmail.com

***Abstract* — Fast multipliers are crucial in digital signal processing systems. The speed of multiply operation is of great importance in digital signal processors and general purpose processors especially since the media processing took off. As the need for efficient design is increasing without compromising the performance, industry has to concentrate on the tradeoffs. Here, a modified Booth multiplier is implemented using an algorithm that reduces the number of partial Products to be generated using the fastest multiplication algorithm. In this work, 8X8 multipliers with maximum range of input from -128 to +127 and negative numbers represented in 2's complement form can be used. Booth Encoder i.e., Partial Product Generator and Hybrid adder are used for the design of modified booth multiplier to achieve minimum delay and less area.**

***Index Terms*— Modified Booth multiplier, digital signal processors, Booth Encoder, multiplication algorithm, Hybrid adder.**

I. INTRODUCTION

Multiplier is a key component of any high performance system such as FIR filters, microprocessors, digital signal processors, etc. Performance of a system is generally determined by the performance of the multiplier as the multiplier is the element with slow operation and consumes more area in any system. Therefore, optimizing the speed and area of a multiplier is a major design issue. As the area and speed are usually conflicting constraints, whole spectrum of multipliers with different area-speed constraints will be designed in parallel. The multipliers with such design constraints have moderate performance in both speed and area. Radix 2^n multipliers which operate on digits in a parallel fashion instead of bits bring the pipelining to the digit level and avoid most of' the problems was introduced by M. K. Ibrahim in 1993. These structures are iterative and modular and the pipelining done at the digit level brings the benefit of constant operation speed irrespective of the size of the multiplier.

A high speed low-power multiplier is proposed adopting the new modified Booth implementing approach. The modified booth encoder will reduce the number of partial products generated by a factor of 2. Power dissipation is recognized as a critical parameter in modern VLSI design. Dynamic power dissipation which is the major part of total power dissipation is due to the charging and discharging capacitance in the circuit. Dynamic power dissipation is calculated by $P_d = \alpha C_L V^2 f$. Power reduction can be achieved by reduction of output Capacitance $C_{L,}$ power supply voltage V, switching activity α and clock frequency f.

In most computers, the operand usually contains the same number of bits. When the operands are interpreted as integers, the product is generally twice the length of operands in order to preserve the information content. This repeated addition method that is suggested by the arithmetic definition is slow that it is almost always replaced by an algorithm that makes use of positional representation. It is possible to decompose multipliers into two parts. The first part is dedicated to the generation of partial products, and the second one collects and adds them.

Booth multiplication allows for smaller, faster multiplication circuits through encoding the signed numbers to 2's complement, which is also a standard technique used in chip design, and provides significant improvements by reducing the number of partial product to half compared to conventional multiplication techniques. Multipliers are categorized relative to their applications, architecture and the way the partial products are produced and summed up. Based on all these, a designer might decide the type of multiplier.

A. Basic Binary Multiplier

A multiplier circuit is able to perform a multiplication of n-bitsXn-bits at a high speed by increasing the speed of the forming process of the partial products so that the delay time may be inhibited from increasing for a large n, and which can inhibit the chip size becoming large. Multiplication is more complicated than addition, being implemented by shifting as well as addition. Because of the partial products involved in most multiplication algorithms, more time and more circuit area is required to compute, allocate, and sum the partial products to obtain the multiplication result. Pencil-and-paper algorithm for multiplication is explained below.

Multiplicand: 0010 -- Stored in register r1

Multiplier: x 1101 -- Stored in register r2

Partial Prod 0010 -- No shift for LSB of Multiplier
" " 0000 -- 1-bit shift of zeroes (can omit)
" " 0010 -- 2-bit shift for bit 2 of Multiplier
" " 0010 -- 3-bit shift for bit 3 of Multiplier
---------- Zero-fill the partial products and ad
PRODUCT 0011010 -- Sum of all partial products stored in r3

B. Partial Product Generation

Since the amount of hardware and the delay depends on the number of partial products to be added, this may reduce the hardware cost and improve performance by considering different methods. Straightforward extensions of the Booth recoding scheme can further reduce the number of partial products, but require a time consuming N-bit carry propagate addition before any partial product generation can take place. Figure 1shows the basic unsigned multiplication using dot notation.

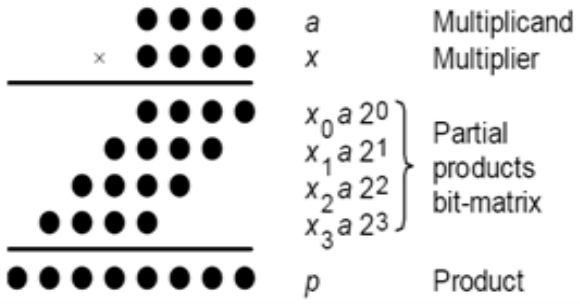


Figure 1: Basic unsigned Multiplication using Dot notation

The number of dots in the partial product section of the dot diagram proportional to the amount of hardware required to sum the partial products and form the final product. Time multiplexing can reduce the hardware requirement, at the cost of slower operation. The latency of an implementation of a particular algorithm is also related to the height of the partial product section (i.e., the maximum number of dots in any vertical column) of the dot diagram. This relationship can vary from logarithmic to linear or tree implementations where interconnect delays are significant. However, in a real implementation there will more be interconnect delay due to the physical separation of the common inputs of each AND gate, and distribution of the multiplicand to the selection elements.

C. Fast Adders

Fast carry propagate adders are important to high performance multiplier design in two ways. First, an efficient and fast adder is needed to make any "hard" multiples that are needed in partial product generation. Second, after the partial products have been summed in a redundant form, a carry propagate adder is needed to produce the final non redundant product. Half adder and full adder are two types of single bit adders. The full adder takes into account a carry input such that multiple adders can be used to add larger numbers. Many researchers reported on the multiplier architectures including array, parallel and pipelined multipliers that have been pursued and the pipelining is the most widely used technique to reduce the propagation delays of digital circuits.

i. Carry Look-Ahead Adder (CLA)

The concept behind the CLA is to get rid of the rippling carry present in a conventional adder design. The rippling of carry produces unnecessary delay in the circuit. For a conventional adder the expressions for sum and carry signal can be written as follows.

S =A xor B xor C…….....*(1)*
$C0 = AB + BC + AC$…….....*(2)*

It is useful from an implementation perspective to define S and *C0* as functions of some intermediate signals G (generate), D (delete) and P (propagate). G =1 implies that a carry bit will be generated, P=1 implies that an incoming carry will be propagated to C0 as shown in figure 2. These signals are computed as

$G = AB$……..…….*(3)*
$P = A$ xor B……..…….*(4)*

Also S and C0 in terms of G and P can be expressed as

$C\,0(G,P) = G + PC$……..*(5)*
$S(G,P) = P$ *xor* C……..*(6)*

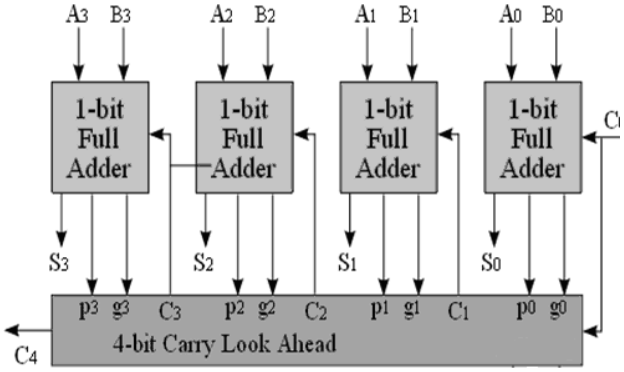


Figure 2: 4-bit Carry Look Ahead Adder

ii. Hybrid Adder

Hybrid Adder is a combination of any two adders and is used in high speed applications. The proposed hybrid adder consists of two carry look ahead adders and a multiplexer as shown in figure 3. Adding two n-bit

numbers with a hybrid adder is done with two adders (therefore two carry look ahead adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known. The propagation delay is less for hybrid adder and at the same time it occupies larger area compared to the other adders.

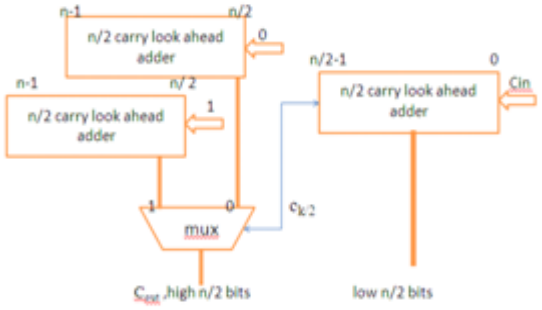


Figure 3: n-bit Hybrid Adder

II. DESIGN OF RADIX-2 AND RADIX-4 BOOTH MULTIPLIER

This section describes an 8x8 signed parallel Booth multiplier which reduces the number of the partial products. Modified booth algorithm is used and for adding partial products efficiently. A 16-bit hybrid adder has been implemented for generating the final result. After deciding on the multiplier architecture, different logic styles for multiplier implementation have been compared and concluded that Booth Multiplier is the most efficient multiplier in terms of power and delay.

One of the solutions for realization of high-speed multipliers is to enhance parallelism and to decrease the number of subsequent calculation stages. It is well known that both Modified Booth algorithm and the hybrid adder are effective in decreasing number of stages.

A. Booth Multiplication Algorithm for Radix-2

Booth algorithm gives a procedure for multiplying binary integers in signed 2's complement representation.
The booth algorithm is explained with the following example:
Example, 2 x - 4
0010 (2) * 1100 (-4)

Step 1: Making the Booth table
I. From the two numbers, pick the number with the smallest difference between a series of consecutive numbers, and make it a multiplier.
i.e., 0010 -- From 0 to 0 no change, 0 to 1 one change, 1 to 0 another change, and so there are two changes on this one
1100 -- From 1 to 1 no change, 1 to 0 one change, 0 to 0 no change, so there is only one change on this one.
Therefore, multiplication of 2 x (– 4), where 2 (0010_2) is the multiplicand and (– 4)

(1100_2) is the multiplier.

II. Let X = 1100 (multiplier)
Let Y = 0010 (multiplicand)
Take the 2's complement of Y and call it –Y
–Y = 1110

III. Load the X value in the table.
IV. Load 0 for X-1 value it should be the previous first least significant bit of X
V. Load 0 in U and V rows which will have the product of X and Y at the end of operation.
VI. Make four rows for each cycle; this is because four bits numbers are multiplied.

U	V	X	X-1	
0000	0000	1100	0	Load the value
				1st cycle
				2nd cycle
				3rd Cycle
				4th Cycle

Figure 4: 4-bit Radix-2 Booth multiplication example

Step 2: Booth Algorithm

Booth algorithm requires examination of the multiplier bits, and shifting of the partial product. Prior to the shifting, the multiplicand may be added to partial product, subtracted from the partial product, or left unchanged according to the following rules.

The first least significant bits of the multiplier "X" is observed, and the previous least significant bits of the multiplier "X - 1". Table 1shows the Radix-2 Booth Encoding.

TABLE I
RADIX-2 BOOTH ENCODING TABLE

X	X-1	Partial product
0	0	Shift only
0	1	Add Y to U, and shift
1	0	Subtract Y from U, and shift or add (-Y) to U and shift
1	1	Shift only

II Take U & V together and shift arithmetic right shift which preserves the sign bit of 2's complement number. Thus a positive number remains positive, and a negative number remains negative.

III Shift X circular right shifts because this will prevent us from using two registers for the X value.

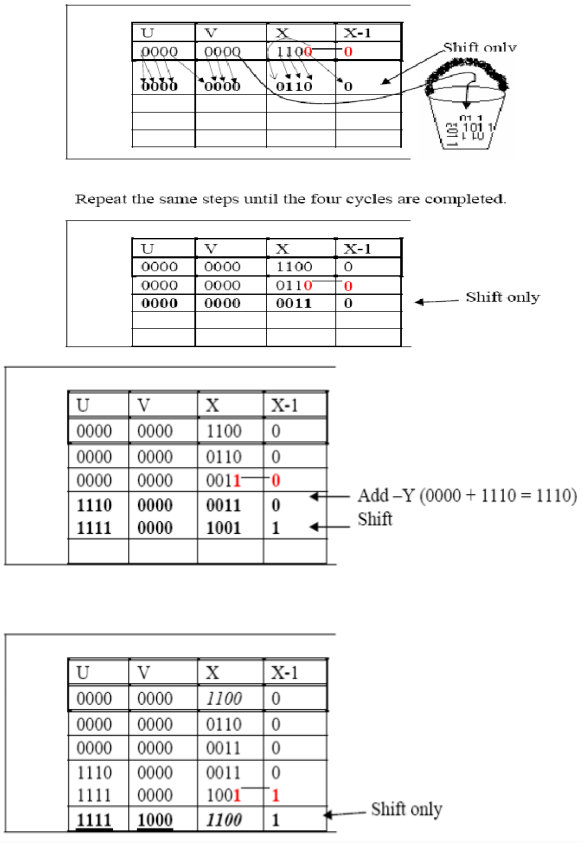


Figure 5: 4-bit Radix-2 Booth multiplication example

After finishing four cycles, the answer is shown in the last rows of U and V which is: 11111000 $_2$

By the fourth cycle, the two algorithms have the same values in the product register.

B. Booth Multiplication Algorithm for Radix-4

One of the solutions of realizing high speed multipliers is to enhance parallelism which helps to decrease the number of subsequent calculation stages. The original version of the Booth algorithm (Radix-2) had two drawbacks that, the number of add subtract operations and the number of shift operations becomes variable and becomes inconvenient in designing parallel multipliers. Also the algorithm becomes inefficient when there are isolated 1's. These are overcome by using modified Radix-4 Booth algorithm which scans strings of three bits with the algorithm given below:

1) Extend the sign bit 1 position if necessary to ensure that n is even.

2) Append a 0 to the right of the LSB of the multiplier.

3) According to the value of each vector, each Partial Product will he 0, +y , -y, +2y or -2y.

The negative values of y are made by taking the 2's complement .The multiplication of y is done by shifting y by one bit to the left. Thus, in any case, in designing a n-bit parallel multipliers, only n/2 partial products are generated. The block diagram of radix-4 booth multiplier is as shown in figure 6.

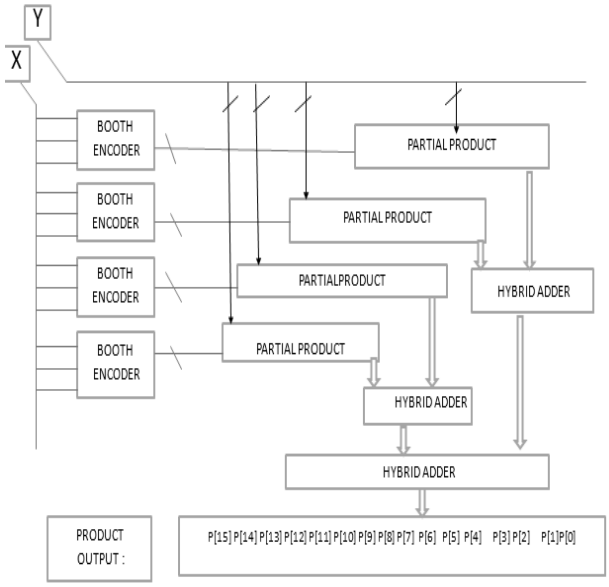


Figure 6: Block Diagram of Radix-4 Booth Multiplier

C. Booth Encoder

It will encode the multiplicand based on multiplier bits. In Radix -4 compare 3 bits at a time with overlapping technique. Grouping starts from the LSB, and the first block only uses two bits of the multiplier and assumes a zero for the third bit. There are two inputs for booth encoder one is multiplicand and the other is 3 bits from multiplier, based on these two inputs it will encode the multiplicand. For 8 bit multiplier the no of blocks and partial products will be 4. The function of booth encoder is as shown in the table2 below.

TABLE II
RADIX-4 BOOTH ENCODING TABLE

BLOCK	PARTIAL PRODUCT
000	0
001	1*multiplicand
010	1*multiplicand
011	2*multiplicand
100	-2*multiplicand
101	-1*multiplicand
110	-1*multiplicand
111	0

D. Hybrid Adder

Multiplication of two numbers is carried out in two steps.

1. Generating partial products: Generation of partial products is done by booth encoder.
2. Adding the partial products: To produce output, all the partial products must be added. This is done by high speed hybrid adder. Hybrid adder is a combination of carry look ahead adder and carry select adder.

III. IMPLEMENTATION OF BOOTH MULTIPLIERS

This design flow would start with a behavioral-style description of the system, written in Verilog, and would take the following steps. Simulation at the high level behavioral model used to confirm that the conceptualized design does function correctly. Logic synthesis describes the design as an interconnection or netlist of logic gates and flip-flops. Technology mapping maps the gates from logic synthesis into the standard cells in the library. At the end of the technology mapping step, physically what each component in our system looks like and what interconnections need are known, but physically what the interconnections will look like were not specified. Placement and Routing takes the standard cell netlist as an input, and produces a full layout.

CAD tools, like Cadence, are used to automate these steps as much as possible. The Cadence Incisive® NC Simulator has been used to simulate the design at the behavioral level. The Cadence Encoutner® RTL Compiler global synthesis has been used to produce the logic synthesis of the design and map it to the required technology. The Cadence SoC Encounter™ RTL-to-GDSII system places the design and routes it to produce the final layout.

IV. RESULTS AND ANALYSIS

The results of the booth multiplier are verified using simulation process. As the main aim of the work is to decrease the propagation delay and multiplier performance depends on the performance of adders, Multiplication of two numbers is carried out in two steps: Generation of partial products has been performed by booth encoder and addition of the partial products. The simulation diagram of Radix-2 Booth multiplier is as shown in the figure 7. The synthesized netlist of the Radix-2 Booth multiplier has one main module in which carry select adder is present.the synthesized netlist of main module is as shown in figure 8. The synthesized netlist of the carry select adder for radix-2 Booth multiplier is as shown in figure 9.

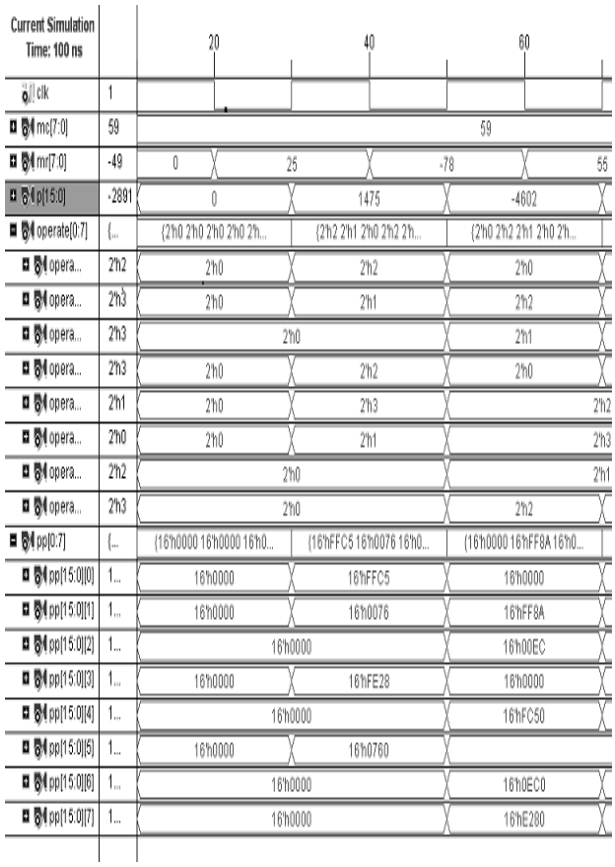


Figure 7: Simulation Diagram of Radix-2 Booth multiplier

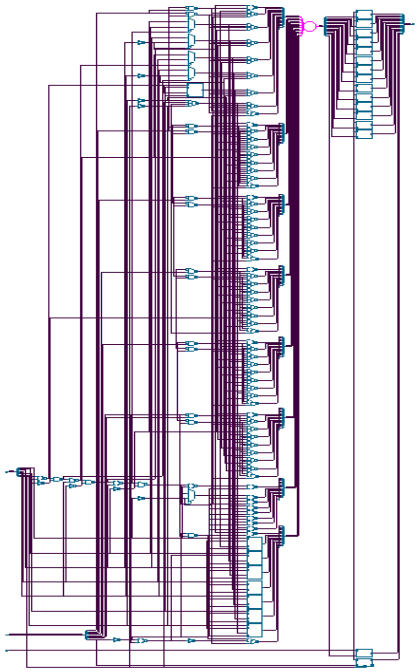


Figure 8: synthesized netlist of Radix-2 Booth multiplier

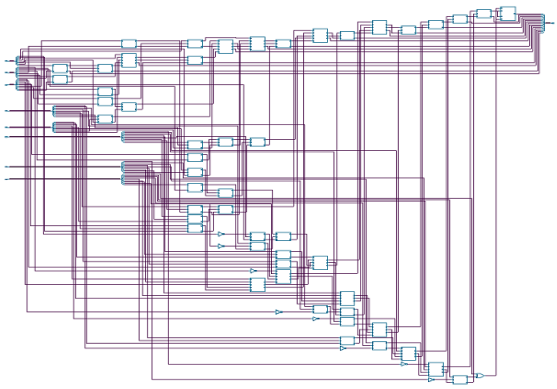


Figure 9: synthesized netlist of carry select adder for radix-2 Booth multiplier

By changing the timing delay values in the script the power and area of the radix-2 Booth multiplier are observed. For different values of timing delays the corresponding slack, power and area are as shown the table3.

TABLE III
DELAY, POWER and AREA for RADIX-2 BOOTH MULTIPLIER

Delay (ps)	Slack (ps)	Power (mW)	Area (um^2)
3000	6	1.42	7504
3500	1	1.33	7548
4000	9	1.18	6686
4200	29	1.17	6603
4500	110	1.15	6470

The output of the SoC Encounter that is final layout design of Radix-2 Booth multiplier and is shown below in figure 10.

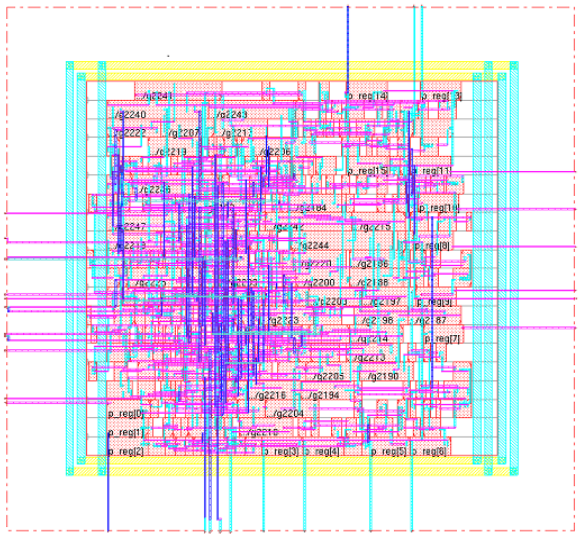


Figure 10:Final layout design of Radix-2 Booth multiplier.

The simulation diagram of modified Booth multiplier is as shown in the figure11. The synthesized netlist of the Radix-4 Booth multiplier has one main module in which carry select adder is present.the synthesized netlist of main module is as shown in figure 12. The synthesized netlist of the carry select adder for modified Booth multiplier is as shown in figure 13.

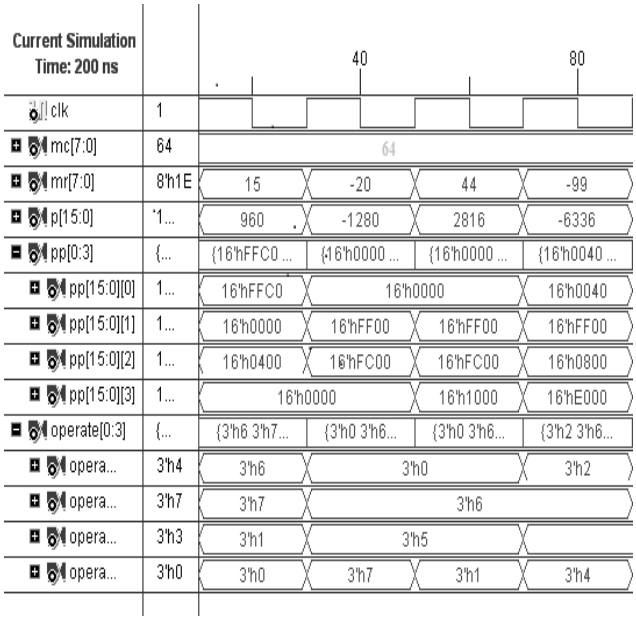


Figure 11: Simulation Diagram of modified Booth multiplier.

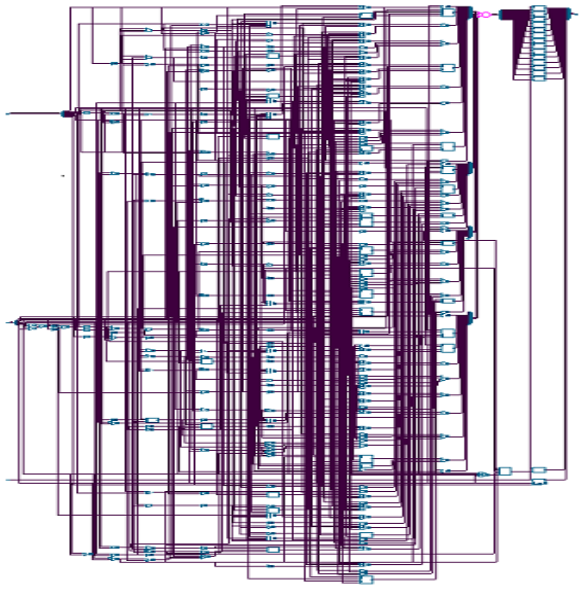


Figure 12:synthesized netlist of modified Booth multiplier

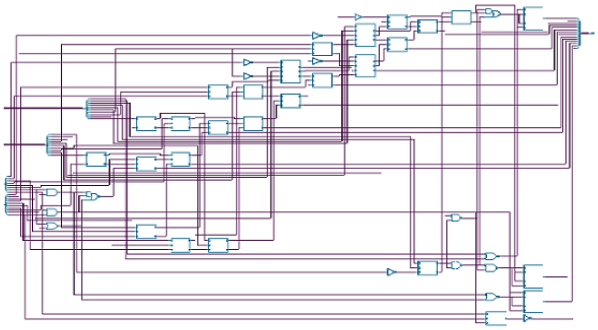


Figure 13: Synthesized netlist of carry select adder for modified Booth multiplier.

By changing the timing delay values in the script the power and area of the modified Booth multiplier are observed. For different values of timing delays the corresponding slack,power and area are as shown the table 4.

TABLE IV
DELAY, POWER and AREA for MODIFIED BOOTH MULTIPLIER

Delay (ps)	Slack (ps)	Power (mW)	Area (um^2)
3000	2	1.12	6749
3500	2	0.98	5911
4000	17	0.955	5582
4200	20	0.944	5565
4500	23	0.9	5545

The final layout design of the modified Booth multiplier for length to width ratio equal to one is shown in figure 14.

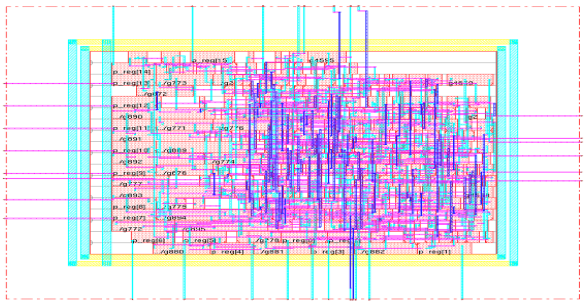


Figure 14: Final layout design of modified Booth multiplier.

For a fixed delay in timing , the power and area of the radix-2 Booth multiplier and Modified Booth multiplier are as shown in the table 5.

TABLE V
COMPARISION OF POWER AND AREA OF BOTH THE MULTIPLIERS FOR FIXED TIMING DELAY

	Radix-2 Booth multiplier	Modified Booth multiplier	% change in the value
Delay (ps)	3000	3000	0
Power(mW)	1.42	1.12	21.126
Area (um^2)	7504	6749	10.06

From the above table it is observed that for same delay the power and area of the modified Booth multiplier are less compared to Radix-2 Booth multiplier.

For a fixed area, the power and delay of the radix-2 Booth multiplier and Modified Booth multiplier are as shown in the table 6.

TABLE VI
COMPARISION OF POWER AND DELAY OF 2 MULTIPLIERS FOR FIXED AREA

	Radix-2 Booth multiplier	Modified Booth multiplier	% change in the value
Delay (ps)	4000	3000	25
Power(mW)	1.2	1.12	6.67
Area (um^2)	6700	6700	0

The table 7 is valid for 8 bit x 8 bit multiplier. The table 7 shows advantage of radix-4 compared to radix-2. It has less propagation delay and at the same time it occupies lesser area.

TABLE VII
PERFORMANCE OF THE BOOTH MULTIPLIERS

	Radix-2 Booth multiplier	Modified (Radix-4) Booth multiplier	% change in the value
Number of slices	88	68	22.7
Number of LUTs	156	126	19.23
Path Delay (ns)	24.22	17.1	29.39

The above table is valid for 8 bit x 8 bit multiplier. The above table shows why to move from radix-2 to radix-4 . The main advantage of using radix-4 is it has less propagation delay, i.e speed and at the same time it occupies lesser area.

Using NC Simulator tool, 8 bit modified Booth multiplier at the behavioral level is coded in a behavioral description using Verilog. It is compiled, checked for syntax errors, elaborated and simulated using a Verilog test bench using the following commands to get the output as shown in figure 15.

Figure 15: Output waveform in NC simulator.

In RTL compiler tool, the mapping of a design into a netlist of standard cells is done. The library containing all these standard cells is usually built according to the fabrication process limitations. The workshop uses a 0.5 um Silicon-on-insulator process manufactured by Peregrine semi conductors. The output is a verilog file describing the netlist. At this point, the number of gates used and the propagation delay of the critical path of the system is reported.

Once the script file is ready, the graphical user interface of the Encoutner RTL Compiler is used to source the script file and synthesize the design of the 8 bit modified Booth Multiplier. The following commands are used to open the graphical user interface of the Encoutner RTL Compiler. Then the final synthesized design is obtained as shown in figure 16 below.

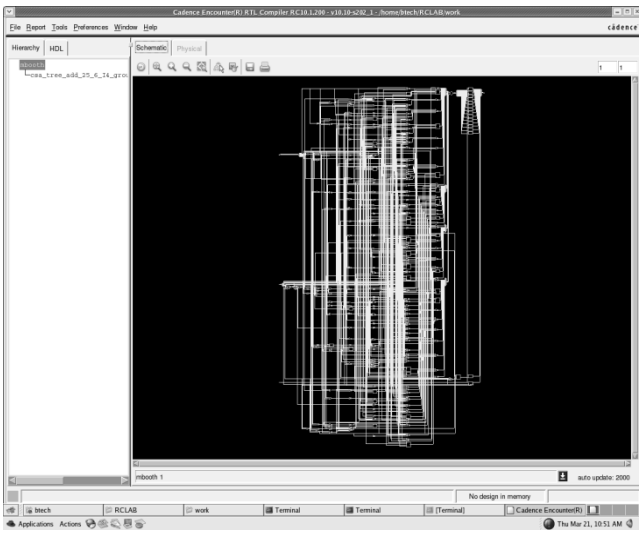


Figure 16: Encounter RTL compiler output after synthesis.

SoC Encounter is used for the placement and routing of the design. In this tool first import the design, specify the floor plan, add the power rails, place the standard cells, and route the design. SoC Encounter output after placing standard cells and after routing are shown in figures 17 and 18.

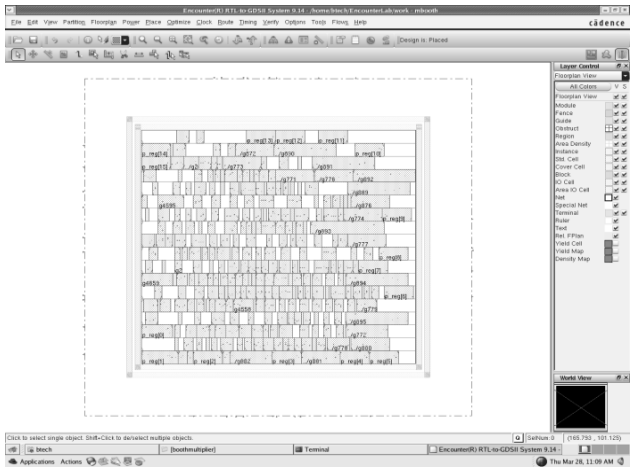


Figure 17: SoC Encounter window after placing standard cells

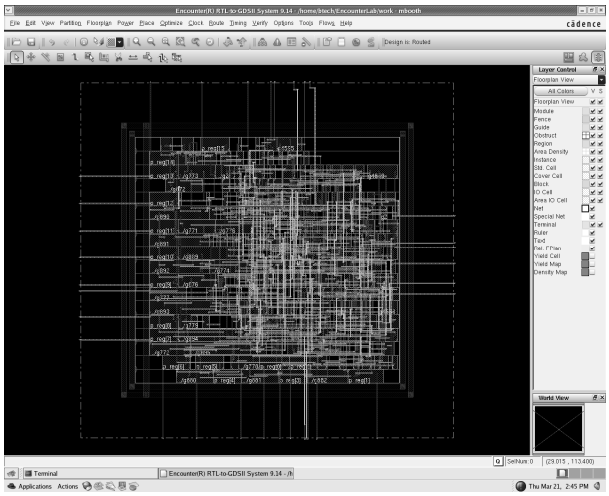


Figure 18: SoC Encounter window after routing

V Conclusion

In this work, 8x8 Radix-4 modified Booth Multiplier has been presented. Modest improvements in area and power over more conventional algorithms have been shown using this algorithm. Algorithms based upon the Booth partial product method are distinctly superior in power and area when compared to non-Booth encoded methods. This result must be used carefully if applied to other technologies, since different trade-offs may apply. The main advantage of using Radix-4 is that it has less propagation delay, and it occupies lesser area. This work is also implemented by using the cadence tools of NC simulator, Encounter RTL compiler and SoC Encounter for simulation, logical synthesis and placing & routing respectively.

REFERENCES

[1] Digital Design Principles and Practices – John F. Wakerly, PHI/ Pearson Education Asia 3rd Ed.,2005.

[2] Computer System Architecture – M. Morris Mano, 3rd Edition, PHI/ Pearson., 2006.

[3] K.H.Chen and Y.S.Chu , "A low power multiplier with spurious power suppression technique" ,IEEE Trans. Very Large Scale Integr .(VLSI)Syst., Vol.15, no-7, pp846-850, July 2007.

[4] Essentials of VLSI circuits and systems – Kamran Eshraghian, Eshraghian Dougles and A.pucknell, PHI, 2005 Edition.

[5] CMOS VLSI Design: A Circuits and Systems Perspective, Third Edition, Neil H.E. Weste, David Harris.

[6] John Rabaey **"**Digital Integrated Circuits", PHI, 1st edition, 1999

[7] http://www.xilinx.com/

[8] Jack Horgan, "Low Power Soc Design", EDAWeekly Review May 17 - 21, 2004

[9] Cadence, "Low Power in EncounterTM RTL Compiler", Product Version 5.2, December 2005

[10] Cadence, "Cadence Low Power Design Flow"

[11] Cadence, "Low Power Application Note for RC 4.1 and SoCE 4.1 USR3", Version 1.0,1/14/2005

Design of Low Cost Sigma-Delta Analog-to-Digital Converter for Audio Applications

Athira G. Krishna
CVR College of Engineering/ ECE Department, Hyderabad, India
Email :athira_rashad@yahoo.co.in

***Abstract*— FPGA (Field-Programmable Gate Array) based solutions in consumer electronics have gained popularity due to low cost and high performance. The time-to market is also shorter and the financial risk is lower compared to ASIC (Application Specific Integrated Circuit). One component that is missing in a low-cost FPGA is the ability to convert an analog signal to its digital counterpart. The aim of this paper is to implement an ADC (Analog-to-Digital Converter) for audio applications using external components together with an FPGA (Field-Programmable Gate Array). The focus is on making the ADC low-cost and it is desirable to achieve 16-bit resolution at 48 KS/s. Since large FPGA's have numerous I/O-pins, there are usually some unused pins and logic available in the FPGA that can be used for other purposes. This is taken advantage of, to make the ADC as low-cost as possible.**

This paper presents two types of converters an Σ-Δ (Sigma-Delta) converter with a first order passive loop-filter and an Σ-Δ converter with a second order active loop-filter. The solutions have been designed on a PCB (Printed Circuit Board) with a Xilinx Spartan FPGA. Both solutions take advantage of the LVDS (Low-Voltage-Differential-Signaling) input buffers in the FPGA. First converter achieves a peak SNDR (Signal-to-noise-and-distortion-ratio) of 62.3 dB (ENOB (Effective number of bits10.06 bits)and it is very low-cost but is not suitable for high-precision audio applications. Second converter achieves a peak SNDR of 80.3 dB (ENOB 13.04) and the cost is more comparatively first one but it is more suitable for mono audio and for stereo audio applications.

***Index Terms*- FPGA, ADC, SNDR, Sigma-Delta converter, ENOB, Xilinx Spartan, LVDS.**

I. INTRODUCTION

An FPGA is an integrated circuit, which have a large number of logic resources that can be configured to implement complex digital algorithms. The configuration can be done after manufacturing and is specified using a HDL (Hardware description language). This paper will take advantage of the strength of the FPGA. The aim of this paper is to implement an ADC (Analog-to-Digital Converter) for audio applications using an FPGA together with external components. Two solutions are presented: (1) a **Σ**-Δ converter with a first order passive loop-filter and (2) a **Σ**-Δ converter with a second order active loop-filter. In both solutions, the FPGA will mainly **b**e used to implement digital filters.

The main objective is to try eliminating the external ADC and replacing it with external components and using the power of the FPGA. The goal is therefore to make it low-cost and it is desirable to achieve CD quality, i.e. 16-bit resolution at 44.1 KS/s. In this design will use 48 KS/s and the goal is to achieve 16-bit resolution. The term "low-cost", in this paper, is only focusing on the external components. The goal is to keep the total cost of the external components at a minimum. However, the FPGA resources used should also be kept at a minimum. Since large FPGA's have numerous I/O-pins, there are usually some unused pins and logic available in the FPGA that can be used for other purposes. This is taken advantage of, to make the ADC as low-cost as possible.

In this section, the fundamental operation of an ADC is described. Furthermore, it describes the basic operation of an **Σ**-Δ converter and in particular the CT **Σ**-Δ converter. Since the **Σ**-Δ converter is a oversampling converter, there is a chapter about digital filtering and decimation (down sampling). The main objective of an ADC is to convert an analog signal into its digital counterpart, so it can be further processed by digital circuits. An analog signal is in its nature continuous in both time and amplitude, while a digital signal is discrete in both time and amplitude. This process can be divided into two sections: Sampling and Quantization See Figure.1 for an illustration of the ADC system.

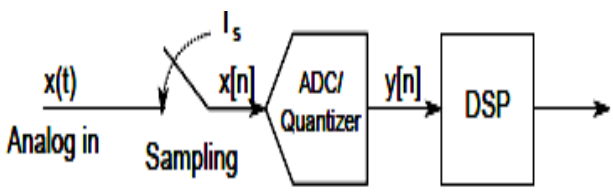


Figure.1: From analog input signal, $x(t)$, to output, $y[n]$, which is later processed by e.g. a DSP .

Sampling is a process that converts a continuous time signal into a discrete time signal. The signal, $x(t)$, is sampled at a uniformly spaced time intervals, Ts. An anti-aliasing filter is usually placed before the sampling [1], to prevent the overlapping. The Nyquist theorem sets a boundary for the sampling frequency. A/D-converters that operates close to the boundary is called Nyquist-rate converters and converters that operate at a much higher frequency is called oversampling ADCs. The analog signal must also be mapped to discrete levels. This is done by the quantization process. The word length, in number of bits N, decides the resolution of the ADC and the number of levels is $2N$.

II. Implementation of a Passive Σ-Δ Converter

This section will describe the implementation of a low-cost passive **Σ**-Δ converter. First there will be a section about the system overview. Thereafter there will be a section about the implementation of the modulator itself. The System Overview is illustrated in Figure. 2 and the specifications for the proposed ADC are listed in the Table.1.

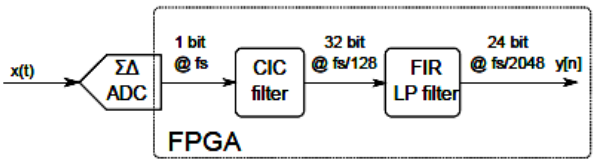


Figure 2: System overview of the passive **Σ**-Δ ADC.

TABLE I
SPECIFICATION FOR THE PASSIVE Σ-Δ ADC.

Specification	Symbol	Value
Sampling frequency	f_s	98.304MHz
Oversampling ratio	OSR	2048
Output sampling rate	f_{OUT}	48KS/s
Supply voltage	V_{dd}	3.3V (Single supply)
Input bandwidth	f_B	20KHz
Input voltage amplitude (max)	A_{in}	1.65 V

A. *The Passive Σ-Δ Modulator*

In order to cut the cost of an **Σ**-Δ ADC, the loop-filter consists only of passive components. The loop-filter of a typical (active) **Σ**-Δ is employing integrators with high gain (e.g. RC-integrators). One can make an integrator of passive components with e.g. a RC-filter, a so called "lossy integrator" with no gain. The linearization of the passive **Σ**-Δ is shown in Figure 3. The gain G is the gain of the quantizer /comparator [2].

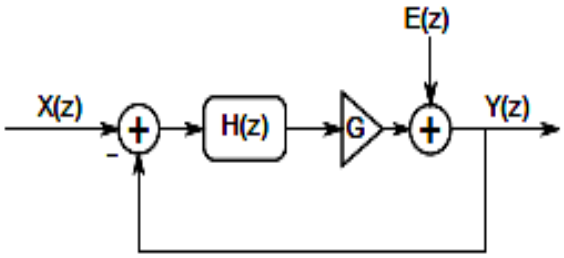


Figure 3: Linearization of the passive **Σ**-Δ ADC.

The transfer function becomes:

$$Y(z) = \frac{GH(z)}{1+GH(z)}X(z) + \frac{1}{1+GH(z)}E(z)$$

The gain factor G is assumed to be constant. [3] estimates the value of G by nulling the input, x. The 1-bit output, y[n], will alternate (ideally) between 0 and 1 at a rate of fs=2. This signal is then passed to the (low-pass) loop filter by a DAC. If the sampling frequency is high enough the signal is attenuated by a factor jH (f = fs=2) j, and this G is roughly:

$$G \approx \frac{1}{|H(f = f_s/2)|}$$

A first order RC-filter with transfer function

$$H(s) = \frac{1}{RCs+1} = \frac{1}{\frac{s}{w_p}+1}$$

The total system of the passive **Σ**-Δ converter is illustrated in Figure.4.

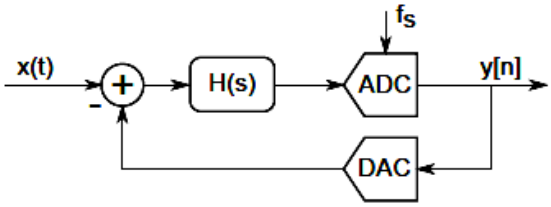


Figure 4: The passive **Σ**-Δ converter.

The ADC in Figure 4 is chosen to be a 1-bit quantizer, employing the LVDS buffer in the FPGA, sampled at fs = 98:304MHz. The DAC is chosen to be a 1 bit DAC, which only uses one pin on the FPGA. Figure 5 illustrate the 1-bit DAC. Here, the output of the FPGA is chosen to be a tri-state buffer and therefore the output of the DAC can either be Vdd, GND or T. This tri-state buffer can be used to create NRZ, RZ and HRZ DAC pulses. T stands for tri-state and is a high output impedance state (no current can flow out of the FPGA). NRZ pulses are either "high" or "low" for the whole sample period, i.e., it doesn't employ the T-state. On the other hand, the T-state can be used to implement RZ

and HRZ pulses which are "off" for half of the sample period. One thing to take into account is the parasitic capacitance associated with the pad, Cp. This capacitance is max 10pF [9]. This implies that the time constant, $R_{DAC}C_p$, is low.

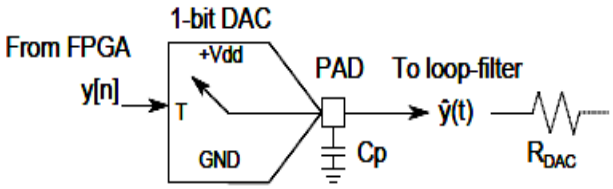


Figure 5: Simple illustration of an 1-bit DAC.

The chosen 1-bit DAC will use NRZ pulses because of the simplicity and "minimal" impact of the parasitic capacitance. The converter is therefore only using three pins on the FPGA: two for the LVDS buffer and one for the NRZ DAC.

B. *Realization of the Passive Σ-Δ Converter*

The Figure .6 illustrates the realization of the **Σ-Δ** converter. The 1-bit digital out will be further processed (filtered and decimated) by the CIC and FIR filter. The reference signal (vref) is mid-range, i.e. $Vdd=2 = 1{:}65V$. The chosen component values are presented in Table 2.

TABLE II
COMPONENT VALUES FOR THE PASSIVE **Σ-Δ** MODULATOR

Component	Value
RIN	6:8*K*
RDAC	6:8*K*
C	1*nF*
R	6:8*K*
CIN	1*μF*

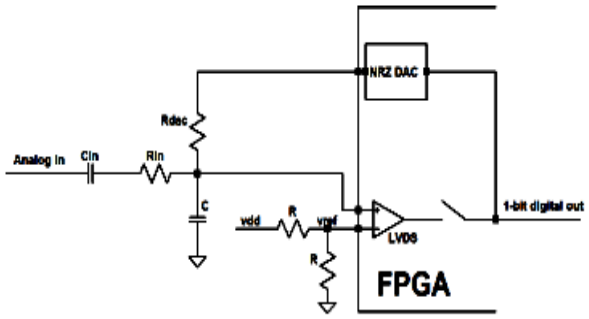


Figure .6: Realization of the passive **Σ-Δ** converter [6].

III. IMPLEMENTATION OF A SECOND ORDER Σ-Δ CONVERTER.

This section will describe the implementation of a second order **Σ-Δ** converter. The **System** Overview of the complete system of the second order **Σ-Δ** converter is illustrated in Figure. 7 and the system specifications are shown in Table 3.

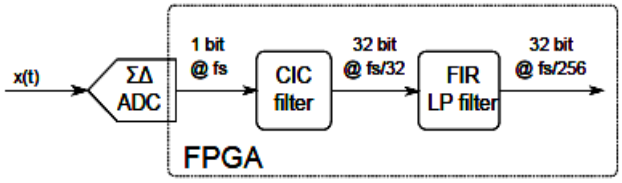


Figure 7: System overview of the second order **Σ-Δ** converter.

TABLE III
SPECIFICATION FOR THE SECOND ORDER **Σ-Δ** ADC.

Specification	Symbol	Value
Sampling frequency	*fs*	12.288MHz
Oversampling ratio	OSR	256
Output sampling rate	*fOUT*	48KS/s
Supply voltage	*V dd*	3.3V(single supply)
Input bandwidth	*fB*	20KHz
Input voltage amplitude (max)	*Ain*	1.65 V

A. *The 2nd Order CT Σ-Δ Modulator*

The 2nd order CT **Σ-Δ** feed-forward modulator is shown in Figure 8.

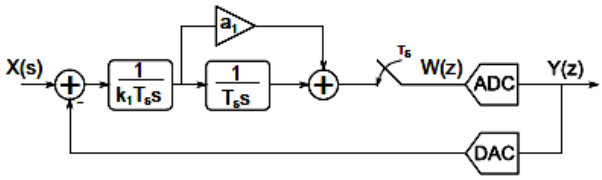


Figure 8: A 2nd order CT **Σ-Δ** feed-forward modulator.

The ADC is a 1-bit quantizer using the LVDS buffer (as a comparator) in the FPGA. The DAC is chosen to be a 1-bit DAC employing NRZ pulses. The DAC will only use one output pin on the FPGA. By using NRZ DAC, the coefficients $k1$ and $a1$ becomes 1 and 1.5, respectively.

B. *Realization of the 2nd order CT Σ-Δ modulator*

The realization of the modulator is shown in Figure 9. The loop-filter is a single amplifier section, derived from [24], this loop-filter only use one OP amplifier, which is better than two in a low-cost perspective.

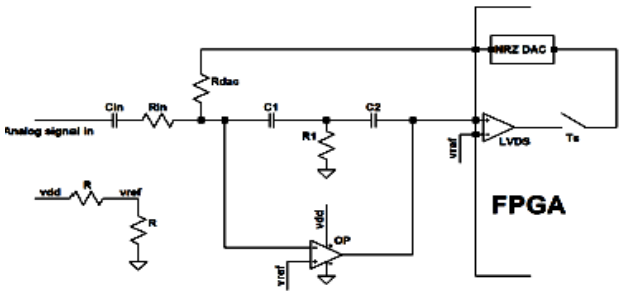


Figure 9: Realization of the 2*nd* order CT **Σ**-Δ modulator.

The reference voltage is mid-range, i.e. *Vdd*=2 = 1:65*V* and is generated by a voltage divider with two resistors. The transfer function from the DAC to the input of the LVDS buffer is:

$$H_\gamma(s) = -\frac{R_1(C_1+C_2)s+1}{R_{DAC}R_1C_1C_2s^2} = -\frac{a_1T_s s+1}{k_1T_s^2 s^2}$$

Where

$$R_1(C_1+C_2) = a_1T_s$$
$$R_{DAC}R_1C_1C_2 = k_1T_s^2$$

Table. 4 show the chosen component values. The chosen component values corresponds to $a1 = 2{:}5$ and $k1 = 156$.

TABLE IV
COMPONENT VALUES FOR THE LOOP FILTER IN THE SECOND ORDER Σ-Δ MODULATOR.

Component	Value
C1	100pF
C2	100pF
R1	1K
RDAC	100K
RIN	100K
R	4.7K
CIN	1μF

IV. Simulation Results

To observe the simulation results the PC generates a sine wave which is sent to an external sound card, the M-Audio Fast Track Pro. The sound card is then generating an analog signal of the sine wave which is sent to the DUT (Device under Test). The DUT is the converter under test, which is a PCB with the FPGA and external components. The result of the A/D-conversion, generated by the DUT, is then fed back to the sound card using S/PDIF with 24 bits resolution, which is then recorded by the PC. The collected data is analyzed in Matlab.

This section presents the simulation results for the two types of Σ-Δ converters. The simulation was done using Simulink / Matlab with the passive modulator and 2*nd* order CT **Σ**-Δ modulator. The filtering and decimation used in this simulation are "ideal", in order to characterize the **Σ**-Δ modulator only. Figure 10 shows an FFT plot of the output of the modulator. The input signal is 2 KHz and has an amplitude of 1V

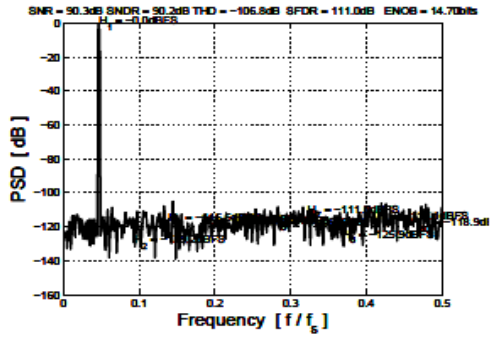


Figure 10: 1024 point FFT plot of the output of the passive **Σ**-Δ modulator.

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The Figure 11 shows the SNDR/SNR vs. input frequency and Figure. 12 show the SNDR/SNR vs. input amplitude of the output of the passive **Σ**-Δ modulator.

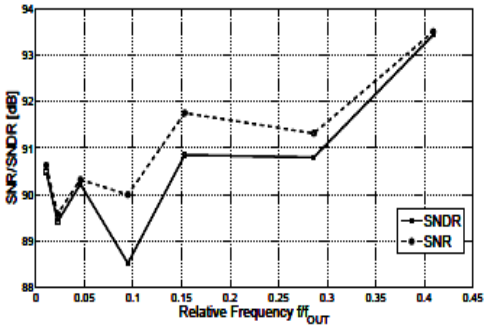


Figure 11: SNDR and SNR vs. Input Frequency. Using a 1V input signal.

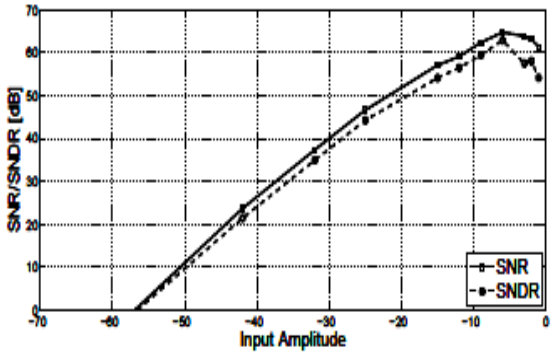


Figure 12: SNR and SNDR vs. input amplitude using a 7.3 KHz input signal.

The Figure.13 shows an FFT plot of the second order converter and Figure 14 shows SNR/SNDR vs. frequency of the output of the converter.

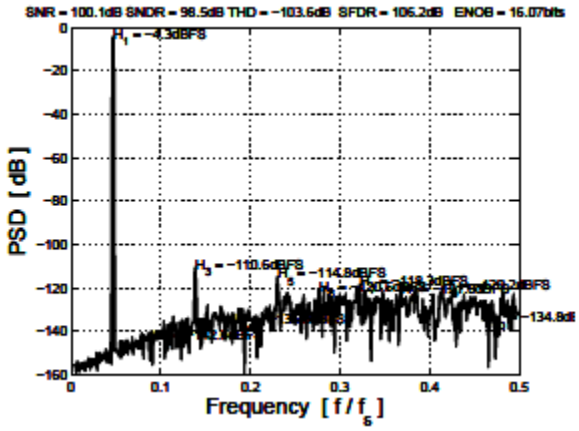


Figure 13: Simulation result of the second order **Σ**-Δ modulator using 1024 points FFT, 1V input amplitude (-4.3 dBFS).

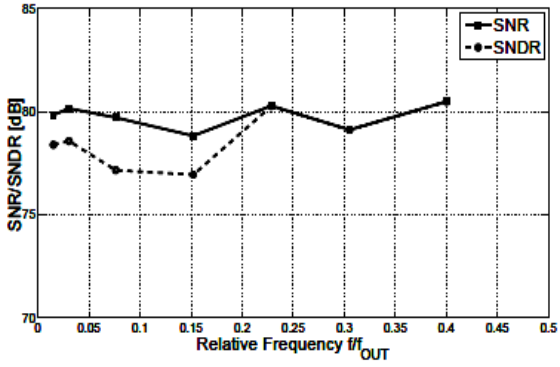


Figure 14: Simulation result of the second order **Σ**-Δ modulator, SNR/SNDR vs. Frequency.

Figure 15 shows the SNDR/SNR vs. input amplitude of the output of the **Σ**-Δ modulator.

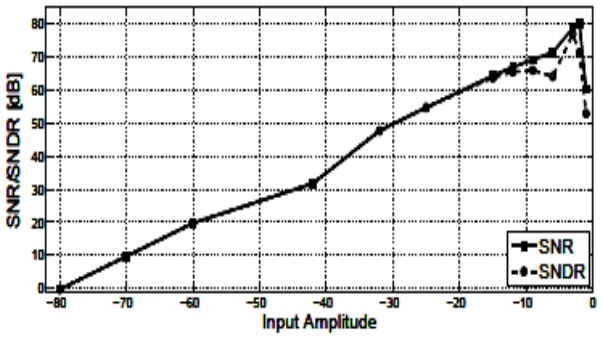


Figure 15: SNR and SNDR vs. input amplitude, using a 7.3 KHz input frequency.

CONCLUSION

The Table 5 shows a comparison between the passive **Σ**-Δ converter and the second order **Σ**-Δ converter and the converter that is used today in a product from Actiwave: PCM1807 from Texas Instruments. I have used the same test setup as indicated in section IV the PCM1807, except that it is powered from another power supply. Since the PCM1807 is a dual channel ADC, the resources are divided by two in order to compare it with my two solutions.

The prices of PCM1807 ($0.90) and LMV793 ($0.45) are taken from Texas Instruments website [5][3]. The prices for the passive components (resistors and capacitors) are set to $0.01. The prices don't include the decoupling capacitors needed. With proper design and careful PCB layout with the PCM1807, the theoretical SNDR is typical 93dB (ENOB _15.15) according to the datasheet of the PCM1807 [21]. But in order to compare the A/D converters, the same test setup is used (except for another power supply used for PCM1807).

According to Table 5, there can be conclusions:

1. The first order passive CT **Σ**-Δ is moderate in SNDR, but with low cost of external components and with relative large FPGA area. If there's a priority in low-cost the first order passive CT **Σ**-Δ is a good choice.
2. The second order CT **Σ**-Δ have the best SNDR, but with large FPGA area and highest cost per channel. With demands for good quality in SNDR the second order CT **Σ**-Δ is a good choice.

TABLE V
COMPARISON BETWEEN THE A/D CONVERTERS. SINCE THE PCM1807 IS A DUAL CHANNEL ADC, ITS RESOURCES ARE DIVIDED BY TWO.

Dynamic parameter	1st order passive CT Σ-Δ	2nd order CT Σ-Δ	Actiwave AB with T1PCM1807
SNR [dB]	63	80.3	77.9
SNDR [dB]	62.3	80.3	77.8
ENOB [bits]	10.06	13.04	12.63
Resources/channel FPGA			
I/O Pins	3	3	4/2
Slice regs	597	610	256/2
LUTs	408	426	146/2
Block RAMs	5	3	0/2
DSP	8	5	0/2
DCM/PLL	1	1	1/2
Resources/Channel Components			
Active components	0	1	1/2
Passive components	6	7	2/2
Total price [$]	0.06	0.53	0.46

3. The PCM1807 have good SNDR, small FPGA area and fairly high cost of external components. If there's demand for small FPGA area and good quality in SNDR an external ADC (such as the PCM1807) is a good choice.

There seems to be a tradeoff between quality (e.g. SNDR), FPGA area and cost. It is some difficulty to

compare the two converters presented in this paper with the PCM1807. For instance, PCM1807 need two voltages (3.3V and 5V) in order to function [7]. This adds up to the total price for the Actiwave AB solution, which is not listed in Table 5.

The two converters presented in this paper can easily be doubled in order to convert stereo audio (like the PCM1807). This doesn't necessary scale the resources of the FPGA and the total price by a factor of two. For instance, one can use LMV794 (which is two LMV793 in a single package) for the second order CT **Σ**-Δ converter in order to convert stereo audio. The price for LMV794 is $0.63 [4] which implies a total price of $0.71 for the second order CT **Σ**-Δ converter with dual channel. The corresponding total price for the PCM1807 (dual channel) is $0.92.

The two converters presented in this paper can be used for other purposes. For example, the passive **Σ**-Δ converter can easily be modified to be able to convert other analog signals, e.g. signals from sensors that perhaps only need 10 bits ENOB and is very low-cost.

The recommendation for Actiwave AB is not to use the passive CT **Σ**-Δ converter for audio applications. Since Actiwave AB is working with high precision audio, this is not an option. But the passive CT **Σ**-Δ converter can be used for other applications, e.g. convert analog signals from sensors.

To cut cost, Actiwave AB could use the second order **Σ**-Δ converter in a dual channel configuration (with LMV794) instead of the PCM1807. However, the LVM794 has to be tested and further investigation of the second order CT **Σ**-Δ converter is necessary in order to achieve 16 bits ENOB.

References

[1] Pervez M. Aziz, Henrik V. Sorensen, and Jan Van Der Spiegel. An Overview of Sigma-Delta Converters: How a 1-bit ADC achieves more than 16-bit resolution. IEEE Signal Processing Magazine, 13:61, 1996. Cited on pages 10 and 11.

[2] Feng Chen and Bosco Leung. A 0.25-mW Low-Pass Passive Sigma-Delta Modulator with Built-In Mixer for a 10-MHz IF Input. IEEE Journal of Solid- State Circuits, 32(6):774–782, 1997. Cited on pages 34 and 35.

[3] Texas Instruments. LMV793, July 9 2013. http://www.ti.com/product/lmv793. Cited on page 57.

[4] Texas Instruments. LMV794, July 9 2013. http://www.ti.com/product/lmv794. Cited on page 58.

[5] Texas Instruments. PCM1807, July 9 2013. http://www.ti.com/product/pcm1807. Cited on page 57.

[6] Lattice Semiconductor Corporation. Simple Sigma-Delta ADC, November 2010. RD1066. Cited on pages 2, 37, and 62.

[7] Texas Instruments. PCM1807: Single-Ended, Analog-Input 24-Bit, 96-kHz Stereo A/D Converter, September 2005. SLES147. Cited on pages 1, 57, and 58.

[8] Lars Wanhammar. Analog Filters Using MATLAB. Springer, 2009. ISBN 978-0-387-92766-4. Cited on pages 24, 48, and 61.

[9] Xilinx. Spartan-6 FPGA Data Sheet: DC and Switching Characteristics, v.3.0 edition, October 2011. DS162. Cited on pages 6 and 36.

[10] Axel Zimmermann, Endric Schubert, and Christian Grumbein. Integration of Analog-Digital and Digital-Analog Converters into FPGA-Based Microcontrollers. 2011. Cited on page 2

Comparison of Adaptive Filtering Algorithms Based on Time Varying Weighting Factor

Mohammed Abdul Nasar
CVR College of Engineering/ECE Department, Hyderabad, India
Email: nasar.mohammed@gmail.com

***Abstract*—In this paper, a Leaky Time Varying Mean Mixed Norm Adaptive algorithm is proposed. The weight drift issue is overcome by minimizing the function defining weighted sum of the LMS and LMF cost functions along with the leakage factor. The weighting factor is applied in time varying environment and made to adapt itself so as to emphasize one cost function over the other based on closeness to the optimum value. The proposed algorithm results are compared with the conventional algorithms and the obtained results show an improvement over the convergence.**

***Index Terms*— Adaptive Filters, Fixed Mixed Norm (FMN), Variable Leaky LMMN (VLLMMN)**

I. INTRODUCTION

The least mean-square (LMS) [3] algorithm and the least mean-fourth (LMF) [4] algorithm can be generalized as minimization of the mean-*kth* error function, that is $J_n = E[e_n^k]$, k is some positive integer, when k=2 and k=4 are substituted above, the equation results in the LMS and LMF algorithms [1,2] respectively.

As can be seen from Figure (1), adaptive filters can be used to solve the problem of system identification, wherein a model is created to overcome the uncertainties in the system when its parameters are unknown to us and may be time varying. In such cases same input x_n is being fed to both the adaptive filter and the system under modeling. The difference between them d_n and the responses of the adaptive filter y_n and the system are then compared i.e. the error e_n is used to adjust the parameters of the filter. With the increase in the number of iterations, the parameters of the adaptive filter reach an optimum value or approach to those of unknown system parameters as it is clearly evident from Figure (1).

In previous work [9], it's been noticed that LMF algorithm performs well compared to the LMS algorithm in the environment which is non-Gaussian. As a variant of the LMS algorithm we find another example of adaptive filter algorithms is the leaky Least Mean Square (leaky LMS) algorithm [10]. So the leaky LMS algorithm was first introduced to overcome the weight drift problem occurring in the LMS adaptive filters which usually occurs due to insufficient excitation of the input. Following the same analysis it's seen that the LMF algorithm also suffers from the weight drift problem under the same conditions as LMS algorithm. Making use of the best properties of these two algorithms leads us to the LMMN algorithm [5], which is found to provide a better performance in different noise environments like Gaussian and Non-Gaussian compared to either LMS or the LMF. But even LMMN algorithm undergoes a weight drift problem under insufficient excitation of the input signal.

The LMS algorithm which reduces the square of the error is a very well known algorithm in adaptive filtering, while the LMF algorithm which reduces the fourth of the error has been proposed in [4] and gained much attention in the literature proposed in [5]-[7]. Both the algorithms are robust to the noise statistics in different environments like Gaussian noise, Uniform noise to name a few, because of which their convergence behaviour are different [4]. From the above discussion it is well understood that the larger gradient of LMF algorithm makes the convergence faster when away from the optimum ($e_n^4 > e_n^2$ for $e_n^2 > 1$). But more desirable characteristics in the neighborhood of optimum are obtained by making use of LMS algorithm.

In the literature work the weighted sum of the two performance measures has been utilized and was proposed to combine the advantages of both in the mixed-norm adaptive algorithm [5]. The mixed-norm LMS-LMF adaptive algorithm is defined by the following cost function:

$$J_n = \delta E[e_n^2] + (1-\delta)E[e_n^4] \quad (1)$$

Where $\delta \in [0,1]$ controls the mixture of the mixed norm algorithm i.e. a value of $\delta = 1$ in the above equation results in LMS algorithm whereas a value of $\delta = 0$ leads to the LMF algorithm convergence behavior respectively. e_n is the error between the adaptive filter and the unknown system output and is usually defined as

$$e_n = y_n - x_n w_n \quad (2)$$

where y_n is the desired value, w_n is the filter coefficient

of the adaptive filter being employed, and x_n is the input vector.

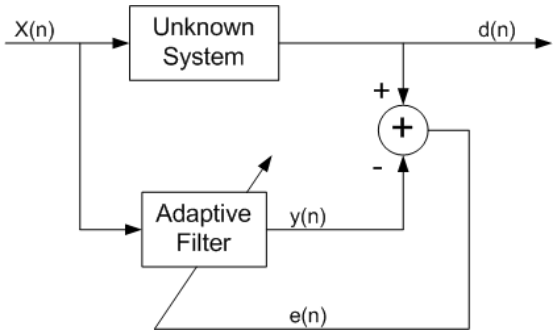


Figure1: Block Diagram of Adaptive System Identification.

So the combination of the conventional LMS and LMF algorithms give LMMN algorithm. But at some times the LMMN algorithm continues the error controlling process even if the input is not present i.e. what we call as weight drift problem in case of adaptive algorithms. To overcome this problem of weight drifting a leakage factor is introduced in the algorithm giving rise to Leaky LMMN algorithm [9].

The LMMN cost function is modified a little bit to obtain Leaky LMMN by introducing a leakage parameter ε in the same way as was done in the literature for the case of the leaky LMS [8]. The term leakage stems out from the fact that, unlike the conventional LMS, where weights remain stationary in case of stalling, in Leaky LMMN the weights "leak out" in case of stalling occurs i.e. the input sequence becomes zero. Therefore, the cost function that is required to minimize the error is given as

$$J(w) = \varepsilon \| w \|^2 + \{\delta E[e_n^2] + (1-\delta) E[e_n^4]\} \quad (3)$$

Where *J* is the cost function in finding out the optimum weight vector δ controls the mixture of the mixed norm algorithm related to the error vector e_n and ε is the leakage factor which mitigates the weight drift problem occurring in the mixed norm algorithm. Following the above discussion the normalized weight error in the case of Leaky LMMN can be obtained from [9] as

$$\| \tilde{w}_{n+1} \|^2 = (1-\mu\varepsilon)^2 \| \tilde{w}_n \|^2 + \mu^2 \| u_n \|^2 v_n^2$$

So that $\| \tilde{w}_n \|^2$ remains bounded for $0 < \mu\varepsilon < 1$.

II. PROPOSED ALGORITHM

The algorithm defined in equation (3) works when the "mixing" parameter or weighting factor is fixed and is does not consider the leakage in the time varying environment and is usually predetermined. In this paper, a self-adapting time variable weighting factor is considered that brings our proposed algorithm to the LMF algorithm when the coefficient vector is away from the optimal value and on the other hand emphasizes the LMS algorithm when the coefficient vector is close to the optimum. Here a time varying weighting factor is proposed to allow the algorithm to adapt itself to the changing input conditions and is denoted as variable δ_n. This factor is then updated every iteration so it is large when we are away from the optimum and decreases as we approach towards the optimum.

In the derivation of the proposed algorithm, modified variable step size (MVSS) algorithm is being used as proposed in [7] to update the weighting factor δ_n. The proposed variable weight leaky mixed-norm LMS-LMF algorithm required to minimize the performance measure can be thus defined as:

$$J(w) = \varepsilon \| w \|^2 + \{\delta_n E[e_n^2] + (1-\delta_n) E[e_n^4]\} \quad (4)$$

where δ_n is a time varying parameter updated according to:

$$\delta_{n+1} = \alpha\delta_n + \gamma p^2(n) \quad (5)$$

and

$$p(n) = \beta p(n-1) + (1-\beta) e(n) e(n-1) \quad (6)$$

The parameters α and β, are the exponential weighting parameters governing the average time constant and are usually confined to the interval [0, l], i.e., these parameters are responsible for the quality of estimation, and $\gamma > 0$. It can be observed from the algorithm defined in equation (1) that it can be restored efficiently when $\alpha = 1$ and $\gamma = 0$, i.e., δ_n is chosen to have a fixed value.

If the constraints α and γ as defined in equation (5) are given, than making use of uni-modal character the cost function defined in equation (3) can be preserved.

Following the discussion above it motivates for the development of the proposed algorithm that recursively adjusts the coefficients of a leaky system which is expressed in the following form, i.e., update equation of the variable leaky LMMN can be written as:

$$w_{n+1} = (1-\mu\varepsilon) w_n + \mu e_n \{\delta_n + (1-\delta_n) e_n^2\} x_n \quad (7)$$

where μ is the step size chosen small enough for the convergence of the algorithm to take place and the sufficient condition for the convergence of the proposed algorithm in the mean square sense can be found out in the same way as the approach used for the mean convergence on the step size and is usually is governed by the equation

$$0 < \mu < \frac{2}{\varepsilon + [E[\delta_n] + 3E[(1-\delta_n)](\sigma_v^2 + \vartheta)\lambda_{\max}(R)]} \quad (8)$$

where Where $\lambda_{\max}(R)$ is the largest eigen value of R, σ_v^2 is the input noise power and $E[\delta_n]$ is the mean of the mixing parameter.

From Equation (6), *p(n)* can be set recursively in the following form:

$$p(n) = (1-\beta)\sum_{i=0}^{n-1} \beta^i e(n-i)e(n-i-1) \quad (9)$$

and therefore

$$p^2(n) = (1-\beta)^2 \sum_{i=0}^{n-1}\sum_{j=0}^{n-1} \beta^i \beta^j e(n-i)e(n-i-1)e(n-j)e(n-j-1) \quad (10)$$

Making use of the above set of recursive equations an expression for the mean of the mixing parameter, namely $E[\delta_n]$ can be obtained as

$$E[\delta_{n+1}] = \alpha E[\delta_n] + \gamma(1-\beta)^2 \sum_{i=0}^{n-1} \beta^{2i} \times E[e^2(n-i)] \times E[e^2(n-i-1)] \quad (11)$$

In the above Equation, its been assumed that the algorithm has converged, and in this case the samples of the error e(n) can be assumed uncorrelated, i.e., $E[e(n-i)e(n-j)] \simeq 0$, $\forall (i \neq j)$.

Also, the mean-square error (MSE) can be set into the following:

$$E[e^2(n)] = E[e_a^2(n)] + \sigma_n^2 \quad (12)$$

where σ_n^2 and $E[e_a^2(n)]$ are the noise power and the excess MSE, respectively.

III. SIMULATION RESULTS

The signal to be processed is worked out for both Gaussian and Uniform noise environment and then the time Variable Leaky Least Mean Mixed Norm (VLLMMN) algorithm is compared to the Fixed Mixed-Norm (FMN) LMS-LMF algorithm in terms of faster convergence. The input signal x_n which is not known to the system and to the adaptive filter is considered to be ± 1 sequence and the channel used is $w_o = [0.3482, 0.8704, 0.3482]^T$.

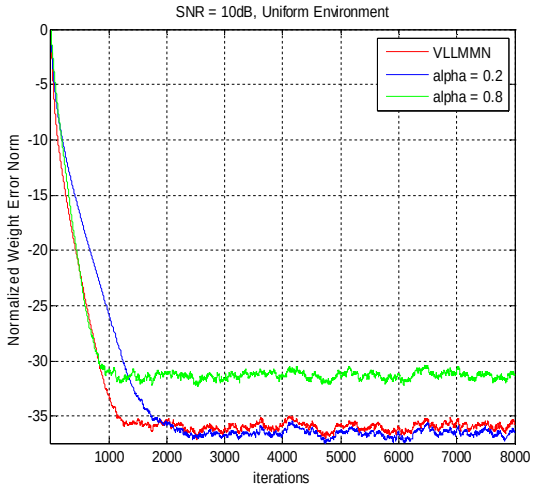
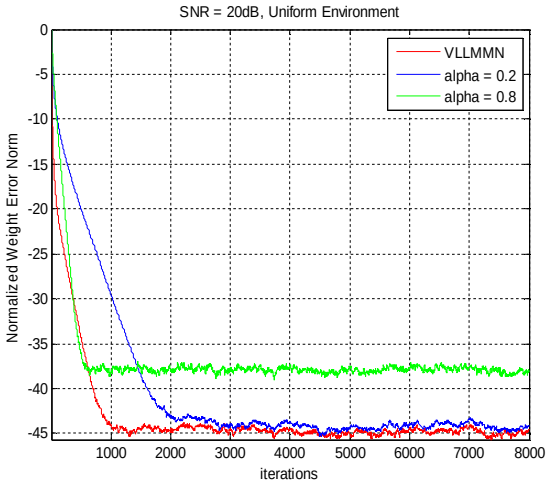


Figure 2: Behaviour of Proposed and the FMN algorithm in Uniform



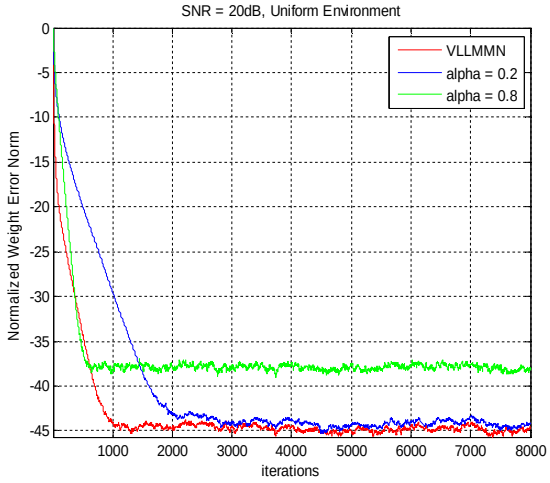


Figure 3: Behaviour of Proposed and the FMN algorithm in Uniform Noise and noise variance 0.2

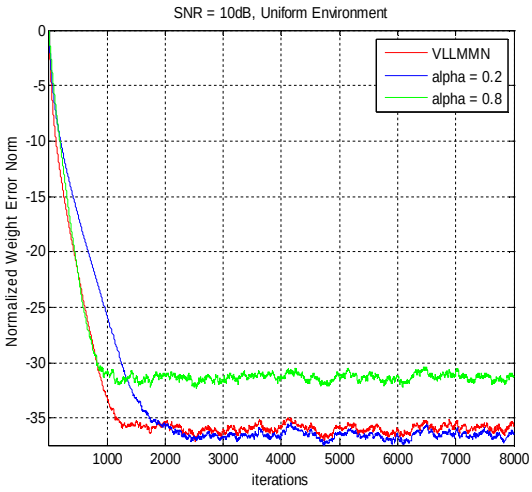


Figure 2: Behaviour of Proposed and the FMN algorithm in Uniform

Considering a white input data, where the variance of the regressors is set to unity and maintaining all the parameters as defined above, the simulations in this paper are performed for Uniform and Gaussian noise environments with noise variance i.e Signal to Noise ratio (SNR) value set at 10 dB and 20 dB respectively. The performance measure considered is the normalized weight error norm $10\log_{10} \| w_n - w_o \|^2 / \| w_o \|^2$ with the number of taps set to 5. The additive noise is a zero mean and has a Gaussian distribution. Results are obtained by averaging 8000 samples over 100 independent runs.

Now comparing the time varying algorithm to the fixed mixed-norm algorithm for different values of mixing parameter δ .

From the above figures the fixed mixed norm algorithm is considered with $\delta = 0.8$ and $\delta = 0.2$. The FMN algorithm with $\delta = 0.8$ behaves almost similarly to the LMS algorithm whereas the FMN algorithm with $\delta = 0.2$ emphasizes the approach towards the LMF algorithm. The superior performance of the proposed algorithm compared to the conventional algorithms can be observed from the Figures (2-5) where in the proposed Variable Leaky LMMN algorithm results outperform the two versions of the FMN algorithm. This is a result of the fact that the mixing parameter for the proposed algorithm is time varying, which accommodates itself according to changes in the environment.

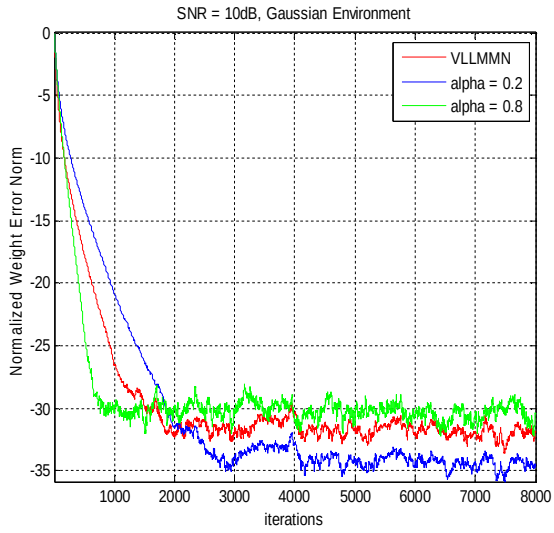


Figure 4: Behaviour of Proposed and the FMN algorithm in Gaussian Noise and noise variance 0.1

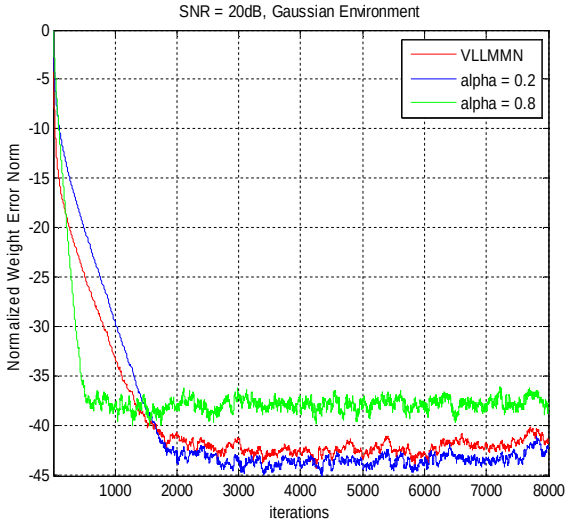


Figure 5: Behaviour of Proposed and the FMN algorithm in Gaussian Noise and noise variance 0.2

It is clearly noticeable from figures (2-5) that the proposed Variable Leaky Least Mean Mixed Norm Algorithm (VLLMMN) algorithm totally overcomes the FMN algorithm. With $\delta = 0.8$, it is observed from the simulations that the later has the same convergence rate as that of the proposed algorithm but results in larger excess steady state MSE. On the other hand, when $\delta = 0.2$ is considered for the FMN algorithm as compared with the proposed VLLMMN algorithm, it results in the same excess steady state MSE as the proposed algorithm, but the later has a faster speed of convergence.

CONCLUSIONS

A time varying mixed-norm algorithm i.e Variable Leaky Least Mean Mixed Norm Algorithm (VLLMMN) is proposed herein, where a combination of the LMS and the LMF algorithms is incorporated using the concepts of variable step size LMS adaptation. It is found to outperform both the LMS and the LMF algorithms in the time varying environment. A bound on the step size to ensure convergence in the mean is also provided. Finally, the consistency and the performance of the proposed algorithm are supported by the simulation results.

REFERENCES

[1] A.H. Sayed, Fundamentals of Adaptive Filtering. New York, NY:Wiley Interscience,2003.

[2] S. Haykin, *Adaptive Filter Theory*, Prentice- Hall, Englewood Cliffs, NJ, 1991.

[3] B. Widrow, J. M. McCool, M. G. Larimore, and C. R. Johnson, "Stationary and Nonstationary Learning Characteristics of the LMS Adaptive Filter," *Proc. IEEE, vol.* 64, No. 8, pp. 1151-1162, Aug. 1976.

[4] E. Walach and B. Widrow, "The Least Mean Fourth (LMF) Adaptive Algorithm and its Family," *IEEE Trans. Inf. Theory, vol.* IT- 30, pp. 275-283, Feb. 1984.

[5] J. A. Chambers, 0. Tanrikulu, and A. G. Constantinides, "Least mean mixed-norm adaptive filtering," *Electr. lett., vol.* 30, *No.* 19, pp. 1574-1575, Sep. 1994.

[6] A. Zerguine, C. F. N. Cowan, and M. Bettayeb, "Novel LMS-LMF Adaptive Scheme for Echo Cancellation," *Electr. lett., vol.* 32, No. 19, pp. 1776-1778, Sep. 1996.

[7] T. Aboulnasr and K. Mayyas, "A Robust Variable Step-Size LMS-Type Algorithm: Analysis and Simulations," *IEEE Trans. Signal Processing, vol.* SP-45, No. 3, pp. 631-639, March, 1997.

[8] W. Sethares et al, "Parameter Drift in LMS Adaptive Filters", IEEE Trans. Accoustics, Speech and Signal Processing, Vol. ASSP-34, No.4, August 1986

[9] Mohammed Abdul Nasar, "The Leaky Least Mean Mixed Norm Algorithm" ISSN 2277-3916, CVR Journal of Science and Technology, Volume 5, December 2013.

[10] R.D. Gitlin, H.C. Meadors and H.B. Weinstein, "The Tap Leakage Algorithm: An Algorithm for the Stable Op-eration of a Digitally Implemented Fractionally-Spaced Adaptive Equalizer," Bell Sys. Tech. Journal, vol. 61, pp. 1817-1840, Oct. 1982.

Design and implementation of High Performance Voltage-Controlled Oscillator using CMOS Technology

G.Venkateswarlu
CVR College of Engineering/EIE, Hyderabad, India
Email: venkigummadilli@gmail.com

Abstract— **In recent years, oscillators are considered as inevitable blocks in many electronic systems. They are commonly used in digital circuits to provide clocking and in analog/RF circuits of communication transceivers to support frequency conversion. Nowadays, CMOS technology is the most applicable solution for VLSI and especially for modern integrated circuits used in wireless communications. Additionally, the trend towards single chip implementation makes the circuit design increasingly challenging.**

The main purpose of this paper is to design a high performance voltage controlled oscillator (VCO) using 90nm CMOS technology. In the beginning, a brief study of different VCO architectures is carried out. Next, a wide comparison between different VCO topologies is performed in terms of phase noise and power consumption. The effect of VCO phase noise on RF transceivers is also analyzed. In the following, all the phase noise contributors in a typical VCO are identified to enable design optimization. To meet the state-of-the-art requirements, several circuit solutions have been explored and the design work ended-up with a Quadrature VCO. The design is verified for the intended tuning range and process, temperature, and supply voltage (PTV) variations. The circuit operates at center frequency of 2.4 GHz. The phase noise of QVCO obtained by simulation is -140 dBc/Hz at 1MHz offset frequency which is 6 dB less compared to conventional VCOs. The power consumption is 3.6mW and the tuning voltage can be swept from 0.2 V to 1.2 V resulting in 2.25 GHz - 2.55 GHz frequency range..

Index Terms— **QVCO, Power Consumption, Phase Noise, Tuning Voltage, Communication Transceivers.**

I. INTRODUCTION

Voltage-controlled oscillators are mostly implemented as a component of phase locked loops (PLLs). PLLs can be used in different areas such as clocking of microprocessors, providing carriers for wireless transceivers or other transmission systems. Usually, in communication applications PLLs require VCOs with a wide tuning range to serve up- or down-conversion over the system bandwidth. Interestingly, in PLLs the VCO phase noise requirements can be relaxed. In other words, the noise produced by a voltage-controlled oscillator at the oscillation frequency will be to some extent filtered out by the system. Therefore, VCO topologies with wide tuning range are usually preferred.

In high performance applications where a low phase noise or jitter is required, VCOs using LC tanks are preferred for their high Q-factor. Therefore, LC-based VCOs will be in focus of the presented designs.

To design a VCO, different requirements should be fulfilled. In this section, we define the VCO metrics individually. In particular, we should meet the oscillation frequency, power consumption, tuning range and phase noise requirements which are the most important in a VCO design. The oscillation frequency may vary from one design to another due to different applications and architectures.

The tuning voltage range is determined by required frequency variations in different applications. The other major issues that should be considered especially in a high performance VCO design are phase noise and power consumption. Generally, it is difficult to fulfill all of the requirements at the same time. For instance, there is usually a tradeoff between power consumption and phase noise. On the other hand, some VCO topologies can improve the phase noise performance while other architectures can dissipate less power. Consequently, regarding the design specifications and their priorities, the designers have to choose the appropriate VCO topology but still are exposed to design tradeoffs. The specifications for our ultimate VCO design aimed at 90-nm CMOS technology are as shown in Table 1.

TABLE I
Ultimate VCO design specifications.

QVCO specifications	Value
Center frequency	2.4GHz
Supply Voltage	1.2V
Phase noise at 1MHz offset frequency	< -130dBc/Hz
Power Consumption	<5mW
Tuning Voltage	0.2-1.2
Frequency range	V2.25-2.55GHz

II. DESIGN AND IMPLEMENTATION OF QVCO

In this section, we present some low phase noise LC architectures. One of the most recent topologies is a quadrature VCO with integrated back gate coupling. Nowadays, quadrature VCOs are widely applicable in transceivers. One of the drawbacks of this topology is higher power consumption than the LC VCO architectures. To get an optimum result regarding the power and the phase noise simultaneously, a much simpler design is presented. At the end of this chapter, we compare all of the benefits and drawbacks of different VCO architectures[1]. Finally, a low noise low power CMOS LC oscillator is designed.

A) Low Phase Noise QVCO

Nowadays, CMOS technology is the most applicable solution for modern wireless communication devices. The challenge of being implemented on a single chip makes the design much complicated. In this topology, high efficient transmission is performed by the help of quadrature-amplitude modulation and the frequency division technique. Recently, some transceivers use quadrature oscillators to drive mixers for performing frequency conversion. However, the signal is susceptible to the phase noise disturbances. There are different methods to produce the quadrature signal. The differential voltage controlled oscillator, the quadrature coupling of two simple LC VCOs, the ring oscillators and the frequency division technique are the most common procedures for producing a low phase noise signal. The quadrature topology is popular among designers due to its high performance regarding the phase noise. The quadrature topology can be done in different ways. Back-gate coupling or adding some transistors to the VCO core are some common procedures. One of these approaches is called source resistive degeneration which has a noticeable impact on phase noise improvement in quadrature VCOs. In this state-of-the-art design, we take advantage of source resistive degeneration and back gate coupling simultaneously. In other words, we put the both procedures into one single model to achieve a significant output with low power dissipation and low phase noise at the same time.

In this section, a 90nm CMOS quadrature VCO with a s ignificant low phase noise is designed. As mentioned in introductory section, we mix two different methods
into one model to achieve the best phase noise performa nce. As observed in the final simulation results, the phase noise and the power consumption have improved significantly in a well designed QVCO[8]. However, a larger area on the chip should be dedicated for the design. Overall, we achieve an optimum performance regarding the phase noise and power consumption.

The phase noise is -140 dBc/Hz at I MHz offset from 2.4 GHz. The QVCO consumes 3 mA from a 1.2V power supply. The QVCO circuit schematic is shown in the Fig. .1. The two CMOS VCOs are coupled back to back by their gates. In other words, the
circuit consists of two CMOS LC VCOs with eight trans istors. In our design the PMOS bulks of each VCO are connected by coupling capacitors as shown in the circuit schematic.

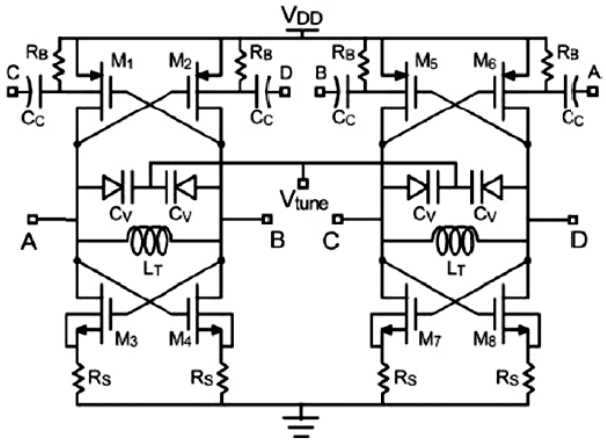


Figure. 1: Circuit schematic of Quadrature VCO

This technique used in our quadrature VCO has an advantage comparing with conventional VCOs. As we notice in old QVCO designs, four more transistors are used as coupling elements [3]. A simple conventional quadrature VCO is depicted in fig.2.

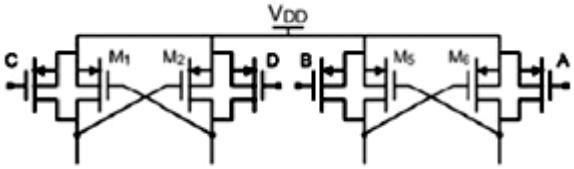


Figure 2:Conventional Quadrature VCO

In our proposed design, these extra transistors are omitte d due to the back-gate coupling technique.
Consequently, the circuit performance improves due to the reduction of noise sources. As described in previous chapters, adding more transistors leads to extra noise of the circuit. Flicker noise of NMOS and PMOS transistors are the main factors that should be considered in our design.

Therefore, the corresponding phase noise can be formul ated as following:

$$L(\Delta\omega) = 10\log\left[\frac{c_0^2}{q_{max}^2}\left(\frac{\overline{i_{n,N}^2}/\Delta f}{2.\Delta\omega^2}.\frac{\omega_{1/f,N}}{\Delta\omega} + \frac{\overline{i_{n,P}^2}/\Delta f}{2.\Delta\omega^2}.\frac{\omega_{1/f,P}}{\Delta\omega}\right)\right]$$

This technique gives more symmetry to the drain current. In this case, more improvement in phase noise is achieved. A designer might think that this technique can be considered for PMOS transistors as well. However, in our circuit, the PMOS transistors should have quite large gm for phase locking. Consequently, this procedure might not be suitable for PMOS transistors. On the other hand, we encounter some limitations when designing the Rsource. High Rsource value can ruin the oscillation initial condition and produce some additional disturbances.

The circuit is designed in CMOS 90nm technology. There is a big challenge for selecting a proper inductance. The quality factor of the inductor should be considered as well. We use a spiral structure for designing the inductor. Its value is 2.1 nH and its corresponding quality factor is 15. As observed in the final results, the value of Rsource is 26 ohm.

The oscillation frequency is functioning between 2.25 to 2.55 GHz when the Vtune is tuned from 0.2 to 1.2 V. Our designed output power varies from -0.5 to -1.6 dBm. In the frequency range of 2.25 to 2.55 GHz, the best result is achieved at 2.4 GHz. The varactor used in our design has a hyperbolic capacitance versus voltage curve. This makes the middle of tuning range a critical point. At 2.4 GHz, the phase noise is -140dBc/Hz at 1 MHz offset frequency. Our designed quadrature VCO consumes 3mA from a 1.2V supply voltage. The equation for calculating the figure of merit for VCO is as following:

$$\mathrm{FOM} = \mathrm{L}\{\Delta\omega\} - 20\log\left(\frac{\omega_0}{\Delta\omega}\right) + 10\log(P_{\mathrm{DC}})$$

As described in the introductory part, we have designed a 2.4 GHz quadrature VCO. Its corresponding phase noise is -140 dBc/Hz at 1 MHz offset frequency. In the design procedure, two simple CMOS LC VCO are coupled together to satisfy the oscillation condition at the desired frequency. The body terminal of PMOS transistors are connected together via coupling capacitors. Additionally, four resistances are added to the source of NMOS transistors to reduce the transconductance as much as possible. Therefore, we have less gm variation at the output. On the other hand, phase noise is decreased as well. This is called source resistive degeneration technique.

III. Low Noise Low Power CMOS LC VCO

Oscillators are inevitable blocks in designing communication systems. There are different LC VCO topologies in communication electronics. LC VCOs are mainly applicable in highly efficient transmitters and receivers. VCOs are used as inputs for the mixers to produce desired outputs. Therefore, they are quite noticeable in highly integrated transceivers. Low noise and high signal amplitude should be achieved for obtaining a reasonable performance in a VCO design. To obtain a state-of-the-art design, two specifications should be met at the same time. LC VCOs are mostly popular due to this issue. They achieve an ultra-low noise with low power dissipation simultaneously. Therefore, the designers are encouraged to design efficient LC VCO topologies. Nowadays, lots of investments have been focused on designing CMOS LC VCOs using on-chip resonators. The drawback is that fully integrated LC VCOs consume lots of power. Therefore, external LC VCO topologies are still used in recent cell phones. In this design, we aim for an optimal circuit using fully integrated VCOs. Our goal is to produce outputs with lower phase noise and power dissipation comparing with conventional off-chip LC VCO topologies[2]. This work mainly concentrates on design of fully integrated VCOs with optimized power consumption and phase noise lower than VCOs with external resonators. For this design, we mainly discuss the complementary LC VCO structure. Then, we compare its performance, regarding phase noise and power consumption, with conventional VCOs.

There are some noticeable advantages that make CMOS LC VCO an identical topology. Complementary VCOs are more economical than their conventional counterparts. Old topologies use only NMOS or PMOS transistors. In our design, we use both type of transistors at the same time. By adding PMOS transistors to conventional NMOS only VCOs, much larger transconductance is achieved. As we know, the tank used in the circuit is lossy. Since we generate a noticeably large transconductance, less current is needed to compensate the resonator loss.

Therefore, much power is saved in this topology. On the other hand, using the PMOS and NMOS pairs simultaneously, we produce symmetrical waveforms at the output. Consequently, the flicker noise upconversion to the 1/f3 region is reduced[6]. The CMOS LC VCO is illustrated in the Fig.3.

If the VCO requirements are fulfilled, the circuit oscillates properly. In the theory, the amplitude increases gradually and stops in a point. Actually, when the negative resistance cannot compensate the resonator loss any further, the output will be stable. However, it is the case when the Vdd is not putting constraints on the output swing at the oscillation startup point. When operating at the current limited regime, the CMOS cross-coupled VCO is the best choice for the state-of-the-art design. Applying the same voltage and bias current, it generates a better phase noise comparing with its NMOS or PMOS counterparts. The phase noise can be analyzed in different aspects. First, the CMOS cross-coupled VCO tolerates a larger charge for the

output swing. This maximum swing is illustrated as qmax in the Hajimiri's model. As the phase noise is inversely proportional to the maximum charge, the CMOS cross-coupled VCO generates a better phase noise comparing with its conventional counterparts. On the other hand, we can improve it to the Without Tail (WT) structure. The WT structure shows even a better performance than the fixed biasing topology. In the WT topology, the number of transistors is reduced.

In another words, we decrease the number of noise sources. Therefore, the flicker noise sources are just of the cross-coupled pairs. Since switched biasing is applied in the design, the cross-coupled pairs do not affect the phase noise performance that much due to their low flicker noise. Overall, in this design, we improve the phase noise performance by omitting the tail transistor. On the other hand, since the tail transistor is neglected

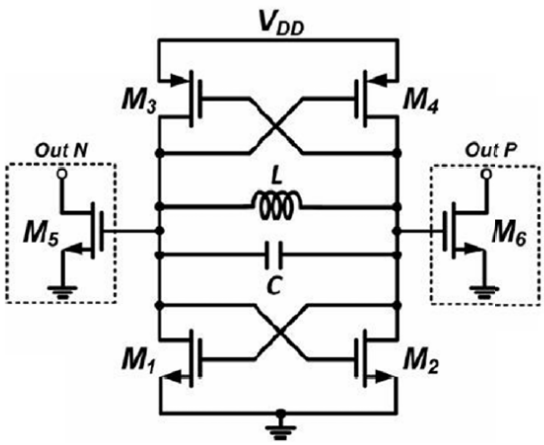


Figure.3: CMOS LC Oscillator cirut schematic

The transconductance produced by cross-coupled pairs should be inversely proportional to the overall resistance of the resonator. As obtained in our experimental simulations, we can optimize the power dissipation by improving the quality factor of our resonator. As a matter of fact, this will optimize the required transconductance as well. However, using fully integrated inductors generates some obstacles for the design. Fully integrated VCOs have low quality factors. On the other hand, there are some boundaries for increasing the quality factor of the inductors.

A. Power Analysis

If we apply Vdd as our supply voltage to the circuit, the voltage measured at the output could be estimated as Vdd/2. Vm represents the output amplitude by which the gate to source voltages can be formulated as following:

$$V_{gs1}=V_{dd}-V_{gs3}=V_{dd}/2+V_m\sin(\omega t)$$

$$V_{gs2}=V_{dd}-V_{gs4}=V_{dd}/2-V_m\sin(\omega t)$$

The NMOS transistors switch on when Vgs≥Vth,NMOS and the PMOS transistors switch on when Vsg ≥ |Vth,PMOS|. As observed in the theory, if we subtract the NMOS and PMOS current from each other the resonator current will be identified. Since one of the PMOS or NMOS transistors is switched on at each cycle, a larger current is conducted into the resonator. Consequently, when the current is driven by one of the M1 or M3 at each cycle, the power dissipation is reduced. On the other hand, since we reduce the number of transistors in each cycle, less noise is driven into the resonator. As observed in above equations, we should consider some limitations for choosing the right supply voltage. If we apply a supply voltage which is larger than the overall threshold voltage of the M1 and M3 transistors (Vth,NMOS + Vth,PMOS), they will be switched on at the same time.

Consequently, the circuit dissipates more power and extra noise will be conducted into the resonator. Increasing the overall noise in the circuit has an inverse impact on the phase noise performance. Overall, to dissipate less power and improve the phase noise performance, we should present a state-of-the-art structure. In this topology, M1 and M3 are not allowed to conduct at the same time in each cycle. This is the same case for M2 and M4 transistors. Now, it is understood the reason to minimize the supply voltage to overall threshold of PMOS and NMOS transistors. Applying the Vdd equal to Vth,NMOS+Vth,PMOS , the output voltage will be estimated as NMOS threshold voltage (Vth,NMOS). This ensures that M1 and M3 or M2 and M4 transistors would not be switched on simultaneously. Therefore, it guarantees that each of the NMOS or PMOS transistors is switched on for half of the oscillation cycle.

The other issue that should be analyzed in details is choosing a right inductor with a suitable resistance. The noise produced by the inductor has a power equal to V_n^2 = 4KTR. Optimizing the inductor's value has several impacts on the performance of the whole circuit. By reducing the inductor's value, its overall resistance will be decreased as well. Consequently, the phase noise performance will be improved because less noise is produced by the resistance. On the other hand, when the inductor generates less resistance, the corresponding transconductance for the transistors will reduce as well.

This leads to less current and hence the power consumption will be optimized. Another advantage of choosing a small inductor is to decrease the reciprocal effect of inductors designed on our chip. On the other hand, when the inductor's size is minimized, a larger capacitor should be chosen to keep the oscillation

frequency at the desired value. Larger capacitors will increase the maximum charge that can be tolerated. Based on Hajimiri's formula[7], increasing the qmax will improve the phase noise performance. If we consider a defined unit area on the chip, the capacitance value that can be allocated to that area is much larger than the inductance that can be specified to that space. Therefore, by reducing the inductor size and increasing the capacitor's value to fix the oscillation frequency at the desired value, the needed area on the chip will be minimized.

However, there are some constraints for decreasing the inductor's value. The tank amplitude can be modeled using a current source which turns on and off very fast from one transistor pair to the other. Since the voltage direction on the resonator changes in every moment, the current direction reverses dynamically through the resonator. Therefore, we can model the whole circuit as current source switching in two directions of Ibias and –Ibias. The current source is feeding the parallel RLCtank all the time. Req is defined as the equivalent resistance of the resonator. At the resonance frequency, the inductor and the capacitor cancel each other due to their admittances.

At the end, what remains is the equivalent resistance of the tank (Req). Since the LC tank mainly weakens the effect of individual harmonics of the input current, the fundamental harmonic can produce a noticeable output swing. Its corresponding amplitude can be estimated as (4/π)IbiasReq. However, the output can be estimated as a sinusoidal waveform at higher frequencies. In sinusoidal waveforms, the output can be estimated as IbiasReq. Therefore, without considering these limitations, reducing the inductor value can be problematic. When decreasing the inductor value, the equivalent parallel resistance decreases as well. Consequently, the tank amplitude decreases noticeably. In our design, the overall resistance in parallel is estimated as $R_p = r_s \times Q^2_{Ris}$ around 320Ω. To fulfill the startup condition, the transconductance should fit in the following formula:

$$g_{m,tank} \geq 1/R_p$$

To minimize the flicker noise upconversion effect, equal transconductance for the NMOS and PMOS transistors should be chosen. The width and length of transistors is decided by following equations:

$$\left(\frac{W}{L}\right)_{NMOS} = \frac{g^2_{m,NMOS}}{I_B \mu_n C_{ox}}$$

$$\left(\frac{W}{L}\right)_{PMOS} = \frac{g^2_{m,PMOS}}{I_B \mu_p C_{ox}}$$

To minimize the short channel noise, proper length and width should be chosen. Regarding phase noise calculation, Hajimiri presents a model as following:

$$L(\Delta\omega) = 10 \log \left[\frac{\frac{i_n^2}{\Delta f} \sum_{n=0}^{\infty} c_n^2}{8 q_{max}^2 (\Delta\omega)^2} \right]$$

Cn represents the coefficients of the VCO Fourier series. As mentioned earlier, qmax shows the maximum charge that can be stored in the capacitor. The noise power spectrum is shown by the term $i_n^2/\Delta f$. As discussed earlier, we can reduce the inductor noise by decreasing its value. Regarding this issue, the current needed for the compensation of lossy resonator will minimize. Consequently, the VCO suffers from less noise which is one of our goals. To meet the desired center frequency, if we reduce the inductor size the capacitor value should be increased[9].

Applying the proper Vdd equal to the overall threshold voltage of an NMOS and a PMOS transistor, only two transistors will conduct in each of the half oscillation periods. This issue saves the power and decreases the overall noise. Overall, the phase noise performance will be improved.

IV. SIMULATIONS AND RESULTS

In this section of the paper, we verify our previous results by a more detailed analysis. Here, we do the final integration of VCO sub-blocks to approach the state-of-the-art phase noise and power consumption. To meet the design specifications precisely, we have tested VCO performance for varying temperature, supply voltage and tuning range. Additionally, a wider comparison is made between different VCO topologies regarding the phase noise and power consumption. As a result, we have obtained a deeper understanding of different VCO topologies regarding their applications and frequency range of oscillation.

A. Phase Noise and Frequency vs. Control Voltage

To verify the frequency range of our designed QVCO, the tuning voltage is swept from 0.2 V to 1.2 V. From the simulation results, the frequency range is observed from 2.25 GHz to 2.55 GHz. The center frequency is 2.4 GHz which matches our specification requirements. Moreover, due to control voltage and frequency variations, the phase noise changes correspondingly[4]. In Fig. 4, the blue plot demonstrates the frequency variation controlled by tuning voltage while the red curve shows the phase noise variation versus frequency and tuning voltage.

As understood from the red plot, the phase noise is considerably high at low tuning ranges. At low tuning voltages, the quality factor of the varactor is quite small. Therefore, the overall quality factor of the resonator reduces and this leads to higher phase noise. However, as the tuning range increases, the phase noise improves and finally it reaches to our desired value at the center frequency.

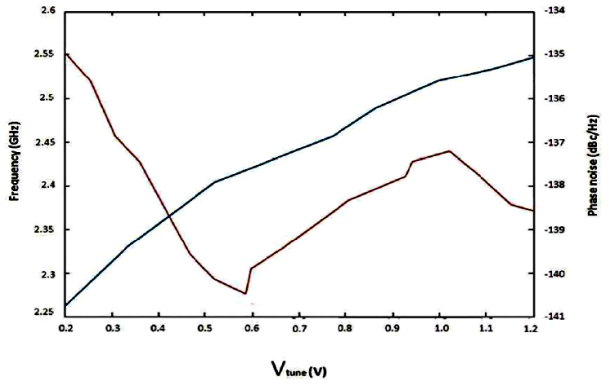


Figure. 4: QVCO Phase Noise and frequency versus control voltage.

B. Reference current source variation

In this section, we have analyzed the Impact of reference current source variation on the center frequency . the supply voltage is set at 1.2 V while the reference current is swept from 150µA to 210µA. As observed from fig.5 there is a small deviation from the center frequency when the reference current is swept from 150µA to 210µA.

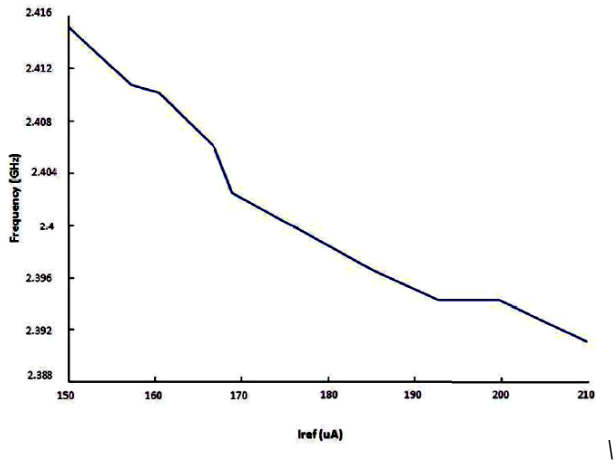


Figure. 5: Impact of reference current source variation on QVCO center frequency

C . Phase Noise and Frequency Vs temperature

In this section , we have analyzed our proposed QVCO performance versus temperature variation . The tall current is set at 3 mA while the supply voltage is 1.2V applying a tuning of 0.6 V, the temperature is swept from -50oC to 175oC . The Fig. 6. demonstrates the phase noise dependency on temperature . as we know the thermal noise is directly proportional to temperature and this leads to poor phase noise performance as the temperature increases .

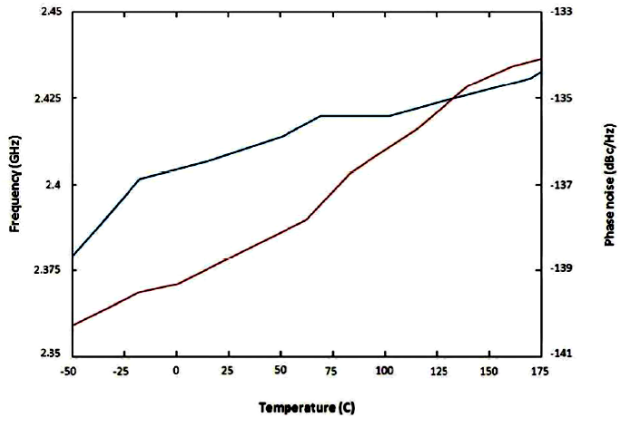


Figure .6: Impact of temperature variation on QVCO phase noise and frequency

CONCLUSION

In this work, we studied the basic theory of an oscillator. In the following sections, the noise contributors affecting the VCO performance are identified. Furthermore, different models interpreting the noise impact on a voltage-controlled oscillator are presented.

The main purpose of this project is to implement a state-of-the-art design considering optimal phase noise and power consumption. Initially, to achieve a high performance VCO, we have designed different high performance LC VCO architectures. Moreover, a wide comparison is carried out regarding the VCO specifications such as phase noise at different offset frequencies, power consumption, FOM and so forth. As a result, a suitable LC VCO topology is chosen for further analysis. Afterwards, we have improved our design to a Quadrature VCO with back-gate coupling and source resistive degeneration.

The designed QVCO oscillates at the center frequency of 2.4 GHz. The phase noise estimated by simulation at 1MHz offset frequency is -140dBc/Hz. The circuit consumes a power of 3.6mW which is less than conventional QVCO architectures. Finally, to verify our design, process, temperature, and reference current variations were tested. As a result, the specification requirements have been met in our design.

REFERENCES

[1] P.K. Rout, U.K. Nanda, D.P. Acharya, G. Panda, “Design of LC VCO for optimal figure of merit performance using CMODE”, 1st International Conference on Recent Advances in Information Technology (RAIT), pp. 761 – 764, March 2012.

[2] S. Zihir, F. Tasdemir, T. Dinc, Y. Gurbuz, “A new resonant circuit for 2.45 GHz LC VCO with linear frequency tuning”, Microwave Integrated Circuits Conference (EuMIC), pp. 390 – 393, Oct. 2011.

[3] P. Liu, P. Upadhyaya, J. Jung, D. Heo, J.-H. Kim, B.-S. Kim, “Dynamically switched low-phase-noise LC VCO with harmonic filtering”, Electronics Letters, vol. 47, pp. 792 – 793, July 2011.

[4] B. Soltanian, P. Kinget, “A Low Phase Noise Quadrature LC VCO Using Capacitive Common-Source Coupling”, 32nd European Solid-State Circuits Conference (ESSCIRC), pp. 436 – 439, Sept. 2006.
[5] Han-il Lee, Tae-Young Choi, S. Mohammadi, L.P.B. Katehi, “An extremely low power 2 GHz CMOS LC VCO for wireless communication applications”, The European Conference on Wireless Technology, pp. 31 – 34, Oct. 2005.
[6] Harikrishnan Ramiah, Tun Zainal Azni Zulkifli, “A Low-Phase Noise and High Output Swing RF LC-VCO in CMOS Technology”, RF and Microwave Conference, pp. 197 – 200, Sept. 2006.
[7] Yang Zhang, Peng Liu, Tang-Nian Luo, Yi-Jan Emery Chen, Deukhyoun Heo, “A low-voltage low-phase-noise bottom-series LC QVCO using capacitor tapping technique”, Microwave Symposium Digest, pp. 237 – 240, June 2008.
[8] M D Wei, S Chang, Y Yang, "A CMOS Backgate-Coupled QVCO Based on Backto- Back Series Varactor Configuration for Minimal AM-to-PM Noise Conversion ", Microwave and Wireless Components Letters, IEEE , pp. 320 - 322, (2009).

SCADA Based Automated Bottle Quality & Quantity Detection and Filling System by Using PLC

Mr.P.Choudesh Varma [1] and Mr.G.Venkateswarlu [2]
[1] CVR College of Engineering, Department of EIE., Hyderabad, India
Email: choudesh82@gmail.com
[2] CVR College of Engineering, Department of EIE., Hyderabad, India
Email: venkigummadilli@gmail.com

***Abstract*— In this paper, we propose an automated bottle quality, quantity detection and filling system in a manufacturing department using a PLC (Programmable Logic Controller) and SCADA. SCADA stands for Supervisory Control and Data Acquisition system. The main objective of the project has four processing stages. Firstly, detect the fault of the bottle by using optical sensor. In the second stage, remove the faulted bottle from the conveyer belt using electronic pusher. In the next stage, detect the quantity (size) of the bottle using proximity sensor. In the final stage, bottle filling process regarding size of the bottle. The quality and quantities of the physical system in the field is sensed by the sensors and fed as inputs to the PLC which in turn sent to PC through RS-232 for necessary processing. A PLC program is developed based on the signals received from the PLC input module, process the signals and send the output signals to the PLC output modules, which is programmed to actuate the necessary electronic actuator**.

The SCADA screens are developed regarding four processing stages on PC using Wonderware-Intouch 9.0 SCADA software. The Allen Bradley micrologix 1000 PLC to be link up with the supporting SCADA Wonderware-Intouch 9.0 by giving necessary tag names. With the help of SCADA, simulation of the physical system is also developed to monitor the quantities to be measured and status of the equipment in the plant from field point.

***Index Terms:* PLC, SCADA, I/O Modules Actuator, Proximity and optical sensors.**

I. INTRODUCTION

Modern bottle quality, quantity detection and filling process is truly sophisticated, this can even be done automatically with computer controlled equipment. The methods of process variables controlling have been changed rapidly in recent years. Bottle quality, quantity detection and filling systems are an important Application in the fields of pharmacy, food processing, fertilizer industries. The main aim of the project has four processing stages.

1. Detect the fault of the bottle using optical sensor
2. Remove the faulted bottle from the conveyer belt using electronic pusher.
3. Detect the quantity (size) of the bottle using proximity sensors.
4. Bottle filling process regarding size of the bottle.

Fault detection: Optical sensor is placed one side of the conveyor belt and it detects the cracks present on the bottle (If the bottle has a crack then transmitted light is reflected and then optical sensor detects [7]the reflected light) if any. Then PLC sends control signals to the pusher through PLC O/P modules and then faulted bottle is removed by the pusher from the conveyor belt.

Quantity detection and filling: Proximity sensors are placed side of the conveyor belt to detect the size of the bottle. Regarding size of the bottle, signals are transmitted from proximity sensors (P.S-2 & P.S-3) to PLC through PLC I/O modules [1] then the data will be updated in the PLC programming. A another capacitive proximity switch is placed one side of the conveyor belt and it detects the bottle which comes near to the filling tank and then the running of conveyor belt stops and solenoid valve is opened, then bottle is filled for a few seconds mentioned in the timer based on quantity of the bottle which is taken in the PLC program.

A capacitive proximity switch which is used for the bottle filling purpose is also used for the counting purpose. The capacitive proximity switch output is given to the counter. Whenever the switch output is ON then there will be a increment in the counter. The counter can be seen in the SCADA screen [4]. By this, we can know how many bottles are present on the conveyor belt. Every updated status of field devices can be monitored on the SCADA screen.

The paper is organized as follows. Section I Introduction to bottle quality, quantity detection ,filling and techniques used for Measurement of physical variables considered and controlling in our process.

Section II: Block diagram of the application considered

Section III: Field devices and specifications
Section IV**:** Programmable logic controllers
Section V: Programming language &results
Section VI: SCADA &, results
Section VII: Conclusition and future enhancement
Section VIII: Acknowledgement
Section IX: references.

II -BLOCK DIAGRAM OF THE APPLICATION

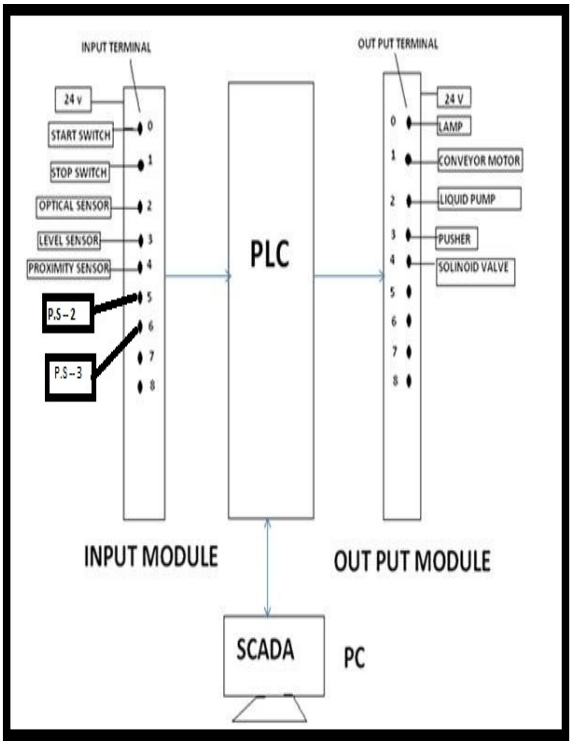


Figure 1.Block diagram

This block diagram explains the inputs, outputs and their interfacing with the PLC and SCADA. In this all inputs and outputs are connected to the input module and output module of PLC respectively. The PLC is interfaced with SCADA using RS-232 by using respective drivers. The PLC requires the power supply of 24V; it is given by using SMPS (switched-mode power supply).

Here, the inputs are proximity switches, level sensors; master start and master stop switches. Three capacitive proximity switches namely proximity sensor, proximity sensor (P.S-2) and proximity sensor (P.S-3) is connected to the PLC as inputs and also an optical switch namely fault detecting sensor is connected to the PLC as input. Level sensors and master start switch and master stop switch are also connected to the PLC as inputs. A pusher, solenoid valve, two motors namely pump motor and conveyor motor are connected as outputs to the PLC as shown in the fig 1.

The process behind in this block diagram is, whenever the ON button in SCADA is turned ON then the conveyor belt motor will be ON then the conveyor belt tends to run. When there is a crack on the bottles which are placed on conveyor belt is detected then the optical sensor will be ON, then a signal is send to the PLC and the PLC sends a signal to the pusher which is an output device to ON, then the pusher pushes the fault bottle out from the conveyor belt.

Whenever the bottle comes near to P.S-2 (half Ltr bottle) and P.S-3(1Ltr bottle) sensors then which sends signals (quantity of the bottle) to the PLC through I/O modules. Whenever the bottle comes under the solenoid valve the proximity switch will ON then sends the signal to the PLC and the PLC sends signal to the conveyor belt motor through output modules to OFF and solenoid valve to open for few minutes or seconds regarding size of the bottle, Which we mentioned in the timer [1] [2] .the process going in the field and status of field devices can be monitored on SCADA screen..

The proximity switch is also connected to the counter to count the bottles running on the conveyor belt. Here we use two level sensors arranged in the overhead tank at bottom and top. When water level in the overhead tank is decreased from the bottom level sensor then the pump motor will ON. When the water level in the overhead tank reaches the top level sensor then the motor will be OFF. Here the ON and OFF operation of pump motor is done by the signal sent by the PLC.

III. FIELD DEVICES AND SPECIFICATIONS

The devices which are interfaced with PLC I/O modules [1] are called as field devices like sensors and actuators. The following devices are used to implement the automated bottle quality, quantity detection and filling system**.**

Frame: In industries series of wheels are placed under the thick and strong conveyor belt which has the capability to bear the weight of the bottles .In industries there is heavy machinery to fill the bottles and capping it .In our project, a frame is designed with iron and wood materials. The length of the frame is 5.5 feet and the breadth of the frame is 1 feet. In our project, the whole apparatus which we used is placed on the frame and it has to bear all the weight of the apparatus.

On the frame, bearings are placed on either side and get welded. In industries there are series of wheels which are used to give support to the conveyor belt but here we are not using such type of heavy machinery, so we designed a flat surface sheet made up of wood material and it gives support to the conveyor belt to weigh the bottles when they are going to fill. Here a motor is also welded on one side of the frame and it is connected to the toothed wheel which is attached with bearings, so motor is used to run the conveyor belt, the frame which is made up of iron and wood material is shown below Fig.2.

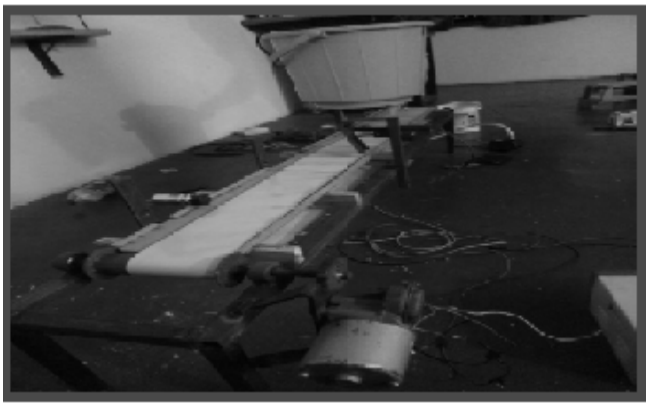


Figure.2 Frame with conveyor belt

Electrical pusher: In industries various pushers are used to push the fault bottles are any fault material present on the conveyor belt. Some of the pushers are mechanical pushers, hydraulic pushers, electronic pushers etc.In our application, we used electronic pusher to push the fault bottle on the conveyor belt found if any. Which is operating for 24v input voltage. We preferred electronic pusher is shown in Fig.3 because it is less cost than other pushers and it is suitable for our application. Pusher is connected to PLC output module terminal-3.we have to consider the terminal at the time of writing the PLC programming, give the address to that particular terminal as

O: 0/3 where O represents output module and3 represents pusher is connected to 3rd terminal of output module

The working of the pusher [8] used in this project is, inside the pusher there is a coil and adjacent to the coil there is a magnetic piece. Whenever current passes through the coil then it acts as magnet. The magnetic piece and the current carrying coil will have the same poles, so like poles repel each other. So the magnetic piece gets repelled. To this magnetic piece we connect a spring and hence it acts as the pusher.

Figure.3 Electrical pusher

Level switch: The main application of this level switch (Fig.4) is to sense the water level in large water tanks and sumps. Level switch is connected to PLC input module terminal-3.we have to consider the terminal at the time of writing the PLC programming[1] [2] , give the address to that particular terminal as I: 0/3 where I represents output module and 3 represents level switch is connected to 3rd terminal of input module.

The rating of this level switch is 10A resistive at 230V AC. The switch type present in this switch is SPDT. The switching angle is +/- 45deg. The medium temperature is max 50deg and medium pressure is max 0.1pa (1bar). The medium density is min 0.8gm/cubic cm. Housing material is polypropylene. Cable material is PVC or neoprene. Cable diameter is 9mm/3 x 1 sq mm. Cable length is 5metres.

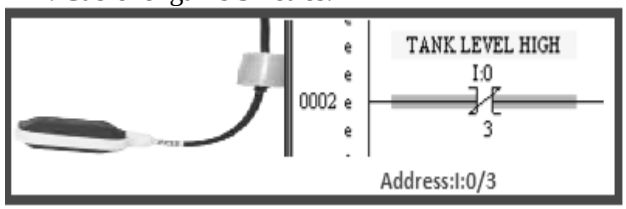


Figure.4 Level switch

DC motor: It is used to run the conveyor belt. This is connected to PLC O/P module through relay 24v operating voltage. Whenever the master start button is pressed then PLC sends the control signals to the O/P modules (terminal-1).then the motor is ON through the relay. .we have to consider the terminal at the time of writing the PLC programming, give the address to that particular terminal as O: 0/1 where O represents output module and 1 represents motor is connected to 3rd terminal of output module.

It is based on the principle that when a current carrying conductor is placed in a magnetic field it experiences a mechanical force. Now a day's DC motor (shown in Fig.5) place a vital role in most of the industrial areas.

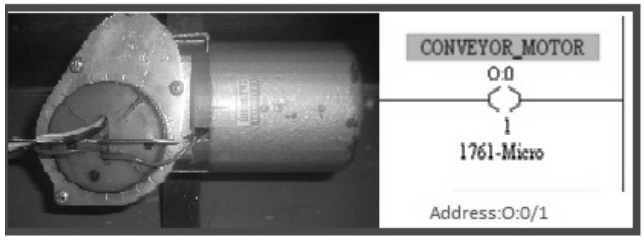
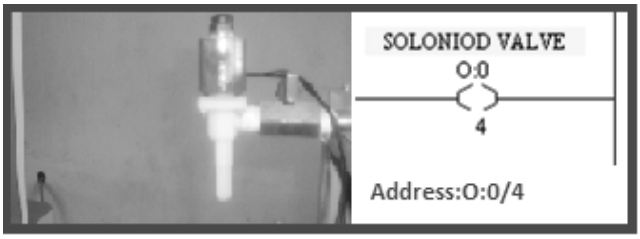


Figure.5 conveyor motor

Solenoid valve: This is connected to PLC O/P module (Terminal4).Whenever the bottle reaches near to filling tank then PLC sends the control signals to solenoid valve to fill the bottle. We have to consider the terminal at the time of writing the PLC programming; give the address to that particular terminal as O: 0/4 where 4 represents level switch is connected to 3rd terminal of input module

A Solenoid valve (Fig.6) is electromechanically operated valve, the valve is controlled by an electric current through a solenoid: in the case of a two-port valve the flow is switched on or off; in the case of a three-port valve, the outflow is switched between the two outlet ports. Multiple solenoid valves can be placed together on a manifold.

If the valve is open when the solenoid is not energized, then the valve is termed normally open (N.O.). Similarly, if the valve is closed when the solenoid is not energized, then the valve is termed normally closed internally piloted valves are used in dishwashers and irrigation systems where the fluid is water, the pressure might be 80 pounds per square inch (550 kPa) and the orifice [9] diameter might be $\frac{3}{4}$ in (19 mm). A direct acting solenoid valve typically operates in 5 to 10 milliseconds. The operation time of a piloted valve depends on its size; typical values are 15 to 150 milliseconds.



.Figure.6 solenoid valve

Proximity switch: A capacitive switch (Fig.7) is a proximity switch that detects nearby objects (bottles) by their effect on the electrical field created by the sensor. Here we are using three proximity sensors, one sensor is for to detect the bottle nearby filling tank that is connected to PLC input module 4th terminal addressed as I:0/4 and two more sensors are proximity sensor (P.S-2) and proximity sensor (P.S-3) are connected to the PLC input modules to detect the quantity of the bottle, P.S-2 (half Ltr bottle) addressed as I:0/5 and P.S-3(1Ltr bottle) addressed as I:0/6.

Simple capacitive switches [9] have been commercially available for many years, and have found a niche in nonmetallic object detection, but are limited to short ranges, typically less than 1 cm.

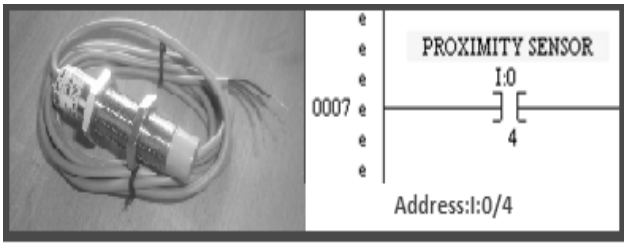


Figure.7 proximity switch

IV. PROGRAMMABLE LOGIC CONTROLLER

Programmable logic controllers (fig.8) are nothing but a type of solid state devices designed to perform logic functions previously accomplished by electromechanical relays mainly used in industrial equipments. These industrial equipments may range from a small ON-OFF switch to a heavy machine. Any component in industry that needs a control can be controlled by using PLC. The main advantage of using PLC is that long and tedious programming can be eliminated. The programming for PLC is done by using the ladder logic diagram. The ladder logic consists of blocks which are in the form of ladders.

In our project PLC (Allen Bradley micrologix 1000 PLC) [1] is used to monitor and provide the required indication and control like Detect the fault of the bottle , Remove the faulted bottle, Detect the quantity (size) of the bottle, filling process and also. The liquid level is controlled using the PLC. We have two levels namely, low and high levels. By using the level sensor, the PLC makes the motor ON and the tank is filled. As soon as the water reaches the high level the motor is stopped.

Figure.8 Allen Bradley micrologix 1200 PLC

I/O Modules: The input module has terminals to which outside process electric signals, generated by sensors or transducers are entered. The output module has terminals to which output signals are sent to activate relays, solenoids, various solid-state switching devices, motors and displays. An electronic system for connecting I/O modules [1] [2] to remove locations can be added if needed. The actual operating process and PLC control can be thousands of feet from the CPU and its I/O modules

The input module (Fig.9) performs four tasks electronically

1. First it senses the presence or absence of an input signal at each of its input terminals..The input signal tells what switch, sensor or other signal is ON or OFF in the process being controlled.

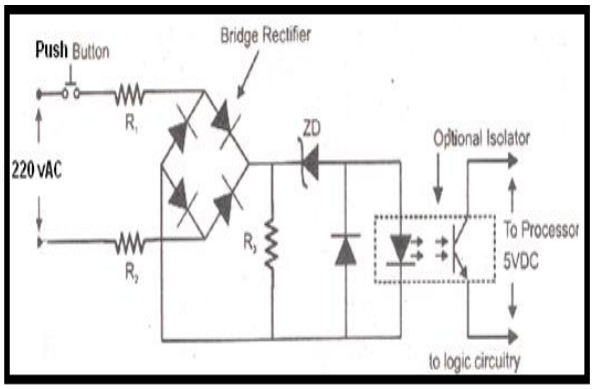


Figure.9.Input module

2. Second, it converts the input signal for high, or on, to a DC level usable by the module's electronic circuit. For a low or OFF input signal, no signal is converted**,** indicating OFF.
3. Third, the input module carries out electronic isolation by electronically isolating the input module from its input.
4. Finally, its electronic circuit must produce an output, via output logic, to be sensed by the PLC CPU.

The output module (Fig.10) operates in the opposite manner from the input module.

A DC signal from the CPU is converted through each module section to a usable output voltage; either AC or DC.A signal from the CPU is received by the output module logic, one for each scan.

If the CPU signal code matches the assigned number of the module, the module section is turned ON. If the matching CPU signal is received, it goes through an isolation stage. Isolation is necessary so that any erratic voltage surge from the output device does not get back into the CPU and cause damage.

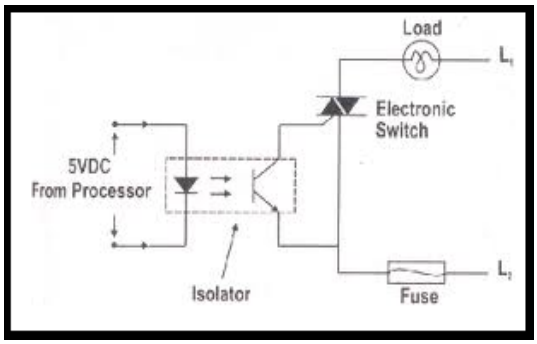


Figure.10.output modules

The isolator output is then transmitted to switching circuitry or an output relay. The output of a module section may be through a relay, or a DC or AC output.

V PROGRAMMING LANGUAGE

PLC programs are typically written in a special application on a personal computer, and then downloaded by a direct-connection cable or over a network to the PLC. We have to Write the programme by considering the connections of field devices to the PLC input and output modules. The programme should satisfy the processing steps of our application. The program is stored in the PLC either in battery-backed-up RAM [1] or some other non-volatile flash memory. Often, a single PLC can be programmed to replace thousands of relays.

Under the IEC 61131-3 standard, PLCs can be programmed using standards-based programming languages, in this we are using ladder programming language

LADDER DIAGRAM (LD): Ladder logic is a programming Language (Fig.11) that represents a program by a graphical diagram based on the circuit diagrams of relay-based logic hardware. It is primarily used to develop software for Programmable Logic Controller (PLCs) used in industrial control applications. The name is based on the observation that programs in this language resemble ladders, with two vertical rails and a series of horizontal rungs between them [1] [3].

The following instructions are the desired PLC programming instructions to write the programme.

1. Normally open

2. Normally closed

3. Timer

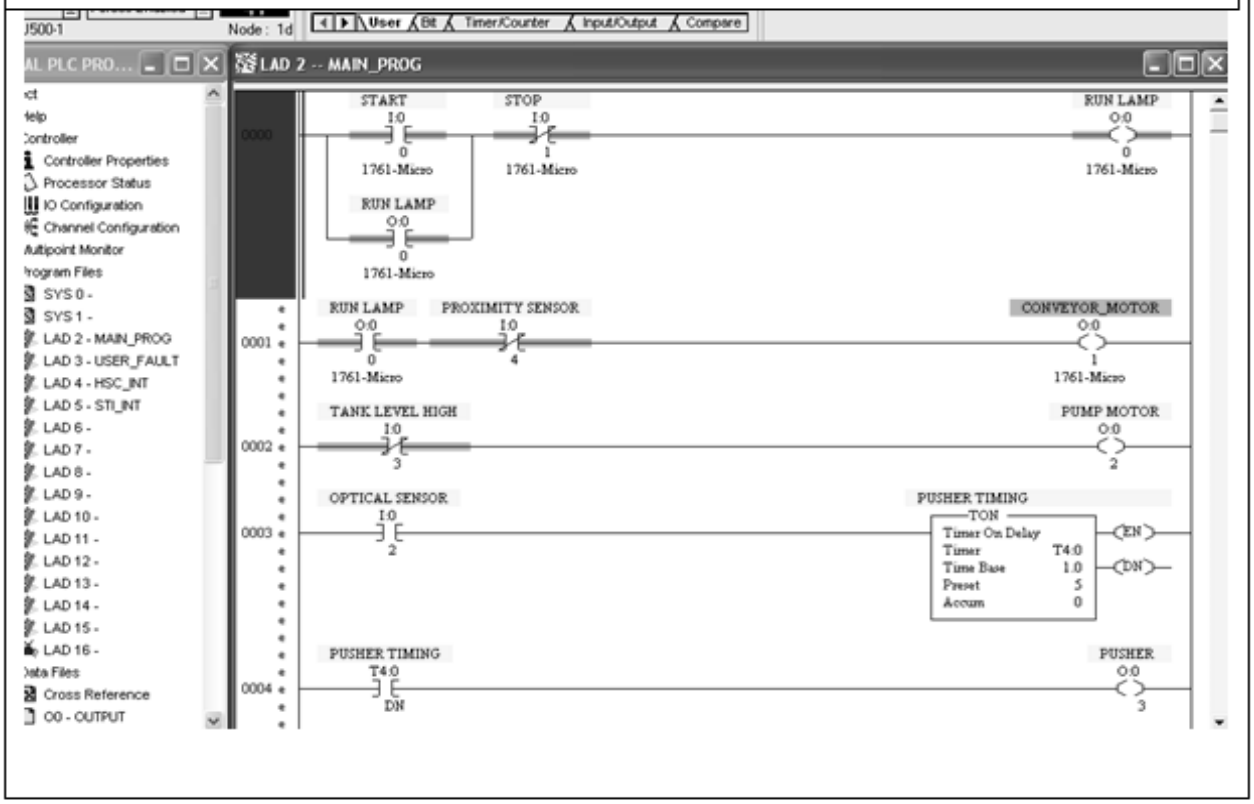
4. Counter

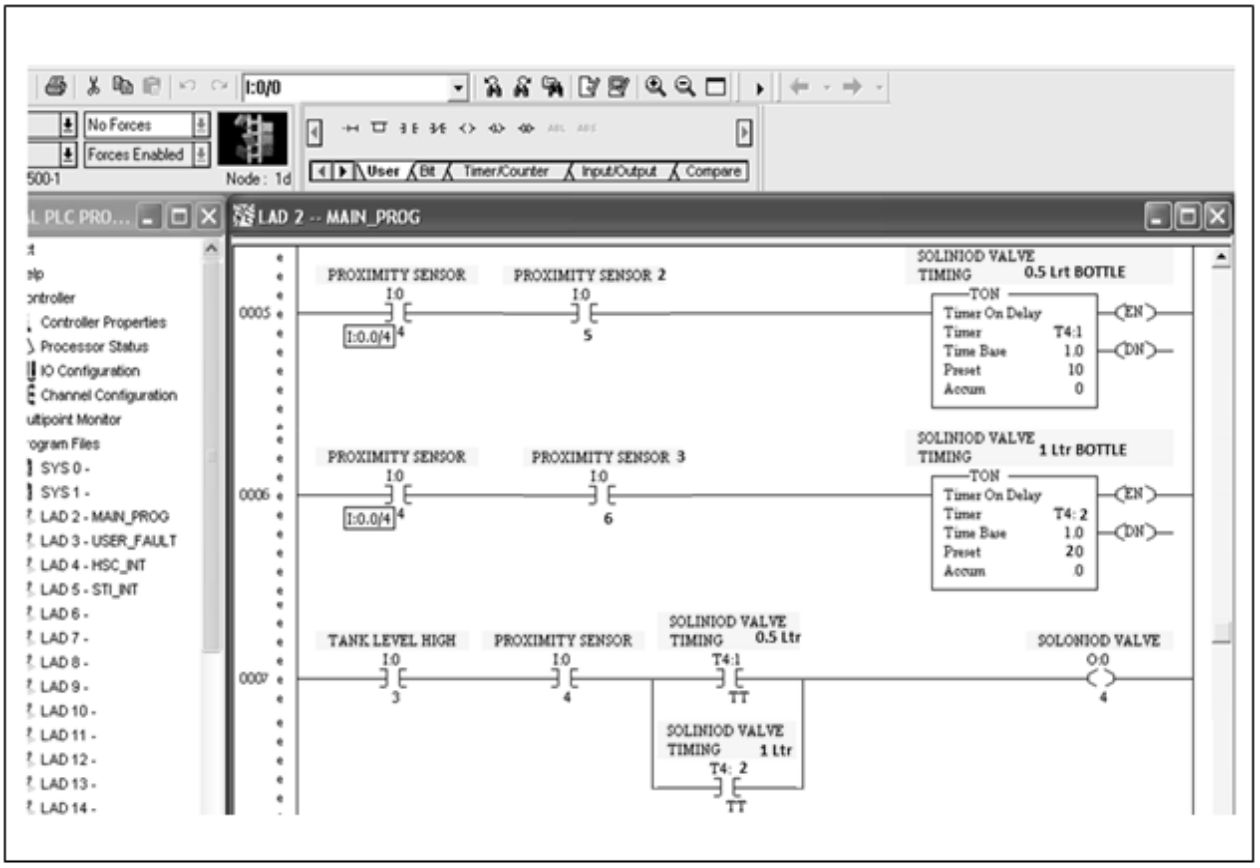
Addressing format

Input->I: 0/0, I: 0/2, I: 0/0, I: 1/0, I: 2/3

Output->O: 0/0, O: 0/1, O: 1/0, O: 2/4

The following are the PLC programming for automated bottle quality, quantity detection and filling system





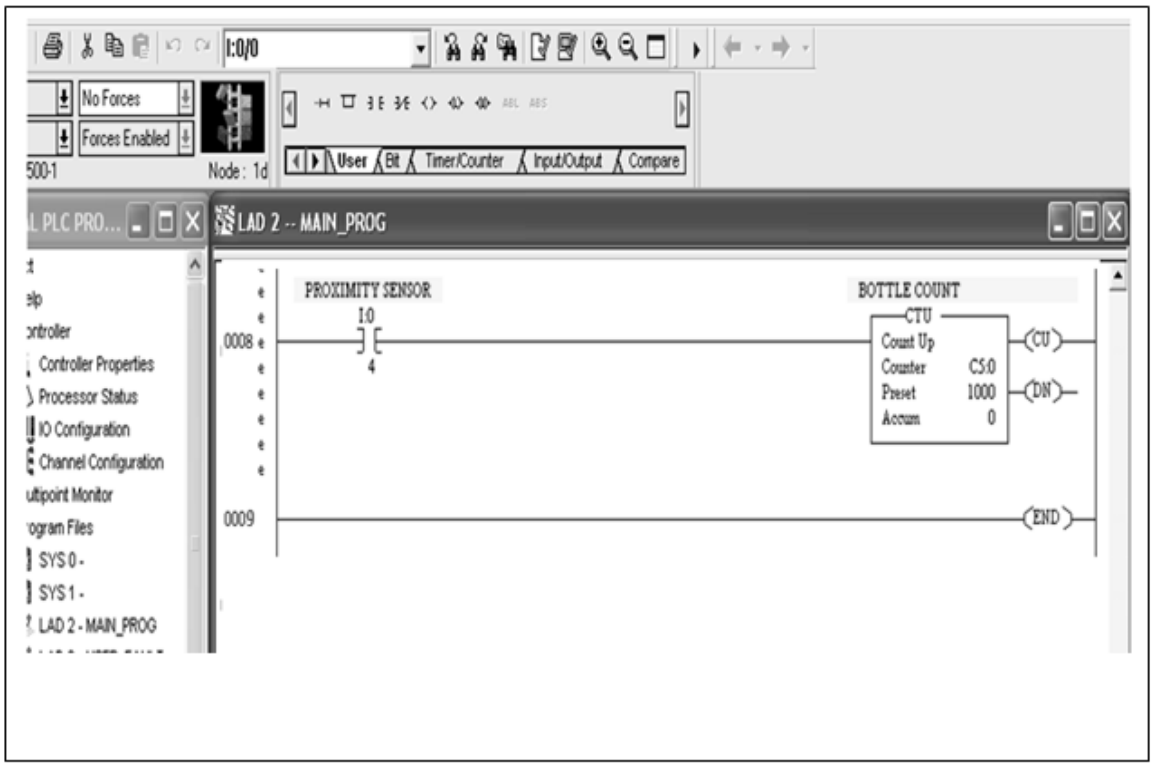


Figure.11.PLC programming

VI. SCADA

In this project we are using Wonder ware InTouch SCADA. For 25 years Wonder ware InTouch has been the world's number one **human machine interface** (HMI).SCADA screens were developed based on the field devices which are interfaced to the PLC input and output modules. We can monitor and control the status of every field device from the SCADA system.

SCADA (supervisory control and data acquisition) [4] is a type of Industrial control system (ICS). Industrial control systems is computer controlled systems that monitor and control industrial processes that exist in the physical world. SCADA systems historically distinguish themselves from other ICS systems by being large scale processes that can include multiple sites, and large distances. Industrial processes include those of manufacturing, production, power generation, fabrication and refining, and may run in continuous, batch, repetitive, or discrete modes.

Whatever the symbols dragged into the screen from the graphics symbolic factory that could be link up with the PLC programming by considering the Tag Name(Fig.12) and instruction address then only we can monitoring and control the status of field devices.

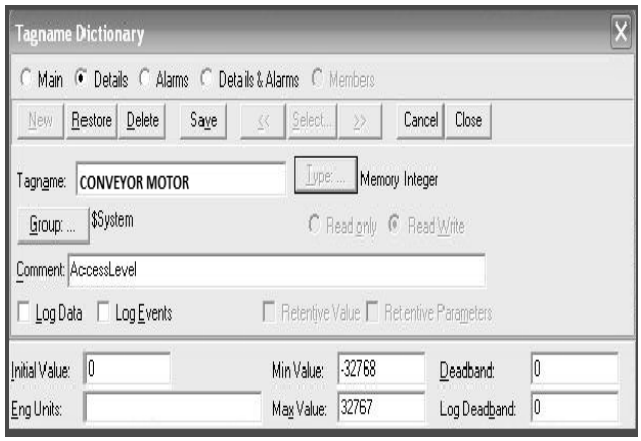


Figure.12.Tag Name Dictionary

Common system components: A SCADA system usually consists of the following subsystems:

1. A human machine interface or HMI (fig.13) is the apparatus or device which presents process data to a human operator [5] [2], and through this, the human operator monitors and controls the process.

2. SCADA is used as a safety tool as in lock-out-tag-out. A supervisory (computer) system, gathering (acquiring) data on the process and sending commands (control) to the process.

3.Remote Terminal Units (RTUs) connecting to sensors in the process, converting sensor signal to digital data

and sending digital data to the supervisory system. Programmable Logic Controller (PLCs) used as field devices because they are more economical, versatile, flexible, and configurable than special-purpose RTUs.

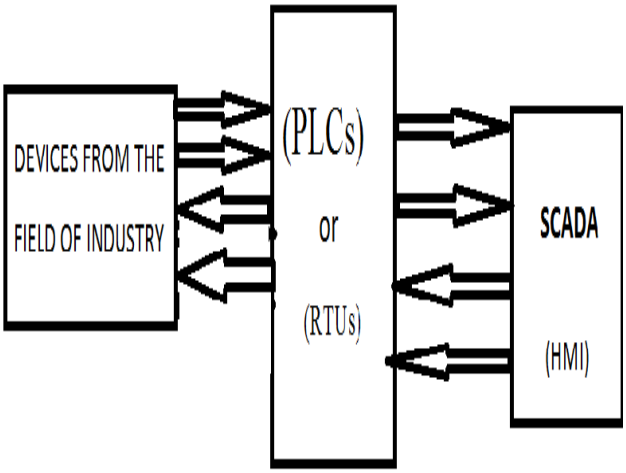


Figure.13.Human machine interface with field of industry

Wonder ware InTouch SCADA : The primary offering, Wonder ware InTouch SCADA, employs a development canvas with a drag-and-drop paradigm and a symbol library(Fig.14), which allows users to drag a graphic symbol from the library and drop it onto the canvas. From there, the symbols can be connected in a way that reflects the design of a plant floor.

Applications designed in Wonder ware InTouch SCADA enable plant engineers and operators to visualize plant floor operations and to issue operational commands such as START and STOP to one or more Programmable Logic Controllers either remotely or locally.

Figure.14.symbol factory

The result is shown in Fig.15. SCADA screen for automated bottle quality, quantity detection and filling system

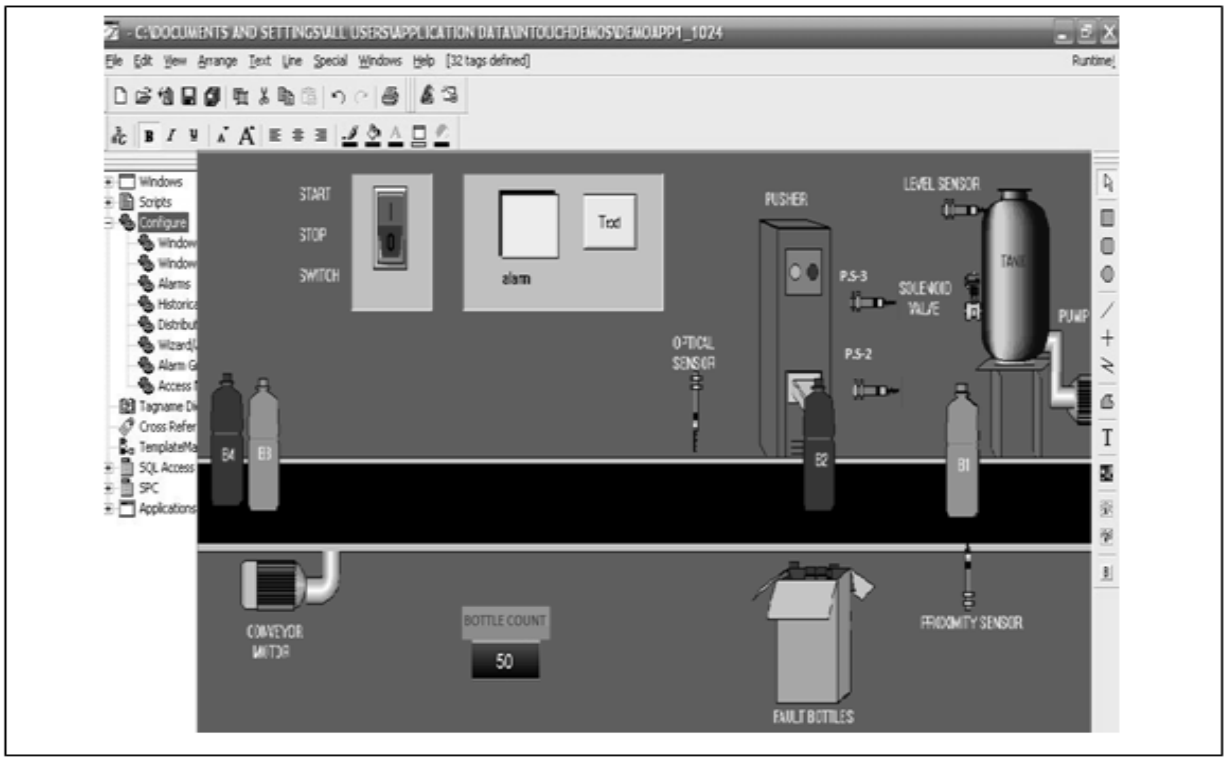


Figure.15. SCADA screen for automated bottle quality, quantity detection and filling system

CONCLUSION AND FUTURE ENHANCEMENT

Automated bottle quality, quantity detection and filling system using PLC and SCADA has been successfully constructed and designed. The system that is produced can be modified to be better if some of the electrical devices and system are upgraded and improved.

The theory and concept of the automatic quality, quantity detection and filling water system is based on the PLC and SCADA. In electrical design, the features and functions of the electrical components are required to determine the system requirement.

Furthermore, the theoretical of the wiring system is required for connecting the inputs and outputs devices to PLC. In programming design, understandings of the desired control system and how to use the Ladder Diagram to translate the machine sequence of operation are the most important parts, because it has direct effect on the system performance. The main aim in this process is to apply PLC to design automatic filling water system and all objectives in this project were successfully done as planned.

Actually, a weakness from the project can be taken as future works so that the improved system will be better in terms of performance. So that, there are several recommendations or suggestions that we can take to increase performance in this project. The performance of automated bottle quality, quantity detection and filling system can be increased based on two recommendations which are;

The system that is proposed now is using only one sensor that is IR sensor to detect position of bottle. It will be better if we add more sensors in this system like a flow sensor to detect water flow or use level sensor to detect water level. Thus, the system will be more sensitive as there will be more sensing points. Besides using PLC as controller, the other controller can be used in the future work. However, many factors must be considered like cost, practically and others.

REFERENCES

[1]. John. W .Webb Ronald A Reis , Programmable Logic Controllers – Principles and Applications, Fourth edition, Prentice Hall Inc., New Jersey, 1998.

[2]. PC Interfacing and Data Acquisition Techniques for Measurement, Instrumentation and Control. By Kevin James; Elsevier.

[3]. Manual book, ‘A Beginner’s Guide to PLC’, version 2.1. Singapore: Omron.2001.

[4]. SCADA: supervisory control and data acquisition by Stuart A.Boyer.

[5]. Securing SCADA system, in author “Ronald L.Krutz”.

[6]. PLC Based Automated Packing Station Using National Instrument’s Lab VIEW Software Package, International Conference on Computing and Control Engineering (ICCCE 2012).

[7]. Lasers and Optical Engineering – by Das P., Springer’s International Students Edition, 1991.

[8]. A course in Electrical and Electronic Measurements and Instrumentation, A.K. Sawhney, Dhanpatrai & Co.

[9] .Modern Electronic Instrumentation and Measurement techniques – by A.D. Helfrick and W. D. Cooper, Pearson/Prentice Hall of India.

Paratransit Operations in Roorkee

S. Praveen[1]
[1] CVR College of Engineering, Civil Engineering Department, Hyderabad, India
Email: samarthipraveen@gmail.com

***Abstract*— Rapid increase of urban population, per capita income, along with inadequate existing transport infrastructure has stimulated the usage of paratransit. The paratransit consist of a shared taxi or small bus that will run along more or less defined route, they are meant to stop in order to pick up the passengers or discharge the passengers to their destinations upon their request. Paratransit systems play a significant role in the urban transport sectors of developing countries. In Many cities more than half of the total public transport demand is met by them. They serve as a cheap and convenient public transport mode.**

Paratransit services provide considerable degree of flexibility to the passengers. They offer flexible on-demand door-to-door service from any origin to any destination in a service area. Paratransit services are operated by public transit agencies, community groups etc.
Samples were collected in Roorkee city, detailed analysis and results based on road user's preferences were presented.

***Index Terms*— Mode, House hold Income, urban population and transport infrastructure**

I. INTRODUCTION

Over the last three decades the word "paratransit" has migrated and taken to separate broad sets of meaning and application. The informal public transport modes or "paratransit" in developing countries encompass a variety of transport modes and service facilities falling in between the conventional transport services, fixed route, scheduled bus, urban rail and private auto mobiles. The concept of paratransit, however differs in the context of developed and developing countries. In developed countries, paratransit is often used for demand responsive systems such as shared-ride taxis, dial-a-ride and subscription buses. In the context of developing countries, the lower standard of living, high population density, availability of cheap labour force etc., have together provided a bewildering array of transport modes bridging the gap between public bus and private auto mobiles.

A. Paratransit

Paratransit is an alternative mode of flexible passenger transportation that does not allow fixed routes (or) schedules. Typically mini-buses are used to provide para transit service, but also share taxis and Jitneys are important providers. Paratransit provides service for people with disabilities and elder to reach their destinations based on their convenience.

Classification of Paratransit:

Paratransit modes are regarded as an important component of urban transport in the cities of developing countries due to its distinguishing characteristics, like low carrying capacity, low speed, low energy requirements, more dependable and small area of coverage. Generally, Paratransit system can be broadly classified into two types; non-motorized and motorised. Both types are again sub-classified into 3 groups based on their seating capacity. They are individual type (seating capacity less than 4), shared type (seating capacity of 5-10) and collective type (seating capacity of 11-20).The non-motorized paratransit includes animal powered and human powered types. The examples of animal powered paratransit are tonga in India and Pakistan, calesa in Philippines, dokar or delman in Indonesia.

TABLE I. TABLE I
TABLE II. PARATRANSIT SYSTEMS IN THE WORLD

S. no	Country	Paratransit
1	Thailand	Tuk-Tuk
2	Dakar & Senegal	Mini buses
3	Uganda, Kenya & Nairobi	Matatu
4	Indonesia	Angkots

Need of Study

Paratransit is the main mode for public transport for short distances i.e., from 2km to 10 kms distance. Most of the people choose it as a primary mode of transport, to facilitate their movement in the city without causing any problem to other mode of transport. Prevailing on the road network of the city, proper planning and management of paratransit is required. To carry out such type of planning activity, it is necessary to enhance the characteristics of paratransit operations in the city of Roorkee.

II. APPROACH AND METHODOLOGY

A. APPROCH

To evaluate and judge the characteristics of paratransit mode in the city of Roorkee, a detail questionnaire which consist of questions related to the user and driver characteristics. The outcome of these

questions is used to generate the data for the evaluation of the paratransit characteristics.

B. METHODOLOGY

The methodology adopted for the present study is based on the flow chart given in figure1.

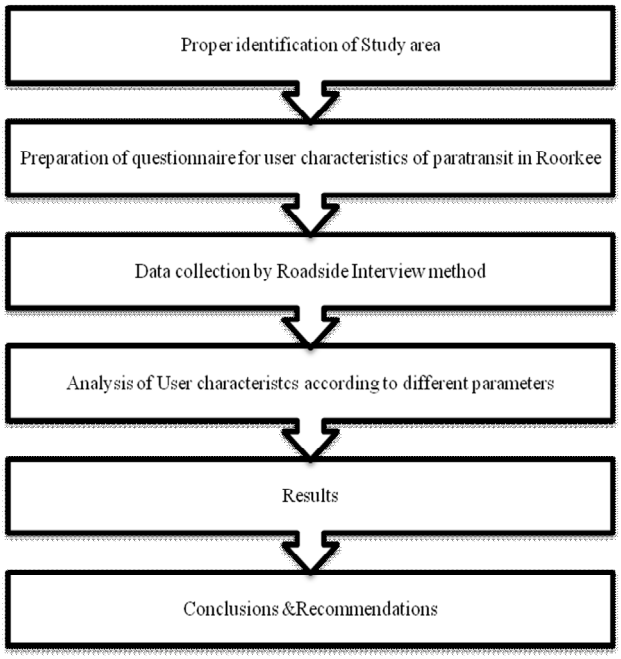


Figure 1. Flow chart showing the methodology

III. STUDY AREA

A. Data Recording and Processing

Data has been collected for various characteristics of users and drivers. Proper identification of location is very important for carrying out field study for data collection. Data Collection has to be made from location where adequate numbers of paratransits are available.
Data collection was done by road side interview method. Data was collected at 3 locations namely SDM Chourah Road ways Junction and Malakpuri chungi. Survey forms were filled according to the information

TABLE II
TABLE III. SAMPLE DATA COLLECTED AT DIFFERENT LOCATIONS

S. no	City	Location	No of Samples
1	ROORKEE	SDM CHOURAHA	35
2	ROORKEE	ROAD WAY	35
3	ROORKEE	MALAKPURI CHUNGI	30

given by both users and drivers. 100 samples were taken for this survey. From the above mentioned locations information was taken from both driver and user regarding various characteristics, the number of samples collected at each location is presented in table2.

SDM CHOURAHA

1. The following figure2 indicates that, 40% of the commuters using paratransit are having self contained flat and 60% of commuters has rental house.

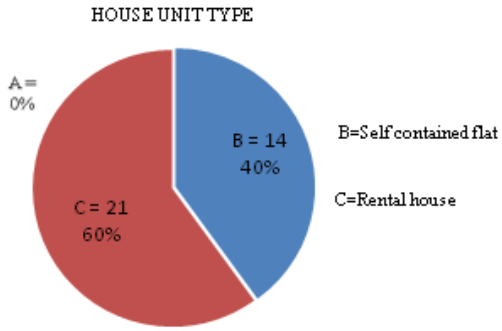


Figure2. Distribution of responses w.r.t house unittype

House Unit Type:
A: Luxury; B: self contained flat; C: Rental House

2. From the figure3, 37% of commuters using paratransit are having monthly income group between Rs.3000 to Rs.5000, 34% of commuters are of income group between Rs.5000 to Rs.10000 and 29% of commuters are of income group greater than Rs.10000.

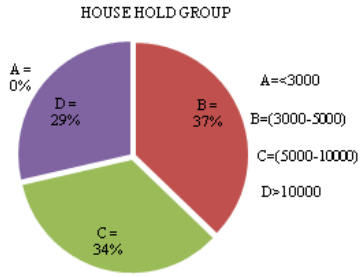


Figure 3. Distribution of responses w.r.t house hold group

3. From the figure4, 11% of the commuters using paratransit are of students, 37% of commuters are industrial workers, 46% of commuters are businessmen and 6% of the commuters are others.

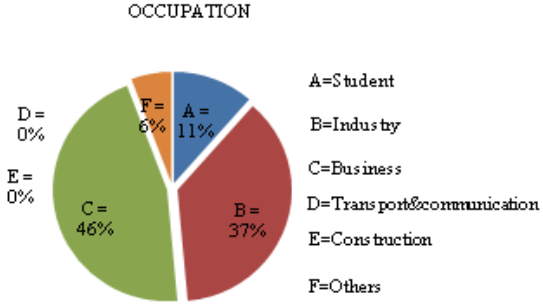


Figure 4. Distribution of responses w.r.t occupation

4. From the figure5, 43% of commuters using paratransit are work-based trip, 31% of commuters are of personal business trip, 20% of commuters are home based trip and 6% of commuters are related to recreation trip.

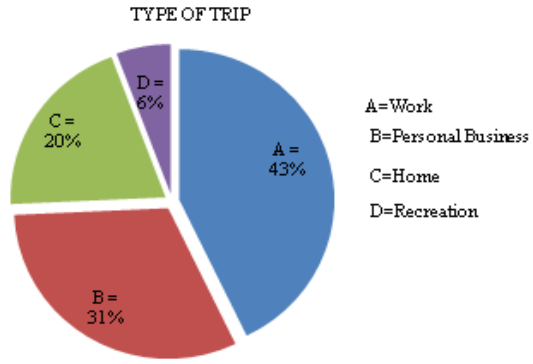


Figure 5. Distribution of responses w.r.t type of trip

5. From the figure6, 34% of commuters using paratransit has good satisfaction, 60% of commuters has average satisfaction and 6% of commuters has poor satisfaction.

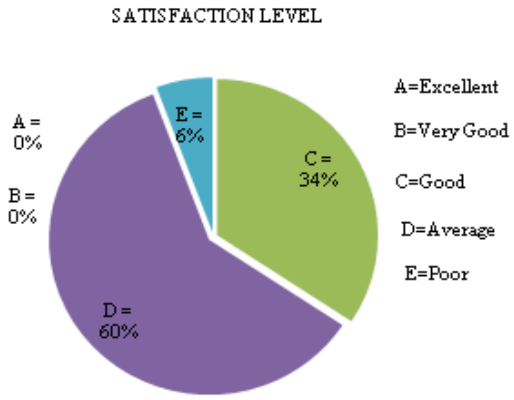


Figure 6. Distribution of responses w.r.t satisfaction level

6. From the figure7, 20% of commuters using paratransit has less than 7km trip length, 40% of commuters has 7 to 10km trip length and 40% of commuters has greater than 10km trip length.

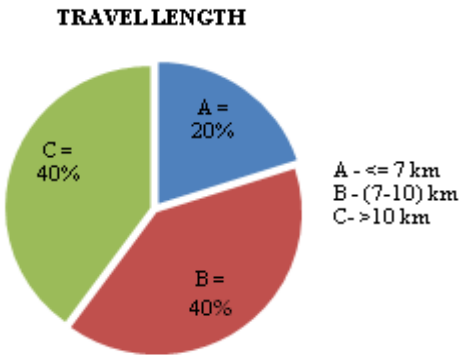


Figure 7. Distribution of responses w.r.t travel length

DISCUSSIONS:
AT SDM CHOURAHA
Houseunit Type:
A=0% ;B=40%;C=60%;
Household Income Group:
A=0%; B=34%; C=37%; D=29%;
Occupation:
A=11%;B=37%;C=46%;D=0%;E=0%;F=6%
Satisfaction Level:
A=0%;B=0%;C=34%;D=60%;E=6%;
Type Of Trip:
A=43%;B=31%;C=20%;D=6%
Travel Length:
A=20%;B=40%;C=40%;

At SDM Chouraha, based on the above observations and analysis it indicates that maximum numbers of commuters are not having personal vehicles. Therefore, most of the people in this location are choosing paratransit as their mode of transport.

ROAD WAY JUNCTION

1. From the figure8, 54% of commuters using paratransit are having self contained flat and 46% of commuters has rental houses.

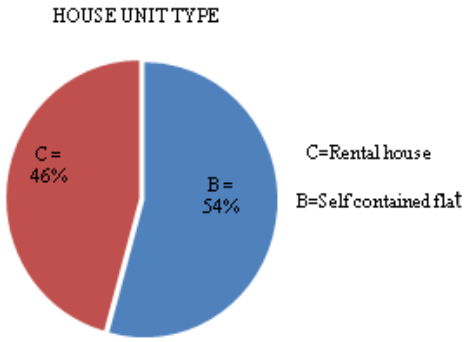


Figure 8. Distribution of responses w.r.t house unit type

2. From the figure9, 48% of commuters using paratransit has no vehicle, 46% of commuters having 1 vehicle and 6% of commuters are having more than one vehicle.

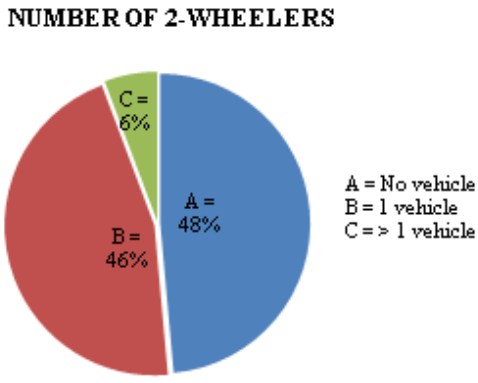


Figure 9. Distribution of responses w.r.t no of 2-wheelers

3. From the figure10, 14% of commuters using paratransit are of Rs.3000-Rs.5000 income group, 34% of commuters are of Rs.5000-Rs.10000 income group and 52% of commuters are having income greater than Rs.10000.

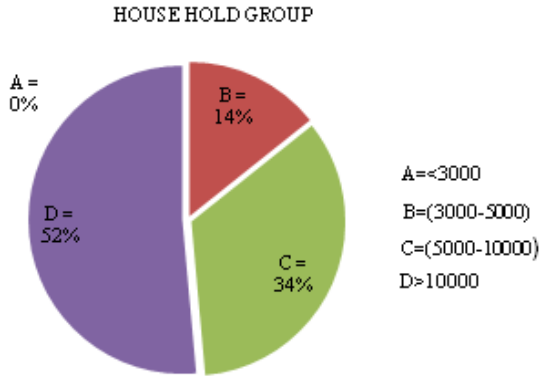


Figure 10. Distribution of responses w.r.t house hold group

4. From the figure11, 3% of commuters using paratransit are students, 37% of commuters are industrial workers and 60% of commuters are businessmen.

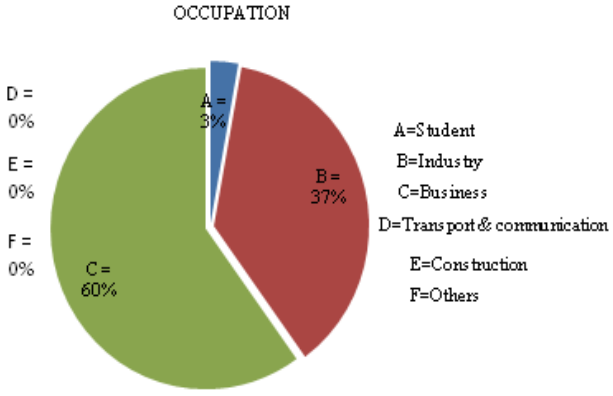


Figure 11. Distribution of responses w.r.t occupation

5. From the figure12, 29% of commuters using paratransit are work based trip, 54% of commuters are personal business trip, 11% of commuters are shopping, 3% of commuters are educational trip and 3% of commuters has recreation trip.

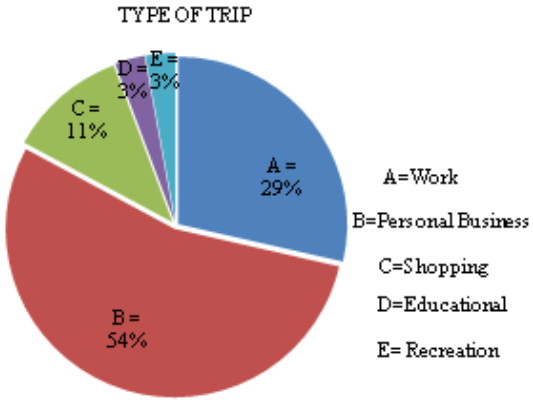


Figure 12. Distribution of responses w.r.t type of trip

6. From the figure13, 40% of commuters using paratransit are having good satisfaction level, 46% of commuters are of average satisfaction level and 14% of commuters are with poor satisfaction level.

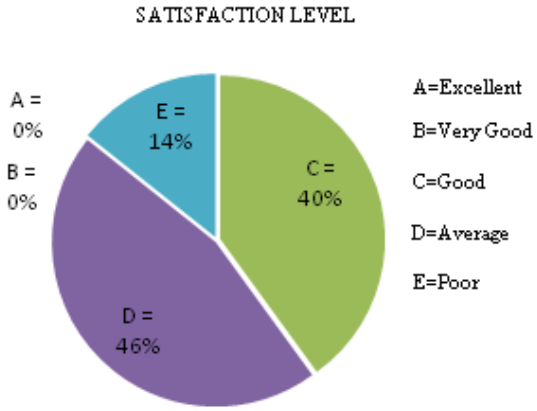


Figure 13. Distribution of responses w.r.t satisfaction level

7. From the figure14, 26% of commuters using paratransit are less than 5km travel length, 34% of commuters are 5-10km travel length and 40% of commuters are greater than 10km travel length.

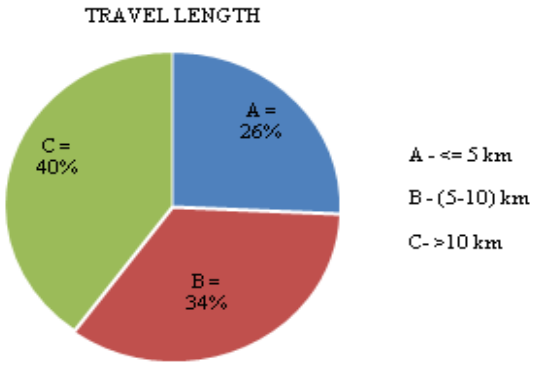


Figure 14. Distribution of responses w.r.t travel length

DISCUSSIONS:
AT ROADWAY JUNCTION
House unit Type:
A=0% ;B=54%;C=46%;
Household Income Group:
A=0%; B=14%; C=34%; D=52%;
Occupation:
A=3%;B=37%;C=60%;D=0%;E=0%;F=0%
Satisfaction Level:
A=0%; B=0%; C=40%; D=46%; E=14%;
Type of Trip:
A=29%; B=54%; C=11%; D=3%; E=3%;
Travel Length:
A=26%; B=34%; C=40%;
Number of 2-Wheelers:
A=48%; B=46%; C=6%;

At Road Ways junction, based on the above observations and analysis, it indicates that maximum number of commuters are having self contained flat and occupation as business. But most of the commuters in this location are using paratransit as their mode for business trips regularly.

MALAKPURI CHUNGI

1. From the figure15, 27% of commuters using paratransit has no vehicle, 60% of commuters has 1vehicle and 13% of commuters are having more than one vehicle

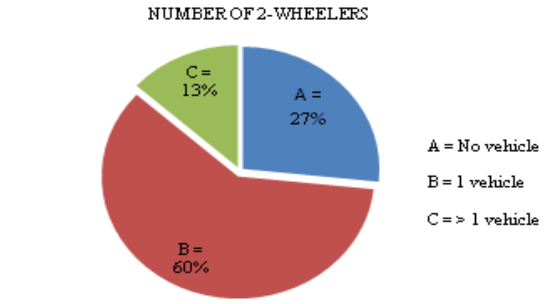


Figure 15. Distribution of responses w.r.t no. of 2-wheelers

3. From the figure16, 3% of commuters using paratransit are luxurious, 50% of commuters are self contained flat and 47% are rental houses.

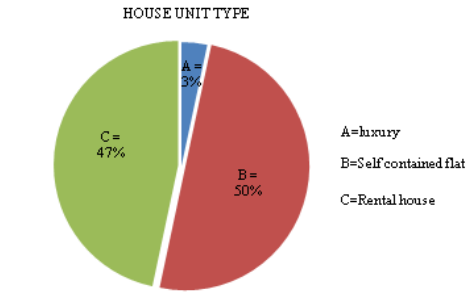


Figure 16. Distribution of responses w.r.t house unit type

3. From figure17, 13% of commuters using paratransit are having monthly household income between Rs.3000-Rs.5000, 34% of commuters are between Rs.5000-Rs.10000 and 53% of commuters are having monthly household income greater than Rs.10000.

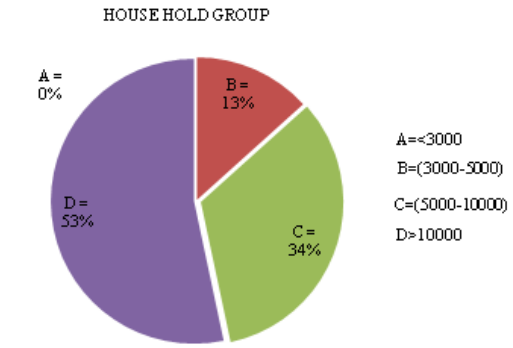


Figure 17. Distribution of responses w.r.t house hold group

4. From the figure18, 20% of commuters using paratransit are students, 27% of commuters are industry based, 50% of commuters are businessmen, and 3% of commuters are construction based.

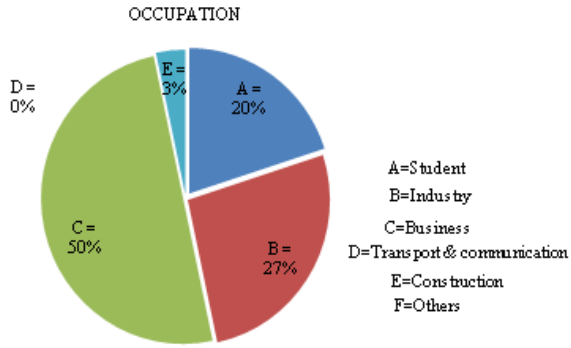


Figure 18. Distribution of responses w.r.t occupation

6. From the figure19, 44% of commuters using paratransit are workbased trip, 23% of commuters are personal business trip, 3% of commuters are shopping, 17% of commuters are educational trip and 13% of commuters has recreation trip

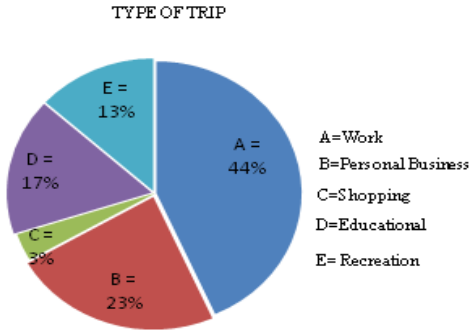


Figure 19. Distribution of responses w.r.t type of trip

6. From the figure20, 57% of commuters using paratransit has good satisfaction level, 30% of commuters has average satisfaction level and 13% of commuters has poor satisfaction level.

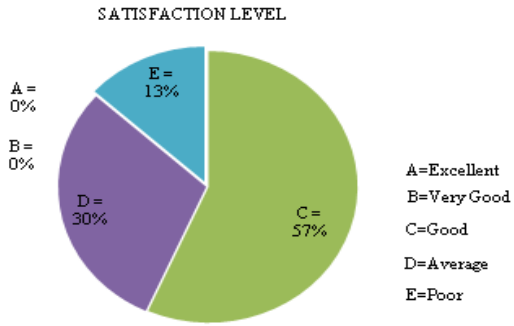


Figure 20. Distribution of responses w.r.t satisfaction level

7. From the figure21, 43% of commuters using paratransit has less than 5km trip length and 57% of commuters has greater than 5km trip length.

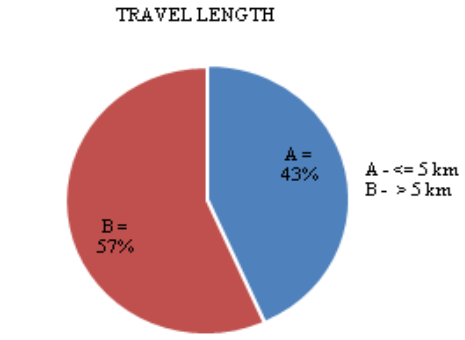


Figure 21. Distribution of responses w.r.t travel length

8. From the figure22, 7% of commuters using paratransit has one or more than one car and 93% of commuters has no car.

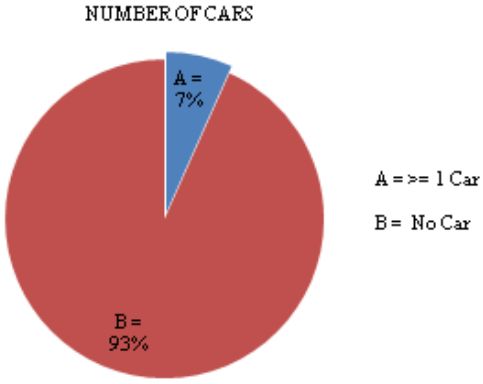


Figure 22. Distribution of responses w.r.t no of cars

DISCUSSIONS: AT MALAKPURI CHUNGI
House unit Type:
A=3% ; B=50%; C=47%;
Household Income Group:
A=0%; B=13%; C=34%; D=53%;
Occupation:
A=20%; B=27%; C=50%; D=0%;E=3%;F=0%
Satisfaction Level:
A=0%; B=0%; C=57%; D=30%; E=13%;
Type of Trip:
A=44%; B=23%; C=3%; D=17%; E=13%;
Travel Length:
A=43%; B=57%;
No of 2-Wheelers: A=27%; B=60%; C=13%;
No of Cars: A=7%; B=93%;

Based on the above observations and analysis at Malakpur Chungi, the maximum numbers of commuters are having atleast one vehicle but many students are using paratransit as their mode in this area.

CONCLUSIONS

i. At SDM Junction, the maximum number of users are rental houses with monthly house hold income group of (Rs.5000- Rs.10000), the users are mostly working in industries nearby which is regarded as their occupation, type of trip generated is work based only ,travel length is greater than 7 kms and their satisfaction level is average.

ii. At Road ways Junction, the maximum number of users are having own houses with house hold income group of greater than Rs.10000, the occupation of the users are mostly business, type of trip generated is personal business, travel length is greater than 5km and their satisfaction level is average.

At Malakpuri chungi Junction, the maximum number of users are of rental houses with house hold income group of greater than Rs.10000 , the occupation of the users are mostly working, type of trip generated is work based trip and educational trips, and their satisfaction level is average.

REFERENCES

[1] Antonio M, “A route set construction algorithm for the transit network design problem”, Vol.36, 2009, pp 2440-2449.
[2] Cathey F. W. et al (2003), “A prescription for transit arrival/departure prediction using automatic vehicle location data”, TR part C, pp 241-264.
[3] Diwakar gupta,etal (2010), “Improving the efficiency of demand-responsive para transit services”, TRR No 44, pp 201-217.
[4] Juan carlos. M (2010), “On the development of public transit in large cities”, TRR vol. 29, pp 379-386.
[5] Kadiyali L. R. (2009). “Traffic Engineering and transportation planning”, Khanna publishers pp 651-657.
[6] Kunle. A (1987), “Para-transit modes in Nigeria” TRR No. 44, pp 339-347.
[7] Mulley C.etal (2009), “Flexible transport services for Research in transportation economics ”, RTE 25, pp 39-45.
[8] Phuong Nguyen-hoang. etal (2010), “What is para transit worth” for Transportation Research, TRR No 44, pp 841-853
[9] Peter. T etal (2006), “Vernacular cabs : Jitneys and gypsies in cities”, TRR No. 44, pp 457-468.
[10] Rastogi. R etal (2003), “Defining Transit accessibility with environmental inputs”, TR Part D, pp 383-396.

Synthesis Characterization and Spectral Studies of Bisdithiocarbamate of Urea and its Metal Complexes

P.Saritha
CVR College of Engineering, Department of H&S, Ibrahimpatnam, Telangana., India
Email: perumandla.saritha@gmail.com

***Abstract*- A novel disodium salt of Bisdithiocarbamates of urea (UBDT) and its metal complexes, Co(II)UBDT, Ni(II)UBDT, Cu(II)UBDT and Cd(II)UBDT were prepared and characterized by Elemental Analysis, Conductivity Measurements, Infrared Spectroscopy, Electronic Spectroscopy and NMR Spectroscopy. Water-soluble UBDT possessed good chelating ability for various metal ions. Its complexes, Co (II), Ni (II), Cu (II) and Cd (II) are amorphous, intractable solid having polymeric structure. The ligand as well as the complex was found to possess high thermal stability.**

***Index Terms* - Synthesis, Bisdithiocarbamates, Metal Complexes and Characterization.**

I. INTRODUCTION

Dithiocarbamates are S, N containing ligands, which display a rich and varied coordination chemistry with a wide range of transition and main group metal complexes. The chemistry of these compounds has aroused special interest because of the analytical purpose, as well as their industrial applicability [1-3]. Their metal complexes present striking structural features and have diversified applications, such as high pressure lubricants in industry, fungicides and pesticides, and also as accelerators in vulcanization [4]. Dithiocarbamates have also found important use in medicine as anti-alcoholic drug [5], anticancer [6], and recently as co-adjuvant in AIDS treatment [7]. This is related to their strong metal binding capacity, hence could act as inhibitors of enzymes [8]. Thermo analytical methods are of great interest due to their wide applicability in the industrial processes that involves the thermal decomposition reactions of solids [9, 10]. Hence research in this area has gained increased attention [11].

II. EXPERIMENTAL METHOD & MATERIALS

Urea (U) was obtained from Loba Chemie Ltd., India. Encore, R. Johnson group, India, supplied carbon disulfide. Qualigens (Glaxo) supplied sodium hydroxide, acetone. Acetates of Co (II), Ni (II), Cu (II), Cd (II), are purchased from E. Merck, India. All the chemicals used were of analytical grade and were used without further purification.

A Preparation of Disodium Salt of Bisdithiocarbamate from UREA (UBDT)

The Bisdithiocarbamates of urea (UBDT) were prepared, from 0.1M Urea, 0.2M Sodium hydroxide and 0.2M carbon disulfide in water with constant stirring below 10^oC. The reaction mixture turned orange in half an hour. It was then allowed to stand at room temperature for several days with intermittent stirring until the carbon disulphide layer completely disappeared. The orange colored mixture was warmed at 50^oC for 1 h, and then cooled to room temperature. The product slowly crystallized into colorless crystals. The crystalline products were washed with acetone and recrystallised from water. The crystals of UBDT are water-soluble and did not melt up to 360^oC.

B. Preparation of Metal Complexes of UREA Bisdithiocarbamate

Metal complexes of various bisdithiocarbamates of urea were prepared by mixing an aqueous solutions of ligand (UBDT) and metal salts of Ni, Cu, Co, Cd in equimolar ratio. The metal complexes are precipitated as fine powder instantaneously. For the coagulation of fine particles in every case, the mixture was stirred magnetically for 30minutes then kept overnight at room temperature, filtered, washed thoroughly with water and dried. The metal complexes are amorphous solids insoluble in water and common organic solvents.

III. PHYSICAL MEASUREMENTS

IR spectra of bisdithiocarbamates of urea were recorded on a Perkin-Elmer spectrometer model 1430 in the range of 4000-600 cm^{-1} using KBr pellets. UV–visible spectra were recorded on a Unicam spectrometer model UV-2-100. ^{1}H-NMR spectra were recorded on a Bruker DRX–300 FT-NMR spectrometer in $CDCl_3$ solutions. The synthesized ligand UBDT and its complexes were subjected to elemental analysis using Perkin Elmer elemental 2380 model. Sulfur was quantitatively determined by oxidizing the bisdithiocarbamates with alkaline potassium permanganate and gravimetric determination as barium

sulfate. The molar conductivity of solution of the synthesized complexes was determined using digital conductivity meter model-DI 9009.

IV. RESULTS AND DISCUSSION

Disodium salt of bisdithiocarbamates of urea (UBDT) and its metal complexes were prepared are stable at room temperature unaffected by atmospheric oxygen and moisture, insoluble in water and in common organic solvents. The complexes are amorphous and do not melt up to 360°C however decomposes above 200°C. The yields of recrystallised products and analytical data are given in *Table-1*.

A. Conductance Measurements

The molar conductance of 0.1M aqueous solution of UBDT was found to be 188$Smol^{-1}Cm^2$, indicating its electrolytic nature [22].

B. IR Spectral Analysis

Bisdithiocarbamates of urea (UBDT) shows three main regions in the infrared spectrum [12-16]. The broad band in the region 3400-3100 cm^{-1} appear due to ν(N-H) and ν(O-H) of water molecules associated with the ligand. The 1450-1550cm^{-1} band due to ν(C-N) vibration of the $S_2C=NR_2$ & the 950-1050 cm^{-1} region which is associated with ν(C-S) vibrations in the ligand [14].

IR spectra of UBDT made it evident that the symmetric and asymmetric stretching vibrations of $–NH_2$ groups of urea observed at 3447 and 3348 cm^{-1} merged into a single band at slightly higher wave number at 3467 cm^{-1} on dithiocarbamylation. The strong absorption due to the stretching vibration of strongly H-bonded carbonyl group (amide I) at 1689cm^{-1} shifted to 1696 cm^{-1} with reduction in intensity and was overlapped by δOH from absorbed water molecules. The amide II vibration, which appears in urea at 1630.7cm^{-1} shifted to 1660 cm^{-1} as a shoulder in UBDT. The thioamide III band of urea at 1466 cm^{-1} shifts to slightly lower frequency at 1460 cm^{-1} in UBDT, which confirmed that nitrogen electron pair is conjugated to dithiolate group. The bands at 1019 and 861 cm^{-1} can be ascribed to the ν_{as} and ν_s of the CS_2 groups.

C. IR Spectral Analysis of Metal Complexes of UBDT

The IR spectral data of metal complexes of UBDT shows very intense band at 1459.6cm^{-1} indicating a sufficient double bond order for C—N, as thioureide band is characteristic of dithiocarbamate intermediate between a C═N band (1690-1640cm^{-1}) and a C—N band (1360 — 1250cm^{-1}). The thioureide band characteristic of dithiocarbamates at 1459.6cm^{-1} splits upon complexation in all the cases with a wide separation of almost 100cm^{-1} in complexes suggested that in UBDT due to electron delocalization –C—N (A) and –C—N (B) bands are equivalent but on coordination metal ion contribution of the canonical forms (*scheme-1*) becomes greater and these two bands become non-equivalent resulting in appearance of two distinct IR bands. [23-24]

The band at 1696 cm^{-1} in UBDT involves significant contribution from NH bending vibrations besides ν (C = O).

TABLE I
PHYSICAL AND ANALYTICAL DATA OF UBDT [a] AND METAL COMPLEXS

Molecular formula	color	M.P (°C)	Yield %	Elemental Analysis found (Calculated) %				
				C	H	N	S	M
$C_3H_2N_2S_4ONa_2.3H_2O$	Yellowish Orange	135	88	11.90 (11.61)	2.51 (2.58)	8.96 (9.02)	40.82 (41.20)	--
$C_{16}H_{20}N_4O_{14}Na_2Co_3$ ($L_2Ac_6Na_2Co_3$)	purple	220[b]	57	18.9 (19.2)	2.32 (2.00)	5.8 (5.6)	25.4 (25.6)	16.9 (17.7)
$C_{16}H_{20}N_4O_{14}Na_2Ni_3$ $L_2Ac_6Na_2Ni_3$	Light green	180[b]	52	18.9 (19.0)	1.90 (2.0)	5.0 (5.6)	26.46 (25.70)	16.7 (17.4)
$C_{14}H_{16}N_4O_{10}Na_2Cu_3$ ($L_2Ac_4Na_2Cu_3$)	Seacrest green	210[b]	61	18.7 (18.8)	1.82 (1.79)	5.9 (6.2)	28.2 (28.7)	20.6 (21.3)
$C_{16}H_{20}N_4O_{14}Na_2Cd_3$ $L_2Ac_6Na_2Zn_3$	yellow	>360	65	16.1 (15.8)	2.1 (1.6)	4.9 (4.5)	25.8 (25.1)	18.2 (19.3)

L & a = -SSCNHCONHCSS; Ac = CH_3COO^- ; b= decomposes without melting

A broad band at 1018.6cm^{-1} with medium intensity, is due to absorbance of asymmetric C—S stretching and a intense sharp band at 860.7cm^{-1} may be assigned to symmetric C—S stretching frequencies. On complexation in most of the complexes the bands corresponding 1018.6cm^{-1} band of UBDT appears with greatly decreased intensity, disappeared in cobalt (II) acetate and nickel (II) acetate complexes. Zinc (II) acetate complex is shifted downward with weak absorption.

The intense bands due to carbonyl stretching overlapped by δOH from water molecules almost disappear in all the complexes. Thus, all these observations lead to conclude that, all the donor atoms *viz.*, O, N, and S are involved in coordination. Presence of

water molecules in all the complexes is ruled out because the bands associated with water molecules are not observed in the IR spectra. The IR spectra of other bisdithiocarbamates can also be interpreted on similar grounds. The characteristic peaks due to dithiocarbamyl groups were observed in every case.

D. NMR Spectral Analysis

A broad signal was observed in 4.9 to 5ppm range due to -NH- proton in ^{1}H-NMR spectrum of UBDT. ^{13}C- NMR spectrum exhibited a single signal at 164.5ppm. It is freak that instead of two signals for C = O and CS_2 carbons only one signal was observed indicating resonance nature hence, it is suggested because of extensive conjugation, only one signal was observed for UBDT[17]. Additional support was obtained from electronic spectroscopy, conductivity measurements. NMR spectra of metal complexes could not be recorded due to insoluble in nature.

E. Electronic Spectral Studies

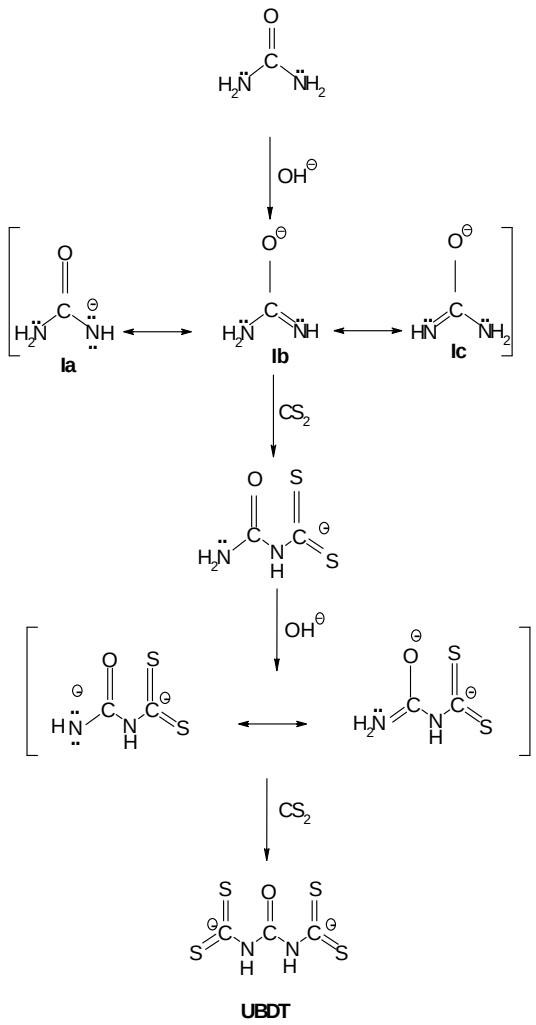
For UBDT a prominent absorption band at 233 nm (log ε 3.45) may be ascribed to π→ π* transition of carbonyl group. The π→ π* transitions associated with conjugated nitrogen (N-C-S) and conjugated sulfur (S-C-S) observed at 284 nm (log ε 2.18) and 297 nm (log ε l.34), respectively. The low absorption intensities as compared to those reported in literature for dithiocarbamates may be ascribed to the symmetrical structure of molecule. For symmetrical molecules many of the electronic transitions especially the n → π * transitions are forbidden because of several restrictions. [18, 19]

In the Cu (II) complex a broad asymmetric absorption band observed in 15000-10500cm^{-1} region with maxima at 12453cm^{-1} is consistent with the distorted octahedral geometry [18-21].

For Co (II) complexes, the ν_3 band from absorption characteristic of octahedral geometry is observed in all the cases and the double peak entails the splitting of $^{4}T_{1g}$ (P) state. The weak bands due $^{4}T_{1g}\rightarrow{}^{4}T_{2g}$ transition are observed for cobalt (II) acetate.

The UBDT complex of nickel (II) acetate shows bands with maxima at 25575cm^{-1}, 13888cm^{-1}, and shoulder at 15220cm^{-1}. These bands are in accordance with the octahedral geometry and correspond to the transitions $3A_{2g} \rightarrow 3T_{1g}(F)$ and $3A_{2g} \rightarrow 3A_{1g}(F)$ respectively. The spectrum showed an upward trend above 1100nm (10000cm^{-1}) indicating that a band may be present in near

infra-red region, which could not be located due to instrumental limitations. This band may correspond to $^{3}A_{2g} \rightarrow {}^{3}T_{2g}$ (F), (ν_1) transition.



Scheme.1-Tentativemechanismfor bisdithiocarbamates formation from urea

TABLE -II
ELECTRONIC SPECTRA OF UBDT METAL COMPLEXES

Ligand/Complexes	Ligand transition band $n \rightarrow \pi^*$		$3A_{2G} \rightarrow 3T_{1G}(P)$ v_3 17000-22000 cm^{-1}		$3A_{2G} \rightarrow 3T_{1G}(F)$ v_2 11000- 17000 cm^{-1}	
	(nm)	*(cm^{-1})*	*(nm)*	*(cm^{-1})*	*(nm)*	*(cm^{-1})*
CoAcUBDT	323 376 393	30959 26595 25445	506 516	19762 19379	812 843	12315 11862
NiAcUBDT	391	25575	522	19157	657 720	15220 13888
CuAcUBDT	405 425	24691 23529			805	12453
CdAcUBDT	391 403	25505 24822	459 490	22271 20042		

CONCLUSIONS

Novel bisdithiocarbamates was prepared from urea, a tentative mechanism involving nucleophilic attack by the anionic species, formed in the presence of strong alkali Sodium hydroxide, on the CS_2 has been proposed in Scheme *I*. Due to the low reactivity of these weak nitrogenous bases, longer reaction time was required. Spectral analysis and conductivity measurements suggested efficient electron delocalization within the molecules of bisdithiocarbamates. UBDT and metal complexes of UBDT are thermally quite stable and heat resistance. BDTCs were water-soluble with good complexing ability for various metal ions. The thermal stability of the ligand UBDT has increased by complexation with metal ions due to formation of ring (chelate) structure which provides additional stability to the complexes. Polymeric nature of the metal complexes was inferred based on amorphous and intractable nature. Further studies of bisdithiocarbamates, its metal complexes and biological activity are in progress.

REFERENCES

[1] Scarcia, V.; Furlani, A.; Fregona, D.; Faraglia, G.; Sitran, S.Palladium and platinu dithiocarbamato complexes containing mono- and diamines. *Polyhedron* **1999**, *18*, 2827–2837.

[2] Bajpai, A.; Tiwari, S. Application of thermogravimetric analysis for characterization of bisdithiocarbamate of urea and its copper (II) complex. *Thermochim. Acta* **2004**, *411*, 139–148

[3] Singha, A.; Dutta, D.P.; Tyagi, A.K.; Mobin, S.M.; Mathur, P.; Lieberwirth, I. Palladium(II)/ally palladium(II) complexes with xanthate ligands: Single-source precursors for the generation of palladium sulfide nanocrystals. *J. Organom. Chem.* **2007**, *692*, 5285–5294.

[4] Ondrušová, D.; Jóna, E.; Šimon, P. Thermal properties of *N*-ethyl-*N*-phenyl-dithiocarbamates and their influence on the kinetics of cure. *J. Therm. Anal.* **2002**, *67*, 147–152.

[5] Vettorazzi, G.; Almeida, W.F.; Burin, G.J.; Jaeger, R.B.; Puga, F.R.; Rahde, A.F.; Reyes, F.G.; Schvartsman, S.International safety assessment of pesticides: Dithiocarbamate pesticides, ETU and PTU A review and update. *Teratog. Carcinog. Mutag.* **1995**, *15*, 313–337.

[6] Milacic, V.; Chen, D.; Ronconi, L.; Landis-Piwowar, K.R.; Fregona, D.; Dou, Q.P. A Novel anticancer gold (III) dithiocarbamate compound inhibits the activity of a purified 20S proteasomeand 26S proteasome in human breast cancer cell cultures and xenografts. *Cancer Res.* **2006**, *66*, 10478–10486.

[7] Rabbi, M.F.; Finnegan, A.; Al-Hartli, L.; Stong, S.; Roebuck, K.A. Interleukin-10 enhances tumornecrosis factor-α activation of HIV-1 transcription in latently infected T cells. Acquired ImmuneDefic. *Syndr. Hum. Retrovirol.* **1998**, *19*, 321–331.

[8] Malik, A.K.; Faubel, W. Methods of analysis of dithiocarbamate pesticides: A review. *Pestic Sci.***1999**, *55*, 965–970.

[9] Santos, J.G.; Conceição, M.M.; Trindade, M.F.S.; Araújo, A.S.; Fernandes, V.J., Jr.; Souza, A.G.Kinetic study of dipivaloylmethane by Ozawa method. *J. Therm. Anal. Calorim.* **2004**, *75*, 591–597.

[10] Conceição, M.M.; Ouriques, H.R.C.; Trindade, M.F.S.; Prasad, S.; Filho, P.F.A.;Souza, A.G. Kinetics of decomposition of alkyl ammonium salts. *J. Therm. Anal. Calorim.* **2004**, *75*, 569–576.

[11] Souza, A.G.; Oliveira, M.M.; Santos, I.M.G.; Conceição, M.M.; Nunes, L.M.; Machado, J.C.Kinetic analysis of the thermal decomposition of dialkyldithiocarbamates chelates of indium(III).*J. Therm. Anal. Calorim.* **2002**, *67*, 359–363.

[12] R. Kellner, G.S. Nikp and N. Trendafilova, *Inorg. Chim. Acta*, 84, 233(1984).

[13] R.M. Silversten G C Bassler and T.C.Morrill, *Spectrometric Identification of Organic Compound*, 4th Edn., John Wiley & Sons, New York, 130(1981).

[14] K. Nakamoto, *Infrared Spectra of Inorganic and Coordination Compounds*, 5th Edn., Wiley Interscience, New York, 167(1968).

[15] D.A.Brown, W.K.Glass and M.A. Burke *Spectrochim Acta*, 32A, 137(1976).

[16] L.J.Bellamy, The *Infrared Spectra of Complex Molecules*, John Wiley & Sons, New York, (1964).

[17] J. Kaur, S.S. Marwaha and G.S, Sodhi, *J.Ind.Chem.Soc.* 76,185(1999).

[18] H.P. Koch, *J.Chem.Soc*, 401(1941).

[19] M.J.Jenssen, Rec.*Trav.Chim*, 79,454,464(1960).

[20] M.J.Jenssen, Rec.*Trav.Chim*, 79, 1006(1960).

[21] W.Kemp, *Organic Spectroscopy*, Macmillan Press Ltd, Hong Kong London 3rd Ed., 276(1991).

[22] S.Glasstibe, *An Introduction to Electrochemistry*, 10th Edn., D.Van Nostrand Company, Inc. New York, 71 (1968).

[23] D.B. Brown, M.B. Robing and R.D. Burbank, *J. Am. Chem. Soc.*, 90, 5621 (1968).

[24] D.B. Brown, M.B. Robing and R.D. Burbank, *J. Am. Chem. Soc.*, 91, 1895 (1969).

An Empirical Study of the Citizen's Perception of Automation Process of Government in India Through E-Governance.

Dr. M.S.Bhat[1] , Dr. Piyush Gupta[2] and Maj.Gen. (retd.) Dr. R.K.Bagga[3]
[1]CVR College of Engineering, Department of EIE, Hyderabad, India
bhatms@rediffmail.com
[2] Senior General Manager, National Institute of Smart Governance, Hyderabad
piyush.gupta@nisg.org
[3]Advisor, Outreach Division, IIIT, Hyderabad
rbagga@iiit.ac.in

***Abstract*--E governance has brought in considerable benefits both to citizens and the administration. From the administration point of view, many routine aspects of administration categorized as programmable work can be computerized thereby increasing efficiency and reducing cost. From the citizen's point of view, e governance would mean automation and standardization of government service delivery thereby eliminating red tape. The reduction in frequency of human interfacing can be an important benefit from the perspective of citizen, as it could minimize delays and chances of corruption. E governance can indeed be very successful if citizen's perception of the e-governance is properly studied and measures taken to improve the situation. In this paper the citizen's perception of e-governance is studied empirically. Based on the response to a structured questionnaire administered to 400 citizens approaching e-seva centers, a statistical study on their perception using Pearson Correlation is made, Chi-Square Test for goodness of fit is conducted and relevant conclusions drawn. The process of sampling is attempted to be done on a quasi-random basis to ensure that the sample is as representative as the population seeking the services to minimize sampling errors.**

***Index-terms*--e-governance, G2C, Citizen's perception, Pearson Correlation**

I. INTRODUCTION

The infusion of technology in every field has always been providing more than commensurate returns. It is undoubted and undeniable fact that technology always brings efficiency, cost reduction, easier replication and better quality and transparency in any process where it is applied. Even the orthodox antediluvian, who romanticizes old way of life and living, would have to admit that technology is value neutral and it is the human nature that makes it double edged sword. The automation in all spheres is enabled mainly through technology. In the earlier stages of technological development, it was merely viewed as a tool for better manufacturing. It is now more than evident that the technology has made heavy inroads into service sectors and the delivery of any service is made better and superior in quality with technology component. From the citizen's perspective, Government is one of the important service delivery institutions-- more so, in modern welfare oriented democratic government set ups. Technology seems to have invaded this domain too and had brought about considerable benefit. E-Governance is something which is keenly embraced by various governments in the world to varying degrees.

II. E-GOVERNANCE CLASFICATION

The idea of e-Government can be classified into four categories- G2C,G2B,G2G, and G2E. This classification is based on differences in nature of interactions that different type of stakeholders have with the government.

*2.1 GOVERNMENT TO CITIZEN(G2C):*This classification refers to the Information and Communication Technology interface between the government and citizens. A G2C service expands the availability and accessibility of the government to an anytime anywhere more. This gives citizens the choice of when to interact with the government – 24 hours a day, 7 days a week; from where to interact with the government- service centre, unattended kiosk or from the comfort of one's home; and how to interact---though internet, fax, telephone, email, face to face etc. In terms of frequency of interaction this is one of the important classifications as there is large volume of interactions in term of numbers. In a democracy where people decide as to who should rule them, the way G2C functions is very crucial, as the service is directed to an

important stake holders. The stake holders collectively are in a position to change the government and a

government sensitive to the needs of the people should endeavor to make this service as efficient as possible. Being the instrument of an important interface, there is no denying the fact this requires constant attention and innovation. That is the reason why this particular service is taken up for specific study in this article and a survey of 400 citizens approaching three e –seva centers at Hyderabad is conducted.

2.2 GOVERNMENT TO BUSINESS G2B: This category of ICT enabled service helps the business community-providers of goods and services- to seamlessly interact with the government. There are number of areas requiring government clearance by business community and often this involves clearance from various departments of the government.

*2.3 GOVERNMENT TO GOVERNEMNT G2G:*This kind of ICT enabled interaction takes place within the sphere of the government. G2G can be horizontal i.e. between different government agencies or vertical i.e. between national, state and local government agencies. In the context of our country, there are large number of state governments and local bodies. The set up is essentially federal and there is good deal of communication in order that there is a well coordinated effort. For smooth coordination and functioning of governments on truly federal basis as intended by constitution makers of India, it is equally important that the interment of G2G interface functions without any hitch

2.4 SIMILARY GOVERNEMNT TO EMPLOYEES G2E: refers to the delivery of services by the Government to its employees. These types of services primarily relate to human resource areas.

III. METHODOLOGY

A structured questionnaire tested for statistical reliability was administered to 400 citizens. The citizens were chosen at random (essentially known as mall intercept method). The nature of arrival rate of the individuals at e-seva Center and their demographic profile is unknown and cannot be predetermined. At any point of time, when survey is undertaken at the e seva center, as the arrival of citizens is unknown before hand and as they do not follow an expected pattern, the sample can be considered random. The survey was done at three e seva centers chosen at random at Hyderabad. We have therefore, two stages sampling process—first in terms of sampling of the center and them sampling of respondents visiting the center. The questionnaire administered to citizens consists of 11 questions with a few questions intended to get the demographic information of the respondents. The questions are all close- ended in nature with options for responses indicated in the question itself. The last question is designed such that it makes the respondents to rank the various attributes of the e-seva center already considered in the order of priority for success of the automation project as a whole as perceived by the respondents. The complete responses received from 363 citizens were analyzed statistically. The rate of return of filled in questionnaire was 90.75% which can be considered as fairly good rate of return of responses for such kind of surveys .

IV. RESEARCH HYPOTHESIS

H1. The usefulness of a G2C e governance project is associated with the fulfillment of expectations of the citizens.

H0: Null Hypothesis:The usefulness of a G2C e-governance project is independent of the fulfillment of expectations of the citizen.

V. CITIZEN'S SURVEY RESPONSE CODE CONVERSION:

To study the relationship between variables of interest, the responses obtained from the 11 item questionnaire was converted from 4 point scale to dichotomous responses. The table 1 gives the citizen response code and the relevant conversion taken for data analysis.

VI. CORRELATION ANALYSIS

The data obtained from citizen questionnaire was subjected to Pearson Correlation analysis Table.2 for the following parameters:

1. Usefulness of e Seva project.
2. Satisfaction of service given by Operator
3. Overall satisfaction from the Center
4. Number of visits to the Center.
5. Distance of the Center from home.

TABLE. I
CITIZEN SURVEY RESPNSE CODE CONVERSION

Description of variable	Response code	Converted code
Variable related to awareness of services available at the center	1. no idea 2. somewhat aware 3. reasonably aware 4. well aware	0 (No idea) if response code is either 1 or 2.. 1 (Well aware) if response code is either 3 or 4.
Variable related to distance from the center	1. less than 1 km. 2. 1 to 3 km 3. 4 to 5 km 4. 6 to 10 km 5. more than 10 km	0 (less than 3 km) if response code is either 1 or 2. 1 (more than 3 km), if response code is either 3,4 or 5.
Variable related to usefulness of center	1. not at all useful 2. slightly useful 3. quite useful 4. very useful	0 (not useful) if response code is either 1 or 2. 1 (very useful if response code is either 3 or 4.
Variable related to services of operator	1. not at all satisfied 2. low satisfaction 3. neither satisfied nor dissatisfied 4. very satisfied	0 (not satisfied) if response code is either 1 or 2. 1 (very satisfied) if response code is either 1 or 2.
Variable related to overall satisfaction	1. not at all satisfied 2. low satisfaction 3. neither satisfied nor dissatisfied 4. very satisfied	0 (not satisfied), if response code is either 1 or 2. 1 (very satisfied) if response code is either 3 or 4
Variable related to gender	1. male 2. female	1 for male 2. for female

TABLE.II
PEARSON CORRELATION MATRIX

parameter	Statistical Attribute	Usefulness of E-seva Center	Satisfaction Of service-Operator	Overall satisfaction From the Center	No of Visits to the Center	Distance of the Center from home
Usefulness of e-seva Center	Pearson Correlation	1	0.409**	0.356**	0.85	.146**
	Significance 2 tailed		0.000	0.000	.107	.005
Satisfaction of Service given By operator	Pearson Correlation	0.409**	1	0.528**	0.049	.029
	Significance 2 tailed	0.000		0.000	.355	.586
Overall satisfaction from The center	Pearson correlation	.356**	.528**	1	0.036	-.014
	Significance 2tailed	0.000	0.000		.491	.797
Number of visits to the Center	Pearson Correlation	0.085	.049	.036	1	.235**
	Significance 2tailed	.107	.355	.491		.000
Distance of the Center from home	Pearson Correlation	.146**	0.029	-.014	.235**	1
	Significance 2tailed	.005	.586	.797	.000	

The analysis of the correlation matrix indicates that a few of the observed matrix were strong. The positive relationship was observed between "satisfaction of service given by the operator and "the overall satisfaction experienced by the citizen from the center" (r=0.528). This indicates that the quality of service given by the operator contributes to the overall satisfaction of the citizen from the centre. Another positive correlation was established between "usefulness of E seva center and "satisfactory of service given by operator" (r=0.356).

The relation between "distance of center from home" and "number of visits to the center" (r=.235), and between "distance of center from home" and "usefulness of e seva Project" (r=0.146) though positive in both cases, is weak in nature. Another important correlation observed is the negative correlation between the "distance of center from home" and "overall satisfaction from the center" (r=-ve0.014). This observation is important from the manner in which the "distance variable was coded in the Citizen Survey Response.

The survey did not intend to cover demographic attributes. However, it was found that there is no significant difference between the prioritized expectation of male and female citizens (Spearman Rank Correlation coefficient=0.7) Hence, the perception of male or female citizens may be considered as overall perception of citizens in general. However, the overall satisfaction of the citizen from the G2C project contributes to the overall usefulness of the project.

The statistical analysis reveals that the overall usefulness of the project depends on the following factors (1) Satisfaction of service given by Operator (2) Overall satisfaction from the center (3) number of visits to the center. The analysis also reveals that the "distance of the center from home of a citizen" has a direct impact on the "overall satisfaction from the center".

VI. CHI-SUARE TEST FOR GOODNESS OF FIT

The results of Chi-Square analysis for Goodness of Fit conducted are tabulated as shown in Table. 3 and the inferences are drawn as under.

TABLE III
TEST STATISTICS

	Usefulness of center	Operator level satisfaction	Overall satisfaction	Distance of center from home
Chi-Square	287.408	236.499	208.333	324.102
Df	1	1	1	1
Significance	.000	.000	.000	.000

The Chi-Square statistics (Table-2) 287.408,236.499,208.333 and 324.102 for usefulness, operator level satisfaction, overall satisfaction and distance with its small significance level, p less that 0.001 for all the variables indicate that a normal distribution provides a Good Fit to the observed data. Thus we can reject the null hypothesis and test results support the research hypothesis that the usefulness of a G2C e-Governance project is associated with the fulfillment of expectations of the citizens.

VII. CONCLUSION

One of the research objectives was to study citizen expectations and performance of the e-Governance project. The data analysis of the citizen survey has given sufficient understanding on their expectations and performance of the project from citizen perspective. The analysis reveals that the citizens have different expectations across the age group, gender or occupational background of citizens. The importance of a similar expectation also differs amongst citizens who have visited the centers to avail government services. The statistical data analysis validates the research hypothesis that citizens find the e-Government project useful if their expectations are met by the project.

REFERENCES

[1] Ahmed Al-Omari and HusseinAl-Omar, E- Government Readiness Assessment Model, Journal of Computer Science 2 (11): 841-845,2006

[2] Andria Di Maio, David McCluire: Using the E-Government Assessment Questionnaire

[3] Bata KDey. E Governance in India: Problems, Challenges and Opportunities - A Future's Vision

[4] Department of Information Technology, Ministry of Communications & IT Government of India, Impact Assessment Study of e-Governance projects in Indian Report, 2007

[5] Evaluating e-Governemnt: M.P Gupta, Jaijit Bhattacharya, Ashok Agarwal, published in Governance Case Studies, Ashok Agarwal, University press, 2007

[6] Piyush Gupta, Challenges and Issues in e-Government Project Assessment, paper presented and published as part of the ICEGOV 2007, Dec10-13, 2007 Macao, China

[7] Piyush Gupta, R.K. Bagga, Book edited "Compendium of Project initiatives in India", University Press ,2008.