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EDITORIAL

It is with immense pleasure that we bring Volume-11 of the Biannual Journal of our college, CVR Journal of Science and Technology. For the first time this journal is brought out in colour. We thank the Management for the same. The figures and graphs in colour will enable the researchers and readers to have more clarity. We have received good number of research papers for review, from our own faculty and from outside our institution also. A rigorous filtration process is done, anti plagiarism check by software, and review by experts are done. Finally research papers were selected for publication in the present volume. We are also happy to share with the readers that the college is **Accredited by NAAC with 'A' grade and NBA Accreditation** is also obtained. Affiliation for all courses and all seats in all branches is also obtained from JNTUH. It is expected that the contributors will further enhance the reputation of the college through this Journal.

The breakup of the papers among various branches is:

The research papers from Civil engineering cover the areas of rheology, fracture energy, nonlinear static procedures on high rise buildings. Research papers from Mechanical engineering cover investigation on wear characteristics and analysis and design of plastic mold for male insulator. A survey paper on computational intelligence is contributed by CSE department. The research papers in the ECE branch cover interesting areas like SoC using ANFIS algorithm, SIFT algorithm, Static and Dynamic Core Assignment and WT based speech compression using VC++.

The research papers from EEE Department cover the areas of Transformerless PV inverter, Rooftop Solar Plants and DG with micro grid. Research papers received from EIE Department cover the areas of orthogonal frequency division multiplexing for SDR, optimizing leakage power in FPGAs and chemical combustion process in rotary kiln using LabVIEW. Contribution from IT department authors is on dynamic load balancing and user level runtime systems. A brief overview on conservation of lakes in India is contributed by H&S faculty.

The management is supporting the research and Ph.D Programmes by liberally sanctioning study leave for the faculty of this college. Faculty members working for Ph.D and on research projects are expected to contribute for the journal. Management is also encouraging the authors of research papers with incentives, based on merit. Some of the research articles accepted for publication in Vol. No. 12 are listed on Pg. No. 111.

I am thankful to all the members of the Editorial Board for their help in reviewing and short listing the research papers for inclusion in the current Volume of the journal. I wish to thank Dr.S.Venkateshwarlu, HOD EEE and Associate Editor, for the pains he has taken in bring out this Volume. Thanks are due to HOD, H & S, Dr. E. Narasimhacharyulu and the staff of English Department for reviewing the papers to see that grammatical and typographical errors are corrected. I am also thankful to Smt. A. Sreedevi, DTP Operator in the Office of Dean Research for the effort put in the preparation of the papers in Camera Ready form.

For further clarity on waveforms, graphs, circuit diagrams and figures, readers are requested to browse the soft copy of the journal, available on the college website **www.cvr.ac.in**, wherein a link is provided and is available in color.

(CONTENTS	age No
1.	Studies on Rheology, Strength and Cementing Efficiency of High Strength Grade Quaternary Blended Self-Compacting Concrete Incorporating High Reactivity Metakaolin M V Seshagiri Rao, S Shrihari, V Srinivasa Reddy	1
2.	Need For Fracture Behaviour Based Designer Friendly Expressions For Fracture	7
	Energy and Minimum Flexural Reinforcement	4
	T Muralidhar rao, T.D.Gunneswara Rao	
3	Investigation on Effects of Nonlinear Static Procedures on High Rise Buildings	13
	Sreenath Mahankali, P.V.V.S.S.R.Krishna	10
4.	Fracture Parameters of Plain Concrete Beams Using ANSYS	18
	Manasa Koppoju, T. Muralidhara Rao	10.70
5.	Transformerless Photo Voltaic Inverter Topologies for Low Power Domestic Applications	29
	G. Janardhan, N.N.V. Surendra Babu	
6.	A Distributed Generation System with Micro Grid for Effective Energy Management	35
	Kalluri Deepika	
7.	Performance Analysis of Rooftop Solar Plants in CVR College of Engineering: A Case Study	41
	P. Rajesh Kumar, Ch. Lokeshwar Reddy	
8.	Investigation of wear characteristics of Fe-Cr-C hardfacing alloy on AISI-304 steel	47
	K.Sriker, P.Uma Maheshwera Reddy, M.Venkata Ramana	
9.	Analysis and Design of Plastic Mold for Male Insulator of Solar Connector using Plastic Advisor 7.0	51
	Lokeswar Patnaik, Sunil Kumar	
10,	SoC Based Sigma Delta ADC Using ANFIS Algorithm for ECG Signal Processing Systems	57
	M. Alakananda, B. K. Madhavi	
11.	SoC Based SIFT Algorithm for Identification of the Quality Objects for Palletization Application	63
	D.Renuka, B.K.Madhavi	
12.	Comparison of WT based Speech Compression Techniques using VC++	69
	K.Arun Kumar, M.VinodKumar Reddy	
13.	User level Static and Dynamic Core assignment in Multicore System	74
	Dhruva R. Rinku, M. Asha Rani	
14.	A Survey on Computational Intelligence Applications in Software Engineering and its Data	77
	K. Narendar Reddy, Kiran Kumar Jogu	22
15.	Dynamic load balancing in cloud using extended hungarian method	83
	S. Jyothsna, Bipin Bihari Jayasingh	07
16.	Performance Analysis of load balancing queues in User Level Runtime systems for multi-core processor	8 8/
17	Vikranth B Implementation of Orthogonal Frequency Division Multiplexing for SDR using MATLAB	01
17.	R. Prameela Devi	91
18	Efficient Design Methodologies for Optimizing the Leakage Power in FPGAs	96
10.	O.VenkataKrishna, B.Janardhana Rao	90
10	Analysis of Industrial Parameters for Chemical Combustion Process in Rotary	101
17.	KILN using LabVIEW with Wireless Technology	101
	G.Venkateswarlu, K.Uday	
20	A Brief Overview on Conservation of Lakes in India	106
_0,	Rohini.A	100
	Papers accepted for next issue (Vol.12, June, 2017)	111
	Appendix: Template of CVR Journal	112
	approximation of the obstitute	112

Studies on Rheology, Strength and Cementing Efficiency of High Strength Grade Quaternary Blended Self-Compacting Concrete Incorporating High Reactivity Metakaolin

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Abstract: The present work aims at determining the most suitable mix proportion that can produce metakaolin based quaternary blended high strength SCC of desirable strength. The results of this study will lead to the reduction of the usage of cement, further sustainable development in the concrete industry by reusing industrial waste by-products (SCMs) as cement replacements and reducing harmful impact on the environment. This study systematically investigate the synergistic effect of metakaolin (MK) and microsilica (MS) on fresh and strength properties of fly ash based SCC of M80 grade. These results are compared to establish the enhanced micro-structural and engineering properties of metakaolin based quaternary blended SCC.By incorporating MK into MS+FA based ternary blended SCC mixes, the amount of fly ash used has almost doubled. From this observation, it can be concluded that MS in blended SCC mixtures imparts high strength while MK inclusion enhances the usage of high quantity of fly ash in SCC mixes for similar strengths and flow properties. The quaternary blended fly ash based M80 grade SCC mix made of MS and MK together is found to be superior to ternary blended fly ash based M80 grade SCC mix made with MS or MK due to reason that for similar strength, less cement is used and more fly ash quantity is consumed. Efficiency factor for quaternary blended SCC mix reveals that for similar strength, 50% of cement can be replaced with FA28%+MS11%+MK11% combination of mixture.

Index terms - Self-compacting concrete, metakaolin, quaternary blended, efficiency factor, rheology, Compressive Strength.

I. INTRODUCTION

Though self-compacting concrete (SCC) can be used on most construction sites, its rheological characterization must be enhanced to better control its placement. Also, the fresh SCC must be stable to safeguard the homogeneity of the mechanical strength of the structure. The stability of SCC can be improved by incorporating fine materials such as metakaolin (MK), micro silica (MS) and fly ash (FA) because an increase in cement content leads to a substantial rise in material cost and often has other negative effects on concrete properties (e.g. increased thermal stress and shrinkage, etc.) [1]. The use of such pozzolans may provide greater cohesiveness by improving the grain-size

distribution and particle packing [2]. But the use of mineral admixtures not only reduced the material cost but also improved the fresh and hardened properties of blended SCCs [3]. In recent years, there has been a growing attention in the use of metakaolin (MK) as a mineral admixture to enhance the properties of concrete [4]. In the literature, however, the use of MK in the production of selfcompacting concrete has not found adequate interest. Considered to have high reactivity other pozzolans, metakaolin is a valuable admixture for concrete/cement applications [5]. Replacing Portland cement with 8-20% (by weight), metakaolin produces a concrete mix which exhibits favorable engineering properties, including: the filler effect, the acceleration of OPC hydration, and the pozzolanic reaction [6]. The filler effect and hydration reaction is immediate, while the effect of pozzolanic reaction occurs between 3 to 14 days.

II.OBJECTIVE

This study systematically investigate the synergistic effect of metakaolin (MK) and microsilica (MS) on fresh and strength properties of fly ash based SCC of M80 grade. These results are compared to establish the enhanced micro-structural and engineering properties of metakaolin based quaternary blended SCC over ternary blended SCC. The use of appropriately proportioned metakaolin and microsilica in fly ash blended SCC reveal the benefits of their synergic effect in improving the rheological properties, strength characteristics of fly ash based M80 grade SCC. The primary objectives of this research work is to quantitatively comprehend and assess the role of metakaolin (MK) in development of early strength in fly ash based SCC of High strength grade (M80).

III. MATERIALS AND MIX PROPORTIONS

The materials used in the experimental investigation are locally available OPC cement, river sand (Zone -II), coarse aggregate (10mm), mineral and chemical admixtures such as fly ash, micro silica and metakaolin, PCE based Super Plasticizer (SP), Viscosity Modifying Agent (VMA). Based on Nan Su mix design method, material quantities such as powder content (Cement + Pozzolan), fine aggregate, coarse aggregate, water and dosages of SP and VMA required for 1 cu.m, are evaluated for high strength grade (M80) of Self Compacting Concrete (SCC). Final mix proportions and optimum proportions of FA, MS and MK combinations in binary, ternary and quaternary blended high strength SCC mix which are assumed after several trial mixes on material quantities computed using Nan Su mix design method; subjected to satisfaction of EFNARC flow properties.

IV. EXPERIMENTAL INVESTIGATIONS

The aim of the present experimental investigations are aimed to obtain specific experimental data which helps to understand the effect of synergic action of metakaolin (MK), micro silica (MS) and fly ash (FA) combinations in SCC mixes of high strength grade (M80) on rheological behavior and strength properties. Test for Compressive strengths at 3, 7, 28, 60 and 90 days were determined by conducting detailed laboratory investigations on high strength grade (M80) for optimally blended self compacting Concrete (SCC) mixes made with fly ash (FA), microsilica (MS) and metakaolin (MK). For calculating the efficiency of metakaolin, microsilica and fly ash combination in quaternary blended SCC, an equation has been proposed by author based on the principle of Bolomey's equation for predicting the strength of concrete containing mineral admixtures. The efficiency factors evaluated can be used for proportioning of high strength grade (M80) of binary, ternary and quaternary blended selfcompacting concrete (SCC) made with SCMs such as fly ash (FA), microsilica (MS) and metakaolin(MK).

V. EVALUATION OF CEMENTING EFFICIENCY FACTORS

An effort is made to quantify the cementitious efficiency of fly ash (FA), microsilica (MS) and metakaolin (MK) in binary, ternary and quaternary blended self-compacting concrete (SCC) systems of high strength grade (M80). The effect of synergic action of metakaolin (MK), microsilica (MS) and fly ash (FA) combination on the strengths of binary, ternary and quaternary blended SCC may be modelled by using a Cementing Efficiency Factor (k). The concept of efficiency can be used for comparing the relative performance of SCMs when incorporated into SCC to the performance of OPC SCC. Efficiency factors found from Bolomey's strength equation are used to describe the effect of the SCMs combination replacement in SCC in the enhancement of strength characteristics. This factor will give only an indication of the added materials' effect on concrete strength, since it does not distinguish between filler effect and chemical reactions. The well-known Bolomey's equation often used to relate strength and water/cement ratio is:S = A [(C+kP)/W) - 0.5] where S is the compressive strength in MPa, C is the cement content in kg /m³, W is the water content in kg/m³, A and B are Bolomey's coefficients /or constants, P is the amount of SCMs replaced bwc,k denotes efficiency factor of SCMs combination.By knowing the amounts of 'C', 'P', 'W' and the strength 'S' achieved for each SCMs dosage replacement, efficiency factor "k" has been computed for each of the replacement dosages. Thus, W/(C+ kP) is the water/effective powder ratio and kP is the equivalent cement content of SCMs combination. 'SCMs /OPC ratio' is an important factor for determining the efficiency of SCMs in SCC. So SCMs proportioning is arrived at based on the strength data experiments on SCMs blended SCC Mixes. Efficiency factors found from this strength equation are used to describe the effect of the SCMs replacement.

VI. TEST RESULTS AND DISCUSSIONS

A. Optimization of Mix Proportions

The initial quantities calculated using Nan Su method for high strength (M80) grade SCC mix are tabulated in Table 1. The computed amount of total powder (i.e., OPC+FA) is 658 kg. For the above quantities, even though flow properties are achieved conforming to EFNARC guidelines, the high quantity of cement computed using Nan Su method is a matter of concern. From durability perspective, the maximum cement content is limited to 450 kg per cum of concrete as per clause 8.2.4.2 of IS 456-2000. After trail mixes, revised quantities in kg per cu.m for high strength grade (M80) SCC mix are arrived by (i) limiting the Cement to maximum permissible amount, (ii) increasing quantity of pozzolan (fly ash) to maximum amount possible and adjusting the super plasticizer without compromising the EFNARC flow properties and desired strength property. The final revised quantities for high strength M80 grade SCC mix are tabulated in Table 2.

Henceforth, the total amount of powder quantity (cement + pozzolanic mixture) adopted for high strength M80 SCC is 700 kg/m3 and water/powder ratio is 0.25 for all blended high strength M80 SCC mixes. For higher grades, Nan Su mix design method computations yield very less powder content. In fact, from the observations it may be stated that Nan Su method is very difficult to apply for higher grades of concrete to arrive at appropriate quantities of materials. Depending on the above calculated base quantities for high strength grade (M80), twenty nine (29) blended SCC mixes were designed in three groups of binary, ternary and quaternary. Table 3 shows various blended high strength grade (M80) SCC mixtures with mix numbers and mix designations. In mix designation, number indicates percentage by weight of total powder content. One reference SCC mix was also prepared by only OPC (Mix C1) while in the remaining mixtures (Mix B1 to B8, Mix T1 to T8 and Mix Q1 to Q12) OPC was partially replaced with fly ash (FA), microsilica (MS), metakaolin (MK) and their combinations. Mix B1 to B8 are binary blended SCC mixtures made of either fly ash (FA) or microsilica (MS) or metakaolin (MK) while Mix T1 to T8 are ternary blended fly ash based SCC mixtures made of microsilica (MS) or metakaolin (MK) and Mix Q1 to Q12 are quaternary blended fly ash based SCC mixtures made of microsilica

(MS) and metakaolin (MK) together. In binary blended high strength grade (M80) SCC mixtures, percentage replacement of fly ash by weight of total powder content is 35% i.e. 250 kg/m3 which is based on preliminary calculation from mix design method. For binary blended SCC mixtures made with percentage replacement of MS or MK, MS and MK are limited to 5-15% and 5-20% respectively. In ternary blended MS+FA based high strength grade (M80) SCC mixtures (Mix T1 to T4) percentage replacement of MS is limited to 5 -20% by weight of total powder content. Similarly in ternary blended MK+FA based high strength grade (M80) SCC mixtures (Mix T5 to T8), percentage replacement of MK is limited to 5 -20% by weight of total powder content. In both the above ternary blended MS+FA based SCC and MK+FA based SCC mixtures (Mix T1 to T8), the cement content is kept constant (65% by weight of total powder content). In high strength grade (M80) SCC mix C1 developed with 100% OPC does not yield desired strength though required flow properties are achieved. In binary blended high strength grade (M80), FA based SCC mix (Mix B1) and MK based SCC mixes (Mix B5 to B8), although required flow properties are achieved but desired strength is not realized while in binary blended MS based SCC mixes, both required flow properties and desired strength are attained, if the MS percentage replacement is limited to 5-10% by weight of powder. The optimal mix chosen for binary blended MS based SCC mix is 5% MS replacement (Mix B2). Henceforth, for high strength grade (M80) mixes, Mix B2 is taken as reference mix. In ternary blended MK+FA based high strength grade (M80) SCC mixtures (Mix T5 to T8), however required flow properties are satisfied but desired strengths are not obtained for any of the mixes. But for MS+FA based ternary blended SCC mixes (T1 toT4), up to 15% MS by weight of powder, both required flow properties and desired strength are attained satisfactorily. So C65+FA20+MS15 (Mix T3) SCC mix is considered optimal in ternary blended high strength grade (M80) SCC mixes. In quaternary blended high strength grade (M80) SCC mixtures (Mix Q1 to Q12) made of microsilica (MS), metakaolin (MK) together, keeping cement content constant (65% by weight of total powder content), MS and MK contents are limited to 7 - 14%. For quaternary blended SCC mix (Mix Q1), initially 7% MS and 7% MK replacements are assumed, keeping cement content constant i.e. 65% by weight of total powder content and rest of powder is fly ash, required flow properties are satisfied but desired strengths are not obtained. So MS and MK are gradually increased to 14% each yet there is no substantial increase in strength though flow properties are

satisfied. Then author proposed to additionally increase fly ash content incrementally by 10% by weight of powder content (700 kg/m3), thereby incrementally increasing the powder quantity by 70 kg. The optimum combination of and pozzolanic mixture is obtained for C50+FA28+MS11+Mk11 SCC mix (Mix Q11) where final total powder content is 910 kg/m3 in which cement content is 455 kg/m3 and pozzolanic mixture is 455 kg/m3. For this optimum mix (Mix O11), MS and MK are optimally proportioned at 14% each and additional percentage of FA is 30% by weight of powder content (700kg/m3), for which required flow and strength properties are fulfilled. From table 3, three optimum SCC mixes are nominated, one each from binary, ternary and quaternary SCC blends. From the experimental investigations, the mixes B2, T3 and Q11 are chosen as optimum binary, ternary and quaternary blended high strength grade (M80) SCC mixes where both flow and desired strength properties are met along with optimal usage of pozzolanic quantities as shown in Table 4 and 5. Thus, by incorporating MK into MS+FA based ternary blended SCC mixes, the amount of fly ash has almost doubled. From this observation, it can be understood that MS in blended SCC mixtures imparts high strength while MK inclusion enhances the usage of high quantity of fly ash in SCC mixes for similar strengths and flow properties. The quaternary blended fly ash based SCC mix made of MS and MK together is found to be superior to ternary blended fly ash based SCC mix made with MS or MK due to reason that for similar strength, less cement is used and more fly ash quantity is consumed to develop blended high strength grade (M80) SCC.

Based on the compressive strength attained at specified age of curing, the efficacy of pozzolans are understood. In this study, pozzolans used for blended SCC mixes are FA, MS and MK. MK blended fresh concretes will set relatively quickly due to high reactivity of MK, which prevents bleeding and settling of aggregates.MK when compared to MS has similar particle density and surface area but different morphology and surface chemistry. MK concrete normally requires smaller SP dose than does the equivalent SF concrete. The workability of FA based SCC concrete, without super plasticizer, increases significantly with increase in FA content due to neutralization of positive charges on cement particles and their resultant dispersal. Loss of workability due to the presence of MK or MS can be compensated for by the incorporation of FA. The degree of restoration of workability, provided by FA, is influenced significantly by the cement replacement level, the MK/FA ratio and the W/P ratio.

TABLE 1 - QUANTITIES IN KG PER CU.M FOR HIGH STRENGTH (M80) GRADE SCC OBTAINED USING NAN SU METHOD OF MIX DESIGN

	Cement	Total Pozzolana (Fly ash)	Fine Aggregate	Coarse Aggregate	S.P	Water
Quantity kg/m3	644	14	810	788	11.84L	150.56 L

TABLE II- FINAL REVISED QUANTITIES FOR HIGH STRENGTH M80 GRADE SCC MIX AFTER TRIAL MIXES

	_
Water (water/powder =0.25)	167L
S.P.	12.21L
Coarse Aggregate	658
Fine Aggregate	714
Total Powder Content	700
Total Pozzolana (fly ash)	250
Cement	450
	Quantity kg/m3

TABLE III - TRAIL MIXES OF VARIOUS HIGH STRENGTH GRADE (M80) BLENDED SCC MIXES TO OPTIMIZE QUANTITIES OF POZZOLANS

Mix Designation	Replacement % (bwp)*	acemer (bwp)*	%1	Additional	O 32	Quantities kg per cu.m	ies 1.m	Total Powder		Slump flow		V-Funnel	L-Box		Achieved
OPC	FA	A MS	MK	% of FA bwp*	OPC	FA N		Content MK 'P'	Slump Diameter mm		T-50 T sec s	T-0 T-5min sec	nin Blocking c Ratio	1	(MPa)
100	1	30		Y	200	0	,	- 700	725		3.30 6.	6.66 8.52	2 0.98		72.35
65	35	'	9	5	450	250		- 700	728		3.24 6.	6.26 8.56	6 0.94	3	58.94
95		S	*	4	599	,	35	200	718		4.14 7.	7.43 8.07	0.89	_	88.56
06		01			630	,	20	- 700	700		4.29 8.	8.12 10.63	63 0.91	-	106.04
85	1	15			595		105	- 700	684		4.17 8	8.26 11.87			78.32
95	,		'n	6	999			35 700	723		3.91 7.	7.01		125	72,15
06	'	'	10	7	063	,	-	70 700	718		4.05	7.66 10.02	02 0.86		75.78
85		1	15	8	595	,	-	105 700	269		3.94 7	91.11 97.7	19 0.87		78.82
80	1	0.0	20		200	,	-	140 700	169		4.25 7.	7.76 13.62	62 0.89		69.35
65	30	0 5		7	455	210	35	200	702		3.58 6	6.64 8.08	68'0 80		81.23
9	Ci	25 10	,	a a	455	175	20	- 700	692		3.90 6.	6.98 9.49	16.0 64	-	84.20
99	60	20 15	,		455	140 1	105	- 700	687		3,61 7.	7.12 9.58	88 0.93	-	90.54
99	-	15 20	i	*	455	105 1	140	- 700	682		3.95 7.	1001 607	0.95		78.91
. 69	8	30	2		455	210	+	35 700	730		3.72 6	6.91 8.41			76.23
. 69	01	- 25	10		455	175	-	70 700	720		4.05 7.	7.26 9.87	73 0.95		77.34
65	2		15		455	140	-	105 700	714		3.75 7.	7.41 9.96			78.12
65	-		20	¥	455	105	-	140 700	709		4.10 7.	7.38 11.45	45 0.99		67.21
65	21	1 7	7		455	147	49 4	49 700	22.9	4	4.42 7.	7.68 12.67	67 0.99		74.88
65	21	1 7	7	10	455	217	49 4	49 770	899		4.76 8	8.01 14.22	22 0.99		76.34
65	21	1 7	7	20	455	287	49 4	49 840	899		4.76 8.	8.01 14.22	22 0.99		72.17
65	-	14 14	7	7	455	86	98 4	49 700	720		4.05 7.	7.26 9.87	71 0.95		80.16
65	÷	14 14	7	10	455	168	98 4	49 770	714		3.75 7.	7.41 9.96	76'0 94	_	81.23
99	-	14 14	1	20	455	238	98 4	49 840	407		4.10 7.	7.38 11.45	45 0.99	0	83.65
65	-	14 14	7	30	455	308	98 4	49 910	677	4	4.42 7.	7.68 12.67	62 0.99		71.37
99	-	14	14		455	49	6 86	98 700	899	4	4.76 8	8.01 14.22	22 0.99		80.94
65	-	14	14	10	455	119	6 86	98 770	677	4.	4.42 7.	7.68 12.67	62 0.99	Je	83.25
65		14	14	20	455	-	6 86		899	4	4.76 8	8.01 14.22			84.72
65	-	14	14	30	455	259	6 86	016 86	730	69	3.72 6	6.91 8.41		-	90.71
65		7 14	14	40	455	329	98 9	086 86	720	4	4.05 7.	7.26 9.87	77 0.95		16.67

bwp*-By weight of Total Powder content (700 kg/m3)

TABLE IV - FLOW PROPERTIES OF OPTIMIZED BLENDED SCC MIXES FOR VARIOUS GRADES

							The same of the sa					
Grade of	Miy No	Mix Designation	R	Replacement % (bwp)*	nent %		Additional 90, of EA	Slump flow		V-Funnel	nnel	L-Box
SCC Mix	OK VIII	(Values indicate percentage by weight of 'P'	OPC	FA	MS	MK	pwb*	Slump Diameter Mm	T-50 sec	T-0 min sec	T-5min sec	Blocking Ratio
	82	C95+MS5	95		S			718	4.14	7.43	8.07	68'0
M80	T3	C65+FA20+MS15	65	20	15			687	3.61	7.12	9.58	0.93
	011	C50+FA28+MS11+MK11	65	Н	14	14	30	730	3.72	16'9	8.41	0.92

TABLE V - FINAL OPTIMIZED MIX PROPORTIONS OF BLENDED SCC MIXES FOR VARIOUS GRADES

Sunday of Street Miss	VG. N.	Mix Designation	(bwp)*	(bwp)*	2	Additional					kg kg	Quantities kg per cu.m					
Diago of Sec. Mix	MILA INC	(Values indicate percentage by weight of 'P'	OPCE	AMS	MK		OPC (i)	OPC FA MS MK (i) (ii) (iii) (iv)	IS M		Total Powder Content 'P' kg (i)+(ii)+(iii)+(iv)	Fine Aggregate	Coarse Aggregate	Water S.P.	S.P.	W/P ratio	
	B2	C95+MS5	95	'n			999	.3	35		700	714	658	167	12.5		
M80	T3	C65+FA20+MS15	65 2	20 15		Г	455	455 140 105 -	. 50		700	714	658	167	12.5		
	011	C50+FA28+MS11+MK11	65 7 14 14	7	14	30	455	259 9	8	L	016	714	658	167	12.5		

bwp* - By weight of Total Powder Content; W/P ratio - Water/Powder Ratio

TABLE VI - COMPRESSIVE STRENGTHS OF VARIOUS GRADES OF OPTIMALLY BLENDED SCC MIXES

Grade of SCC Mix	Mix No B2 T3	Mix Designation (Values indicate percentage by weight of Total Powder) C95+MS5 C65+FA20+MS15	3 days 35.43 26.18	7 days 57.56 50.12	Compressi (M 14 days 78.71 65.98	(MPa)	60 days 91.22 90.54	90 days 93.19 94.51
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TABLE VII - EFFICIENCY FACTORS FOR VARIOUS GRADES OF BLENDED SCC MIXES AT DIFFERENT AGES OF CURING

		Mix Designation	8		Efficien	iency Factors		
Grade of SCC Mix	Mix No	(Values indicate percentage	33	7	14	28	09	06
		by weight of Total Powder)	days	days	days	days	days	days
	B2	C95+MS5	1.00	1.00	1.00	1.00	1,00	1.00
M80	T3	C65+FA20+MS15	0.34	89'0	0.59	0.85	86.0	1.04
(SOLETING)	011	C50+FA28+MS11+MK11	1.74	1.21	1.06	0.94	1.00	1.08

B. Compressive Strength

This investigation is carried out to study the compressive strength of binary, ternary and quaternary blended SCC mixes of high strength grade (M80) made with fly ash (FA), microsilica (MS) and metakaolin (MK) at 3,7,14,28, 60 and 90 days. Table 6 presents the compressive strength at various ages of curing for binary, ternary and quaternary blended SCC mixes of high strength grade (M80). It can be observed that there is no much variation in strength at the stipulated age of curing, in all SCC mixes as shown in Figure 1.MK based blended SCC mixes attain much higher early strength when compared to other SCC mixes while FA based SCC mixes are accomplishing strengths at later age. So MK+FA based SCC blends derive both the benefits of FA and MK in concrete by attaining early and later strengths. Use of MS in high strength grade (M80) acts as a micro-filler in making the concrete dense. Metakaolin cementing reaction rate is very rapid, significantly increasing compressive strength before first three days. Also MK being less expensive than MS when incorporated into MS+FA based ternary blended SCC mixes, the amount of fly ash used has almost doubled. From this observation, it can be understood that MS in blended SCC mixtures imparts high strength while MK inclusion enhances the usage of high quantity of fly ash in SCC mixes for similar strengths and flow properties. Addition of MK to binary or ternary blended SCC mixes will enhance early hydration because of it high reactivity.

C. Cementing Efficiency

This study understands the behavior of MK in FA+MS+MK SCC mix in order to quantify the strength efficiency of FA+MS+MK in SCC at 3,7, 14,28, 60 and 90 days. This evaluation makes it possible to design FA+MS+MK SCC for a desired strength at any given percentage of replacement. The strength efficiency factor 'k' is evaluated for three cases: (1) MS is singly blended in SCC, (2) MS is blended with FA in SCC and (3) MK is blended with MS+FA in SCC. Based on the C95+MS5 compressive strength as reference, 'A' value was calculated using Bolomey equation and then efficiency factors for FA+MS+MK and FA+MS in SCC mixes were then determined using same Bolomey's equation. From table 7, it can be observed that efficiency factors for binary (Mix B2), ternary (Mix T3) and quaternary (Mix Q11) blended high strength SCC mixes are 1.00, 1.04 and 1.08 respectively. All the three M80 grade SCC mixes give similar strength and satisfy EFNARC specifications. The efficiency factor for quaternary (C50+FA28+MS11+MK11) blended high strength SCC mixes is 1.08 which means that 1 kg of cement can be replaced with 1.08 kg of FA+MS+MK pozzolanic mixture.

VII CONCLUSIONS

Based on the test results and discussions, the following conclusions are drawn:

 For binary and ternary blended SCC mixtures made with percentage replacement of MS or MK, MS and MK are limited to 5-15% and 5-20% respectively.

- In quaternary blended high strength grade (M80) SCC mixtures made of microsilica (MS) and metakaolin (MK) together, keeping cement content constant (65% by weight of total powder content), MS and MK contents are limited to 7 – 14%.
- 3. Incorporating MK into MS+FA based ternary blended SCC mixes, the amount of fly ash has almost doubled. From this observation, it can be understood that MS in blended SCC mixtures imparts high strength while MK inclusion enhances the usage of high quantity of fly ash in SCC mixes for similar strengths and flow properties.
- 4. The quaternary blended fly ash based SCC mix made of MS and MK together is found to be superior to ternary blended fly ash based SCC mix made with MS or MK due to reason that the less cement is used and more fly ash quantity is consumed to develop blended high strength grade (M80) SCC of same strength. Also Quaternary blended fly ash based SCC mix giver better early strength than ternary blended SCC mix.
- From this observation, it can be understood that MS in blended SCC mixtures imparts high strength while MK inclusion enhances the usage of high quantity of fly ash in SCC mixes for similar strengths and flow properties.
- Efficiency factor for quaternary blended SCC mix reveals that for similar strength, 50% of cement can be replaced with FA28%+MS11%+MK11% combination of pozzolanic mixture.

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Need for Fracture Behavior based Designer Friendly Expressions for Fracture Energy and Minimum Flexural Reinforcement

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Abstract: Present National and International codes of practice lead to a size invariant expression for minimum percentage of flexural reinforcement. But the influence of member size or fracture parameters namely, fracture energy and critical crack tip opening displacement are not considered. ACI 446.1R-91 (Re-approved 1999) strongly recommends application of fracture mechanics principles to quasi-brittle material like concrete. Detailed literature study is made on the influence of fracture energy, critical crack tip opening displacement, size of the member, compressive strength of concrete and yield strength of concrete on minimum flexural reinforcement of concrete members. Several researchers have proposed expressions for minimum flexural reinforcement of concrete members, but the review of literature on fracture behavior of lightly reinforced concrete members show contradiction in conclusions. Designer friendly expressions for fracture energy and minimum flexural reinforcement are essential to the practicing engineers to evaluate fracture energy and minimum flexural reinforcement without knowing about the RILEM standards.

Index Terms--- Fracture energy, Size effect, Effective length of fracture process zone, Compressive strength and Minimum flexural reinforcement.

I. INTRODUCTION

A certain minimum amount of reinforcement is necessary in any concrete member to impart adequate ductility. In this regard, codes of practice of different Nations have provided size invariant expressions for minimum flexural reinforcement to be maintained in the concrete members. Standard codes of practice have considered the minimum flexural reinforcement as dependent on either compressive strength of concrete or yield strength of steel. A detailed review of literature on minimum flexural reinforcement of reinforced concrete members is presented.

II. LITERATURE REVIEW ON MINIMUM FLEXURAL REINFORCEMENT OF CONCRETE MEMBERS

Bosco et al [1990] reported experimental studies on 30 RC beams made of concrete of average compressive strength 91Mpa. The beams were reinforced in such a way that they fall in five different classes with respect to the brittleness number. It was found that beams of same brittleness number revealed same variation in load-same variation in load-deformation irrespective of the beam depth and the area of steel.

Bosco et al [1990] used the experimental loaddeformation variations for defining minimum flexural reinforcement in high strength concrete (HSC) beams. A transitional brittleness number was defined when a change in the behavior of beams occurred from brittle to ductile, which corresponds to ρ_{min} .

Ananthan et al [1990] developed a model to determine the influence of strain softening in concrete beams. Softening beam theory was used in the model development. The size effects were determined by using an empirical equation for the fracture process zone derived from the experimental results available in literature. A linear stress-strain relationship in the post-peak region was used.

Bosco et al [1992] conducted experiments on 46 more beams with five different strengths ranging from 16-76 Mpa to calculate the transitional brittleness number Np, which defines a change in the behavior from brittle to ductile. Reinforcement corresponding to that was defined as rho min. Based on experimental data, an expression for minimum flexural reinforcement was proposed:

$$\rho_{\min} = \frac{K_{IC} \left(0.1 + 0.0023 f_c\right)}{f_v \sqrt{D}}$$
 (1)

Baluch et al [1992] combined the concepts of fracture mechanics as well as constitutive relations and strain variations to arrive at a theoretical model for prediction of residual strength of RC beams. The crack propagation with increase in the moment was predicted using the theoretical model and validated with experiments. The model was used for a crack controlled design. The design moment and the crack depth are the design parameters. A criterion was proposed for minimum flexural reinforcement to avoid unstable crack propagation. The moment corresponding to the maximum load of reinforced concrete beam is greater than the initial cracking moment of a plain concrete beam. The expression for minimum flexural reinforcement is:

$$\rho_{\min} = \frac{1.9134 K_{IC}^{0.82}}{f_{y}^{0.9922 \left(1.7 - \frac{2.6C_{s}}{D}\right)}}$$
(2)

Gerstle et al [1992] studied the tensile cracking behavior of singly reinforced concrete beams in flexure using the fictitious crack model. An analytical model was proposed by considering the equilibrium of tensile and compressive forces and deformation of concrete. An expression for minimum reinforcement was defined but it does not contain the yield stress of reinforcement, f_y which was objected by many researchers.

$$\rho \min = \left(\frac{E_c}{E_s}\right) \left(\sqrt{0.0081 + 0.0148 \frac{f_c D}{E_c w_c}} - 0.09\right)^{\frac{1}{2}}$$
(3)

Wafa F. F. and Ashour S.A. [1993] presented experimental results of 20 high strength concrete beams tested in flexure to examine minimum flexural reinforcement requirement without fracture mechanics principles. The variables were flexural reinforcement ratio and concrete compressive strength. The flexural reinforcement ratio ranging from 0.21 to 0.88%, and the 28-day concrete compressive strength ranging from 45 to 90 MPa were considered. The test results were compared with the minimum reinforcement ratios of both the ACI: 318-89 and ACI: 318-95 Codes. Effects of specimen size and fracture parameters were not considered in this paper.

Ruiz et al [1998] performed experimental studies on lightly reinforced beams in which the importance of concrete cover and bond between steel and concrete on the behavior of RC beams was described. Beams with a large cover showed a secondary peak between concrete cover and steel yielding, which provides a hint as to the role of reinforcement cover in crack propagation.

M.Bruckner and R.Eligehausen [1998] research results suggest that minimum reinforcement ratio dependent on size of the member. The experiments on beams with depths varying from 0.125m to 0.5m and with 0.15 % of reinforcement revealed that the load-deformation curves of these beams showed a large plateau after the peak load indicating very ductile behavior. It was observed that with increase in beam size, the brittleness increased. The need for a size-dependant definition of minimum reinforcement was emphasized. The value of, pmin is obtained by solving the following condition

$$\rho_{\min} \ge \frac{M}{bd (d - 0.5\gamma x) f_{\nu}} \langle \rho_{bal}$$
 (4)

Ashour S.A. [2000] tested nine reinforced highstrength concrete beams to investigate the effect of concrete compressive strength and flexural tensile reinforcement ratio on load-deflection behavior and displacement ductility of cracked rectangular reinforced concrete beams. Concrete compressive strengths of 48, 78, and 102 MPa and tensile reinforcement ratios of 1.18, 1.77, and 2.37% were used. Displacement ductility was investigated and it was found that for a displacement ductility index of 3, the ratio ρ/ρ_b should not exceed 0.25 and 0.50 for concrete beams with concrete compressive strength of 102 and 48 MPa.

Iyengar K.T.S.R. et al [2002] used fictitious crack model to model the propagation of cohesive cracks in a beam of quasi-brittle material such as concrete. The stress-displacement relation was assumed as a generalized power law function. Expressions for moment-rotation relations were given. The analysis gives the effect of the softening exponent on the size effect and snapback behavior of beams. The effect of the elasticity co-efficient of the central elastic layer on moment-rotation relation was also determined.

Shamu et al [2004] performed fracture studies on reinforced concrete beams based on bi-linear tension softening response of concrete. The proposed model predicts the minimum reinforcement in flexure as well as the crack width in RC beams.

Raghu Prasad et al [2005] considered strain softening of concrete in tension along with fracture mechanics principles. An improved model based on fundamental equilibrium equation for progressive failure of plain concrete beam was presented and extended for lightly reinforced concrete beam.

Fantilli A.P et al [2005] experimentally investigated the transition from the un-cracked to the cracked phase in lightly reinforced concrete beams by testing five full-scale beams under three-point bending. All beams had the same dimensions and the same percentage of flexural reinforcement. But the diameters of bars and the number of bars used are varied. Test results demonstrate that during the growth of crack, the moment rotation diagrams, the tensile strains in concrete and the shape of crack profiles depend on the mechanical response of bar diameter.

Kumar S. and Barai V. S. [2008] presented finite element formulation of cohesive crack model for predicting non-linear Mode-I fracture behaviour of geometrically similar notched plain concrete beams. The effect of finite element mesh on load bearing capacity of the beam was further analyzed. It was shown that for normal size-range structures, the values of peak load determined using the concept of linear elastic fracture mechanics deviates from those obtained using cohesive crack model. Influence of some important softening functions of concrete on the global response and size-effect curve was also presented.

Carpinteri. A et al [2010] presented a new fracture mechanics based model for the analysis of reinforced concrete beams in bending describing both cracking and crushing growths taking place during the loading process by means of the concept of strain localization. The nonlinear behaviour of concrete in compression is modelled by the Overlapping Crack Model. On the basis of different nonlinear contributions due to concrete and steel, a numerical finite element algorithm is proposed. According to this approach, the flexural behaviour of reinforced concrete structural elements is analyzed by varying the main geometrical and mechanical parameters. It is concluded that the ductility is an increasing function of the compression steel percentages, the concrete compressive strength, the stirrups contents, whereas it decreases as the tensile steel percentage and/or the structural dimension increase.

III. SIGNIFICANCE OF PRESENT STUDY

In the near future, there is going to be a gradual change in the design methodology from the strength based design to fracture based design. And in this, fracture energy of concrete and minimum flexural reinforcement play a vital role. When the concrete strength increases to high strength levels, its fracture properties also change. While designing a structure using high strength concrete, the designer usually ignores the altered properties of concrete and possible changes in the overall response of the structure, because of the lack of adequate information in the present codes of practice.

In view of the safe design of structures, it is essential to develop designer friendly expressions for quantifying the fracture energy and minimum flexural reinforcement, which will be very useful to the practicing engineers. By using such formulae, laborious testing can be avoided to estimate them. If such formulae are developed, then the Practicing engineers need not know what the RILEM standards are and how to implement them in the field to evaluate the fracture energy of concrete.

IV. DISCUSSION ON LITERATURE FINDINGS

On the basis of minimum reinforcement expressions suggested by different researchers, the following conclusions are made.

 According to the minimum percent flexural reinforcement expressions given by Bosco et al, Ruiz et al and Hawkins et al, the minimum percent flexural reinforcement is found to be decreasing with the increase in size of the beam for a given compressive strength of concrete.

The minimum percent flexural reinforcement is observed as increasing with the increase in the compressive strength of concrete. As per Bosco et al, Ruiz et al and Hawkins et al, when the compressive strength of concrete is increased from 20Mpa to 30Mpa, the percent increase in minimum flexural reinforcement for 200mm depth beam is 15.77%, 27.18% and 25.49% respectively and the percent increase in minimum flexural reinforcement for 1000mm depth beam is 15.8%, 28.91% and 25.51% respectively. For a compressive strength of 20 MPa, the percent decrease in minimum flexural reinforcement when the beam depth is varied from 200mm to 1000mm is 55.29%, 21.45% and 25.19% respectively. The variation of minimum reinforcement with size of beam for different compressive strengths of concrete is presented in Fig. 1, Fig. 2 and Fig. 3 respectively.

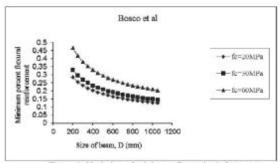


Figure 1. Variation of minimum flexural reinforcement with size of beam (Bosco et al, fy=250MPa)

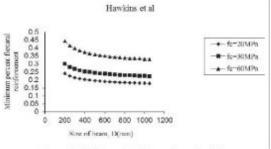


Figure 2. Variation of minimum flexural reinforcement with of beam (Hawkins et al, fy=250MPa)

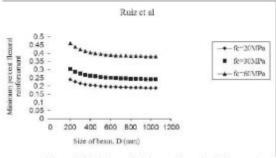


Figure 3. Variation of minimum flexural reinforcement with size of beam (Ruiz et al, fy=250MPa)

2) The findings of Bosco et al, Hawkins et al, Ruiz et al reveal that the minimum percent flexural reinforcement decreases with the increase in size of the beam for a given yield strength of steel. It is also observed that the minimum percent flexural reinforcement decreases with the increase in the yield strength of steel. For 200mm depth of beam with fy=250Mpa, the percent decrease in minimum percent flexural reinforcement between Bosco et al and Hawkins et al is 16.43% and the Bosco et al and Ruiz et al is 16.36%.

For 200mm depth of beam with f_y =415Mpa, the percent decrease in minimum percent flexural reinforcement between Bosco et al and Hawkins et al is 16.43% and the Bosco et al and Ruiz et al is 18%. For 200mm depth of beam with f_y =500Mpa, the percent decrease in minimum percent flexural reinforcement between Bosco et al and Hawkins et al is 16.44% and the Bosco et al and Ruiz et al is 18.4%. The variation of minimum reinforcement with size of beam when yield strength of steel increased is presented in the Fig. 4, Fig. 5 and Fig. 6 respectively.

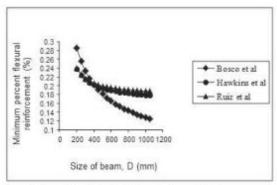


Figure 4. Variation of minimum flexural reinforcement with yield stress of steel (f,=250 MPa)

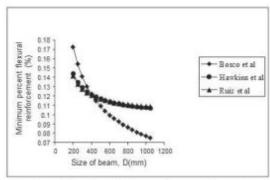


Figure 5. Variation of minimum flexural reinforcement with yield stress of steel (f,=415 MPa)

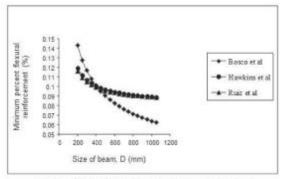


Figure 6. Variation of minimum flexural reinforcement with yield stress of steel (f_y=500 MPa)

3) According to Bosco et al, Hawkins et al, Ruiz et al, the minimum reinforcement is found to be increasing with the increase in compressive strength of concrete for a given size of beam. The percent increase in minimum flexural reinforcement for 20MPa compressive strength of concrete in Bosco et al and Hawkins et al and Bosco et al and Ruiz et al is 16.43% and 18% respectively. The percent increase in minimum flexural reinforcement when the compressive strength of concrete is varied from 20MPa to 100MPa in Bosco et al, Hawkins et al, and Ruiz et al is 55.76%, 59.4% and 61.18% respectively.

The variation of minimum reinforcement with compressive strength of concrete is presented in Fig. 7.

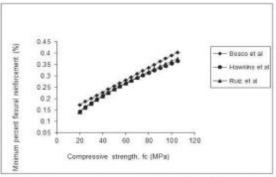


Figure 7. Variation of minimum flexural reinforcement with different compressive strengths of concrete (fy=250MPa)

4) Minimum percent flexural reinforcement predicted by Baluch et al is very high compared to the minimum reinforcement predicted by the other researchers, Bosco et al, Hawkins et al and Ruiz et al. For f_y=250MPa and f_c=20MPa, minimum reinforcement variation with increase in size of beam is presented in the Fig. 8. It is found that the minimum percent reinforcement decreases with the increase in size of the beam.

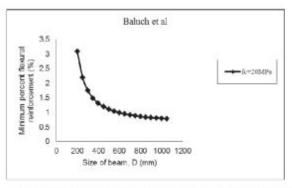


Figure 8. Variation of minimum flexural reinforcement with different compressive strengths of concrete (f_y=415MPa)

5) For a particular compressive strength of concrete, Gerstle et al prediction of minimum reinforcement variation with increase in size of beam is entirely different from the trend shown by other researchers, Bosco et al, Hawkins et al, Ruiz et al and Baluch et al. Minimum reinforcement variation with the increase in size of beam for compressive strengths of concrete, 20MPa, 30MPa and 60MPa, is presented in Fig. 9. It is found that the minimum percent flexural reinforcement increases with the increase in size of beam when compressive strength of concrete is increased. According to Gerstle et al, when the compressive strength

of concrete is increased from 20Mpa to 30Mpa, the percent increase in minimum flexural reinforcement for 200mm depth beam is 11.08% and the percent increase in minimum flexural reinforcement for 1000mm depth beam is 9.45%.

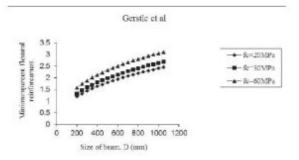


Figure 9. Variation of minimum flexural reinforcement with compressive strength of concrete (f,=250MPa)

The minimum reinforcement expressions given in the present National and International codes of practice like BIS: 456-2000, ACI: 318-2007 and BS: 8110-2003 are dependent on either yield stress or compressive strength of concrete or only the tensile strength of concrete. Hence, the codes of practice are giving a minimum reinforcement value which is invariant of size of the member, where as in case of AS: 3600-2005, the minimum reinforcement expression consists of size of the member. But no-where in code it is mentioned whether fracture mechanics size effect is considered or not. The minimum reinforcement expressions by BIS, ACI, BS and AS are given in Table 1. The minimum reinforcement as per AS: 3600-2005 is decreasing with the increase in the size of the specimen. The variation of minimum reinforcement with the size of member is presented in Fig. 10.

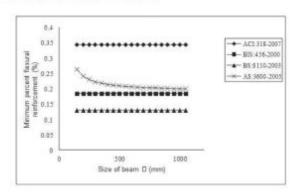


Figure 10. Variation of minimum flexural reinforcement with size of beam as per present codes of practice

Table 1. Minimum reinforcement expressions by National and International codes of Practice

Code of Practice	Expression for minimum minimum met (%) $ ho_{\min}$
845-256-2000	$\left(\frac{0.85}{f_x}\right)\!\!\times\!\!100 \qquad \text{where} f_y = \min \mathrm{Mps}$
AC:338-2007	$\frac{\sqrt{f_s}}{4f_g}{\times}100~{\rm g}~{\rm where}~f_s,f_c~{\rm are in MPs}$
65.8110-2903	$0.24 \text{ ser } f_{p} = 250 MPa$ $0.13 \text{ ser } f_{p} = 460 MPa$
AS:3503 2005	$0.22 \left(\frac{D}{d}\right)^2 \left(\frac{f_c}{f_c}\right) \approx \text{where, } f_c = 7.5 \sqrt{f_c} \left(D8I\right)$

V. CONCLUSIONS

- 1. A detailed review of literature on the behavior of lightly reinforced concrete members showed contradiction of conclusions. Bosco et al [1992] in their studies indicated a decrease in minimum steel ratio with the increase in beam height (h) in the proportion of $h^{-0.50}$. The study of Hawkins et al [1992] and Baluch et al [1992] indicated the variation of minimum reinforcement with size as $h^{-0.167}$ and $h^{-0.8511}$ respectively. Studies by Gerstle et al [1992] showed minimum reinforcement ratio variation with size as $h^{0.4083}$ whereas Ruiz et al [1996] predicted the variation of minimum steel ratio with size as $h^{-0.1382}$.
- 2. Based on literature study, it is felt that:
 - i. Can an analytical model be developed for estimating the minimum flexural strength of RC as well as high strength concrete?
 - ii If so, how to quantify the fracture energy of normal as well as high strength concrete?
- iii. Can an expression for minimum flexural reinforcement be obtained using the analytical data developed in (i) and (ii) knowing the compressive strength of concrete, yield strength of reinforcing bars and fracture energy of concrete?
- Whether the expressions developed in (iii) stands valid or not.
- 3. In near future, there is going to be a gradual change in the design methodology from strength based design to the fracture based design. And in this, fracture energy of concrete and the minimum flexural reinforcement play a vital role. In view of the above, it is necessary to develop designer friendly expressions for quantifying the fracture energy and minimum flexural reinforcement, which will be very useful to the practicing engineers.

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NOTATIONS

- D Total depth of member
- w_c Critical Crack Opening Displacement
- K_{IC} Critical Stress Intensity Factor (Fracture Toughness)
- b Width of member
- f_t Material tensile strength
- Ec Modulus of Concrete
- ρ_{min} Minimum flexural reinforcement
- f_v Yield Strength of Steel
- C_s Cover to tension steel
- Ast Area of Steel
- f_c Characteristic Compressive Strength of Concrete
- E_s Modulus of Steel
- Stress block parameter
- x Neutral axis depth
- ρ_{bol} Balanced steel ratio
- M Moment corresponding to first crack

Investigation on Effects of Nonlinear Static Procedures on the High Rise Buildings

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Abstract: The objective of the paper is to evaluate and compare the structural behavior and response demands by non linear static procedures (NSP's) such as Capacity Spectrum Method recommended in ATC40 Displacement Coefficient Method recommended in FEMA356. So, for the investigation of the two methods, two of 3-dimensional high rise RC structures with different characteristics are analyzed for investigation. To obtain nonlinear behavior of the buildings under lateral loads, the base force-roof displacement graphs such as capacity curves are determined by pushover analysis. Then four different seismic hazard levels are considered and their corresponding structural responses are determined by using the two evaluations namely CSM and DCM and results are obtained. Comparing structural response quantities (such as maximum displacements) obtained from the NSPs for considered high-rise RC buildings, effects of different evaluations such as DCM and CSM in performance evaluations of the structures are comparatively investigated.

Index Terms— Pushover Analysis, Capacity Spectrum Method, Displacement Coefficient Method.

I. INTRODUCTION

Past two decades, structural collapses and damages due to severe earthquakes have caused great loss to economy, mostly in large cities. Subsequently, it is important to discuss and examine the present country codes available and also to develop parallel methods which are more realistic in approach to the normal force based design. So for this purpose, displacement is chosen for realistic approach rather than traditional force based methods which is called performance based design (PBD) having displacements (deformations) have been started. In so many nations, like Japan and United States of America various codes are developed like {Vision 2000 (SEAOC 1995), FEMA 356 (FEMA 2000), Bluebook [Structural Engineers Association of California (SEAOC) 1999], FEMA 273 (FEMA 1997), and ATC 40 [Applied Technology Council(ATC) 1996] }. So, the term PBD(Performance Based Design) became more popular in the branch of Structural and earthquake Engineering. And mostly Structural Engineers have to take keen interest in the concepts of PBD in order to design structure resistant to Earthquake attacks. The basic concept of PBD is to perform desirable characteristics even in unfavorable and sudden loadings. And also, it is not possible to verify and check the performance of structure in different states by force based methods. So, to study about the performance of the

structure in different states PBD is the best approach. Smaller earthquake attacks have caused an abnormal inelastic behavior in buildings. After recent earthquakes, many buildings have faced to the damages which cannot be repaired or highly economical to repair.

The concepts in PBD, which have multiple stages in design, provide an improvement in the present available codes. So, to determine the response demands for earthquake assessments of structures within Performance Based Design Concept, analysis procedures like non linear static analysis procedures (NSP's) are becoming more popular in Structural Engineering due to its realistic nature. Already some Seismic Codes like Eurocode No. 8 included the non linear static procedures (NSP's) in them. Though nonlinear time history analysis is the most realistic approach in determining the seismic response demands of structures, it need larger input data like (damping ratio, sets of accelerograms etc..,) and provides results which are very difficult to interpret (such as seismic response demands with time and variation of displacement, absorbed energy, etc...). So, to overcome such difficulties, NSPs are mostly used in ordinary engineering applications to avoid large assumptions required by the designer. As a result, simplified NSPs like ATC40, FEMA356, and other became popular.

In NSP's, by pushover analysis for a specified seismic hazard level capacity curves are obtained, from which as we can determine the maximum displacement. From it, other results like plastic rotations, story drifts, displacements, etc. are extracted by using this curve. In FEMA 356 and ATC 40, Single degree of freedom (SDOF) system approach is used in determination of displacement demands in NSPs, which is called as displacement coefficient method (DCM) and capacity spectrum method (CSM), respectively.

The aim of this study is to evaluate and compare structural and nonstructural response demands obtained from CSM recommended in ATC 40 and DCM recommended in FEMA 356, which are most commonly used in practice for performance evaluation. In recent years high-rise buildings are becoming more popular and there are more chances of collapsing due to earthquakes. For these reasons, this investigation performed on the different NSPs is primarily focused on high-rise RC buildings. In this study, two of three-dimensional high-rise RC buildings, including regular and irregular configurations are studied. Then, four different seismic hazard levels such as E1, E2, E3 and E4 are determined by using CSM and DCM. In

order to determine the performance levels of the buildings, maximum plastic rotation and maximum story drift demands are found for each structure pushed until the related maximum displacement demand is achieved. In the study, maximum displacements in the four hazard levels of two different configurations such as regular and irregular are determined and compared.

A. The Pushover Analysis Method

In general, to determine the performance of the structure various lateral loads are applied on the building initially starting from zero to the required displacement level and weak points in the structure are found out. Then the performance of the building is determined by studying the status of plastic hinges formed at given target displacement or performance point related to the particular earthquake intensity level. The building is safe and efficient if the demand does not exceed capacity at all hinges. Though the loads applied, earth quake intensities and the evaluation procedures are theoretically correct with respect to the real earthquake events that are occurring; it may differ from the rigorous dynamic analysis in many ways.

B. Evaluation Procedures

Though the methods for structure evaluation are differ from one another, their basic approach are almost the same and all of them use the bilinear approximation of the pushover curve. This static procedure equates the properties of Multi degree of freedom (MDOF) structures to relevant Single degree of freedom (SDOF) equivalents, and approximates the expected maximum displacement using the Response spectrum of relevant seismic intensity. The different methods in Pushover analysis are ATC 40 (1996) Capacity Spectrum Method (CSM); FEMA 356 (2000) Displacement Coefficient Method (DCM); FEMA 440 (2005) Equivalent Linearization - Modified CSM; FEMA440 [3]- 2005- Displacement Modification-Improvement for DCM

II. DESIGN SPECIFICATIONS

For the investigation of Pushover analysis on high rise buildings, two different types of buildings have been modeled in SAP2000. First one is a regular building and the second one is an irregular building and different types of Seismic hazard levels have been considered.

A. Definitions of Seismic hazard levels

For determining structural responses of the RC buildings four different seismic hazard levels are considered investigated for two different NSPs. These seismic hazard levels are:

- 1. Low-intensity earthquake (E1);
- Moderate earthquake (E2);
- 3. Design earthquake (E3);
- 4. Maximum earthquake (E4);

As defined in ATC 40 (ATC 1996), FEMA 356 (FEMA 2000), seismic hazard levels indicates nearly the maximum

intensity of earthquake which is expected at the relevant earthquake site. In many codes (ATC 40, FEMA 356, TEC, etc.), the maximum, design, and moderate earthquake for a building with building importance factor (I) of 1, are one with a probability of 2%, 10%, and 50% of occurring within a period of 50 years, respectively. For the low-intensity earthquake, seismic hazard level classifications given in ATC 40(ATC 1996), FEMA 356 (FEMA 2000) are used. Then, the values related to the different earthquake intensity levels are taken from the design spectrum given in the TEC. And with reference to it E1 is 0.3 times E3; E2=0.5 times E3; E4=1.5 times E3.

B. Description of the Building

The test building is a Ten storey's reinforced concrete building, with each storey having a height of 4.00 m and bay sized having 8.00 m along both directions. The columns at the base are rectangular with dimensions 700x650 mm, and same dimensions continued till roof. Column longitudinal reinforcement may be taken between the range of 1.0% and 2.5%, while 8 mm diameter bars are used as transverse ties. Beams are designed to dimensions of 750x650 mm in all storeys and are lightly reinforced (nearly up to 0.4% steel ratio). The cross-sectional dimensions of columns are relatively narrow, so that the capacity of early designs to be as much as possible low cost in usage of concrete, as it will be in situ mixed and conveyed manually and placed and because of the relatively very low level of seismic action. Hence, in the test structure the columns are slender and not strong enough to carry a large amount of bending caused by lateral forces generated during an seismic attack and subsequently are highly flexible than beams. More details about formwork and reinforcement details can be found in Table. The building has been designed according to IS450:2000,that is the Indian Standard design code, following allowable design stress procedures and simplified structural analysis models. The values of dead and live loads were specified in the Indian Standard Codes, which are still in effect today. Structural elements possess no special reinforcement bars for confinement in the critical section and no capacity design provisions were used in their design. In order to resist negative moments at beams due to gravity loads Longitudinal bars in beams, are bent upwards at their end. However, high intensity earthquake vibrations can alter the moments at the ends of the beams (from sagging to hogging moment). As a result the steel in bottom section of beams at support may not be adequate for earthquake resistance. Moreover, widely spaced stirrups (300 to 400 mm) do not provide required confinement. Hence, stirrups are unable to withstand large curvature demand due to earthquake loads. For this project two models of high-rise buildings of G+10 are considered. The design specifications of two cases are shown in Table 1 and the 3D view and plan of first case and second case are shown in the Fig. 1, Fig.2, Fig.3 and Fig.4 respectively.

III. DESIGN SPECIFICATIONS OF STRUCTURES

The design specifications of the building1 and building2 are shown in table1

TABLE 1
DESIGN SPECIFICATIONS OF BUILDINGS

General Aspects	Design Variable	Selected Criteria For Building	
General configuration for	Support Configuration	Fixed	
design	Occupancy and Use	Commercial	
	Design Standard Code	IS 456:2000	
	Initial Damping	5%	
	Concrete	M30	
	Reinforcement bars	HYSD415	
Related geometric properties	Irregularities	Regular and Symmetric Building(Building1) & Irregular with L-shape and Symmetric Building(Building2)	
	Basements	Not considered	
	Number of Stories	11	
	Inter-Story Height	4m	
	Distribution of bays	Uniform	
	Typical bay length	8m in both direction	
	Beam Dimensions	750*600mm	
	Column Dimensions	700*600mm	
Load Configurations	Additional Dead Load	2KN/m	
8.50	Live Load	3KN/m	
Basic considerations for	Configuration model	3D model	
Nonlinear analysis	Seismic Hazard Levels	Low, moderate, Design and maximum	
	Plastic moment hinges consideration	Both Beams and columns	
	Plastic moment hinges location	At 5% of span length from each node	
	Software	SAP2000	

The 3D view and plan of the building case 1 and building case 2 are shown in Fig.1 and Fig.2 and Fig.3, Fig.4.

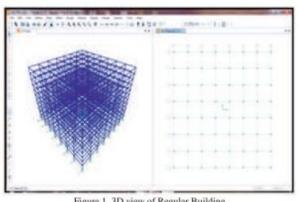


Figure 1. 3D view of Regular Building

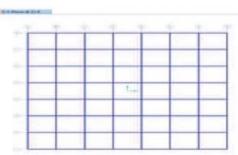


Figure.2. Plan of Regular Building

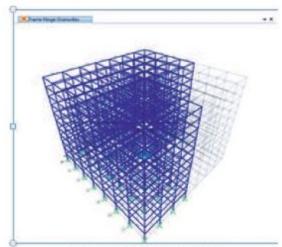


Figure.3. 3D view of Irregular Building



Figure.4. Plan of Irregular Building

IV. RESULTS

The two cases for different hazard levels are analyzed by using SAP2000. The formation of plastic hinges is shown in the Fig.5. The graph related to CSM of irregular building is shown in Fig.6 and the DCM results of irregular building are shown in Fig.7.

Table 2: Comparing the Difference in CSM and DCM for four Seismic

Buildi	Seismi	Difference	%of difference in
ng	C Hazar	between CSM&DC	Maximum
	d	M	Displacement
	Level		3353
Buildi	E1	0.030426	5.89%
ng1	E2	0.188204	36.62%
	E3	0.13827	26.90%
	E4	0.202729	39.336%
Buildi	E1	0.064137	14.4638%
ng2	E2	0.058631	14.494%
	E3	0.052299	12.22%
	E4	0.05467	14.529%

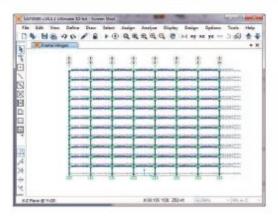


Figure 5. Formation of Plastic Hinge in YZ Direction

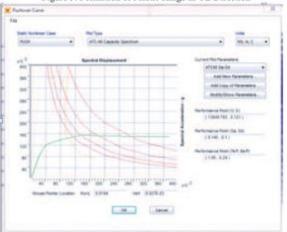


Figure 6. CSM Result of Irregular Building (E3)

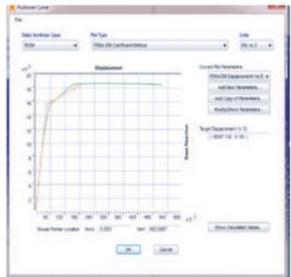


Figure 7. DCM Result of Irregular Building (E3)

V. CONCLUSIONS

This paper presented the comparison between the two methods of NSP's by using SAP2000. SAP2000 is one of the best softwares for analyzing the structures as it has a very high accuracy. It is the best tool for exploring and comparing different methods of approach in analyzing. The pushover analysis is one of the important approaches for analyzing the behavior of structure towards seismic attacks. The effect level of the earthquake hazard levels can be easily studied in the form of deformations of the structures. Non-linear pushover analysis serves the basis for determining the capacity of the RC building in terms of base shear and roof displacement when displacement based approach is adopted.

Displacement based approach tends to give realistic opinion of demand over the building as it uses roof displacement as preliminary input parameter. In future times these types of approaches become more popular as the high rise buildings are increasing more in number. Capacity curves of the structures have been plotted. The graph is linear to some extent of base shear and then it becomes constant, this is due to the formation of plastic hinges in the structure. Capacity Spectrum Method is one of the good approaches for Non linear Static Procedures as this approach gives the results about displacements, spectral acceleration (Sg) and Time Periods (T).

The Maximum Displacements for frames by Displacement Coefficient Method recommended by FEMA356 are higher than that of Capacity Spectrum Method recommended by ATC40.For Regular Building (Building Case1) the Percentage Difference in Maximum Displacement between DCM and CSM is gradually increasing from Low Hazard Level to Maximum Hazard Level (E1 to E4). So it concludes that in case of Regular buildings for low seismic hazard levels both the methods will give almost same results where as for high seismic hazard levels, the difference between two methods differ in a great manner. For irregular building (Building Case2) the Percentage Difference in the Maximum Displacement between DCM and CSM is constant for all Hazard Levels (E1 to E4). It concludes that even though the both approaches are different they arise at same results in case of Irregular Buildings.

Though the values are high for the DCM method, it is one of the good approaches for Seismic Evaluation of RC Frames

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Fracture Parameters of Plain Concrete Beams Using ANSYS

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Abstract: The present paper analyses the size dependency of the fracture energy and the fracture toughness of concrete determined as per the RILEM Work-of-fracture method (WFM). Normal and high strength concrete notched beams have been modeled using the finite element software, ANSYS 12.1 to study the variation of the fracture parameters. The fracture parameters (G_F , K_I and SIF) are determined using Work of fracture method by testing geometrically similar notched Plain normal and high strength concrete (20,30,40,50,60,70MPa) specimens of different sizes in a size ratio of 1:4 with different notch depths ($a_0/d = 0.15$, 0.30 and 0.45) under three point bending through load-deflection curves. The variation of both the fracture energy, fracture toughness and the stress intensity factor as a function of the specimen size and notch depth was determined using RILEM Work-of-fracture method. Fracture energy, fracture toughness and stress intensity factor calculated using Workof-fracture method are increasing with the increase in size of specimen and decreasing with the increasing notch depth

Index Terms—Crack length, Fracture energy, Fracture toughness, Stress Intensity factor, Brittleness, Peak load, Finite element analysis, ANSYS.

I. INTRODUCTION

Concrete, the highest consumed material in the construction field endowed with the inherent qualities of easy mouldability to the desired architectural shape and finish, high resistance to fire, easy and economically available raw ingredients with high compressive strength. Cracking in any material occurs when the principal tensile stress reaches the tensile strength of the material at that location. The study of the conditions around the crack tip is called fracture mechanics. None of the conventional strength theories like elastic or plastic theory describes how the cracks propagate in a structure. The safety and durability of concrete structures is significantly influenced by the cracking behavior of concrete. Therefore, concrete structures are mainly designed to satisfy two criteria namely, safety and serviceability. The evaluation of adequate margin of safety of concrete structures against failure is assured by the accurate prediction of ultimate load and the complete load-deformation behavior or momentcurvature response .Based on the tensile stress-deformation response, most engineering materials can be categorized into three main classes:

Brittle: stress suddenly drops to zero when a brittle material

Ductile: stress remains constant when a ductile material yields.

Quasi-brittle: It is characterized by a gradually decreasing stress after the peak stress.

A. Modes of Fracture

According to the mode of failure, fracture behaviour is classified into three categories. The three basic modes of failure are presented in Fig1.1. Mode I failure is known as the Opening mode failure. In this mode, the displacement of the crack surfaces is perpendicular to the plane of the crack. Mode II failure is known as the Sliding mode or Planar Shear mode failure. In this mode, the displacement of the crack surfaces is in the plane of the crack and perpendicular to the leading edge of the crack. The third basic mode is known as the Tearing mode or Anti-Plane Shear mode failure. In this mode, the displacement is in the plane of the crack and parallel to the leading edge of the crack. In practice, it is difficult to develop pure mode II or mode III fractures in concrete structures. Thus, besides pure mode I, mode of failure is often a combination of basic modes which is called mixed mode.

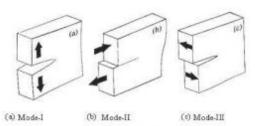


Figure 1. Modes of Fracture

B. Stress Intensity Factor Ki

The stress intensity factor is utilized as a part of fracture mechanics to predict the stress state ("stress intensity") close to the tip of a notch brought about by a remote load or residual stresses. It is a hypothetical construct normally applied to a homogeneous, linear elastic material and is helpful for giving a failure criterion for brittle materials, and is a basic technique and is a critical technique in the discipline of damage tolerance. The idea can likewise be connected to materials that display little scale yielding at a notch tip.

C. Fracture Energy G_f

The strain energy discharge rate (or essentially energy discharge rate) is the energy dispersed during fracture per unit of newly created crack surface region. The energy discharge rate failure criterion expresses that a notch will grow when the accessible energy discharge rate G is greater than or equivalent to a basic worth Gc. The amount Gc is the fracture energy.

D. Non-Linear Fracture Parameters

Fracture Energy using Work-Of-Fracture Method. Based on a measured load-deflection curve of a fracture specimen, typically a three point bend beam (including the effect of its own weight), the work of load P on the load-point displacement δ in RILEM method is calculated as $W_f = \int P d\delta$.

Figure 1.shows a typical three point bend test set up for the determination of fracture parameters using RILEM Work-of-Fracture method.

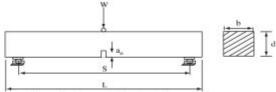


Figure 2. Three point bend test set up The fracture energy according to the RILEM3 definition, Wf

$$G_F(\alpha_0, d) = \frac{Wf}{B[(1-\alpha_0)d]}$$
 Where $\alpha_0 = \left(\frac{a_0}{d}\right)$

E. Fracture Toughness Kg

Fracture toughness is the property which portrays the capacity of the material containing a crack to resist fracture. If a material has high fracture toughness it will presumably undergo ductile fracture. For two dimensional issues (plane stress, plane strain, anti-plane shear) including crack that move in a straight path, the Mode I fracture toughness is identified with the energy release rate, Gf by

$$K_{IC} = \sqrt{GfXE}$$

II. SAMPLE LOAD CALCULATION

The most extreme load and Fracture Load are observed to appear as something else and an exceptional quality for the fracture load is obtained.

The peck load carried by M20 grade concrete having beam size of 100mm x 150mm & a/D: 0.15

BendingEquation:
$$\frac{M}{I} = \frac{\sigma cbc}{y} = \frac{E}{R}$$

$$\sigma cbc = \frac{fck}{3} \frac{20}{3} = 6.67 \text{N/mm}^2$$

For simply supported beams, the maximum bending

$$M = \frac{w\ell}{4} = \frac{wX1050}{4}$$

M = 262.5w

Where width of beam is = 100mm

Effective depth, d = 150 - 22.5 = 127.5mm

Moment of inertia

$$I = \frac{100 \, X \, (127.5)3}{12} = 17.272 \, \text{x} \, 10^{6} \text{mm}4$$

Depth of Neutral axis
$$y = \frac{127.5}{2} = 63.75 \text{mm}$$

$$\sigma cbc = \frac{M}{\ell} xy = \frac{262.5 w}{17.272 \times 10^{\circ}6} \times 63.75 = 6.67 \text{ MPa}$$

Live Load, w = 6884.28 N

Self weight of Beam:

0.1X 0.15 X 25 = 0.36kN/m = 360N/m

Dead Load w_D = 378 N

Total Load = $w + w_D = 7262.28N$

The Peak load values of various grades of concrete (M20 - M70) with different a/D ratiosand different beam sizes are calculated and tabulated in the Table I.

TABLE I. PEAK LOAD VALUES FOR BEAMS OF DIFFERENT SIZES, GRADES AND NOTCH-DEPTH RATIOS

Grade of	Size of Beam	a/D	Peak Load N
concrete	(mm x mm)	0.15	3536.643
	100 X 75	0.13	2428.88
	100 A.73	0.45	454.79
		0.15	7262.28
M20	100 X 150	0.13	5046.57
	100 X 150	0.45	3260,209
		0.15	15280.77
	100 X 300	0.3	10850.1
	100 /4 500	0.45	5764.11
		0.15	5255.13
	100 X 75	0.3	3594.327
		0.45	634.6788
9		0.15	10699.27
M30	100 X 150	0.3	7377,365
1100100	5007.55.00.5	0.45	4699,154
2		0.15	22154.84
	100 X 300	0.3	15512
	77577575	0.45	10154.77
		0.15	6975.346
	100 X 75	0.3	4760.936
	100.00.10	0.45	814.7379
1000000		0.15	14139.69
M40	100 X 150	0.3	9710.487
		0.45	6139,539
		0.15	29035.78
	100 X 300	0.3	20178.67
		0.45	13034.46
		0.15	8695.558
	100 X 75	0.3	5927.546
l.		0.45	994.79
		0.15	17580.52
M50	100 X 150	0.3	12043.61
0.000000	100000000	0.45	7579.92
-		0.15	35916.73
	100 X 300	0.3	24845.33
		0.45	15915.08
		0.15	10415.77
	100 X 75	0.3	7094.155
		0.45	1174.856
1200200		0.15	21020.54
M60	100 X 150	0.3	14376.73
		0.45	9020.309
		0.15	42797.68
	100 X 300	0.3	29512
	1.00 /4.000	0.45	1879.69
	909900000	0.15	12135.98
	100 X 75	0.3	8260.765
7		0.45	1354.916
		0.15	24460.96
M70	100 X 150	0.3	16426.35
		0.45	10460.69
		0.15	49678.62
	100 X 300	0.3	34178.67
		10'10'	27170.07

III. FINITE ELEMENT MODELLING

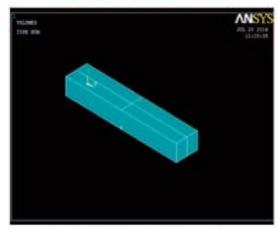


Figure 3. 3D Modeling of notched concrete beam

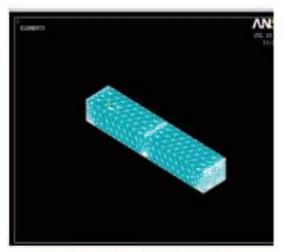


Figure 4. 3D Meshing of notched concrete beam

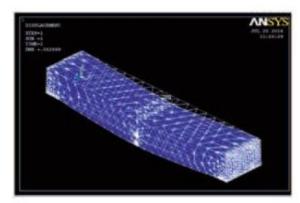


Figure 5. Deformed shape of notched concrete beam

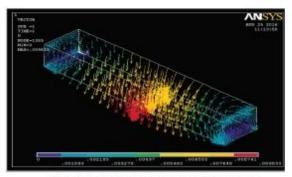


Figure .6. Vectorload Plot of notched concrete beam

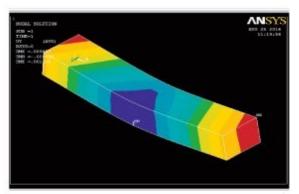


Figure 7. Stress variation over the notched concrete beam

IV. ANALYSIS OF NOTCHED CONCRETE BEAMS

The load-deflection figure shows a different deformation and behavior under the loads for beams, thus beam specimens had been made with two variables (notch depth/beam depth ratio, and Concrete grade) were tested to the ultimate load capacity so as to research deflection behavior in this study.

For particular depth, notch depth-beam depth ratio, The Stress intensity factor is observed to be increasing with the increase in the load and this stress intensity factor determined at crack tip. The following table shows the test results of the beams.

Grade of concrete	Size of Beam (mm x mm)	a/D	Deflection mm	Stress intensity factor N/mm
	(1410)0346303444	0.15	0.062869	4.77808
	100 X 75	0.3	0.047178	3.00501
		0.45	0.009912	0.581767
		0.15	0.10838	5.06743
M20	100 X 150	0.3	0.083037	3.70101
		0.45	0.083037	1.89274
	100 X 300	0.15	0.205183	6.42495
		0.3	0.160362	4.57469
		0.45	0.118737	2.22868
M30	100 X 75	0.15	0.076864	7.14012
		0.3	0.057006	4.47298
		0.45	0.011293	0.678518
	100 X 150	0.15	0.130372	6.57468
		0.3	0.099113	5.41035
		0.45	0.070993	3.05666
		0.15	0.242896	6.09492
	100 X 300	0.3	0.188195	5.328

Grade of concrete	Size of Beam (mm x mm)	a/D	Deflection mm	Stress intensity factor Number
		0.45	0.115158	3,404411
		0.15	0.088355	9.42384
	100 X 75	0.3	0.065392	5.65244
	A. T. C.	0.45	0.012554	0.871014
		0.15	0.149211	10.536
M40	100 X 150	0.3	0.11298	8.22713
	3	0.45	0.080327	3.99358
		0.15	0.275686	11.3609
	100 X 300	0.3	0.210886	8.95672
	- 5. A. S. W.	0.45	0.150406	4.36984
	7	0.15	0.096178	12.736
	100 X 75	0.3	0.072495	7.37656
		0.45	0.013675	3.1247
		0.15	0.183628	12.2141
M50	100 X 150	0.3	0.125368	7.94811
		0.45	0.087948	4.40057
	2	0.15	0.30523	13.6341
	100 X 300	0.3	0.231193	9.36027
		0.45	0.164004	5.16299
		0.15	0.1069	13.2991
	100 X 75	0.3	0.079203	8.82835
		0.45	0.014744	5.12879
	100 X 150	0.15	0.180488	12.9171
M60		0.3	0.136615	9.48784
		0.45	0.10416	5.2368
	100 X 300	0.15	0.33284	16.1583
		0.3	0.250691	11.1184
		0.45	0.177231	5.75713
	- serveronese ar	0.15	0.115315	15.4955
	100 X 75	0.3	0.092228	10.2801
	55	0.45	0.015742	4.1456
		0.15	0.194449	16.0312
M70	100 X 150	0.3	0.144513	10.8405
	0004-0009000	0.45	0.102579	6.07302
	E.	0.15	0.357694	18.7562
	100 X 300	0.3	0.288795	12.8765
		0.45	0.189231	6.63946

TABLE II

DEFLECTION, STRESS INTENSITY FACTOR FOR BEAMS OF DIFFERENT SIZES, GRADES AND NOTCH-DEPTH RATIOS

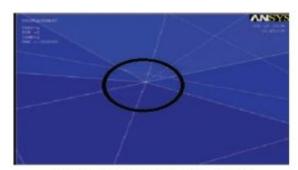


Figure 8. Deflection at point of application of load

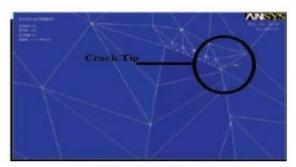


Figure 9. Stress intensity factor at crack tip

V. RESULTS ANALYSIS

A. Peak Load Vs Notch-depth Ratio

When the grade of concrete and the size of the beam is constant, then the peak load and the deflection were found to be decreasing with the increase in the notch depth ratios. This is due to the increase in the brittleness of the member, in other words, the increase in the crack length in a member makes it to behave in a brittle manner. The following graphs shows relation between peak load and notch – depth ratio.

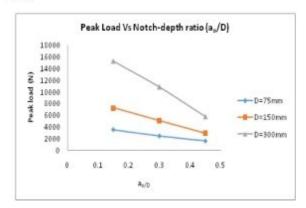


Figure 10. Peak Load vs Notch-depth ratio (M20 Concrete)

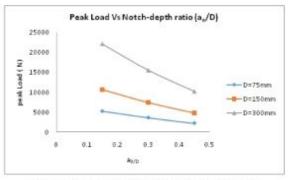


Figure 11. Peak Load v_sNotch-depth ratio (M30 Concrete)

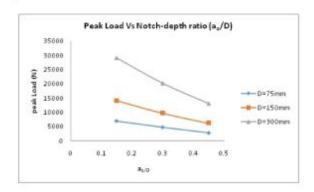


Figure 12. Peak Load v_sNotch-depth ratio (M40 Concrete)

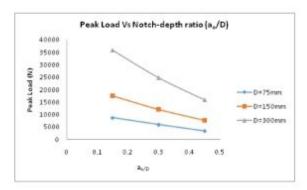


Figure 13. Peak Load v_sNotch-depth ratio (M50 Concrete)

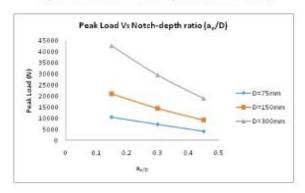


Figure 14. Peak Load vsNotch-depth ratio (M60 Concrete)

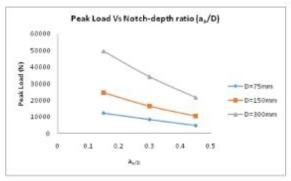


Figure 15. Peak Load v_sNotch-depth ratio (M70 Concrete)

B. Depth Vs Fracture Energy (G)

From the following graphs it is clear that in a particular notch depth-beam depth ratio, the fracture energy is observed to be increasing with the increase in the beam depth. This is due to the increase in the depth of uncracked ligament which has enhanced the load resisting capacity and hence the fracture energy of the larger depth beams. Same trend was observed with the increase in the notch depth to beam depth ratio. Similar trend was observed in all the higher grades of concrete (M30, M40, M50, M60, M70)

TABLE III
FRACTURE ENERGY FOR BEAMS OF DIFFERENT SIZES,
GRADES AND NOTCH-DEPTH RATIOS

Grade of concrete	Size of Beam (mm x mm)	a/D	Fracture Energy (G _f) N-mm
		0.15	118,9005
	100 X 75	0.3	61.4389
		0.45	2.253866
N 1		0.15	413,7122
M20	100 X 150	0.3	179.7514
		0.45	118.641
		0.15	1590.953
	100 X 300	0.3	874.1657
		0.45	378,2803
		0.15	174,8352
	100 X 75	0.3	107,4548
		0.45	3.457815
		0.15	720,9258
M30	100 X 150	0.3	382.877
0000000	000000000000000000000000000000000000000	0.45	169.2044
		0.15	2698,787
	100 X 300	0.3	1278,975
	100 74 500	0.45	599.3161
		0.15	283.4675
	100 X 75	0.13	160.6794
	100 X 15	0.45	5.153569
		0.45	1153.086
M40	100 X 150	0.13	587.6143
	100 X 150	0.45	242,7794
-		0.15	3609,718
	100 X 300	0.13	1858,153
	100 X 300	0.45	1149.008
C 1 C	C: CD		-
Grade of	Size of Beam (mm x mm)	a/D	Fracture
concrete			Energy (G _f)
			N-mm
		0.15	430.9933
	100 X 75	0.3	214.858
	3200000000	0.45	7.299549
		0.15	1712.186
M50	100 X 150	0.3	754,939
550900	50000000	0.45	333,6196
		0.15	5481.438
	100 X 300	0.3	2894.537
		0.45	1304.962
		0.15	556,7235
M60	100 X 75	0.3	280.9394
	100 2.15	0.45	8,660802
	100 X 150	0.15	1896.978
		0.13	982.0472
	100 74 150	0.45	500.306
		0.45	7122.385
	100 X 300	0.13	3699.201
		0.45	
		0.45	1665.591

	100 X 75	0.15	699.7285
		0.3	380.9375
		0.45	10.66446
M70	100 X 150	0.15	2378.209
M/U		0.3	1186.913
		0.45	536.5238
	100 X 300	0.15	8880.893
		0.3	5235.318
		0.45	2070.237

C. Fracture Energy Vs Notch Depth

Increase in the notch ratio (a/D) increases the brittleness of the member. In other words, increase in crack length in a structure pushes the structure to behave in a brittle manner. It indicates that the increase in notch depth ratio decreases the fracture energy. In other words, increase in crack length of a structure requires less fracture energy for extending the crack. A decrease in fracture energy for crack extension indicates the brittleness of the structure.

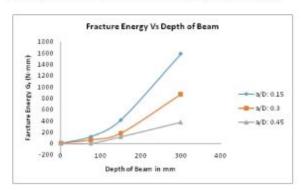


Figure 16. Fracture Energy Vs Depth of Beam (M20 concrete)

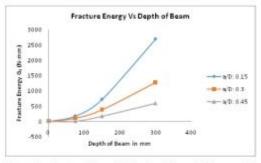


Figure 17. Fracture Energy Vs Depth of Beam (M30 concrete)

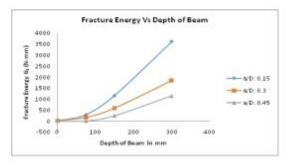


Figure 18. Fracture Energy Vs Depth of Beam (M40 concrete)

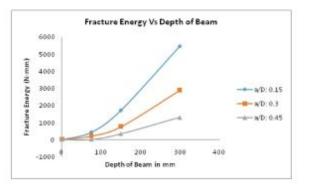


Figure 19. Fracture Energy Vs Depth of Beam (M50 concrete)

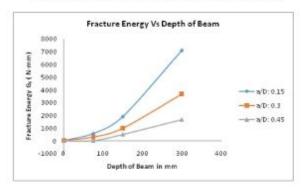


Figure 20. Fracture Energy Vs Depth of Beam (M60 concrete)

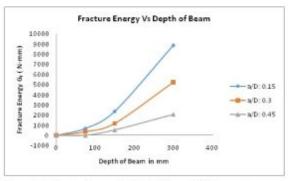


Figure 21. Fracture Energy Vs Depth of Beam (M70 concrete)

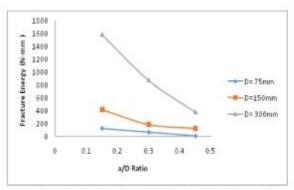


Figure 22. Fracture Energy Vs Notch depth (M20 concrete)

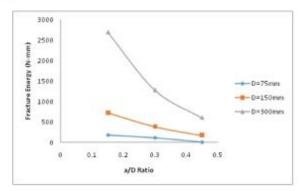


Figure 23. Fracture Energy Vs Notch depth (M30 concrete)

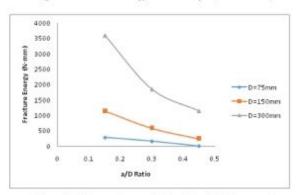


Figure 24. Fracture Energy Vs Notch depth (M40 concrete)

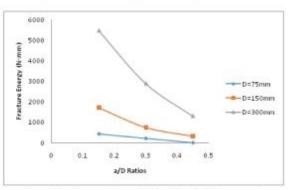


Figure 25. Fracture Energy Vs Notch depth (M50 concrete)

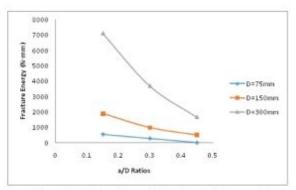


Figure 26. Fracture Energy Vs Notch depth (M60 concrete)

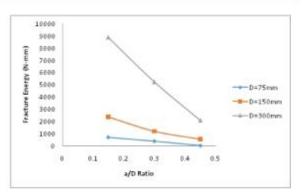


Figure 27. Fracture Energy Vs Notch depth (M70 concrete)

D. Peak Load Vs Depth of Beam

From the following graphs it is clear that in a particular notch depth to beam depth ratio, the Load carrying capacity is observed to be decreasing with the increase in the notch depth to beam depth ratio. If notch depth to beam depth increased the depth of uncracked ligament portion will be decreased so stiffness of member will be reduced. So load carrying capacity will gradually decrease. Same trend was observed with the increase in the notch depth to beam depth ratio. Similar trend was observed in all the higher grades of concrete (M30, M40, M50, M60, M70)

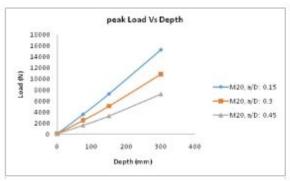


Figure 28. Peak Load Vs Depth (M20 Concrete)

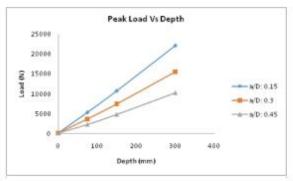


Figure 29. Peak Load Vs Depth (M30 Concrete)

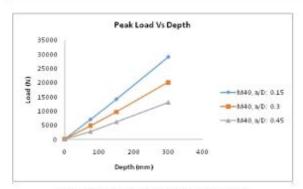


Figure 30. Peak Load Vs Depth (M40 Concrete)

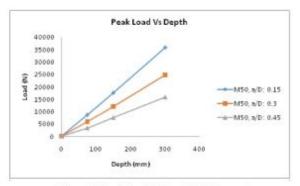


Figure 31. Peak Load Vs Depth (M50 Concrete)

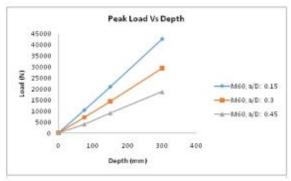


Figure 32. Peak Load Vs Depth (M60 Concrete)

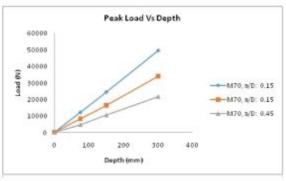


Figure 33. Peak Load Vs Depth (M70 Concrete)

E. Peak Load Vs SINT (Grade Wise)

In a particular size of the beam and for a particular notch depth ratio, the stress intensity factor is observed to be increasing with the increase in the grade of the concrete. This is due to the increased load resisting capacity of the beam with the increase in the grade of concrete.

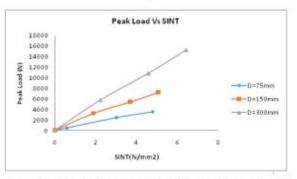


Figure 34. Peak Load vs SINT (M20 Concrete, a/D: 0.15, 0.3, and 0.45)

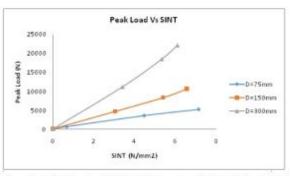


Figure 35. Peak Load vs SINT (M30 Concrete, a/D: 0.15, 0.3, and 0.45)

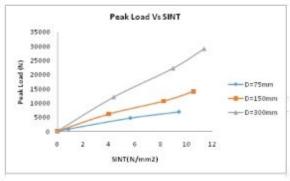


Figure 36. Peak Load vs SINT (M40 Concrete,a/D: 0.15, 0.3, and 0.45)

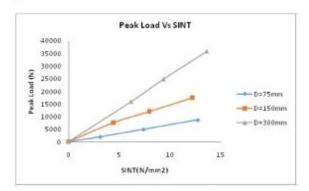


Figure 37. Peak Load vs SINT (M50 Concrete, a/D: 0.15, 0.3, and 0.45)

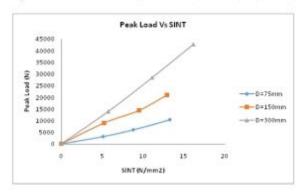


Figure 38. Peak Load vs SINT (M60 Concrete, a/D: 0.15, 0.3, and 0.45)

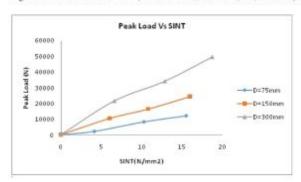


Figure 39. Peak Load vs SINT (M70 Concrete, a/D: 0.15, 0.3, and 0.45)

F. Fracture Toughness Vs a₀

Fracture Toughness is found to be decreasing with an increasing the notch depth ratio. Increase in the notch depth ratio (a/D) increases the brittleness of the member. In other words, increase crack length in a beam it behaves in a brittle manner.

TABLE IV

FRACTURE TOUGHNESS FOR BEAMS OF DIFFERENT SIZES, GRADES AND NOTCH DEPTH RATIOS

Grade of concrete	Size of Beam (mm x mm)	a/D	Fracture Toughness (K _I)
		0.15	1630.551
	100 X 75	0.3	1172.099
		0.45	224.4949
		0.15	3041.527
M20	100 X 150	0.3	2004.835
	390.11.5580.3659.347	0.45	1628.77
	Miscopologia	0.15	5964.461
	100 X 300	0.3	4421.192
		0.45	2908.368
	100 X 75	0.15	2188.163
		0.3	1715.451
		0.45	307.7274
	100 X 150	0.15	4443.351
M30		0.3	3238.135
		0.45	2152.639
	100 X 300	0.15	8597.053
		0.3	5918.291
		0.45	4051.29
	10040800409995	0.15	2993.999
	100 X 75	0.3	2254.136
M40		0.45	403.6956
		0.15	6038.525
	100 X 150	0.3	4310.684
		0.45	2770.805
	100 X 300	0.15	10684.07
		0.3	7665.504
		0.45	6027.837

Grade of concrete	Size of Beam (mm x mm)	a/D	Fracture Energy (G _f) N-mm
-		0.15	3903.577
	100 X 75	0.3	2756.153
- 1		0.45	508.0138
		0.15	7780.419
M50	100 X 150	0.3	5166.345
(65)4315		0.45	3434.419
	P40000000	0.15	13921.14
	100 X 300	0.3	10116.19
		0.45	6792.45
	100 X 75	0.15	4643.469
		0.3	3298.596
		0.45	579.1644
W2222	615940843888	0.15	8571,443
M60	100 X 150	0.3	6167,214
		0.45	4401.905
	100 X 300	0.15	16608.7
		0.3	11969.52
		0.45	8031.691
	WOODS NAME OF	0.15	5410.337
	100 X 75	0.3	3991.962
- 4		0.45	667.9269
		0.15	9974.348
M70	100 X 150	0.3	7046.427
		0.45	4737.552
	100 X 300	0.15	19274.71
		0.3	14798.95
		0.45	9306.139

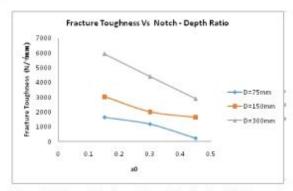


Figure 40. Fracture Toughness Vs notch-depth ratio (M20 Concrete)

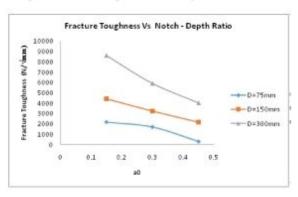


Figure 41. Fracture Toughness Vs notch-depth ratio (M30 Concrete)

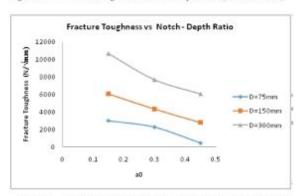


Figure 42. Fracture Toughness Vs notch-depth ratio (M40 Concrete)

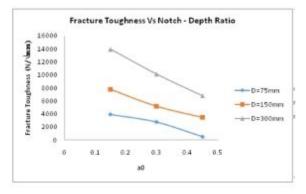


Figure 43. Fracture Toughness Vs notch-depth ratio (M50 Concrete)

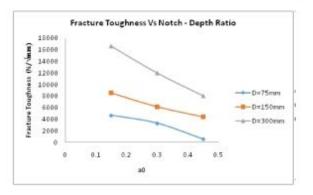


Figure 44. Fracture Toughness Vs notch-depth ratio (M60 Concrete)

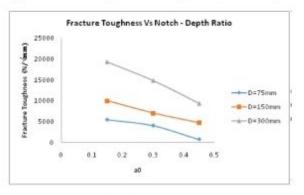


Figure 45. Fracture Toughness Vs notch-depth ratio (M70 Concrete)

VI. CONCLUSIONS

The fracture behavior of the notched plain concrete beams of different sizes and notch depth ratios for different grades of concrete has been analyzed based on the modelling of beams in ANSYS. The variation of fracture parameters has been studied and presented below.

- 1. In a particular size of the beam and for a particular notch depth ratio, the fracture energy and fracture toughness are observed to be increasing with the increase in the grade of the concrete. This is due to the increase in the depth of uncracked ligament which has enhanced the load resisting capacity. Hence, the fracture energy of the larger depth beams. Same trend was observed with the increase in the notch depth ratios.
- 2. In a particular grade of concrete and for a particular size of the beam, the fracture energy and fracture toughness are observed to be decreasing with increase in the notch depth ratios. This is due to the decrease in the depth of uncracked ligament. Same trend was observed with the increase in the size of the beams.
- 3. When the grade of concrete and the size of the beam is constant, then the peak load and the deflection were found to be decreasing with the increase in the notch depth ratios. This is due to the increase in the brittleness of the member. In other words, the increase in the crack length in a member makes it to behave in a brittle manner.
- 4. In a particular size of the beam and for a particular notch depth ratio, the stress intensity factor is observed to be increasing with the increase in the grade of the concrete.

This is due to the increased load resisting capacity of the beam with the increase in the grade of concrete.

- 5. In a particular size of the beam and for a particular notch depth ratio, the peak deflection value is observed to be increasing with the increase in the grade of the concrete. This is due to the increased load resisting capacity of the beam with the increase in the grade of concrete.
- Increase in the notch ratio (a/D) increases the brittleness of the member. In other words, increase in crack length in a structure pushes the structure to behave in a brittle manner.
- 7. It indicates that the increase in notch depth ratio decreases the fracture energy. In other words, increase in crack length of a structure requires less fracture energy for extending the crack. A decrease in fracture energy for crack extension indicates the brittleness of the structure.

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Transformerless Photo Voltaic Inverter Topologies for Low Power Domestic Applications

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Abstract: In the last two decades there is significant growth in solar power due to the developments in photovoltaic (PV) and power semi conductor technologies. Traditionally a photovoltaic system consists of either a line frequency transformer on ac side or a high frequency transformer on dc side to provide galvanic isolation between PV panels and grid. By removing transformer from PV system, the size of the system can be reduced significantly and efficiency can be improved. However, with the presence of parasitic capacitance between PV and ground, a variable common mode voltage appears in the system. This results in increase of leakage current and distortion in grid current. This paper presents a study on various inverter topologies that are used in harvesting the solar power. Further, a simulation study is carried out on a single phase H4 topology to assess the performance using bipolar and unipolar pulse width modulation (PWM) techniques. The simulation study is carried out in MATLAB SIMULINK and results are

Key words: Transformerless Inverter, parasitic capacitance, Variable common mode voltage, leakage current, Bipolar PWM and Unipolar PWM.

I. INTRODUCTION

Renewable energy, especially solar energy became popular in the last two decades due to shortage of fossil fuels and environmental concerns. On the other hand, it is also due to significant advances in photo voltaic conversion technology and reduction in cost-per-watt on a large scale production. Solar power has grown consistently by 20 to 25% per annum over the last two decades. Various types of power electronic topologies are developed in literature to pump solar power into the grid [2].

Grid connected PV inverters are mainly classified into four types: (i) Central Inverter (ii) String Inverter (iii) Module integrated Inverter or Micro Inverter (iv) Multi String Inerter [2].

Central Inverter: Central inverter is used for large power plants [3]. PV modules are arranged in parallel stings and connected to a central inverter shown in Fig.1. Initially, line commutated thyristor based inverters were used in the topology. However, IGBT devices replaced thyristors gradually due to high efficiency and low cost [5]. This topology has following dis advantages:

- High voltage DC cables are needed between PV panels and inverter
- · Power loss increases due to common MPPT
- · Power loss due to module mismatch
- · Losses in string diodes
- · Less reliability due to single inverter

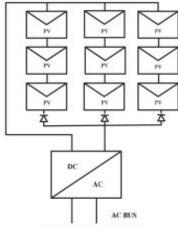


Figure 1. Central Inverter

String Inverter: String inverters are developed in 1995. The PV panels are connected in series to form arrays. Each array is connected to a separate inverter as shown in Fig. 2. If the string voltage is sufficiently high, there is no necessity to boost the voltage. Otherwise, a DC-DC converter or a line frequency transformer is required to boost the output voltage. This additional component decreases the efficiency.

Module Integrated Inverter: In this topology, each PVmodule connected to a separate inverter which is connected to the grid as shown in Fig.3 [2]. This kind of connectionensures maximum power from PV modules due to individual Maximum Power Point Tracking.

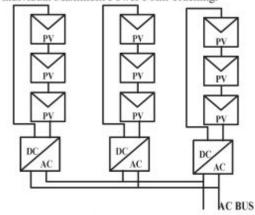


Figure 2. String Inverter

Due to its modular structure further expansion of the plant is easier [2]. The topology has drawbacks (i) Reduction in overall efficiency due to higher voltage amplification (ii) Higher capital cost.

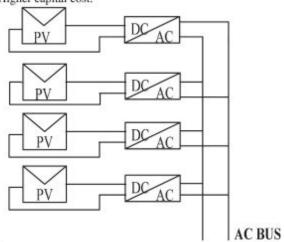


Figure 3. Module integrated inverter

Multi String Inverter: This inverter is developed in 2005. It combines the advantages of string inverters and module inverters. Each String is made of several solar panels is coupled to its own DC-DC converter with individual MPPT and feed energy to common dc to ac inverter shown in Fig. 4 [2]. The advantages of the topology are low cost, flexibility and high energy [14].

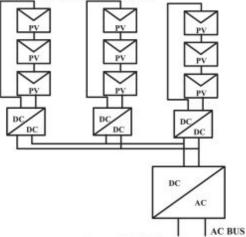


Figure 4. Multi String Inverter

II. GRID CONNECTED INVERTERS

The DC voltage generated from PV panels has to be converted into AC voltage of required magnitude and frequency. A typical PV system consists of PV panels, DC-DC converter, DC-AC converter and a line frequency transformer on AC side or high frequency transformer on DC side. A PV topology using transformer on DC side is shown in Fig. 5 and PV topology using a transformer on ac side is shown in Fig. 6.

In high power applications, the PV systems are including a transformer to provide galvanic isolation between PV panels and the grid. This helps in reducing the common mode leakage currents and also provides safety [14].

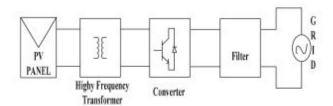


Figure 5. PV inverter topology using high frequency transformer on dc side of the converter.

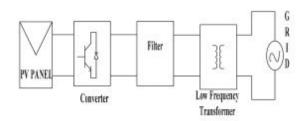


Figure 6. PV inverter topology using low frequency transformer on ac output side of the inverter

In low power domestic applications, transformer occupies large space and also reduces the efficiency of the PV system. By removing the transformer, the size of the PV system can be reduced and the efficiency can be improved. A PV transformerless topology is shown in Fig. 7.

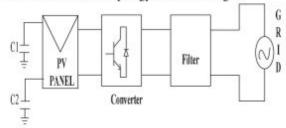


Figure 7. PV inverter topology without using Transformer

Since there is no transformer, the issues like galvanic isolation and variable common mode voltage are arisen. A variable common mode voltage results in leakage current that flows through parasitic capacitances from PV panels to the ground. This results in the increase of system losses, reduction in quality of the grid current [2].

III LOW POWER GRID CONNECTED INVERTER TOPOLOGIES

In low power applications, the PV system consists of PV panels, DC-DC converter and DC-AC inverter. In single phase applications, a full bridge inverter (H4 topology) shown in Fig. 8. can be used. The power semi conductor devices, IGBTs (Insulated Gate Bipolar Transistor) can be controlled using following two modulation techniques: (i) Bipolar PWM (ii) Unipolar PWM.

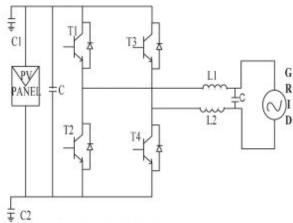
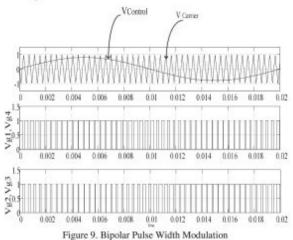


Figure 8. Full Bridge H4 Inverter Topology

A) Bipolar PWM Technique

In this technique, gate signals are generated by comparing a reference sinusoidal signal $V_{control}$, with a high frequency triangular waveform, $V_{carrier}$ as shown in Fig. 9. When $V_{control} > V_{carrier}$, the switches T1 and T4 are on and T2, T3 are off. When $V_{control} < V_{carrier}$ T2, T3 are on and T1, T4 are off. When T1, T4 are on the output voltage, $v_o = +V_{dc}$. When T2, T3 are on the output voltage, $v_o = +V_{dc}$. The output voltage oscillates between $+V_{dc}$ and $-V_{dc}$. This results in more ripple in the output current which leads to more power loss.



A) Unipolar PWM Technique

In this technique, the two legs of the inverter are controlled separately by using two reference sinusoidal signals, $V_{control1}$, $V_{control2}$ which are in phase opposition as shown in Fig. 10. When $V_{control1} > V_{carrier}$ T1 is on and T2 is off. When $V_{control2} < V_{carrier}$ T1 is off and T2 is on. When $V_{control2} > V_{carrier}$ T3 is on and T4 is off. When

 $V_{control2} < V_{carrier}$ T3 off and T4 on. When T1,T4 are on $v_o = +V_{dc}$, when T2, T3 are on $v_o = -V_{dc}$. When T1, T3/T2,T4 are on $v_o = 0$. The output voltage oscillates between $+V_{dc}$, 0 and $-V_{dc}$. As there are three levels in the output voltage, the ripple in the load current is less and efficiency is more compared to bipolar PWM technique. However, this results in variable common mode voltage. To overcome this various topologies are presented in literature.

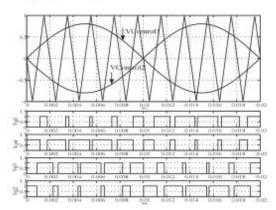


Figure 10. Unipolar Pulse Width modulation

C) H5 Topology

This topology is obtained by adding an extra switch T5 to the H4 topology. H5 inverter topology is modified form of H4 full bridge inverter by adding an extra switch T5 as shown in Fig.11. [9]. Switches T1, T3 are operated at grid frequency and switches T2, T4 are operated at switching frequency [10].

During positive half cycle T5, T4 are switched simultaneously at high frequency and T4 continuously is on. During freewheeling period T5 is off and the Current flows through T1 and anti parallel diode off.

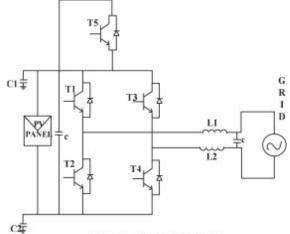


Figure 11. H5 Inverter Topology

On the other hand, during, during negative half cycle T2, T5 are triggered at high frequency simultaneously where as T3 triggered continuously. Current flows through T5, T3 and T2. During negative zero voltage vector T5 is turned off and current freewheels through T3 and antiparallel diode of T1 [7].

This topology has following disadvantages: (i) High conduction losses, as three switches are on simultaneously. (ii) Reactive power control is not possible using H5 topology.

D) H6 Topology

This topology is obtained by adding two additional switches T5, T6 and diodes D5, D6 as shown in Fig.12. During positive half cycle, T1, T4 are on continuously, T5, T6 commutated simultaneously at high frequency where as T2, T3 commutate together in complement to T5 T6 pair. Hence current flows through T5, T1, T4 and T6, during positive zero voltage vectors. H6 inverter topology provides a three leveled output [7]. H6 topology provides constant common mode voltage thus generates very small leakage current. Hence high efficiency can be obtained.

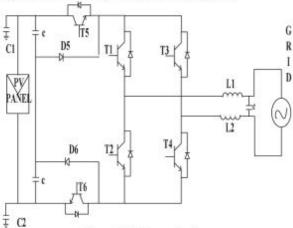


Figure 12. H6 Inverter Topology

E) Heric Topology

Highly Efficient Reliable Inverter (HERIC) is obtained from H4 topology by adding additional switches as shown in Fig. 13. This one of the most popular transformerless inverter topology [6]. When upper switch T1 or T3 is on, voltage output will be $+V_{dc}$, when T2 or T4 is on results an output of zero. During positive half wave, T6 is turned on and is used in freewheeling period of T1,T4. During zero voltage vector, T1, T4 or T2, T3 are in off state. PV is disconnected from grid by short circuiting the ac side of the inverter so that this topology is predominantly ac decoupling topology [13].

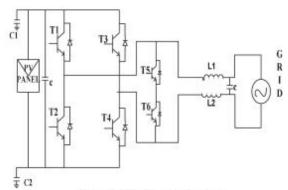


Figure 13. HERIC Inverter Topology

IV. SIMULATION RESULTS

The H4 topology shown in Fig.5 is simulated with bipolar and Unipolar PWM techniques in MATLAB SIMULINK. The simulation parameters are given in Table

Table I: Simulation Parameters

500V	
0.8	
50Hz	
2.4kHz	1
10 Ω	
10 mH	
	0.8 50Hz 2.4kHz 10 Ω

The simulation results using bipolar PWM techniques are shown in Figs. 14-16.

Fig.14. shows output voltage. From the figure, it can be seen that the output voltage oscillates between +500V and -500Vas discussed section III. The FFT of output voltage is shown in Fig.15. From the figure , it can be seen that the output voltage has a fundamental component of $401V\ (V_{dc}\times modulation\ index)$. Moreover, it can be seen that the harmonics appear around multiples of switching frequency, 2.4 kHz. The output current is shown in Fig.16. From the current waveform it can be seen that there is significant ripple in the load current,

The simulation results using Unipolar PWM are shown in Figs. 17-19. The output voltage has three voltage levels, +500, 0 and -500V as shown in Fig.17. From the FFT result, Fig. it can be seen that the output voltage has a fundamental component of 400.5V. Further it can be seen that the harmonics appear at double the switching frequency in Fig.18. From the current waveform shown in Fig.19. , it can be observed that the ripple is very less compared to that of bipolar PWM. On the other hand, during negative half cycle T2, T5 are triggered at high frequency simultaneously where as T3 triggered continuously.

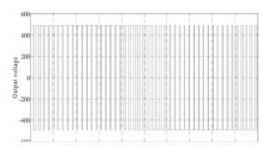


Figure 14: Output Voltage of H4 Full Bridge using Bipolar PWM of inverter topology.

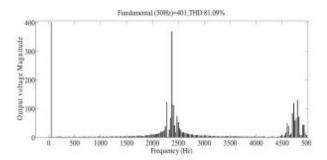


Figure 15. FFT analysis of Output voltage using bipolar PWM

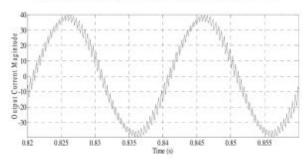


Fig.16. Output current of H4 bridge using bipolar PWM

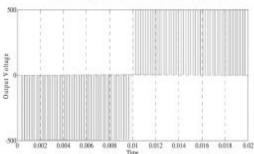


Figure 17: Output Voltage of H4 Full Bridge using unipolar PWM of inverter topology.

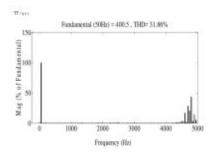


Figure 18. FFT analysis of Output voltage using unipolar PWM

It is evident that, from the Fig.16 and Fig.17, the ripple using bipolar PWM is more when compared to the ripple using unipolar PWM. Thus Unipolar PWM considered as efficient in terms of ripple component and efficiency.

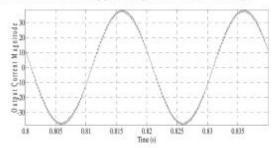


Figure 19. Output Current of H4 bridge inverter using Unipolar PWM

V. CONCLUSIONS

The solar power gained significant momentum in the last two decades due to advances in PV panel and power semi conductor technologies. This paper studies various topologies used in photovoltaic systems. The work aims at transformerless topologies for low power domestic applications. Various popular topologies are discussed in detail. The H4 topology is simulated using bipolar and Unipolar PWM techniques. From the simulation results it is concluded that Unipolar PWM technique results in (i) Less ripple in the load current. (ii) Better Total harmonic distortion compared to bipolar PWM technique.

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A Distributed Generation System with Micro Grid for Effective Energy Management

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Abstract: A Distributed generation (DG) system with Micro grid(MG) powered by the renewable energy sources like solar, wind and fuel cells along with the battery is under study. The profile of the power consumed from the grid and the power delivered back to the grid is found. The load forecasting data is considered by the Microgrid system simulation with industry and domestic loads and it is observed that the load demand is met efficiently with the available energy resources and some part of the energy is fed back to the grid as well. Also, the voltage at the PCC is observed with different loads such as domestic loads and industry loads.

Index Terms—Distributed Generation, Microgrid, Fuel Cell, Wind Energy, Solar Energy, load forecasting

I. INTRODUCTION

Today, the local energy generation is very prominent for the sustainability of energy for future. Distributed generation system refers to the energy generated at the consumer point. A microgrid along with the distributed generation system can be used as a backup for the grid in case of emergencies like grid outages. A microgrid system gives scope for greener energies and also has advantages of providing flexible electricity. Therefore, with the microgrid systems, the consumers become more energy independent and environment-friendly.



Figure 1. Schematic of a Microgrid with utility Interconnection

A microgrid is powered by renewable resources like wind energy, solar energy, fuel cell and the backup diesel generators, batteries. [1] The microgrid infrastructure provides the platform for efficiency improvement and enhanced energy consumption within a small area. Power generation happening at the load end reduces the transmission losses. Also, the distribution system is comparatively less complex in construction. The load is considered uncontrolled in most of the situations, and hence the required amount of power must be generated dynamically. With the conventional power plants, there are primary and secondary load control mechanisms. However, the scenario is different here and unconventional control of the source must be considered. The sources considered here are Solar Photovoltaic, Fuel-cell, and power from wind energy. Out of these, the solar and wind power generated is purely dependent on the solar insolation levels, and wind power output depends on the wind speed available. Fuel cell power output is controllable as the hydrogen and oxygen inputs are controlled at the inlet value. Normally combined heat and power is considered as a source but for Indian conditions, heat is not available naturally in a large scale. So it is not considered in the simulation. It is observed that efficiently managing the resources could save the operating cost of the system and hence more profits can be obtained. The coordination of the supply from different sources increases the overall efficiency of the system. It is a recommended practice to also have the power supply connection from the grid. This helps in meeting the load demand with the generation possible at the load end with the renewable energy sources and the balance load demand is met by the grid. Whenever the load is completely met by the generation from these renewable energy sources and there is excess power available, it is required to feed the excess power back to the grid. The power exchange can be measured to observe whether the power is taken from the grid or the power is fed back to the grid. This is called Net-Metering. [2]

Considering the operation of the microgrid, traditionally there are two modes. Mode 1: The Microgrid is connected to the main grid so that the power can be either consumed or delivered back to the grid. (Grid Connected Mode (GCM)) [3]. Mode 2: The Micro grid is disconnected with the grid during the emergencies and has the capability to run the local loads. (Islanded Mode) [4]. A typical Microgrid System with utility connection is shown in figure

It is also required to control the microgrid in the islanded and grid-connected modes [4], [5]. A study is done on the energy management in the microgrid, in grid-connected mode and its effectiveness is discussed.

The contents of the paper are as follows. The first section gives the introduction to the problem addressed. The objectives are discussed in the second section. The methodology used for the analysis is explained in the third section. The results and discussions are in the fourth section followed by conclusions.

II. OBJECTIVES

This study is meant to understand the power exchange at the point of common coupling and role of net-metering when different types of loads are connected to the system. A Microgrid is the next generation system architecture. So, the loads and sources are modeled and connected to the system to form a microgrid. As the loads are consuming power, if there is not enough power generation available, the voltage at the point-of-common-coupling would drop. Load shedding may be considered as an option, but the reliability indices will go down and this is not accepted by the consumer as promised power quality has to be supplied. There may also be a penalty for power-not-supplied. Hence power has to be supplied from some source to assist the internal power generation. For this purpose, power is bought from the grid. The grid also welcomes power to be supplied to it when the voltage and frequency requirements according to the IEEE standards are met.

Another objective is to study how the single phase loads connected to the three phase supplies are effecting the voltage profile at the bus. This is considered important as uneven voltages in the three phase at the point-of-commoncoupling will result in the flow of neutral-currents for which the system is not designed for. Here, household load is assumed to be connected to Phase-a, the small-scale industrial load is connected to Phase-b and a three-phase heavy industrial load is connected to all the phases so that the power drawn from phase-a is comparatively less than that of Phase-b while Phase-c supplying the least. The scenario would be different when power is fed back to the grid from the loads and is to be analyzed.

III, METHODOLOGY

The Microgrid system at the distribution side is taken into consideration. It is powered up by solar, wind, fuel cell and UPS. The micro grid system is connected to different types of loads like domestic load, industry load (connected to single phase) and Heavy Industry load (connected to three phase). This type of system is taken into consideration. Distributed generation system refers to the energy generated at the consumer point. At every point based on the load forecasting the generation- demand balance is met from the local generation and the grid.

At each load end, there are different types of power generators installed and connected to the load. Solar, fuel cell and wind powers along with a battery are considered to be generating power all day. Whenever there is enough power generation, there is no power drawn from the grid. If excessive power generation is available, power is supplied to the grid.

The data is taken from a .dat format file which is given in the Appendix and respective column data is extracted. This is now analyzed and computed for the grid power consumed and the grid power supplied. This is traditionally called day-ahead power exchange prediction based on the forecasted load and generation availability. Energy management can also be implemented at this stage for optimized profitability but is considered to be beyond the

scope of the paper. The methodology used is shown in figure 2.

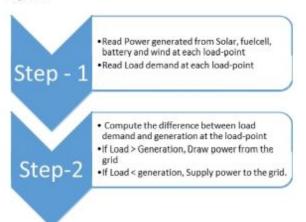


Figure 2. Methodology used to compute grid power exchange

At each load point, the power drawn from the grid is assumed to be supplying the excessive load and hence the current and voltage associated with that load is observed. This power drawn is estimated by distributing the power among the split-phase load as S1 and S2 (virtual, represented as a current source connected in anti-parallel. The total power is randomly distributed. The relation between powers in the split phases is shown as:

$$S_1=S*random [0 1]$$
 (1)

The current in each phase is computed as follows. The relation between power assuming the reactive power (Q=0). Therefore, the apparent power is given by

$$S = \frac{1}{\sqrt{2}}V_{rms}\frac{1}{\sqrt{2}}I_{rms}$$
 if if $V_{rms} > 0$ (3)
 $S = 0$ otherwise

Where V_{rms} and I_{rms} are the RMS voltage and current at the

So, from equation 3, the current expression can be derived

$$I_{rms} = \frac{2S}{v}$$
 (4)

 $I_{rmp} = \frac{2S}{V_{rmp}}$ (4) The power that is drawn or supplied to the grid are to be managed in a way not to affect the voltage profile at the bus. The other things considered during the simulation are a) Meet the load demand by maintaining voltage and frequency within the limits.

- b) Understand the benefits of adding a surplus power generation.
- c) Analyze the power market situations, provide custom components to control the load to be operated during maximum internal power generation at the load center.
- d) Setting up communication interfaces between load and control center.
- e) Study of the effect of addition of load on the system on a phase.

The load data and the data of generation available at the load end is assumed to be known by forecasting techniques. The power that has to be exchanged from the grid is precalculated so that the benefits can be analyzed. The streetlighting and other auxiliary loads are assumed to be constant and are included as a RL model. There is no reserve considered in this model and can be the future enhancement of the paper.

IV. SIMULATION, RESULTS AND DISCUSSION

A. MATLAB based simulation

A Distributed generation system with solar, wind fuel cell and the batteries[1] connected to a microgrid is simulated in the MATLAB-Simulink environment.

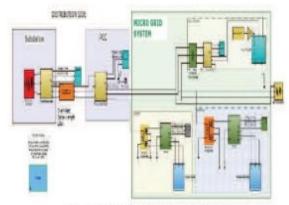


Figure 3. MATLAB-SIMULINK Model

The developed micro grid system can be simulated for the required time, i.e. the load forecasting can be done for 6,12,18,24 hrs. as per requirement to understand the voltage fluctuations and power exchange between the utility grid and microgrid.

The MATLAB-Simulink model is as shown in the figure 3. This system includes a three phase grid supply, a small transmission line and loads connected at PCC. The micro grid system is modeled with different types of load like domestic load, small scale industry loads and heavy industry load, modelled as a current source, connected in anti-parallel, as if drawing the amount of load current from the grid.

Further industry and house are modeled as shown in the figure 4. Each house load or industry load is further divided number of loads. A sample Industry load is shown in the figure 4.

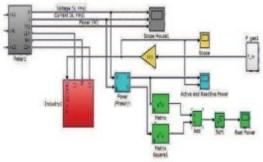


Figure 4, Small Scale Industry/House Model
A domestic load is modeled with 5 different house loads.
A small-scale industry is modeled with five different

industries. Both the above loads are simulated as a singlephase loading. A heavy industry load is modeled which is a 3-Ph load. Analysis on the model is done for three different cases.

Case A: All the connected loads in the MG system are assumed to be domestic loads. In that case, the voltage fluctuations and power exchange at the PCC are as shown in the figure 5 & 6 respectively.

Case B: In this case, along with the domestic loads, smallscale industry load is added. In that case, the voltage fluctuations and power exchange at the PCC are as shown in figure 7 & 8 respectively.

Case C: In this case, along with the domestic load, smallscale industry load, heavy industry load is also added. In that case, the voltage fluctuations and power exchange at the PCC are as shown in figure 9 & 10 respectively.

B. Results

The results for the three different cases simulated are shown in the following figures. It is to be noted that all the figure's x-axis corresponds to a 24hr horizon, sampled at each minute.

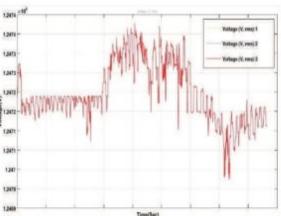
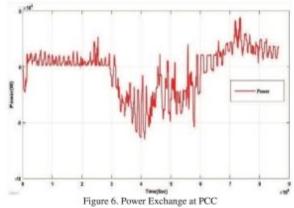


Figure 5. Voltage Profile at PCC



1860

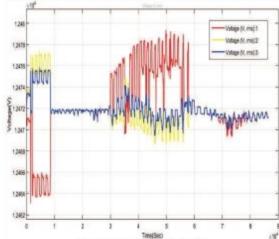


Figure 7. Voltage Profile at PCC

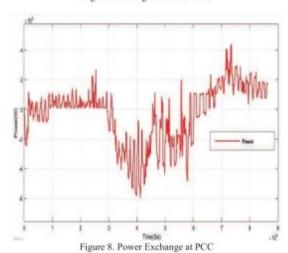


Figure 9. Voltage Profile at PCC

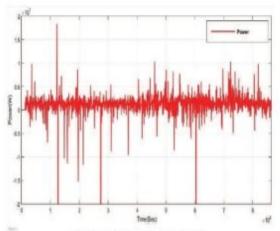


Figure 10. Power Exchange at PCC

The domestic load is further considered as five independent house loads and the power met by the load is shown in Fig 11. The domestic load for a sample load is shown as a solid line. The solar power generated during the day time is shown as a dotted line.

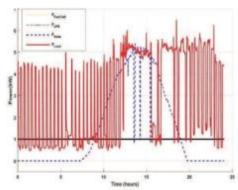


Figure 11. Power met by domestic load

The small-scale industry load is also considered as five industries and power met by the load is shown in Fig 12. The industry load for a sample load is shown as a solid line. The solar power generated during the day time is shown as a dotted line. Whenever the power generated exceeds the demand the power is fed back to the grid as shown in the negative region.

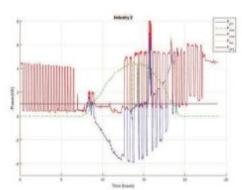


Figure 12. Power met by small-scale industry load

The power met by the heavy industry load is shown in Fig 13. This is also similar to the industry load discussed above.

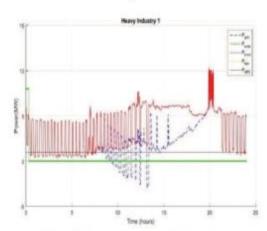


Figure 13. Power met by Heavy industry load

C. Discussion

It can be observed that always there is a power exchange between the utility grid and micro-grid. Whenever the load demand is not met by the local generation, the utility supplies the required power. Whenever there is an excess power in the micro grid it is sent back to the utility grid.

The rated voltage at the PCC is 12.47 kV. Whenever there is a power exchange happening from the grid, the voltage tends to change. In figure 4, the voltage variation can be observed to be deviating from 99.98% to 100.03% of the rated value. This is well between the allowable deviation of ± 10%. It can also be observed that the voltage is not different in different phases. The power exchange at the PCC can be analyzed from figure 5. It is obvious from the graph that most of the time, the icrogrid is producing power not only enough for the local loads, there is a surplus of power available. So, the measured power shows negative values, indicating the flow from microgrid to the grid. There is a maximum feeding to the grid during noon time, due to the maximum power generation from Solar Photovoltaics.

The second case considered is the influence of the presence of a small-scale industrial load in the system, at a phase. Now this should cause unbalance in the system voltage, as different loads are connected on different phases. This can be observed in figure 6. Two household loads connected to two phases have similar voltage profile, while the third phase has a voltage which is fluctuating because of the quantity of load. It is again observed that the deviation is between 99.98% to 100.08%, which is much less than the allowable ± 10%.

The second observation is that the voltage fluctuations at the PCC are different in three cases. It can be observed that when the industry load is introduced along with domestic load at phase c, the fluctuations are more in that phase. When the heavy industry load is introduced, all the phases are disturbed showing high voltage and current fluctuations. The power exchange is again predominantly happening from the microgrid to the grid. Two conclusions can be made from figure 7. Firstly, there is always a scope for adding additional load in the microgrid area and see that the power exchange is close to zero but in the negative region. Secondly, load can be scheduled to be connected to the microgrid during noon time. This can reduce the peak value in the graph to look flat, so that the power quality at the PCC is improved.

As mentioned in case 3, figure 8 shows the voltage fluctuation, where the voltage deviation is found to be predominant in all the three phases. The deviation is happening between 91.42 to 104.25% of the rated. This is again within the standards. The voltage profile seems to now shift from the negative to the positive region, i.e., power is now drawn from the grid predominantly. During night time, there is much fluctuation in the power flow.

All the load demands are met by the energy sources available at the microgrid as well as the utility grid in all the three cases. The individual load profile shown in figure 10 and figure 11 shows that whatever is the load demand, that power is supplied after considering the available sources of fuel cell, solar, wind and battery power. The loads at household and industry are chosen in a way to see that there is always a load present and distributed among the 24hr horizon. The power coming from solar can be precisely found here. These are assumed to be rooftop solar photovoltaics installed. The fluctuation in the load is considered to check the stability of the system under such conditions and it is found that the sum of generation plus the grid power exchange is capable of supplying uninterrupted power to the load. This is desirable so as to maintain power quality at the load end.

V. CONCLUSIONS

In the paper, the Micro-grid system that connects the household loads and various industry loads is studied. The total load demand is met from the energy generated from renewable energy sources like solar, wind and fuel cells, the UPS system and the grid. The power consumed and the power fed back to the grid in a day is analyzed and found to be well within the standards. It is seen that the energy is fed back to the grid whenever the generated energy at the load side exceeds the demand. Also, the voltage fluctuations at PCC are observed for various load conditions.

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APPENDIX

Time (hrs.)	Use (kW)	Gen [kW]	Grid (kW)	Solar [kW]	Fuel Cell[KW]	UPS
0.00	6.46	0.00	4.46	0.00	1.00	1.00
1.00	6.39	0.00	4.39	0.00	1.00	1.00
2.00	4.56	0.00	2.56	0.00	1.00	1.00
3.00	2.41	0.00	0.41	0.00	1.00	1.00
4.00	2.44	0.00	0.44	0.00	1.00	1.00
5.00	2.41	0.00	0.41	0.00	1.00	1.00
6.00	2.42	0.00	0.42	0.00	1.00	1.00
7.00	2.52	0.00	0.52	0.00	1.00	1.00
8.00	2.42	0.20	0.23	0.20	1.00	1.00
9.00	3.06	1.23	-0.16	1.23	1.00	1.00
10.00	2.80	2.20	-1.40	2.20	1.00	1.00
11.00	2.65	3.17	-2.52	3.17	1.00	1.00
12.00	2.30	3.80	-3.51	3.80	1.00	1.00
13.00	6.91	4.20	0.70	4.20	1.00	1.00
14.00	7.31	4.38	0.94	4.38	1.00	1.00
15.00	3.42	4.22	-2.80	4.22	1.00	1.00
16.00	2.91	3.68	-2.77	3.68	1.00	1.00
17.00	2.77	2.85	-2.08	2.85	1.00	1.00
18.00	7.27	1.57	3.70	1.57	1.00	1.00
19.00	2.82	0.49	0.33	0.49	1.00	1.00
20.00	6.59	-0.08	4.66	0.08	1.00	1.00
21.00	7.99	0.00	5.99	0.00	1.00	1.00
22.00	7.86	0.00	5.86	0.00	1.00	1.00
23.00	6,62	0.00	4.63	0.00	1.00	1.00
24.00	6.51	0.00	4.51	0.00	1.00	1.00

Performance Analysis of Rooftop Solar Plants in CVR College of Engineering: A Case Study

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Abstract: The growing electrical energy demand in developing countries like India has triggered the scientists and engineers to think of new and innovative methods in the field of renewable energy sources especially solar energy. Grid connected PV systems have become the best alternative to bulk electrical power consumers like industries and other institutions. In this paper 280kWp Photovoltaic Grid Connected Power Plant commissioned at CVR College of Engineering is taken for research study. This Plant uses three different mechanisms to trap the Solar energy from the Sun, namely Seasonal tilting, Single axis tracking and Single axis Polar tracking. The twelve months of a year is segmented into two time frames viz. from September to March and other from April to August. In one time frame Single Axis Polar Tracking Power Plant is giving better performance whereas in other time frame Single axis tracking Power Plant is giving better output. Further research and investigation has to be done on these results to predict the performance of the plants in these two time frames and exact reasons for these outputs.

Index Terms— Grid Connected Solar Power Plant, Polar Tracking, Single Axis Tracking, Solar Radiation, Seasonal Tile

I. INTRODUCTION

Increasing electrical energy demand and high cost fossil fuels, global warming and environmental issues increase the importance of the use of clean and renewable energy sources. There are many types of naturally available sources of energy which can be replenished over a period of time. Solar energy, wind energy and biomass energy are few to mention as examples. All these renewable sources of energy have the capability of converting the naturally available sources of energy into electrical Energy [1].

Today's daily Electrical energy needs, cost of fossil fuels and effect of greenhouse gases on environment forces the industrial and other institutions to seek for new ways to generate their own electrical demand using renewable energy.

India has an abundance of solar radiation, with the peninsula receiving more than 300 sunny days as an average in a year. Due to its proximity to the equator, India receives abundant sunlight throughout the year [2]. For countries like India, Solar energy became the best alternative and viable renewable energy to fulfill the electrical energy requirements of majority of the people living in both urban and rural areas for variety of applications.

The most familiar way to generate electricity from solar energy is to use photovoltaic cells, which are made up of silicon that converts the solar energy falling on them directly into electrical energy. This is a direct energy conversion which involves photo-electric effect. Large scale applications of photovoltaic for power generation, either on the rooftops of houses or in large fields connected to provide clean, safe and strategically sound alternatives for production of electrical power generation [3].

Solar PV solution has the potential to transform the lives of many people, who rely on highly subsidized kerosene oil and other fossil fuels, primarily to light up their homes. Renewable energy source is a practical solution to address the persistent demand supply gap in the power industry.

II. TYPES OF PHOTO VOLTAIC SYSTEM

On the basis of working operation, PV systems can operate in four basic forms [4].

A. Grid Connected PV Systems

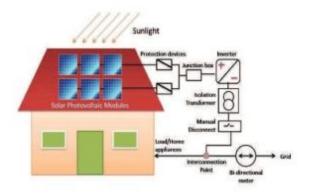


Figure 1. Block diagram of Grid connected PV Plant with net metering

The "Fig. 1," shows the block diagram of Grid connected PV plant with net metering. These systems are connected to a broader electrical network called Grid. The PV System is connected to the utility grid using a high quality sine wave inverters, which converts DC power generated from the solar array into AC power. During the day, the solar electricity generated by the system is either used immediately for local loads or export to electricity supply companies. In the evening, when the PV System is unable to

generate electrical power, electricity can be imported from the grid [5].

B. Standalone Systems

The "Fig. 2," shows the block diagram of standalone PV system. PV systems not connected to the electric utility grid are known as Off Grid PV Systems and also called standalone systems. Direct systems use the PV power immediately as it is produced, while battery storage systems can store energy to be used at a later time, either at night or during cloudy weather. These systems are used in isolation of electrical grid, and maybe used to power local loads.



Figure 2. Block diagram of standalone PV system

C. Hybrid System

The "Fig. 3," shows the block diagram of Hybrid PV system. A hybrid system combines PV with other forms of power generation, usually a diesel generator. Bio gas is also used. The other form of power generation is usually a type which is able to modulate power output as a function of demand. However, more than one form of renewable energy may be used e.g. Wind and Solar. The Photo Voltaic Power generation serves to reduce the consumption of fossil fuel.

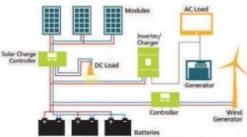


Figure 3. Block diagram of Hybrid PV System

D. Grid Tied with Battery Backup PV system

The "Fig. 4," shows the block diagram of Grid tied with Battery Backup PV system. Solar energy stored in batteries can be used at night time. Using net metering, un used solar power can be sold back to the grid. With this system consumer will have power even if grid fails [6].

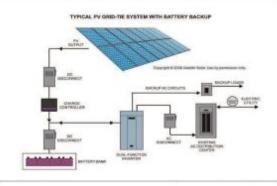


Figure 4. Block diagram of Grid tied with Battery Backup PV System

III. SITE DETAILS

The grid connected solar power plant under this research study is located on roof top of CVR College of Engineering. This college is located in vastunagar, Mangalpalli village, which comes under Ibrahimpatnam district located in Telangana state in India.

Project location	Climate data location
Location: Hyderabad	Location: Hyderabad
Latitude: 17.20 °N	Latitude: 17.45 °N
Longitude: 78.60 °E	Longitude: 78.47 °E
Elevation: 545.00 m	Elevation: 545.00 m

The solar radiation data of project location is not available at exact project location. So the solar radiation data and other climate conditions at project location are assumed to be the same that is available at the nearest climate data location given by NASA [7]. Climate data of the location as per information provided by NASA are tabulated in Table I below.

TABLE I.

MONTH WISE AVERAGE GLOBAL HORIZONTAL RADIATION, AMBIENT TEMPERATURE, GLOBAL INCIDENT IN COLL.PLANE AND EFFECTIVE GLOBAL RADIATION

Month	GlobHor kWh/m ²	T Amb	Globalne kWh/m ²	GlobEff kWh/m ²
January	158.4	23.00	199.1	194.3
February	164.6	25.70	193.5	188.7
March	203.9	29.10	218.4	212.6
April	202.3	31.40	196.8	190.5
May	206.1	32.60	187.7	180.9
June	161.2	29.20	143.9	138.3
July	13.0	26.80	126.0	121.2
August	146.4	25.70	138.6	133.6
September	162.6	26.10	167.1	161.8
October	166.6	25.50	186.1	181.0
November	152.6	24.00	187.5	182.8
December	154.0	22.10	198.8	194.1
Year	2017.8	26.77	2143.3	2079.6

IV. PLANT DESCRIPTION

The Grid connected solar power plant located on Roof top of CVR College of engineering has total installed capacity of 280kW_p. This 280kWp capacity solar power plant is further decentralized into 5 sub plants for proper operational and maintenance.

The Electrical Energy output of the Solar Power Plant is directly proportional to amount of Solar radiation that solar Array will receive at any point of time. More the amount of solar energy received by the solar array, more the electrical energy output. vice-versa.

So the new classification of Solar power plants based on the way how the solar array receives the solar energy from the sun can be categorized into three types

- (A) Seasonal Tilt/Manual tilte
- (B) Single- Axis Tracking
- (C) Single- Axis Polar Tracking

The complete capacity of solar plant on each block of CVR College of Engineering is tabulated in Table II including the dates on which each plant operation started to their full capacity.

Out of 280kWp of installed capacity 120kWp on rooftop of EEE Block and 20kWp on rooftop of Library block makes use of Seasonal tilt mechanism.80 kWp on Main block and 60kWp on CSE block uses tracking mechanism to extract the Solar energy from the sun. Overall, 140 kWp solar plant uses seasonal tilt mechanism and remaining 140 kWp solar plant uses tracking mechanism for electrical power generation [8].

DETAILS OF NAME OF SUB PLANTS, THEIR CAPACITIES AND DATE OF COMMENCEMENT OF PLANT

TABLE II.

Name of the Sub Plant	Installed Power	Date of Commencement of Plant
CVR EEE Block	120.00 kWp	03-03-2014
Single Axis Tracking-MB	40.00 kWp	18-01-2015
Library	20.00 kWp	23-02-2015
Polar Tracking -MB	40.00 kWp	11-03-2015
CVR CS Block	60.00 kWp	22-10-2015
Overall Plant Capacity	280.00kWp	

A. Seasonal Tilt/Manual tilt

Placing the modules facing the south with some tilt with respect to horizontal roof, on which panels are mounted. In this method for every month we need to adjust the tilt of solar modules. This is called seasonal tilting but changing the position of solar panels every month is quite difficult, we try to restrict the change the tilt of modules for every season.

B. Single- Axis Tracking

In single axis trackers, a long horizontal tube is supported on bearings mounted upon pylons or frames. The axis of the tube is on a north-south line. Panels are mounted upon the tube, and the tube will rotate on its axis to track the apparent motion of the sun through the day. In these methods panels are oriented in East-West direction. The moment sun rises in the East solar panels automatically face east direction It will be horizontal when LST is 12:00 noon and will face the West in the evening. This method of tracking the sun is called Single-Axis tracking

C. Single- Axis Polar Tracking

In Single-Axis tracking, the modules are mounted flat at 0 degrees with respect to horizontal. While in Single Axis Polar Tracking the modules are installed at a certain tilt (10 degrees) with respect to horizontal axis. It works on same principle as Single-Axis Tracking, keeping the axis of tube horizontal in north-south line and rotates the solar modules from the east to the west throughout the day. This method of tracking is named as Single axis Polar tracking. These trackers are usually suitable in high latitude locations

Main components of Grid connected PV Plant are [9]

- 1. Solar Panels/ Solar Modules/ Solar Array
- 2. String inverter
- 3. DC Cables
- 4. AC Cables
- 5. Junction Boxes
- 6. Net meter (bi-directional Meter)

Solar panels/ Modules/Array will collect the energy from the sun in the form of solar radiation, this solar radiation is converted into DC electrical energy by solar Array. This DC Electrical energy is given as input to grid interactive String inverters with the help of DC Cables. These string inverters convert DC electrical Energy into AC electrical energy. The output AC electrical energy of inverter will be sent to local junction box with the help of AC Cables. From the junction box depending upon local load requirement the AC power will be either pumped to electrical grid or utilized for local energy requirements. There will be a bi- directional energy meter is installed at incoming transformer from the external grid [10]. Generated Solar Electric Power is synchronized at 11kV bus. This Net meter increment the energy units when ever local load requirement is more than AC electrical energy output of Solar Plant and vice-versa.

The below "Fig. 5," shows the exact on site photograph of 40-kWp Single axis tracking power plant commissioned on Main block of CVR College of Engineering. It is evident from photograph that Solar array at 9:30 A.M. facing towards the east.



Figure 5. Single axis Tracking-Position of panels at 9:30 A.M

Similarly, "Fig. 6 and 7," shows the position of solar panels at 3:00 P.M and 12:30 P.M respectively. As mentioned earlier Single axis tracking plant always follows the position of the sun in the sky throughout the day to collect the maximum energy from the sun.



Figure 6. Single axis Tracking-Position of panels at 3:00 P.M



Figure 7. Single axis Tracking-Position of panels at 12:30 P.M

The "Fig.8," shows the 3-D view of Single axis Polar tracking power plant.

Solar Panels and string inverters are the heart of grid connected solar power plant. Multi crystalline Solar panels are used in the solar array. Each Solar panel has maximum electrical output power of 250 Watt at 1000 W/Sq.m Solar radiation. Panels are manufactured by Kohima Energy Private Limited. Model Number of Solar panel is KE-60-M250. These Solar panels have 25 years' manufacturer guarantee.



Figure 8. 3-D view of Single axis polar tracking plant

The inverters used in this power plant are 20-kW Refusol grid interactive string inverter. Model number is REFUsol 008K-020K. This is a three phase sine wave inverter as per IP 65 standards with 98.2% maximum efficiency.

V. RESULTS AND DISCUSSIONS

The details of energy output of each and every string inverter and sub plant can be monitored online by web interface AE Sitelink [11]. Total energy outputs of Single axis tracking power plant are compared with Polar tracking power plant from April'15 to October'16.

The energy outputs of these two Power plants are monitored in the above mentioned specified period and are tabulated in Table III. The "Fig. 9," shows the graphical representation of energy outputs of single axis tracking power plant with single axis Polar Tracking Power plant over a monitored period April'15 to October'16. After observing the data, we can divide the time frame taken into two slots. One is from April to September and another one is from October to March

From the "Fig 9," and data from Table III, we can conclude that during the period from April to August the energy generated by Single axis tracking power plant is more than Single axis polar plant. Whereas from September to March it is evident that output of Single Axis Polar tracking power plant is more than Single axis tracking plant.

As performance of both plants is varying between these two time frames , one random date is chosen from each time frame. May 22nd 2016 is selected for first time frame and October 14th 2016 is chosen for other time frame.

The "Fig. 10, 11 and 12," show the energy outputs of each 20kW String Inverter which are connected to Single axis Polar Plant, Single axis tracking Plant and Seasonal tilt Power Plants respectively. From figures one can conclude that on 14th October 2016 the performance of Single axis Polar Plant is best among three types of Solar PV Power Plants [12].

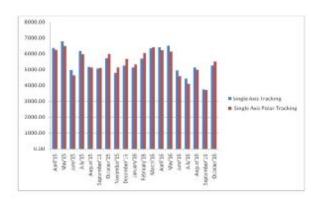


Figure 9. Energy outputs of single axis tracking power plant with single axis Polar Tracking Power plant over a monitored period

MONTH WISE ELECTRICAL ENERGY OUTPUTS OF TRACKING AND POLAR TRACKING POWER PLANTS AND THEIR PERCENTAGE VARIATION

TABLE III.

Month- year	Single Axis Trackin g	Single Axis Polar Tracking	Net Differe nce	% Percentage Variation
April'15	6362.30	6251.90	110.40	1.74
May'15	6782.40	6486.50	295.90	4.36
June'15	4960.30	4640.60	319.70	6.45
July'15	6188.20	5964.70	223.50	3.61
August'15	5174.10	5149.20	24.90	0.48
September 15	5061.90	5101.40	-39.50	-0.78
October'15	5726.20	6005.50	-279.30	-4.88
November'15	4785.20	5139.90	-354.70	-7.41
December'15	5248.00	5677.50	-429.50	-8.18
January 16	5148.60	5335.00	-186.40	-3,62
February'16	5681.80	6045.40	-363.60	-6.40
March'16	6341.00	6425.10	-84.10	-1.33
April'16	6403.60	6222.50	181.10	2.83
May'16	6515.00	6137.80	377.20	5.79
June'16	4956.20	4585.70	370.50	7.48
July'16	4435.30	4106.00	329.30	7.42
August'16	5148.60	5003.00	145.60	2.83
September'16	3757.20	3724.50	32.70	0.87
October'16	5278.40	5505.90	-227.50	-4.31

Similarly, the "Fig. 13,14 and 15," show the energy outputs of each 20kW String Inverter which are connected to Single axis tracking plant, Single axis Polar Plant and Seasonal tilt Power Plants respectively. It is evident from charts that on 22nd May 2016, performance of Single axis tracking plant is best among three types of Solar PV Power Plants [12].

After comparing the outputs of Single axis tracking Power Plant and Single axis Polar Plant, we can conclude that from September to March Polar tracking Power Plant is giving more output. Whereas from April to August Single Axis tracking is giving more output [12].



Figure 10. Energy generated by Single Axis Polar tracking-20kW String Inverter output on 14th October '16



Figure 11. Energy generated by Single Axis Tracking-20kW String Inverter output on 14th October 16

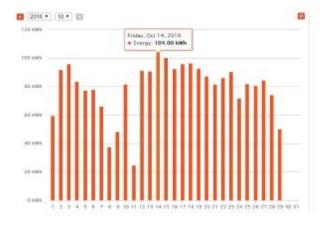


Figure 12. Energy generated by Seasonal tilt -20kW String Inverter output on 14th October '16

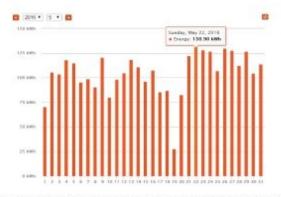


Figure 13. Energy generated by Single axis tracking-20kW String Inverter output on 22rd May '16

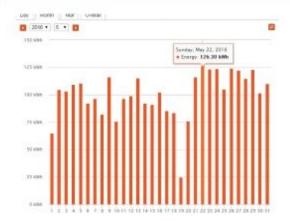


Figure 14. Energy generated by Single Axis Polar tracking-20kW String Inverter output on 22nd May '16

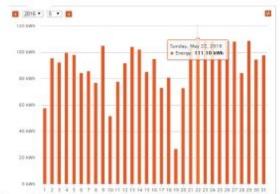


Figure 15. Energy generated by Seasonal tilt -20kW String Inverter output on 22rd May '16

VI. CONCLUSIONS

In this paper, a 280kWp Grid Connected Photo Voltaic Power Plant commissioned at CVR College of Engineering is taken for research study. The electrical energy outputs of different Solar PV Power Plants are studied and analyzed.

The twelve months' time in an year is divided into two time frames viz. From September to March and other from April to August. A random date of 14th October 2016 is chosen in first time slot. On this day Single Axis polar tracking gives better performance among the three. A random date of 22nd May 2016 is taken in second time

frame. On this date Single Axis tracking gives better performance among the three.

Further research has to be done on these results for better analysis and exact reasons to investigate performance of the plant in these two different time frames. Since these results obtained are only for 19 Months, at least two complete cycles will give us better idea because weather and climate conditions may not be the same every year in the monitored time frame.

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Investigation of wear characteristics of Fe-Cr-C hardfacing alloy on AISI-304 steel

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Abstract-Wear plays a pre-dominant role in effecting tribological properties and service life factor of machinery components and tools. Every machine parts and tools have to undergo different stages of wear like Fatigue, Abrasive and Adhesion etc. To improve the surface and tribological properties hardfacing is used widely. Hardfacing is one of the oldest techniques used in surface engineering process to improve the surface properties of materials. Fe-Cr-C composed hardfacing alloys are used widely in severe abrasive conditions as these are superior in abrasive resistance. The aim of present study deals with characterization of wear tribological properties of Fe-Cr-C composition based hardfacing alloy on AISI 304 steel in form of mono and multilayers by SMAW process. The wear tests were carried out on Pin-On-Disc Tribometer and worn structures were examined under optical microscope. Phase and structural characterization were done by X-Ray diffraction.

Index Terms—first term, second term, third term, fourth term, fifth term, sixth term

I. INTRODUCTION

Surface engineering is one of the most efficient processes using widely to improve surface properties of materials to retain them in critical condition [1]. In surface engineering process, hardfacing is the oldest technique used to repair worn parts and protect from Abrasive, Adhesive, Chemical attacks by adding a protecting layer without changing material properties [7]. Since past five decades most of the researches were carried out to generate data which can raise industrial revolution in fields of protection shield layers of materials.

Fe-Cr-C hardfacing alloy with Ni addition are common hardfacing alloys used widely as these are superior in abrasive resistance in severe abrasion conditions [10]. The present study is concerned with wear characterizations of Fe-Cr-C based hardfacing alloy on AISI 304 steel applied in form of mono and multilayers. Many investigations were carried one role of mono and multilayers on resistance towards wear have contributed lot of benefits to industries in improving tribological properties of materials[6].

Superior abrasive wear resistance can be obtained by multilayering process leads to hardening of material due to formation of high volume fraction of carbides. Wear of material not depends on abrasive material but also depends on other parameters such as oxidation rate, thermal fatigue and heat impacts [7].

II. EXPERIMENTAL PROCEDURE

A. Specimen Preparation

AISI 304 steel of 8 × 34 mm and 8 × 38 mm dimensioned cylindrical rod are taken for hardfacing. These specimens were subjected to surface treatment at 6600 degrees. Before hardfacing process surface of pins were cleaned with ethyl alcohol. Fe-Cr-C based hardfacing alloy deposited in form of multilayer and monolayer depositions.

TABLE I.
CHEMICAL COMPOSITION OF PIN AND HARDFACING ELECTRODE.

Material	% C	% Cr	%Mn	%Ni	%Si	% S	% P	%Fe
Cylindrical Pin	0.08	20.0	2.0	10.0	1.0	0.03	0.04	Rem
Hardfacing electrode	0.40	10.50	1.80	19.0	0.45	820	*	Rem

Fe-Cr-C based hardfacing alloy is deposited in form of mono and multilayer by using a flux coated shielded metal arc welding (SMAW) having a diameter of 4mm electrode. The chemical compositions of pin and hardfacing electrode are reported in table 1. The welding parameters and design details of pins are reported in table 2 and table 3.

TABLE II. SHIELDED METAL WELDING PARAMETER

Parameters	value
Length of electrode	8mm
Diameter of electrode	450mm
Voltage	30 volts
Current	140 amps

TABLE III.
DESIGNING DETAILS AND LAYERS ON PINS ARE REPORTED IN TABLE

Specimen	Length (mm)	Diameter (mm)	No of layers deposited
Tribo pair 1	40	8	1
Tribo pair 2	40	8	3

B. Hardness and Surface roughness

The hardness of the prepared specimen before hardfacing and after hardfacing with mono and multilayered are measured by using Rockwell hardness tester. The Fig.1 shows the details of harness results. The surface roughness of specimens after hardfacing is measured by using Surftest SJ-301 surface roughness tester and surface roughness maintained 0.03 μm.

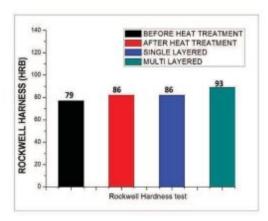


Figure 1. Hardness of specimens.

C. Wear Test

The sliding wear tests are carried out for both tribo pairs at constant parameters by using Ducom's Pin on Disc TR-20 machine in controlled room temperature under applied contact load of 30N with speed 300 rpm as per ASTM G-99A. The two tribo pairs are made contact with surface of SS alloy steel disc and revolved with track diameter of 25mm and each 2000 revolutions. Wear is not only depends on load but also dependent on the sliding speed. If sliding speed is more then, more distance is covered by the sample and static wear will be more. The wear will higher for higher sliding speed.

Sliding speed of disc (m/sec) =
$$\frac{\pi D N}{60000}$$
 (1)

Total distance travelled (m) =
$$\frac{\pi D N T}{60000}$$
 (2)

Where D = Diameter of track, N= speed of disc, T= Time travelled.

The mass loss of pin is calculated as the difference of their weights before the wear test and after the wear test. The volume loss of the pin is calculated by conversion of mass loss through equation 3.

Volume loss of pin, mm³=

$$\frac{M \ ass \ Loss}{D \ ensity} \times 1000$$
 (3)

Wear rate
$$W_a (mm^3/Nm) = \frac{\Delta G}{dMS}$$
 (4)

Where is weight loss, M is load applied, d is density and S is frictional distance travelled.

Wear resistance
$$W_r = \frac{1}{Wa}$$
 (5)

D. Results

The Figure 2 and Figure 3 show the resistance of single and multilayer hardfacings towards wear attack. These are heat treated and hardfaced specimens, showing a good resistance towards wear. As compared to single layer the multilayer hardfacing having good binding strength and lead to increase in resistance towards sliding and abrasive wear. The figure 2 shows the sudden raise of peaks due to high wear rate because the worn out particle due to sliding wear formed as abrasive particles and lead to high wear rate due lesser binding strength of single layer depositions.

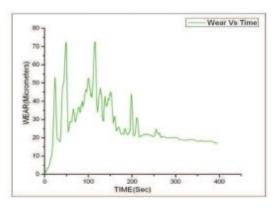


Figure 2. Wear Vs Sliding Time of Single Layer Hardfacing

Compared to mono layer the multilayer deposition of 10.5% Cr-19% Ni hardfacing shown a good resistance to wear and less amount of wear rate as shown in Figure 2.

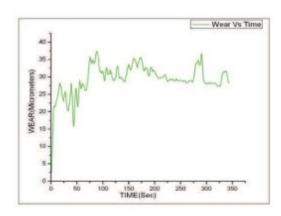


Figure 3. Wear Vs Sliding Time of Multilayer Hardfacing.

The mass loss, volume loss and wear rate are higher for mono and wear resistance is very poor when compared to multilayer hardfacing depositions. This is due to brittleness of specimens and poor binding strength. It may be offered due to operations done on grinding and lathe machined caused the surface harder and brittle.

The results of sliding wear and corresponding mass and volume loss of pin are mentioned in table 4.

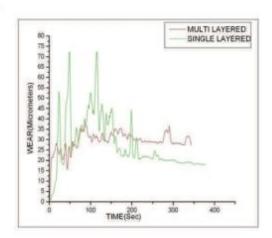


Figure 4. Comparison of Wear Vs Sliding Time of Multilayer over Single Layer Harfacings.

TABLE 4. WEAR CHARACTERISTICS OF PINS.

Mass loss (g)	Volume loss (mm3)	Wear rate (mm3/Nm)	Wear resistance (Nm/mm3)	Wear resistance (Nm/mm3)
Single layer	0.14	17.78	3.8×10-3	263.15
Multi	0.06	7.54	1.6×10-3	625.00

10.5% Cr-19% Ni hardfacings showed excellent wear resistance. This resistance is offered due to higher binding strength offered between bare specimen and hardfacing alloys as the bare specimen has subjected to heat treatment to improve its properties.

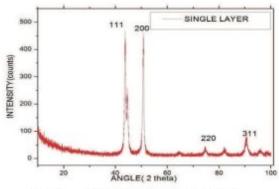


Figure 5. XRD Plots of Single Layer Hardfacing

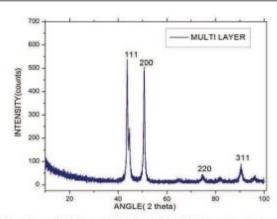


Figure 6. XRD Plots of 10.5% Cr-19% Ni Multilayer Hardfacing

Figure 5 and 6 shows XRD plots of Single and multilayer hardfacing layers hardfacings are having Face centered cubic structure with Austenitic phase. It states that there was no phase change after wear test.

E. Worn surfaces

Due to the slip actions and frictional force between the specimens and discs, mass transfer from specimens exists. The mass transfer can be observed during each test and due to this mass transfer the specimens were predominantly had a layer composed of wear debris and oxides test

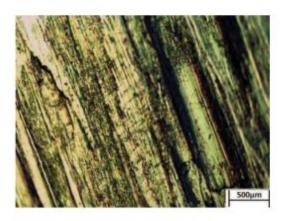


Figure 7. Worn Surface of 10.5% Cr - 19% Ni Single Layer Hardfacing after Wear Test.

Figure 7 and Figure 8 shows worn surfaces of both single and multi layered surfaces hardfacings. Figure 7 shows ploughing strips are very shallow on the surface as compared to multilayer hardfaced worn surfaces and little amount of oxide layer and void formation observed in single layer deposition.

The worn surfaces shows the formations of welded regions due abrasive particles and severe adhere wear has taken place and also severe wear transition occurred in single layer deposition. The particles which are formed while test are acting as abrasive in nature are mainly responsible for this ploughing nature and abrasive wear. The morphology of worn surfaces reports the severe formation of wear debris is mainly occurred on single layer as compared on multi layer and major loss of volume and wear rate is also occurred on single layer surface.



Figure 8. Worn Surface of 10.5% Cr - 19% Ni Multilayer Hardfacing after Wear Test

One of the common features absorbed in the both worn surfaces is formations of ridges running parallel to the sliding direction. The damaged spots in the form of craters can be seen in single layer depositions are decreased in multilayer depositions. The multilayer hardfaced deposition showed mild wear transition and no severe cracks was formed. The loosed wear debris formations were observed in previous hardfacing but here no such criteria were observed.

III. CONCLUSIONS

Multilayer hardfacing reduces rate of pin holes, cracks formations and also reduces internal stress in interface layers and leads to increase in volume of carbides which strongly influences the hardness of the material.

Multilayering can reduce the internal void formations and external surface defects and results in greater binding strength and hardness as the carbon content is increased with high fraction of carbide formations results in excellent resistance to external load and wear.

Increase in carbon content increase the hardness but also increases the brittleness of the material but on other way it can form more carbides which resists towards abrasive wear

In some cases the finishing operations are also responsible for hardening of surface layers.

The morphology of worn surfaces on Multilayer showed only plough nature on the surface and good wear resistance compared to single layer. As in single layer showed uneven cracks formation, voids and severe plough.XRD results stated that all hardfacing are in austenitic phase and after wear test no phase transformation was observed.

Broken flake particles from specimens acted as abrasive particles increased the wear rate due lesser birding strength. Cr-Ni based hardfaced alloy showed good binding strength, good wear resistance and fewer amounts of oxide layer formations on the surfaces of specimens as compared with all hardfacings. A buffer layer is preferred for these hardfacings

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Analysis and Design of Plastic Mold for Male Insulator of Solar Connector using Plastic Advisor 7.0

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Abstract— The intricacies in plastic mold design are accommodated by precise and correct methodology in design steps and taking into considerations the right factors. In this paper a two plate finger cam actuated injection mold is designed for a component namely 'male insulator of solar connector', the material selected for it is Poly Phenylene Oxide (Noryl-PPO). The male insulator component has intricate projections on its surface and has a threaded brass insert as well. The 3-D model of the component and extraction of core and cavities was performed in Plastic Advisor 7.0. Plastic advisor software is a powerful simulation tool to locate gate location and predict the defects in the component.

Index Terms—Mold design, Male Insulator, Solar Connector, Plastic advisor 7.0

I. INTRODUCTION

Injection molding is an ideal plastic manufacturing process. Due to its ability to manufacture complex plastic parts with high precision and production rates at low operation costs only a relatively high initial investment for mold design and fabrication [1]. The molding may cause defects and its processing offers a challenge during its development phase. The cost of the mold is high and any process that is not optimized renders heavy overheads during its development cycle and production. So, designing the mold which ensures best suitability for the features on the component with smooth flow of molten plastic is the demand of plastic industry [2].

Solar insulators are single contact electrical connectors commonly used in solar connectors. It consists of a plug and socket design. The plugs and sockets are placed inside a plastic shell that appears to be the opposite gender- the plug is inside a cylindrical shell that looks like a female connector but is referred to as male and the socket is inside a square probe that looks male but is electrically a female. The female connector has two plastic fingers that have to be pressed towards the central probe slightly to insert into holes in the front of the male connector. When the two are pushed together, the fingers slide down the holes until they reach a notch cut into the side of the male connector, where they pop outward to lock the two together. The male insulator consists of threaded insert of brass which is placed inside the die and then the molten plastic is introduced into the impression inside the mold.

Materials cooled to get desired form. Injection molding process can be divided into four stages which are Plasticizing, injection, packing and cooling [3]. The operations are to be carried out precisely. The tool is clamped together under high loads and is subjected to high injection pressures and high heat levels from the incoming polymer. During the cooling cycle, the mold is cooled until it reaches ejection temperature. All these factors combine to make the mold tool highly stress dynamic heat exchanger.

It is important, therefore, to ensure that the mold design takes all factors into consideration. Additionally, there are several other requirements that are needed to be considered, among which are the type of tool needed, e.g. two-plate, side core, spilt, three-plate, hot runner. And the mold material, the cavity construction, the required tool life and temperature control.

In addition to runners and gates, there are many other design issues that must be considered in the design of plastic molds. Firstly, the flow must allow the molten plastic to flow easily into all the cavities. The removal of solidified part from the mold is also equally important, so a draft angle must be applied to the mold walls. The design of the mold must also accommodate any complex features on the part such as undercuts or threads which will require additional mold pieces. Most of these devices slides into the part of the cavity through the side of the mold, and are therefore known as sliders or side-actions.

II. PROCESS VARIABLES AND MACHINE SPECIFICATIONS AND COMPONENT DETAILS

A. Speed related process variables

The process variables related to speed are mold opening and closing speed, injection speed, screw rotation speed, component retracting speed.

B. Pressure related process variables

The process variables related to speed are injection pressure, holding pressure and hydraulic jack pressure.

C. Temperature related process variables

The process variables related to temperatures are melt temperature and cooling water temperature.

D. Time related process variables

The process variables related to time are injection time, holding pressure time, pause (dwell) time, cooling time and cycle time.

The extent of variability encountered is a good indicator of the level of inherent stability present within the molding process. Hence, the smaller the variation, the more consistent and stable is the process.

The given molding machine is HMT 80T machine (Toggle series), the clamping unit and injection unit specifications are shown in Table 1 and table 2 respectively.

TABLE I. CLAMPING UNIT

Clamp force	80 Tons	
Distance between the tie bars	330 mm × 330 mm	
Size of the platen	485 mm × 485 mm	
Clamp stroke	345 mm	
Mold height	80mm to 350 mm	
Ejector stroke	110 mm	

TABLE II. INJECTION UNIT

Screw diameter	28 mm	
Shot weight	96 gm	
Theoretical shot volume	108 cm ³	
Maximum injection pressure	2670 kg/cm ²	
Injection rate	55.2 cm ³ /s	
Plasticizing capacity	20.8 gm/s	
Screw rotation	253 rpm	

In injection molding, cost and complexity of the mold increases as the criticality of the produced part increases. For this male insulator to avoid more complexity split cavity, mold with finger cam actuated ejection system is preferred.

The objectives of this research are to achieve maximum production by checking flow analysis results, injection pressure, fill time analysis, confidence of fill, temperature variance and weld lines etc. before manufacturing.

TABLE III. COMPONENT DETAILS

Material	Noryl (PPO- Poly Phenylene Oxide)	
Density	1.06 g.cm ³	
Specific heat	1.47 kj/kg/°C	
Melting temperature	250-300 °C	
Shrinkage	0.005- 0.01 m/m	
Tensile strength	55- 65 MPa	
Compressive strength	91 MPa (13,200 psi)	
Coefficient of thermal expansion	60 × 10 ° K ⁻¹	
Thermal conductivity	0.22 W.m ⁻¹ K ⁻¹ at 23°C	
Thermal diffusivity	$0.14 \text{ m}^2/\text{s}$	

The component details are shown in table 3. The 3D model and 2D drawing are shown in figure 1 and figure 2a and figure 2b respectively.



Figure 1. 3D model of male insulator of solar connector

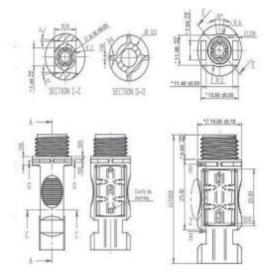


Figure 2a. 2 dimensional details of the component (male insulator)

Software is used to evaluate the mold design to make sure it will produce the most consistent and highest quality parts from each cavity of the tool. It uncovers the weakness of the dimensional geometry of the product and also it improves manufacturability.

In doing mold flow analysis, maximum production cycle time can be reduced, reduction in tooling and machining cost.

Also checking of the overall component before product design and therefore able to optimize the design process can be done.

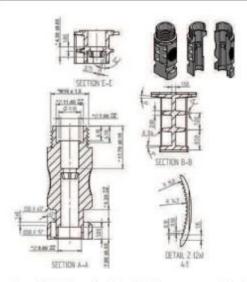


Figure 2b. 2D dimensional details of the component (male insulator)

III. SIMULATION

The simulations are performed in Plastic advisor 7.0 which is a powerful tool to simulate the best gate location, confidence in fill, fill time, determining weld lines and air traps.

A. Selection of best gate

The result of the best gate location is obtained by Plastic advisor 7.0 and is shown in figure 3.

In this simulation, dark blue portions shows best gate location and as the colour changes from dark blue to red, the gate location becomes worst.

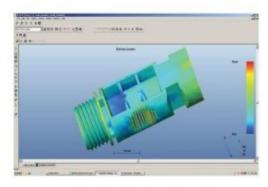


Figure 3. Result of best gate location

B. Confidence of fill

Confidence of fill depicts the reach of the molten plastic into all the intricate portion of the cavity. Confidence of fill is essential for instilling strength in the component. The result of confidence of fill is shown in figure 4.

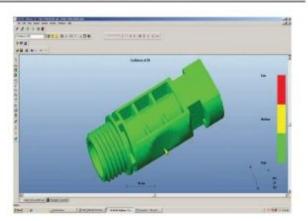


Figure 4. Result of confidence of fill

C. Confidence of fill in two cavities with runner system

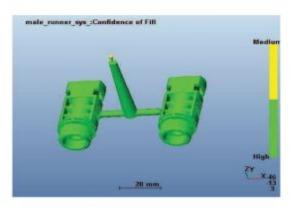


Figure 5. Confidence of fill in two cavity with runner system.

Filling pattern plays an important role in determining and identifying any potential aesthetic issues such as short shot, air traps and weld line due to wrong location of gate [4].

The confidence of fill when the cavities are increased to two along with the runner system is shown in figure 5.

D. Fill time

Fill time indicates the time the molten metal is taking to fill the cavity, it affects the amount of sheer heating at surface and thinning the plastic is experiencing thus affecting the material viscosity, the pressure inside the cavity and overall part quality.

Fill time dictates the effective solidification of the plastic component, poor solidification leads to poor structure of the plastic component. The result of the simulation for fill time is shown in figure 6.

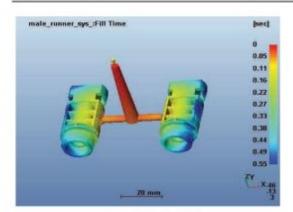


Figure 6. Result of fill time

E. Pressure drop

Pressure drop facilitates the quality of the structure of the component as well as quicker solidification and removal of the component from the mold.

The result of simulation for pressure drop is shown in figure 7.

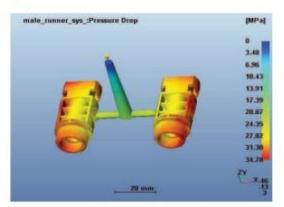


Figure 7. Result of pressure drop

F. Flow front temperature

Flow front temperature is the temperature at which shows the temperature of the polymer when the flow front reaches a specified point in the center of the plastic cross section.

It also facilitates uniform flow ability and uniform shrinkage, weld lines, hesitations, flow mark and material degradation due to high temperature in the component. The result for flow front temperature is shown in figure 8.

The flow front temperature should not drop more than 3° to 5°. While doing the simulation it looks for hot spots, cold spots or check where the material is excessively cooling or heating

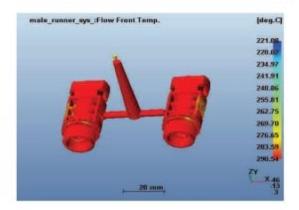


Figure 8. Result of flow front temperature

G. Cooling quality

The cooling quality has to be uniform throughout the component. The result of cooling quality is shown in figure 9.

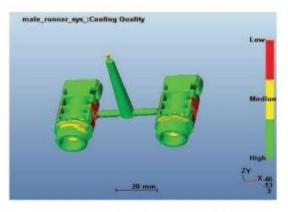


Figure 9. Result of cooling quality

H.Quality prediction

The quality of the component can be predicted using mold flow analysis. The result of quality prediction is shown in figure 10.

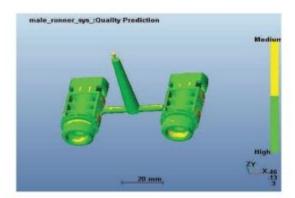


Figure 10. Result of quality prediction

I. Weld lines

Weld lines are formed when the flow waves of molten plastic merges with each other. It is undesirable and prominently visible on the component.

The result of weld line formation is shown in figure 11.

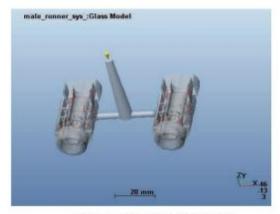


Figure 11. Result of weld line formation

J. Air traps

Air traps causes blow holes in the component thus decreasing the quality and strength of the component. It is highly undesirable and it has to be taken care beforehand itself so that once the production starts there should not be any design modification. The result of air traps in the component is shown in figure 12.

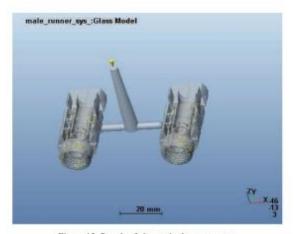


Figure 12. Result of air trap in the component

Air traps also causes blemishing on the component and difficulties in ejection of the component. Proper venting and changing the process parameter in speed and pressure are done to control it.

TABLE IV. SUMMARY OF MOLD FLOW ANALYSIS

Confidence of fill	
Injection time	0.55 s
Injection pressure	34.78 MPa
Weld lines	Partial
Air traps	Partial
Shot volume	10.90 cm ³
Quality	Good
Filling clamp force	2.95 T
Packing clamp force estimate @20%	1.88 T
Packing clamping force estimate @80%	7.51 T
Packing clamping force @120%	11.26 T
Clamp force area	26.47 sq.cm
Cycle time	8.78 s
Surface temperature variance range	-7.57°C to 9.25 °C
Freeze time variance range	2.16 s to 5.61 s

The results obtained from mold flow analysis is very good although weld lines and air traps are present in the analysis, they can be avoided by changing the molding parameters at the time of production. The summary of the simulation is shown in table 4.

All the results obtained are acceptable hence the design process can be started.

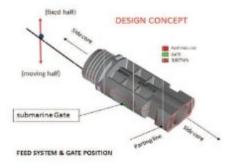


Figure 13. Design concept for male insulator

K. Feed system calculations

The maximum diameter of the sprue bushing should be greater than the nozzle orifice by 0.5- 1.0 mm. The length of the sprue channel should be as short as possible and never be over 100 mm. The sprue included angle has to be 4°- 5°. The diameter of the runner is calculated by equation 1 [5].

Runner diameter, D =
$$\sqrt{W} \times \sqrt[4]{L} / 3.7$$
 (1)

.Where, W = Weight of the component L= length of the runner

$$D = \sqrt{10.8} \times \sqrt[4]{34.2} / 3.7$$

= 2.15 mm

L. Shot weight

Shot Weight= Weight of the component + Weight of the feed system Weight of the component = 5.4 +5.4 = 10.8 gm Weight of the feed system= 10% of molding= 0.54 gm Therefore, shot weight= 10.8 + 0.54= 11.34 gm

M.Clamping force or tonnage calculation

The clamping force calculation is shown in equation 2 [5].

Clamping force= Projected area of the molding (cm²) × 1/3 times of Injection pressure (kg/cm²) (2)

Injection pressure= 2670 kg/cm²

Clamping force= $(8.18 \times 2670) / 1000 = 21.84 \text{ T}$

N. Working length of finger cam

Finger cam has the advantage of easy handling and smooth opening and closing of die. It is shown in figure 14. The length of the finger cam invariably depends on the size of the component and mold, it is calculated in equation 3 [6].

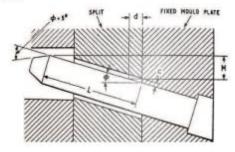


Figure 14. Finger can actuator

Working length, $L = (M/\sin \Phi) + (2c/\sin \Phi)$ (3) Where,

M = Spilt movement= 27.39 mm

 Φ = Angle of finger cam = 15°

c= Clearance = 0.5 mm

 $L=(27.39/\sin 15^\circ) \times (2\times0.5/\sin 15^\circ)$

= 107.83 mm

O. Cooling system

Serial cooling channel system has been adopted for this mold for better cooling quality. For this, cooling holes of 6.0mm diameter with 1/8BSP (British standard pipe) plugs have been made.



Figure 15. Cavity layout and mold size

IV. CONCLUSIONS

Plastic advisor 7.0 has given the results for the best gate location, confidence of fill, quality, weld lines and air traps. Weld lines and air traps which are appeared in the analysis can be overcome by changing the process parameter related to speed and pressure during production. Instead of water different types of oils can be used for effective cooling of the die. Thermal and stress analysis can be performed over the die by using ANSYS.

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SoC Based Sigma Delta ADC Using ANFIS Algorithm for ECG Signal Processing Systems

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Abstract: This paper presents a design of low power sigma delta ADC by using ANFIS algorithm which is applicable for high resolution ECG signal processing systems. The ECG signal analysis which is also known as a comprehensive analysis of the Heart, which helps for collecting the information of abnormal and normal conditions of the heart. The resolution of the ECG signal helps in the diagnosis of heart abnormalities. With the proposed design, the resolution of the ECG signal is improved and reduced power consumption levels of ADC. The ANFIS algorithm is used to decide the sampling clocks of ADC which changes the power consumption levels in the ECG system. The main advantage of this ANFIS algorithm is to take instantaneous decisions. This ANFIS system can also be called as an intelligent system which makes use of neural networks. The ECG signal data is used as an input data for implementing the whole system SoC (System-on-chip) design using 90nm technology. The SoC includes the integration of 14 bit sigma delta ADC, ANFIS system, multiplexer, down sampling and up sampling circuits. The algorithm is designed in MATLAB and the whole system is modelled using VERILOG language. The simulation results were shown in Xilinx system generator, the synthesis is performed in Synopsys Design vision. The physical design of the chip is carried out in Cadence Encounter tool. The complete system can operate at 400 MHZ frequency and the power consumption of the system can be given as 15mw. This high resolution low power system level design is used for health care monitoring applications.

Index Terms--- ADC, ANFIS algorithm, SOC domain, ECG signal processing, power consumption.

I. INTRODUCTION

The Electrocardiograph is a machine that performs electrocardiography and results in electrocardiogram. The electrocardiogram is a painless test, which records the electrical activity of the heart. For every heart beat an electrical signal is generated from the top of the heart to the bottom. These electrical signals were set to rhythm of heart beat.

The hierarchy level design of the ECG signal processing system consists of an Analog- to- Digital converter and digital signal processing system. A dynamic system clock source is given to both ADC and the DSP system. The primary components of DSP signal processing system includes instrumentation amplifiers and operational amplifiers. The ECG signal processing system with sigma-delta ADC is shown in the Fig 1.

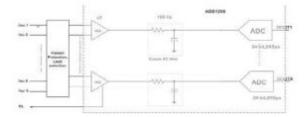


Figure. 1 Example of an ECG signals processing system with sigma delta ADC.

Delta sigma converter is a type of oversampling and noise shaping analog-to-digital converter. The main purpose of the ADC is to convert the analog ECG signal data into digital ECG data.

The pattern of an ECG signal with PQRST format can be given as shown in the below Fig 2.

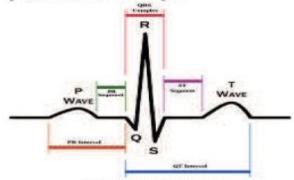


Figure. 2 Example of an ECG pattern.

The ECG data base can be obtained from the web based source called physionet[17] which is a free access source of signals.

This paper is organized as: Section II shows the brief explanation about analog –to-digital converter. Section III explains about the Adaptive Neuro Fuzzy Inference system algorithm and its architecture. Section IV gives the block diagram for experimental environment. Section V includes the methodology applied in the project and finally section VI includes the simulation results and chip layout for the proposed work.

II. ANALOG -TO-DIGITAL CONVERTERS

The analog-to-digital converter is a system that converts an analog signal into a digital signal. A digital-to-analog converter (DAC) performs the reverse operation.

The ADC can also be defined as the on-chip interface between digital domain and the real domain of analog signals.

The general process of converting an analog signal into digital signal consists of two steps .They are: 1) sampling 2) quantization. Consider the analog signal x (t) when performing the sampling process the analog signal is converted into sampled signal and then the sampled signal is quantized and finally the signal is converted into digital.

Different types of analog -to-digital converters are flash ADC, successive approximation ADC, pipe line ADC, and time interleaved ADC. The highest resolution ADC is Sigma -delta ADC [2] which is a cost efficient low power converter. The basic building blocks of ADC are comparators, amplifiers and integrators. The brief explanation about sigma -delta ADC can be given below:

A. SIGMA-DELTA ANALOG-TO-DIGITAL CONVERTER

The sigma delta Analog to digital converter [2] is a 1-bit sampling system. This type of ADC can also be called as an oversampling ADC. Delta-sigma ADCs implement oversampling, decimation filtering, and quantization noise shaping to achieve high resolution and excellent antialiasing filtering.

The block diagram of the ADC is as shown in Fig 3. The components of the ADC are summing amplifier, integrator, quantize (comparator), DAC, digital filter.

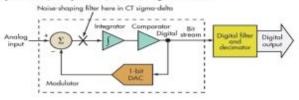


Figure. 3 Sigma-Delta Analog To Digital Converter.

The input analog signal and the output signal of 1-bit DAC are applied to the summing amplifier and the output analog signal is given to the integrator. In integrator, the noise shaping of the obtained signal is performed and the resultant signal is allowed to pass through the quantizer. The quantizer results only two levels for the obtained signal. The amplitude of the quantized signal can be "1" or "0". Hence the analog signal is finally converted into 1-bit digital signal and then again the feedback is given to the summing amplifier.

Finally, the obtained 1-bit digital stream of data is given to the digital low pass filter which results in the N-bit digital signal for the given input analog signal.

This is the working principle of sigma delta ADC which has a very important role in the functioning of an ECG signal processing system.

III. ANFIS ALGORITHM

The Adaptive Neuro Fuzzy Inference System is a type of network which is a combination of artificial neural network and fuzzy logic control [5],[13]. This network can also be called as hybrid intelligent network. The integration of both neural network and fuzzy control has a potential to capture the benefits of both, in a single frame. These networks may be linear or non linear, predictable or unpredictable. The neural network has the ability to recognize the patterns and adapt them with changing environment.

The important steps for developing a neuro fuzzy system

- 1) Fuzzification of the input parameters.
- 2) Computation of degree for linguistic terms.
- 3) Conjunction of fuzzy inferred parameters.
- 4) Defuzzification of the output.

The adaptive fuzzy inference system architecture[4],[6] with two inputs such as X, Y and the corresponding output F is given in Fig4.

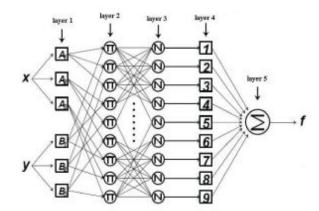


Figure. 4 ANFIS structure for two-input one output.

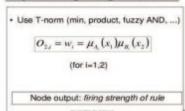
A two-input, one-output zero order ANFIS [4] with three Membership functions per input (nine fuzzy if-then rules) is shown in Fig. 4. It is composed of five layers. The square nodes in the first and fourth layer represent adaptive nodes, e.g. they depend on a set of parameters; the circle nodes are

The operations performed in each layer are shown below: Layer 1: Every node in This, is adaptive with a node function. Each input node has linguistic variables which can be called as membership functions.

$$\mu_{\lambda}(x_1) = \frac{1}{1 + \left| \frac{x_1 - c_1}{a_i} \right|^{2s}}$$

where x is the input node and a and c are the parameters of the membership function.

Layer 2: Firing Strength of Rule



Layer 2: each node in this layer calculates the firing strength of a rule. The output obtained from this layer is the strength obtained by performing rule matrix operations.

Layer 3: Normalize Firing Strength

• Ratio of
$$i^{th}$$
 rule's firing strength vs. all rules' firing strength
$$O_{3,i} = \overline{w}_i = \frac{w_i}{w_1 + w_2}$$
 (for i=1,2)

Layer 3: Every node in this layer calculates the ratio of rule firing strength to the sum of all the firing strengths of the rules. The outputs of this layer are the normalized firing strengths.

Layer 4: Consequent Parameters

Layer 4: every node in this layer is multiplied with a node function, with a consequent parameter set.

Layer 5: Overall Output

	$\sum w_i f_i$
	$O_{S,1} = \sum_{i} \overline{w}_{i} f_{i} = \frac{\overline{\gamma}}{\sum_{i} w_{i}}$
Note: Detput	is linear in consequent parameters p.q.r.
$= \frac{w_1}{w_1 + w_2}$ $= \overline{w_1}(p_1x_1 + \overline{w_2})$ $= 6\overline{w_1}x_1 \text{ by.}$	$f_1 + \frac{w_1}{w_1 + w_2} f_2$ $g_1 x_1 + g_2 x_2 + g_3 x_3 + g_4 x_4 + g_4$ $+ (\overline{w}_1 x_1)g_1 + (\overline{w}_1 x_2)g_2 + (\overline{w}_2 x_3)g_3 + (\overline{w}_2 x_4)g_4 + (\overline{w}_3 x_4)g_5 + (\overline$
-	ut: Weighted Evaluation of RHS Polynomials

Layer 5: This layer consists of only one node which calculates the final output of the Neuro fuzzy system.

Hence this is the working principle of adaptive neuro fuzzy inference system.

Some of the important considerations for determining the rules are as follows: For example, if 'g' is Very Low and 'f' is Very Low then the sampling clock is selected as HCLK or if 'g' is Very High and 'f' is Very High then the sampling clock is HCLK. The sampling clock of the ADC is selected as MCLK For example, if g is Medium and f is Medium then the sampling clock is MCLK. For example, if g is Low and f is Low then the sampling clock is LCLK. Table I tabulated the fuzzy adjustment rule table for the frequency of the sampling clock of the ADC. It maps the two input fuzzy sets to an output fuzzy set.

TABLE I
FUZZY ADJUSTMENT RULES FOR THE FREQUENCY OF THE SAMPLING
CLOCK

		1	T		1
g f	Verylow	low	medium	high	Very high
Verylow	HCLK	LCLK	LCLK	LCLK	HCLK
low	HCLK	LCLK	LCLK	LCLK	HCLK
medium	HCLK	MCLK	MCLK	MCLK	HCLK
high	HCLK	HCLK	HCLK	HCLK	HCLK
veryhigh	HCLK	HCLK	HCLK	HCLK	HCLK

The terms such as verylow, low, medium, high, veryhigh are called as linguistic variables for input parameters.

HCLK, MCLK, LCLK are the linguistic variables for the output of the ANFIS system. An example for different clocks is as shown in the Fig 5.

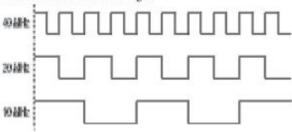


Figure. 5 Example showing the three different types of clocks

In this paper, an ECG signal data is taken as input data to implement the ANFIS algorithm[8]. The membership functions are developed to perform fuzzy rules to produce the best logic control for the proposed system. Consider 'f' & 'g' are the parameters of the ECG signal in which 'f' is the amplitude of the signal and parameter 'g' is the slope value of the input ECG signal. The expressions for the parameters can be given as:

 $F(n)=abs(p(n)) \qquad (1)$ $G(n)=abs(p(n)-p(n-1)) \qquad (2)$

Where p(n) is the amplitude of the ECG signal.

The main concept of the proposed system is to select the base sampling rate in the normal regions and oversampling rate in abnormal regions of the body signals. The sampling rate is controlled by the fuzzy logic control technique. By this technique the quality of the waves can be efficiently improved.

IV. BLOCK DIAGRAM FOR EXPERIMENTAL ENVIRONMENT

The proposed ECG signal processing system in Fig.6 includes a sigma-delta ADC, ANFIS system, two down sampling circuits, interpolation filter, phase locked loop(PLL), Multiplexer. The details of each component in the system are described below:

 Sigma –delta analog to digital converter: the ADC[3] can be realized by making use of various architectures depending upon the characteristics of the signals. The proposed 14 bit sigma delta ADC [3] was implemented by using sigma adder, delta adder, digital-to-analog converter. It is used for converting the analog ECG signal into digital stream. This design is used for the proposed ECG signal proposed system because of its various characteristics such as various sampling rates can be used and it is a high resolution ADC.

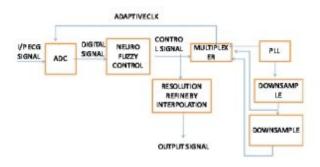


Figure. 6 Block diagram of the proposed system.

- 2) Adaptive Neuro Fuzzy Inference system: The adaptive neuro fuzzy controller[8] was implemented by making use of adders, multipliers, dividing blocks. It is used for deciding the sampling clock of ADC from the given different clocks. It performs the comparison for the body values from the ECG signal. Next, it obtains the variance between various amplitudes of the ECG signal and results in the two parameters such as 'f' & 'g' with this comparison. The final step is to decide the sampling clock for the proposed ADC. The sampling clock can be HCLK, LCLK, MCLK according to the given input pattern.
- 3) Down sampling circuits: The down sampling circuit consists of anti-aliasing filter and a decimation filter. In these circuits, first the HCLK signal which is generated from the PLL is allowed for filtering, by anti-aliasing filter and then it is sub sampled by a decimation factor. Then the HCLK signal is sampled to MCLK and then the MCLK is sampled to LCLK. By the design technique, three various frequencies of clock can be produced by using two down sampling circuits.
- 4) Multiplexer: The Multiplexer is a device that selects one of the inputs from the various inputs given depending upon the selection line. The control signal for the multiplexer can be given from the adaptive neuro fuzzy inference system and the inputs for the multiplexer are HCLK, MCLK, LCLK signals which are obtained from the clock generator and down sampling circuits. The output of the multiplexer is given as a sampling clock of ADC[2] which varies the power consumption levels of the device.
- 5) Interpolation filter: Interpolation[14] is a process of converting the sampled signal into highest sampling rate by adding the samples in particular intervals of time by using various design techniques. Here, the input for the interpolation filter is the control signal obtained from the adaptive neuro fuzzy inference system. By performing interpolation the signal can be converted into highest sampling rate signal by which the resolution of the converted ECG signal can be increased which is used for diagnosis of heart beat signals.

V. METHODOLOGY FOR THE PROPOSED DESIGN

The working flow of the proposed system in detail can be explained from the flow chart which is shown below in Fig.7

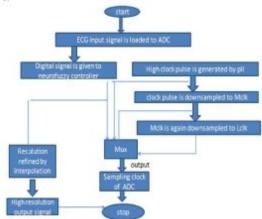


Figure. 7 working principle of the proposed ECG signal processing system

The chip includes the integration of Sigma-Delta ADC, ANFIS system, multiplexer, down sampling circuits, pulse generator, up sampling circuit, decimation filter and interpolation filter. The input ECG signal[8] is taken from physionet [5] which can be in the format of MIT-BIH Arrhythmia data in which each signal has 360 samples per second. The frequency of the general ECG signal is 360 Hz. This taken signal consists of each sample of length of 14-bits and is loaded in the MATLAB. From the workspace of MATLAB the ECG signal is given to the sigma delta ADC for converting the analog ECG signal to the digital signal.

The digital signal data is given as input for neuro fuzzy system such as ANFIS(adaptive neuro fuzzy inference system). Here, the obtained input from the ADC is allowed to obtain the membership functions required for performing the fuzzy rule matrix operations. The outputs obtained from the rule matrix are normalized and the normalized outputs were allowed for defuzzification. The final result obtained from the defuzzification layer of the system is the final output of the ANFIS system. The output of the ANFIS system can be HCLK or MCLK or LCLK which can be decided by the given digital input signal. This output signal is given as a selection line for the multiplexer.

The multiplexer is a 4X1 MUX which consists of four inputs and two selection lines and single output. The ANFIS system output is taken as a selection line for the multiplexer. The inputs for the multiplexer can be given from the down sampling circuits. HCLK can be given from clock generator, MCLK, LCLK signals which are derived from the down sampling circuits are given as inputs for the multiplexer. By performing the operation of multiplexer we can get a decision control signal depending on these clock signals. The output obtained from the multiplexer can be given as a sampling clock of sigma-delta ADC.

Depending on the sampling clock given to the ADC, the power consumed can be changed at different clock periods. The output obtained from the multiplexer can be allowed to undergo upsampling so that by adding the samples to the control signal the resolution can be improved and by performing the interpolation, finally resolution refined signal is obtained from the whole system.

Firstly, the proposed design is implemented by using the co simulation of MATLAB, Xilinx system generator[16]. The verilog code has been manually written for the ANFIS algorithm and it is interfaced with the other blocks such as downsampling circuits present in the system generator tool. Finally after interconnecting the ADC with ANFIS system the logical simulation is performed in MATLAB. By using the hardware description language verilog the design is simulated in Xilinx system generator and Design Vision compiler which belongs to SYNOPSYS tool was used for the synthesis of the design in VLSI circuit using 90nm technology. The placement and routing of the chip is performed in Cadence Encounter and a chip layout is generated for the proposed design. The photo of chip layout is illustrated in Fig 13.

Synthesis results show the area of the proposed signal processing system is 121613µm². Which was synthesized in 90nm technology The power consumption for the whole design can be obtained from the design vision. It consumes 15mW at 300 MHz operating frequency with 1.62V supply voltage. The specifications are listed in table III.

TABLE II
OUTPUT SAMPLING CLOCKS OF ADC AND POWER CONSUMPTION
LEVELS

LEVELS				
SAMPLING CLOCK	FREQUENCY	POWER		
HCLK	400MHZ	5.4W		
MCLK	285MHZ	3.08W		
LCLK	222MHZ	1.4W		

VI. SIMULATION RESULTS OF THE COMPLETE SYSTEM

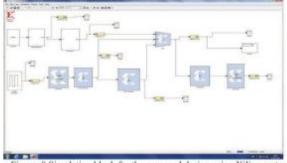


Figure. 8 Simulation block for the proposed design using Xilinx system generator & MATLAB

The input given to the system is an ECG signal data. The ECG signal data loaded in to the MATLAB can be shown in the below Fig 9.

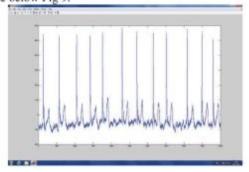
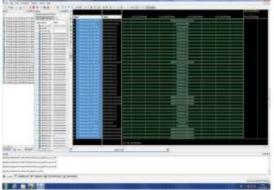


Figure. 9 Input ECG signal used for the simulation of the proposed system



Figure, 10 Photo Snaps for The Simulation Results of The Proposed Signal Processing System

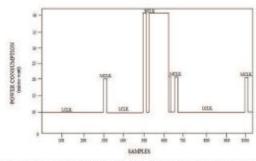


Figure. 11 Clock information and distribution of power consumption

VII. SYNTHESIS RESULTS

The synthesis of the proposed design is performed using Design Vision Compiler of Synopsys tool. The RTL netlist of the design is as shown in the Fig. 12.

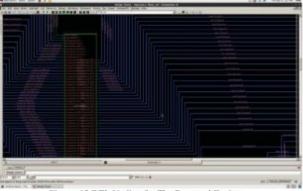


Figure. 12 RTL Netlist for The Proposed Design

The specifications of the proposed design includes area, power, resolution, frequency, process are shown in the table listed below:

TABLE III

CHIP PESTI TS OF THE PROPOSED SYSTEM LEVEL DESIGN

Specification	Chip Results	Chip Results	
Process	UMC 90nm		
Core Area	121613µm²		
Power	15mw		
Supply Voltage	1.62v	- 5	
Operating Frequency	300mhz		
Resolution	16 Bit		

The chip layout for the proposed design is as shown in the Fig 13. This process is performed in Cadence Encounter tool.

By performing this physical design we can obtain the netlist, DEF(Design Exchange File) & GDS –II(Graphical Data System) file. With these files we can go for further steps such as fabrication of the chip for the proposed design. This can be used for real time applications.

VIII. CHIP LAYOUT FOR THE COMPLETE

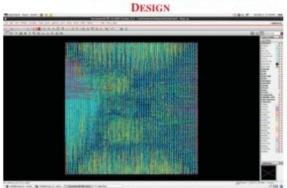


Figure. 13 Physical design of the proposed ECG system chip layout in Cadence Encounter

IX. CONCLUSIONS

In this project the system level design of the low power ECG signal processing system which includes the integration of sigma-delta ADC, ANFIS system, multiplexer, up sampling and down sampling circuits is implemented. The sampling clock of sigma delta ADC is selected by using the decision technique which is done by using intelligent algorithm called ANFIS algorithm which can also be called as an intelligent system. The design is modeled by taking the ECG signal features as the input parameters. As the ANFIS approach provides a general frame work for combination of NN and fuzzy logic, the efficiency of ANFIS for deciding the sampling clock of ADC can be concluded by observing the power consumption levels of ADC at different clock periods. The SoC implementation of the proposed design reduces the area, power consumed by the circuit. The results show that this work can not only improve the quality of the ECG signals but also improves the power consumption of the devices. The obtained chip area is about 121613µm2 and the power consumed by the device is 15mW.the resolution of the ECG signal is increased by 0.14%. This is applicable for real time health care monitoring applications.

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SoC Based SIFT Algorithm for Identification of the Quality Objects for Palletization Application

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Abstract: In some of the manufacturing industries automation problems occur most commonly like quality control and palletization. This paper proposes a system level design for the identification of quality objects for palletization process to solve the automation problems. The quality of the object is identified by using SIFT (Scale Invariant Feature Transform) algorithm which is one of the image processing algorithms most popularly used for local feature detection. By using SIFT algorithm featurepoint extractions are performed for an input image. After featurepoint extraction, feature matching is performed by comparing the extracted featurepoints of the input image and original image featurepoints which are stored in database. The output comes after the feature matching will actuate the palletization process to differentiate the type of objects. The processing of an image using SIFT algorithm for palletization process is designed in MATLAB by using Xilinx System Generator and simulations are performed. Then the HDL code is generated for the whole design by using system generator. The generated HDL code is synthesized by Design vision compiler in Synopsys tool. To integrate the whole system design into SoC (System on Chip) using 90nm technology physical design is performed in Cadence Encounter tool. Due to this design the whole system obtains optimized area and power.

Index Terms- Palletization, SIFT, Featurepoints, Gaussian pyramid, DoG, Extrema detection, Xilinx System Generator.

I. INTRODUCTION

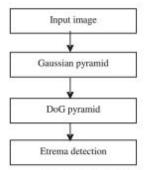
In present days due to the advancements in digital technology, manufacturing industries are using the fully In industries automation machines. during manufacturing of the products some of the automation problems will occur such as quality control and palletization process. These are the most recurring process in manufacturing industries [1]. Quality control is used to check the quality of the products after the completion of product manufacturing to differentiate the good products from the defective products. Palletization process is a process of stacking the products on a pallet which will come from production line in industries for distribution or storage purpose. Different type of palletizers are used in industries. They are mechanical palletizer and robotic palletizer. Mechanical palletizers are fast, inflexible and have larger product changeover downtime. Robotic palletizers are slower but flexible and have shorter product changeover downtime [2-3]. The quality control of the object is performed by using image processing algorithms in vision system which is most commonly used in robotic application for the object recognition. Traditionally some of the image processing algorithms like edge based, adaptive thresholding [4, 5] are used for object recognition but for complex objects these algorithms are difficult for object recognition. To solve this problem SIFT algorithm is used to detect the local feature points of an image, because SIFT can be able to detect the features even in invariant size, rotation, view and illumination [6]. Image processing algorithm can be implemented in Field Programmable Gate Array (FPGA) due to the recent developments in the FPGA hardware architecture. FPGAs have great processing speed and flexibility to process the image processing algorithms in real-time applications [1].SIFT algorithm performs high computations to detect the feature points of the image. So the SIFT is suitable to implement in FPGA because of its pipelined structure of architecture [7, 8]. But due to the increasing of low power and area consumption requirements in the present days of markets (VLSI systems) System on Chip (SoC) design is used instead of FPGAs, because of the advantage of low power consumption and reduced area for the typical design. SoC is an Integrated Circuit (IC) which will integrates the whole system design into a single chip.

In this paper, a system level design is implemented for the identification of object using SIFT algorithm. It will actuate the control flow of a palletization process and the proposed system is integrated into SoC to obtain optimized area and power.

This paper is organized as section II gives the brief description of SIFT algorithm. The block diagram and logical design for the proposed system is explained in section III. The implementation of the proposed system in SoC is described in section IV. In section V and VI results and conclusion are given.

II. SIFT ALGORITHM

SIFT algorithm proposed by David Lowe [7] is an image processing algorithm which is used to detect the local feature descriptors of the faces or any object. SIFT is used in many robotic applications for object recognition and tracking the objects in computer vision system. SIFT has a great ability to detect the feature points of an object even in invariant conditions also such as different in size, rotation, intensity and view. SIFT algorithm is divided into three steps to detect the feature points of an image. They are Gaussian pyramid, Difference of Gaussian (DoG) pyramid and Extrema detection [9] as shown in Fig. 1.



Figure, 1 Steps of SIFT algorithm

A. Gaussian pyramid:

The input image I(x, y) is multiplied with Gaussian kernel $G(x, y, \sigma)$ by using Gaussian filter. It will generate the Gaussian image $L(x, y, \sigma)$ [10] and is shown in (1)

(1)

(2)

By changing the value blur point of the image will be changed. A Gaussian pyramid consists of multiple octaves with multiple scales. Scale is nothing but a number of Gaussian blur images. One octave consists of stack of Gaussian blur images [9].

B. DoG (Difference of Gaussian):

Difference of Gaussian is constructed by subtracting two Gaussian images as shown in (3). An example is shown in Fig. 2 DoG constructed from Gaussian pyramid with four scales and one octave.

(3)

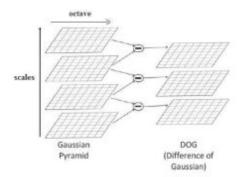


Figure. 2 Gaussian pyramid and DoG with 5 scales and 3 octaves C. Extrema detection:

After the construction of DoG, local maxima and minima points are constructed by selecting a sample point from one DoG image and compared that point value with its neighbouring point and adjacent DoG image points value either maximum or minimum as shown in Fig. 3. Then from these maxima and minima points a stable point is taken as keypoint or featurepoint of an image by adding threshold value [10].

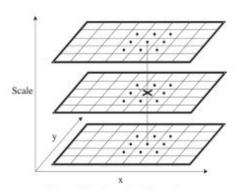


Figure. 3 Maxima and minima points

III. LOGICAL DESIGN FOR THE PROPOSED SYSTEM

Block diagram of the system is shown in Fig. 4 for the processing of the image by using SIFT algorithm to detect the feature points. It will actuate the control flow of a palletization process. The processing of the image by using SIFT algorithm is clearly explained in section II, and gives the output as feature points will separate the type of objects and detect the defective object for physical actuation of a palletization process.

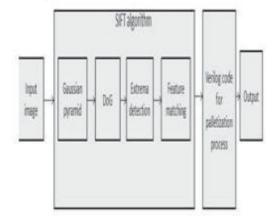


Figure. 4 Block diagram of the proposed system

For this block diagram, control flow chart is shown in Fig.5. In this design, three input images are taken as A, B and B defective. First the input image is preprocessed by converting into 300x300 pixels of grayscale image [11]. Then the image is processed by using SIFT algorithm to extract feature points of the image.

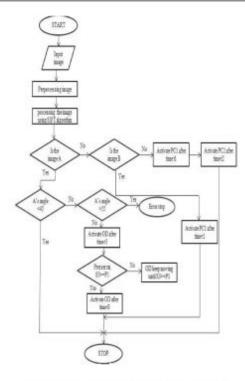


Figure. 5 Control flow chart of the proposed system

If the image comes after the processing using SIFT algorithm is type A with angle less than 45°, then the process is stopped. If angle of image A is greater than 55° then the Orientation device (OD) will be activated which is a mechanical palletizer [1] used to set the inclination of the image until the pressure S1 is greater than or equal to P1. After that OD will be deactivated. If output comes from SIFT algorithm as image B, then the PC1 (pneumatic cylinder) will be activated. If output image is B defective, PC1 and PC2 will be activated.

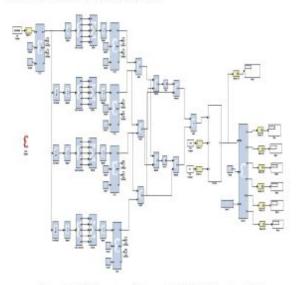


Figure 6: Whole system diagram in MATLAB using Xilinx System Generator

The whole control flow of the proposed system is designed first in MATLAB using Xilinx System Generator as shown in Fig. 6 and HDL code (Verilog code) is generated.

By using the Xilinx system generator blocks the control flow chart is designed in MATLAB for identification of quality of the objects for the palletization process. First the preprocessed image is stored in FIFO block to construct Gaussian blur image [11]. In this, we have constructed Gaussian pyramid with four scales is nothing but four Gaussian blur images and one octave. From the four Gaussian blur images three DoG images are constructed by using Addsub block to subtract the two successive Gaussian blur images. Then the maxima and minima points are constructed by comparing the three DoG images using Relational block and from the maxima and minima points featurepoints are extracted by using Logic OR block. Feature matching is performed by comparing the extracted feature points with the original featurepoints which are stored in From workspace block of SIMULINK block which is used to store the values of an image from MATLAB workspace. The output which comes after the feature matching is given as input to Black Box block (it is used to interface the HDL code and Xilinx system generator blocks).In this Black box Verilog code is given which is written manually for the control flow of a palletization process and simulation is performed for the system model. A System generator token is added to the whole system model which will serve as a control panel for controlling panel and simulation parameter. Then the HDL code is generated by the System generator token according to its specifications [12].

IV. IMPLEMENTATION OF THE PROPOSED SYSTEM IN SOC

The generated Verilog code from the MATLAB is compiled in Xilinx to generate the RTL schematic as shown in Fig. 7

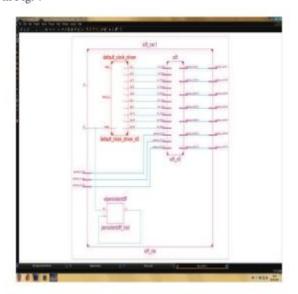


Figure. 7 RTL schematic

Then the Verilog code is synthesized by using Design vision compiler in Synopsys tool to generate RTL Netlist and to perform the area analysis, timing analysis and power analysis which is shown in section V. To integrate the whole system into SoC using 90nm technology, physical design is performed in Cadence Encounter tool. After the physical design, chip layout design and GDS (Graphical Data System) file will be generated. GDS file is used in chip fabrication for Real-Time application.

V. RESULTS

A. Simulation results in MATLAB:

The featurepoint extraction of input object A, B and defective B are shown in Fig. 8, 9 and 10 respectively performed by using SIFT algorithm in MATLAB using Xilinx system generator blocks.

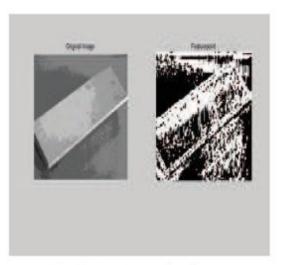


Figure. 8 Featurepoint extraction of image A

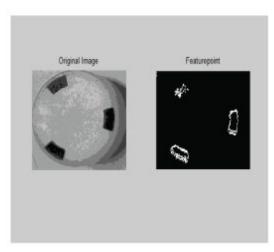


Figure. 9 Featurepoint Extraction of image B

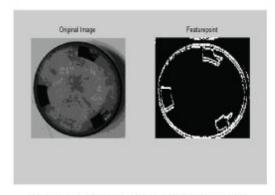


Figure. 10 Featurepoint extraction of image B defective

B. Simulation results in Xilinx:

After the whole system is designed in MATLAB, Verilog code is generated. Then the generated Verilog code is compiled and simulation results are observed in Xilinx software. For input image A with angle 50°, the output obtained is OD=1 and stop=1 is shown in Fig. 11. For input image B, the output obtained is PC1=1 and stop=1 is shown in Fig. 12. For input image B defective, the output obtained is PC1=1, PC2=1 and stop=1 is shown in Fig. 13.

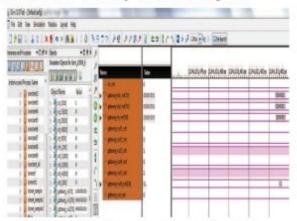


Figure. 11 Simulation result for image A with angle 506

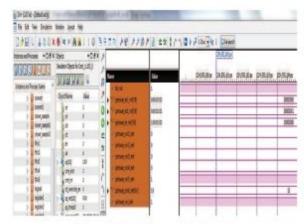


Figure. 12 Simulation result for image B

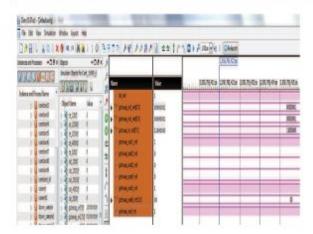


Figure. 13 Simulation result for image B defective

C. Synthesis results:

After the simulation of proposed system in Xilinx, Verilog code is synthesized in design vision compiler by using Synopsys tool to generate RTL Netlist. Area, power and timing analysis are performed. RTL Netlist generation is shown in Fig. 14 for the proposed system

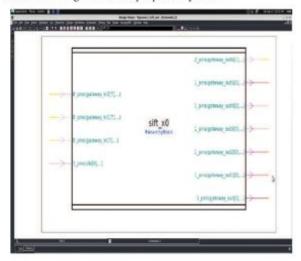


Figure. 14 RTL Netlist

Table I shows the area, timing and power report of the total system.

TABLE 1.

AREA, TIMING AND POWER REPORT OF THE CHIP

Parameter	Chip Results
Area	34727 m ²
Timing	8ps(clock period)
Power	12mw

D. Physical design results:

To integrate the whole system design into SoC physical design is performed to generate chip layout. In Fig. 15 shows the generated chip layout for the whole system.

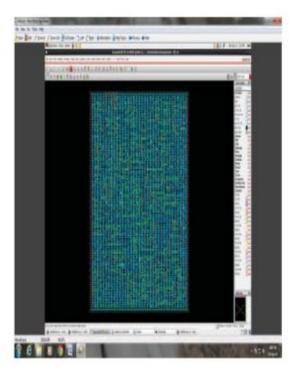


Figure. 15 Chip layout for the whole system design

VI. CONCLUSIONS

In this paper, the proposed system is designed in MATLAB using Xilinx System Generator for identification of quality of the objects for palletization process. Featurepoint extractions of the images are performed by taking 300x300 pixel size of input image and simulation results are performed in Xilinx. Then the whole system design is synthesized by Design vision compiler in Synopsys tool and RTL Netlist is generated. Physical design is performed for the proposed system to integrate into SoC in 90nm technology by using Cadence Encounter tool. Due to this proposed system the optimized area of 34727μm² and power of 12mw are obtained.

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Comparison of WT Based Speech Compression Techniques Using VC++

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Abstract: The main purpose of this paper is to compresses the speech signal using wavelet transform. Psychoacoustics is the scientific study of sound perception. From the psychoacoustic point of view, we have selected Wavelet analysis for the digital speech compression. Also Wavelet Transform eliminates the irrelevancies and redundancies present in the speech signal. The two popoular models of Wavelet Transform for speech compression are-Filter bank model and Lifting Scheme. Filter Bank model is also called Subband Filtering model. Both models decompose the speech signal into approximate and detailed components. But the lifting scheme is fast compared to the filtering model. We have tested some of the lifting scheme WT algorithms like Haar, Daubechies series, Cohen-Daubechies and Cohen-Daubechies-Feauveau bidirectionnel wavelet and have implemented them.

Keywords- Wavelet Transform, Psycoacoustics, Speech compression, Haar wavelet, Daubechies series, Cohen-Daubechies-Feauveau wavelets.

I. INTRODUCTION

The generation of human speech is very complicated. It involves lungs, vocal tracts and vocal folds. The message is formulated in the brain and is converted into an acoustic signal by vocal tract system. The vocal tract system is similar to the electronic parts like power supply, oscillator and resonator.[2] The structure of speech generation contains lungs, ribcage and abdominal muscles. Controlled airstream is produced between the vocal folds by this combination. From the lungs, the chest cavity expands and contracts to force air. By opening and closing of glottis the resistance of the air is changed. Finally a sound is produced from of the vibration of vocal cords.[2]

The human speech generation system is shown in Figure 1.

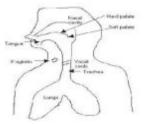


Figure 1 Generation of Human speech

The generation of human speech is analogous to the electronic circuit as shown in below figure.

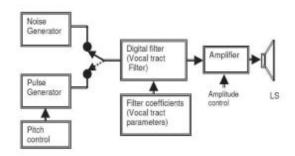


Figure 2 Electronic structure of speech generation

For efficient transmission and storage, we compress the signal. If the signal is uncompressed, it requires large memory. Consider the telephone level speech signal in the range of 300 Hz to 3400 Hz coded on at 8 bits per sample, and sampling rate of 8000 samples per second is defined as an uncompressed speech signal. [5]. This non-compressed signal requires storage capacity of 28.8Mbytes for one-hour duration and transmission rate of 64Kbps. The main idea of speech compression algorithm is to represent the non-compressed speech with less number of bits and optimum speech quality. Wavelets are used for the speech compression.

II. SPEECH COMPRESSION MODELS

With modern telecommunication, speech compression plays an important role. Speech compression is also speech coding. It is the process of indicating digital speech signal with a small number of bits with the normalized speech quality and low computational complexity. [1] Also these techniques will remove the unimportant components from the original speech.

The main requirements of the speech compression algorithms are

- High compression ratio- The compression ratio gives memory size and transmission rate required after compression.
- Low computational complexity- For real-time encoding and decoding, to minimize the power and delay coding, the computational complexity should be minimum.

- Limited storage requirements- Generally the speech coding algorithms use speech buffers between intermediate stages. So the size of the buffer is low.
- 4) Floating-point Multiplications- The algorithms require many numbers of floating-point multiplications. We can replace floating-point operations with integer operations.
- Immune to noise- Sometimes noise may distort the speech signal. Speech compression technique should control noise.
- 6) Minimum audible distortion-At a given bit rate, the speech compression algorithm will provide minimum audible distortion.

A .Waveform Coders

Waveform coders are used to represent the speech signal without underlying the speech model. They use scalar and vector quantization techniques to represent the samples of speech signal. [5] Robust than parametric coders but have the disadvantage of operated at higher data rates than vocoders.[3] Some of wave-coders are discussed below.

i) 64Kbps G.711 PCM, DPCM and DM

It uses scalar quantization model. It is simple, but costly in terms of data-rates. There are two types of PCMs-Uniform and Non-uniform. In uniform PCM, the step-size is fixed irrespective of input speech signal, whereas in non-uniform PCM, the step size is changed. If the speech is coded at 64Kbps using μ-law and A-law called 'uncompressed' standard (G7.11 standard). This format is used as a reference for different speech compression techniques.

In DPCM, the difference between original and estimated samples is quantized and transmitted. In DM, the error sample is given to the comparator. If error is positive, output of the comparator is positive pulse else if error is negative, output of the comparator is negative pulse. For data rates at and below 32Kbps, DM and DPCM have better performance than PCM.

ii) 32Kbps G.721 CCITT ADPC,

It also uses scalar quantization model. It provides better quality and less memory compared to original PCM.[7] The coding of speech is done for 4-bits per sample instead of 8bits per sample.

iii) Vector Quantizer

In this, the sample space is converted into symbol space with quantization error and low bit rate. This method is too difficult to implement, but is used in today's fast digital signal processors.

B. Sub-band and Transform Coders

The Sub-band coder is a waveform coder's method in f-domain. [8] At Txr, The speech is passed through an analysis filter bank and by down-sampling method; the bandwidth of each sub band of the input speech signal is reduced. At the Rxr, by up-sampling and synthesis filter bank, the original speech is retrieved. [9] The structure of the sub band coder is shown in figure 3.

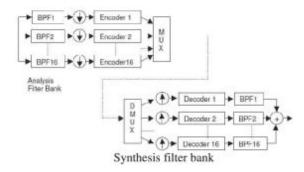


Figure 3 Sub band coder structure

Transform coder in other hand, a waveform coder in transform domain. At Txr, by using any of these transform techniques, DCT,DFT,WHT, WT, the speech signal is quantized and encoded.[4] At Rxr, it is decoded and inverse transformed. The structure of transforming coder is shown below.

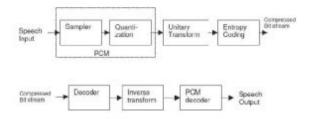
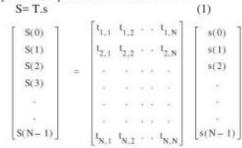


Figure 4 Transform coder structure

In this coder, the input is processed frame by frame and each frame is processed by 'transform' technique. If s is speech signal and N is frame length then S is speech after compression, represented in matrix form as



(2) Equation 2 is called analysis equation. And s= T⁻¹S is called synthesis equation.

III. WAVELET TRANSFORM

Wavelet is a mathematical function, used to represent data. Another definition is – wavelet is 'small wave' having its energy concentrated in the form of time. Any function can be represented in terms of wavelets similar to Fourier series. [1] It also provides time and frequency analysis simultaneously.

Let f(t) is real-time signal and Continuous Wavelet Transform of f(t) is given by

$$W(a,b) = \int_{-\infty}^{\infty} f(t)\psi *_{a,b}(t)dt$$
(3)

Where 'a' & 'b' are variables, $\phi_{a,b}(t)$ is wavelet function and is given by

$$\psi_{a,b} = \frac{1}{\sqrt{|a|}} \psi(\frac{t-b}{a})$$

(4)

The variable 'a' represents the amount of scaling or dilation of function and is also called dilation variable. [6] The variable 'b' represents a time shift or translation of the function and is also called translational variable.

The inverse wavelet transform is given by

$$f(t) = \frac{1}{|a|^2} \int_{-\infty}^{\infty} W(a,b) \psi(a,b) dadb$$

(5)

The block diagram of speech compression using wavelet is shown below. Firstly, the input is decompressed using wavelet transform and then small wavelets are removed by thresholding operator. [4] (Sometimes the small wavelets represent noise) The coefficients obtained after the thresholding are encoded. During the reconstruction, the compressed speech is decompressed using inverse wavelet transform.

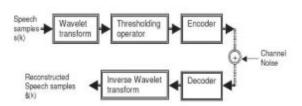


Figure 5 Wavelet Speech Compression Block Diagram

A. Lifting based Algorithms

We used some of the lifting based algorithms. Those are given by

1. Haar Wavelet algorithm

In this algorithm, initially the input samples are classified into two frames: Even and Odd frames. To get the A-coefficients, take average of even and odd samples and then to get the D-coefficients, subtract odd samples from even. This is explained in figure 6.

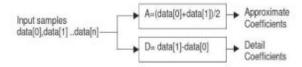


Figure 6 Haar Wavelet algorithm

Inverse transform is obtained by

$$data[0] = data[0] - data[1]/2$$

 $data[1] = data[1] + data[0]$ (6)

2. CDF Wavelet algorithm

It can be done with two methods- using lifting technique and using a filter bank technique. But lifting technique is faster than filter bank method. CDF wavelet is represented by CDF(n,ñ).where n represents primary wavelet's vanishing moments and n represents dual wavelet's vanishing moments.

CDF with lifting technique is explained in following figure 8.

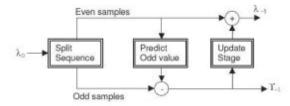


Figure 7 Steps in Lifting Technique

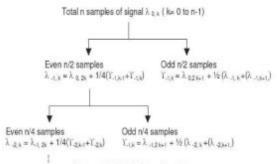


Figure 8 CDF Lifting Technique

Compared to Haar wavelet, CDF gives more compact representation of speech.

3. D-Wavelet algorithm

D stands for Daubechies. This algorithm provides a good smoothness and good support of compactness compared to the other algorithms. There are 4 stages of Lifting Daubechies-4.

a) Split stage:

 $\lambda_{-1,k} \leftarrow \lambda_{0,2k}$ (Even samples) and $\Upsilon_{-1,k} \leftarrow \lambda_{0,2k+1}$ (Odd samples)

b) Update stage:

$$\lambda_{-1,k} \leftarrow \lambda_{-1,k} + \sqrt{3}\Upsilon_{-1,k}$$
 (7)

c) Predict stage:

$$\Upsilon_{-1,k} \leftarrow \Upsilon_{-1,k} - \frac{\sqrt{3}}{4} \lambda_{-1, k} - \frac{\sqrt{3} - 2}{4} \lambda_{-1, k-1}$$
 (8)

d) Normalization stage:

$$\lambda_{\text{-1},k} \leftarrow \frac{\sqrt{3}-1}{\sqrt{2}} \ \lambda_{\text{-1},k} \quad \text{and} \quad \Upsilon_{\text{-1},k} \leftarrow \frac{\sqrt{3}+1}{\sqrt{2}} \Upsilon_{\text{-1},k} \tag{9}$$

IV. TEST SETUP FOR VC++

Microsoft Visual C++ is abbreviated as VC++ or MSVC is an Integrated Development Environment from Microsoft. It is proprietary software and used for C, C++ programming languages. It is used in speech processing, image and video processing.

Test set up is prepared in Visual C++ for speech compression using WT transform. This test setup provides following facilities for the analysis compared to Matlab.

- Selection of wavelet.
- · Playing speech file.
- · Select the speech file.
- · Selection of threshold value.
- · Selection of block length.
- Variation of threshold for lossy compression.
- · Displaying speech waveform.
- Displaying original file size, compressed file size and compression ratio.
- Also displaying the parameters like signal to noise ratio, mean square error, and root mean square error for comparison between original and reconstructed speech file.

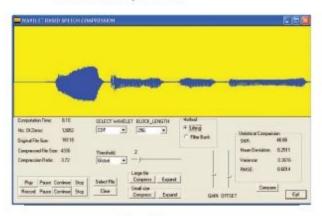


Figure 9 Test set up

V. RESULTS

We have implemented the wavelet compression techniques using vision C++ software. Here, we compare the compression ratio and quality of speech for various types of wavelet transform algorithms like Haar, CDF, cubic lifting method, Daub-4, Daub-8, Daub-16. We have also measured the statistical parameters of speech quality. They are-MSE, RMSE, SNR, and mean deviation.

For the Haar transform, the compression ratio and speech quality is shown in the following figure. Simple algorithm and compression ratio of 3.31 is achieved.

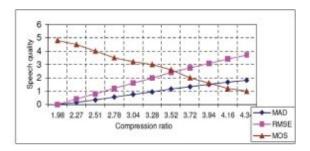


Figure 10 Compression ratio vs speech quality for Haar

For the CDF transform, the compression ratio and speech quality is shown in figure below. Compression ratio of 4.5 is achieved. [10] If the threshold value is increased, we can't reconstruct the original speech signal.

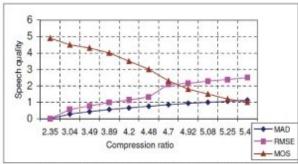


Figure 11 Compression ratio vs Speech quality for CDF

For cubic prediction lifting method, the compression ratio and speech quality is shown below. Here we achieve the compression ratio of 5.34.Compared to the above two algorithms, this algorithm got the loss-less compression.

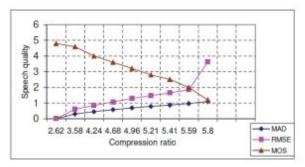


Figure 12 Compression ratio vs Speech quality for Cubic prediction

For Daub-4 wavelet algorithm, compression ratio and speech quality is given below. The compression ratio of 3.9 is achieved.

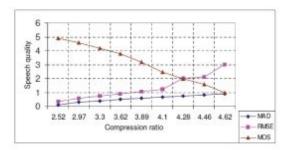


Figure 13 Compression ratio vs Speech quality for Daub-4

For the Daub-8 wavelet algorithm, compression ratio and speech quality is given below. The compression ratio of 4.2 is achieved.

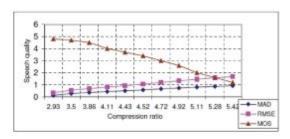


Figure 14 Compression ratio vs Speech quality for Daub-8

For Daub-16, compression ratio of 4.61 is achieved. Compression ratio and speech quality of this wavelet is given by

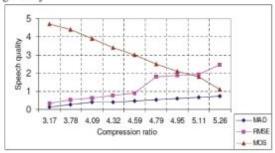


Figure 15 Compression ratio vs Speech quality for Daub-16

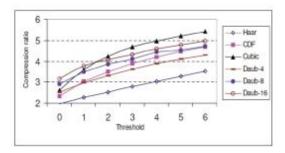


Figure 16 Compression ratio of various wavelet algorithms

Compression ratios of different wavelet algorithms like Haar, CDF, Cubic, Daub-4, 8, and 16 are compared in the figure above.

VI. CONCLUSIONS

It is concluded that wavelet based algorithms are the best for speech compression. We tested and implemented some of the lifting scheme algorithms like Haar, CDF and Daub algorithms. They gave best compression ratio and low computational complexity. The frame size of each wavelet is considered as 256 bytes. VC++ software is used. It selects the wavelet, plays the speech file, then applies threshold and finally displays the output speech waveform with parameters like SNR, MAD, MSE, and RMSE. The lifting scheme of wavelet transform is very good from the point of view of computational complexity and loss-less compression. Some algorithms gave lossy-compression and some gave loss-less compression.

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User level Static and Dynamic Core assignment in Multi-core System

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Abstract: There has always been a debate over the advantages of multi-core architecture over single core. It is obvious that the full advantage of multi-core can be achieved only if the programs are run in parallel [Amdahl's law] and the load is distributed evenly among all the available cores. In this context, processor or CPU affinity plays a major role in improving the performance of the system where time constraints are present. But, hard CPU affinity can also degrade the performance of the system in some scenarios. The alternative is to dynamically allocate the CPU core at application level. This paper studies these two techniques at application level to assign a particular CPU core once and stick to it, or switching among various cores dynamically by considering CPU usage.

Index Terms—multi-core, CPU affinity, static scheduling, dynamic load balancing, CPU utilization

I. INTRODUCTION

To enhance the performance of an embedded system, multi-core architecture [7,10] is one of the possible solutions which allows the system to process numerous jobs simultaneously by parallel computation. At the same time the return on the investment has been a debating issue. As Amdahl proved that just by increasing the number of cores, the processing power can't be multiplied arithmetically, [1] but it depends on various factors like program parallelization. Even considering all favorable conditions for Kernel scheduling for multi-core few more factors affect the performance of the system.

Linux kernel has been giving significant importance to multiprocessor architecture [4,9,13,15]. Modern operating systems provide multi-core aware infrastructure [19], interrupt load-balancer, affinity facilities [3], CPUSETS [6], and CPU isolation [5]. These functions help running tasks adapt to system characteristics including SMP scheduler, synchronization very well by considering CPU utilization. Still there is enough scope to improve the performance of the system by providing user level control to decide a particular process to be run on a pre-defined CPU core.

'CPU or processor affinity' increases the performance of the system by assigning the process to one particular core, that avoids cache miss [17,18]. Processor affinity takes advantage of the fact that some remnants of a process that was run on a given processor may remain in that processor's memory state (for example, data in the CPU cache) after another process is run on that CPU. Scheduling that process to execute on the same processor could result in an efficient use of process by reducing performance-degrading situations such as cache misses [15]. This approach would be useful, if the application has multiple-instances and is non-threaded, such as some graphics-rendering software.

In some applications (particularly Real-Time control applications) [2], it may be desirable to specifically assign a task to its own dedicated core. For example, a time critical task such as a control loop can be implemented in this manner.[14] This allows the remaining tasks in the system to share the other processor resources among themselves—and ensures that nothing interferes with the time critical process.

On the other hand, there are limitations with CPU affinity. Most importantly, CPU affinity wastes the CPU usage if the task goes in to wait or sleep mode. This degrades the performance of the system, as once the core has been assigned, the process can't run after a wait or sleep unless the assigned core is free.

Load balancing on the cores is an alternative to achieve better performance. Utilization of a processor is usually considered as the criterion in load balance [8]. To generate the maximum balanced load, tasks should be assigned to the processor core with the lowest utilization [12]. Beyond OS schedulers that try to balance the load,[16] it is advantageous to provide monitoring and CPU switching at user level, using system calls within a program. On a Linux platform, a program in C can achieve this.

II. METHODOLOGY

This paper is based on literature available as mentioned in the references, as well experimental study on systems running with Linux operating system. Implementation of static (CPU affinity) and dynamic process allocation to a CPU core is done using qTcreator GUI and C language in Linux environment. To give reasonable understanding to the user, pseudo code is provided, where the original programs are tried and tested. The examples cited are to demonstrate the successful running of programs and to prove the concept. In the real world scenario, the context and applications may vary widely, thus differ in results.

III. IMPLEMENTATION

A. Static Core Assignment

Static or off line scheduling to achieve process affinity[11]:

A process can be given affinity [18] to a particular CPU core as per the user choice. This can be controlled by a GUI built using qtCreator, which in turn runs the kernel level commands to assign the affinity to a particular process, as shown in fig 1. Any number of processes can be listed in the drop down list of the application, and the n numbers of cores are given as buttons. Whenever the user selects a particular process from the drop down list and assigns to a particular core, the process is assigned to that core. System calls 'system' and 'taskset' are used to achieve processor or CPU affinity.



Figure 1 quad core with process

Pseudo code for task affinity on multi-core:

- create four core options as four buttons;
- · create 'process' options as dropdown menu items;
- read 'process' choice from dropdown menu into "process name";
- · read the 'core selection' from button;
- assign task on core 'n' using system call: system ("taskset n+1 "process name" &");
- · 'process' runs on core 'n'
- update the label on button with "process name"

B. Dynamic Core Assignment

Load balancing on a multi-core system can be achieved by continually monitoring the loads on various CPU cores and assign the desired program to the least loaded core. The proc file system is a pseudo-file system which provides an interface to kernel data structures. It is commonly mounted at /proc. Most of it is read-only, but some files allow kernel variables to be changed. The PID of the desired process is read from process status file of the kernel by tracing the name of the process. With this, the desired process can be fetched. The same way the load on each CPU core at current state is read from the kernel data structures and identified the least loaded core. After these two steps, the desired process can be assigned to the least loaded core using the PID of the process and appropriate affinity mask in the 'taskset' system call.

Proc/stat file contains the CPU usage statistics in ASCII file format. The same can be read into the program and decode the fields to identify the total CPU usage and idle time, and also for all the existing cores. Each core details are given in each line in the file.

In a quad core system, the load balancing program runs on core 0, while monitoring and assigning the loads to cores 1, 2 and 3. This has been implemented through an algorithm as given here. Simplified load balancing algorithm.

//check the process pid of process name from PID list through/proc

- process_pid = get_pid("process name");
- read file proc/stat;
- · read each field using the file pointer;
- · while cpu count is less than 5
- · read CPU usage for each core
- store the values of CPU core usage data
- increment count until it reaches number of cores
- CPUx usage = time lapsed between reads CPUx idle time
- compare the loads to find the least loaded core
- assign the process to this core using taskset -p lowest_load, "process pid"



Figure 2 comparison of CPU usage

With this, as shown in figure 2 the load balancing scheduler monitors the load on various CPU cores continually, and assigns the desired process with its process ID to the least loaded core. This ensures that the desired process can be run continuously without waiting for the CPU.

IV. OUTPUT

A. Static Core Assignment

GUI program is run on the system. Browser, camera, and media player have been given in the drop down list of the program. Four buttons were provided to select any core among 0 to 3. Once Browser was selected and is assigned to core 1, the browser was switched and continually run on core 1. The same was checked using top kernel command from terminal application. Similarly core 0 was assigned to Camera application. The buttons were also updated with their number along with the assigned application. The glitch in the video streaming disappeared after the camera application had the affinity with core 0. Hence it is proven that applications which are non-threaded run better with CPU affinity.



Figure 3 Static core Assignment

Figure 3 shows output of Static core assignment of processes. It shows browser process is running on core 1.

B. Dynamic Core Assignment

The main program was compiled using gcc along with other source files. Camera application, 'cheese' was taken as the program that should be assigned dynamically to the least loaded core. The cheese program was launched, and then the load balancer program 'task_switch' was also launched in another terminal. The 'task_switch' program started displaying the loads of various cores, and identified the least loaded core. Camera application was assigned to the least loaded core by changing the affinity mask, which could be either 2, 4, or 8 for core 1, 2, or 3 respectively.

The period of monitoring has been taken as three seconds, and for every three seconds the terminal window was updated with current load values of all cores, and affinity mask was also updated accordingly. The same was checked using top command running on another terminal. The screen shots of the same were given below in figure 4. All the cores were used efficiently with fine load balancing.

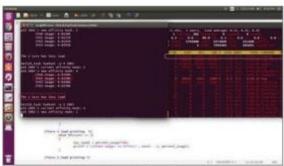


Figure 4 Dynamic Core Assignment

V. CONCLUSIONS

This paper tried to touch couple of enormous possibilities to achieve optimal performance of a system, beyond OS kernel level scheduling. Also demonstrated that the programs at application level may be used to enhance efficiency of scheduling further using various monitoring techniques and assignment methods. Further, considering static and dynamic core assignments, to get the best of the both worlds, an algorithm can be developed to mix them,

and achieve in a single program, giving the user the control to run the program.

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A Survey on Computational Intelligence Applications in Software Engineering and its Data

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Abstract: Ubiquitous software has become an indispensable technology for science, engineering, and business. Software is everywhere, as a standalone system, or part of a new technology, or as a service in the cloud. Hence, it has paramount importance. As size and complexity of software systems are increasing, software engineering problems such as software effort estimation, software testing, software defect prediction, software project scheduling, software reliability maximization, software module clustering, and software maintenance have become more difficult to handle. In order to reduce the high cost of performing software engineering activities and to increase software quality and reliability, computational intelligence techniques are being used for problem solving using research oriented approaches and for decision-support. Computational intelligence has been used in different fields for a long time. There has been a recent surge in interest in the application of computational intelligence techniques in software engineering. Search based software engineering and machine learning for software engineering are the areas of computational intelligence research which have been showing promising results in this context. Search based software engineering reformulates software engineering problems as optimisation problems, and then using optimisation algorithms problems are solved. Software engineering produces lot of data related to software, like effort estimates, source code, test cases, data on bugs and fixes, version data, and metrics data. As part of analytics on software data, machine learning techniques are used to solve some software engineering problems and for effective decision making. The objective of this survey paper is to identify software engineering problems and applications of computational intelligence techniques to solve those problems. In survey, computational intelligence applications for solving different software engineering problems are identified and presented. In this paper, some research questions which indicate research directions and some possible research topics are presented. New research issues and challenges posed by the hard problems in software engineering could stimulate further development of new theories and algorithms in computational intelligence.

Index Terms - Computational Intelligence, Software Engineering Problems, Search Based Software Engineering, Optimisation Techniques, Machine Learning, Software Data Analytics.

I. INTRODUCTION

As size and complexity of software systems are increasing, software engineering problems have become more difficult to handle. In order to increase software reliability and to reduce the high cost of performing

software engineering tasks, computational intelligence techniques and algorithms are being used as problem solving, decision-support, and research approaches. As per the definition in [1], "Computational intelligence is the study of adaptive mechanisms to enable or facilitate intelligent behavior in complex and changing intelligence environments. As such, computational neural networks, combines artificial computing, swarm intelligence and fuzzy systems". Software sizes are becoming bigger. The complexity of software is increasing with size non-linearly, and in addition, software complexity further increasing as it is changing very rapidly to keep pace with changing user business dynamics and needs. Increased software complexity poses many problems. Computational intelligence is the appropriate vehicle to address software problems. In this paper, two areas of computational intelligence which are showing promising results in software engineering are considered for review. They are: 1) "Search-Based Software Engineering" (SBSE). 2) Machine Learning for Software Engineering. "Search-Based Software Engineering (SBSE)" [5] reformulates software engineering problems as optimisation problems. These reformulated problems are solved using optimisation algorithms. Some of the software engineering problems which can be reformulated as optimization problems are; 1) software project scheduling with an aim to minimize cost and time of completion of different tasks, 2) test case design with an aim to maximize code coverage and bug detection, 3) test case design with an aim to minimize testing effort and maximize bug detection, 4) during starting of an iteration in WinWin spiral model identifying set of requirements maximizing user satisfaction and probability of completion in given time and cost. Similarly, many more problems with different optimization criteria can be reformulated as optimization problems. Some of the search based optimisation techniques which are being used are: 1) Genetic programming 2) Genetic algorithms 3) Ant colonies 4) Particle swarm optimization 5) Hill climbing 6)

As per the definition in [2], "machine learning deals with the issue of how to build programs that improve their performance at some task through experience". Software systems process data, but software is data too [3]. Software engineering activities and different stake holders produce lot of data related to software. Machine learning makes use of software data to create machine learning models to solve software engineering problems. Some of the software

engineering problems which can be addressed by machine learning models are; 1) predicting effort for the next project based on machine learning model, which is created using the data from previous completed projects, 2) predicting project duration for the next project based on machine learning model, which is created using the data from previous completed projects, 3) software defect prediction can be made using the defect prediction models created using previous versions of software.

Major types of machine learning include; decision trees, concept learning, artificial neural networks, reinforcement learning, Bayesian belief networks, genetic programming and genetic algorithms, instance-based learning, and analytical learning.

Some problems can be viewed either as optimization or machine learning problem. For example, test case design can be viewed as an optimization or machine learning problem. That is where research comes into picture to figure out which approach and technique is better.

The aim of this paper is to carry out basic survey (not exhaustive survey) to find research openings in the context of application of computational intelligence techniques in software engineering.

II. SOFTWARE ENGINEERING PROBLEMS AND SOFTWARE DATA

An iteration in a software development model consists following activities (phases):

- Software requirements collection, specification and planning phase, 2. Design phase
- 3. Implementation and testing phase

The maintenance activity takes place in parallel with development. While next version is under development previous deployed versions will be under maintenance. Some problems which are encountered frequently are identified and listed out in this paper. Some of the problems which are encountered during software engineering are identified by different authors in [3], [4], [5], [6]. [7], [8], [9], [10], [11]. They are categorized and listed below:

A. Software Engineering Problems

- Software requirements collection, specification and planning phase:
 - · Eliciting, recording of all functions and constraints
 - Ambiguity, completeness, conflicts in requirements, prototyping, requirements tracing
 - · Cost and time estimation for the project
 - Tasks, dependencies, duration, resources for the project

2. Design phase:

- High-level (architectural) architectural design problems, modularity, coupling
- Low-level (detailed) algorithms selection, complexity of modules, cohesion
- Design alternatives, inconsistencies in software design

- 3. Implementation and testing phase:
 - · Software reuse
 - · Source code searching
 - · Integration method, defect prediction
 - · Test case generation, test case prioritization
 - · Prediction of test effectiveness
 - · Bug management/triage, debugging

4 .Maintenance phase:

- · Software understanding and comprehension
- · Impact analysis, ripple effects during changes
- · Regression testing
- · Automatic software repair, quality enhancement
- Reengineering legacy software, software module clustering

5. Problems related to umbrella activities:

- · Configuration management
- · Prediction of software quality and reliability
- · Classification of software components

B. Software Data

Lot of data are generated during software development and maintenance. Over the time from different projects the data populate databases in the range of terabytes and more. Data related to software are listed below.

- · Source code, data on versions, code analysis data
- · Test cases designed, test execution data
- Data on bugs and fixes
- Metrics data on size, design, code, testing, project, process, and maintenance
- · Cost and schedule data
- · Usage and run time data of deployed software
- · User feed back

III. COMPUTATIONAL INTELLIGENCE TECHNIQUES TO SOLVE SOFTWARE ENGINEERING PROBLEMS

In this section computational intelligence techniques which are applied to software engineering problems are surveyed and presented. The survey is not exhaustive. This survey gives basis for further refinement in the subsequent work.

A. Solving Software Engineering Problems with Optimization Techniques (SBSE)

"Search based software engineering" reformulates software engineering problems as optimization problems. The problems and optimization techniques are discussed in detail in [4],[5],[8],[9],[12]. The optimization techniques are used by different researchers in solving different software engineering problems. Simulated annealing approach is used in solving many problems like improving software quality prediction[13], next release problem [14], finding[15]. Genetic programming program flaw applications can be found in software cost predictive modeling [16], in reliability modeling[17], and in model for quality enhancement[18]. Software release planning [19] and software test data generation [20] are solved by genetic algorithms. Hill climbing technique is used to improve program structure by module clustering [21]. Hill climbing technique and genetic algorithm are

applied for regression test case prioritization [22]. Software modularization using hill climbing, simulated annealing, and genetic algorithm is presented in [23],[24]. "Search based software engineering techniques" use metrics as fitness functions in one form or the other [25]. Proposing new metrics for using in optimization techniques is also an important research area. There is little work on the combinations of search algorithms [26]. Research on exploring the potential of combinations of search algorithms has lot of scope. Bug detection using particle swarm optimization is given in [27]. Ant colony optimization techniques [28] and particle swarm optimization [29] techniques have potential to be used in solving software engineering problems and have not been used much in the literature. In addition to the papers listed out in this section, interested researcher on SBSE can look into the repository of papers on SBSE maintained by Y.Zhang [49].

B. Solving Software Engineering Problems with Machine Learning Techniques

Application of machine learning in the context of software engineering are discussed in [6], [7], [10], [11]. Solutions to different software engineering problems using machine learning techniques are attempted by many researchers. Instance based learning is used in component retrieval and reuse [6] and software project effort estimation [30]. Genetic programming is applied for understanding and validating user software requirements [31]. One of the supervised learning methods, "concept learning", is used to derive functional requirements from legacy software [6]. To predict effort required for software development, artificial neural networks & decision trees [32], bayesian analysis [33], artificial neural networks & naïve bayes classifier [34], and artificial neural networks [35] are applied and results are presented. For predicting software defects bayesian belief networks have found applications [36], [37], [6]. Detecting bad aspects of code and design are important. Because, it enables refactoring, to improve quality of code and design. Bayesian approach is used in detecting design and code smells [38]. Overview on techniques based on machine learning used for software engineering is given in [39]. Even though there is active research happening in machine learning applications in software engineering, more research is possible as machine learning has the potential [40].

IV. DISCUSSION AND RESEARCH DIRECTIONS ON COMPUTATIONAL INTELLIGENCE APPLICATIONS IN SOFTWARE ENGINEERING

Standalone software, distributed software, or software as a service in the cloud need to be designed, coded, and tested before deployment. As part of evolution and maintenance (corrective, perfective, adaptive, and preventive) software is changed. During change software is not available for use. Change is applicable to all the above mentioned types of software. The computational intelligence techniques and research directions presented in

this paper are applicable to standalone, distributed and cloud software as service.

The application of computational intelligence techniques in software engineering started more recently. Diversity, size and complexity of software systems are increasing. In addition, due to frequent changes to software systems to keep pace with changing user business requirements and personal needs, the software systems are getting deteriorated and becoming complex. Due to this scenario, the earlier easily solvable software engineering problems have now become more challenging. To address software engineering problems, researchers started exploring the application of computational intelligence techniques. Survey indicates results are encouraging and there is lot of potential in further research in this area. Computational intelligence techniques are grouped under two headings. They are; optimization techniques and machine learning techniques. Optimization techniques and machine learning techniques are listed in introduction section. Some techniques are used as optimization and machine learning techniques. Similarly, some problems can be viewed either as optimization or machine learning problem. For example, project estimates can be viewed as an optimization or machine learning problem. That is where research comes into picture to figure out which approach and technique is better. Some problems which are encountered frequently are identified and listed out in this

A. Research Directions in Software Data Analytics

There are many research questions that need to be addressed related to software data analytics. These questions indicate the scope for research work in those lines. Some of them are listed below.

- What data and how to analyse the data to address a particular software engineering problem?
- How to integrate heterogeneous data? Much of the software data is unstructured, while some data is stored in structured format [3].
- Which algorithm is better for data analysis? Do we need to design a new algorithm for a particular situation?
- How to customize existing algorithms to suite to the data, problem and situation?

B. Some of the More Specific Possible Research Topics in the Category of Software Data Analytics

- Project cost and time estimation. Design and use of hybrid models to predict estimates.
- Building machine learning models using metrics data and predict the defects and design quality for the software that is going to be deployed. Prediction will help to know whether further testing is required or not.
- Building machine learning models using source code and source code analysis data to design test cases and prioritizing test cases.
- Building machine learning models using source code and source code analysis data for automatic bug repair.

- Building machine learning models using coupling data to predict regression testing effort. Prediction will help to make decision whether change can be implemented or it has to be deferred.
- Building machine learning models for software testing [40].
- Building machine learning models using bug data for defect prediction.
- Building machine learning models using version data to predict software maturity index.

Research on software data analytics requires software data. But, from where to get the data. There are some options available. They are:

- Use software data from reliable public domain sites contributed by research groups.
 Example: http://promisedata.org/repository [41] and other repositories [42].
- Lot of software data are available from the sites of standard open source tools.
 - Example: Software data on different plug-ins to eclipse
- Data published in research papers and text books.
 Example: COCOMO database containing 63 projects published in Boehm's text book [43].
- Create small programs with problems and parameters related to your research interest. Research findings based on small size programs need to be justified that results are in fact applicable to bigger size programs (scalability).
- 5) Use synthetic data. Synthetic data are "any production data applicable to a given situation that are not obtained by direct measurement" according to the McGraw-Hill Dictionary of Scientific and Technical Terms. Synthetic data are generated to meet specific needs or certain conditions. This can be useful when designing any type of technique, algorithm, or a method, because the synthetic data are used as a simulation or as a theoretical value, situation, etc.

C. Research Directions in the Application of Optimization Techniques

There are many research questions that need to be addressed related to solving software problems using optimization techniques ("Search Based Software Engineering"). These questions indicate the scope for research work in those lines. Some of them are listed below.

- What are the benefits of solving a software engineering problem using optimization techniques?
 Can the benefits be quantified? For example: Test case design to maximize code coverage. It should be quantified to indicate how much extra code coverage is achieved by using optimization techniques over traditional techniques.
- For a particular optimization criterion or criteria which algorithms perform better? Why?
- · Can we customize the algorithms for better results?

- Can we propose new metrics which can be input for existing optimization techniques for solving a problem? How these metrics are different?
- Can we create an hybrid algorithm (from existing algorithms)? But, why?
- Can we identify a new problem to which existing optimization techniques can be applied?
- In solving a problem, use of optimization techniques versus machine learning models (Software data analytics). Why the results are not same? Justify.

D. Some of the More Specific Possible Research Topics in the Category of Application of Optimization Techniques in Software Engineering

- Modular design (clustering) with an aim to reduce change propagation due to ripple effects during maintenance and regression testing.
- Modular design with an aim to maximize cohesion and minimize coupling. Application of search based optimization techniques in design can be found in [44].
- Refactoring software design during an iteration in a sprint of scrum agile process model with an aim to reduce coupling and to increase cohesion. Refactoring using SBSE is presented in [45].
- Test case design for scrum agile process with an aim to reduce testing time.
- Test case design with an aim to maximize code coverage and bug detection.
- Test case design with an aim to maximize bug detection and minimize testing effort. Some work on test case design is given in [46].
- Prioritising the test cases with an aim to reduce testing effort with same bug coverage. Recent work on prioritizing test cases can be found in [47].
- Test case design to detect critical defects [48].
- Debugging with an aim to minimize the time to locate the cause for the bug. Code, cohesion and coupling metrics can be used for this purpose.
- Reengineer the software with an aim to minimize coupling and maximize cohesion.
- Version management with an aim to minimize redundancy and retrieval time of a required component.
- During reuse, aiming to identify and retrieve most appropriate component for a given situation.
- 13) Model based testing with an aim to maximize the likelihood of early detection of defects and estimation of software testing effort.

For carrying out research using optimization techniques in software engineering requires software (program) as input. This program can be developed for research purpose or any free open source tool can be downloaded.

Computational Intelligence initial subjects of interest are; fuzzy systems, neural networks, evolutionary computation, and swarm intelligence. But, different authors of research papers treat computational intelligence as an umbrella, under which more and more algorithms, techniques, and methods are slowly added, as advancement is taking place as part of basic research and applied

research. That is how computational intelligence subjects of interest have grown.

V. CONCLUSIONS

The software engineering problems which can be addressed by computational intelligence are identified from different publications. Some of them are: software effort estimation, software testing, software defect prediction, software project scheduling, software reliability maximization, software module clustering, and software maintenance. Different computational intelligence techniques which can be used to solve some of the software engineering problems are surveyed and given. As size and complexity of software systems are increasing, software engineering problems have become more difficult to handle. In this context, based on the survey, it is found that computational intelligence techniques which include optimization techniques and software data analytics play a significant role in solving software engineering problems and developing high quality software products with low maintenance cost. Based on the survey, some research questions and research topics related to software data analytics and application of optimization techniques to software engineering problems are identified and presented. Research topics indicate computational intelligence in software engineering and its data has tremendous scope for aspiring researchers.

Detailed research directions for software in the cloud will be presented in future work. Some of the research directions in this context are; virtualization, multi-tenant modeling, testing as a service (TaaS), design of cloud services user interface, design of cloud computing metrics, performance testing of SaaS, security testing of SaaS, and architectures for dynamic scalability.

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Dynamic load balancing in cloud using extended hungarian method

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Abstract: Cloud Computing is a type of service based computing or utility computing. Our objective is to develop an effective load balancing algorithm using hungarian method to minimize response time and to increase the resource utilization. Load balancing in cloud need to consider the allocation of virtual machine and scheduling tasks on the virtual machine depending on various client and application given objectives. Hungarian method is a kind of assignment problem which works efficiently for static assignments. We are extending hungarian algorithm to work efficiently in dynamic environment like cloud. The availability status and load on each virtual machine are to be updated periodically and assigning tasks dynamically.

Index Terms-- cloud computing, load balancing, tasks, virtual machine(VM),hungarian method.

I. INTRODUCTION

A Cloud can be considered as an enormous collection of resources. Cloud computing is providing easy accessibility for required services and users can also deploy applications at competitive costs. Large data centers provide services through various cloud platforms. Cloud computing provides services at infrastructure level are called as infrastructure as a service.

The cloud service provider (CSP) makes on demand provisioning of hardware like processing power, I/O, large amounts of storage etc. Users accesses the services of cloud through a virtual machine, where number of virtual machines share a single physical server. Cloud computing provides a service oriented platform for cloud users.

The following cloud architecture is a three tier architecture where the number of clients are conneted to the data center(DBServer). Here the data center is the collection of host machines. The clients are sending their requests through client machines or virtual machines. The estimated cost to process the requests depends on the processing power of the data center and how the requests are scheduled so that the load on each virtual machine is distributed evenly to avoid delay and improve throughput.

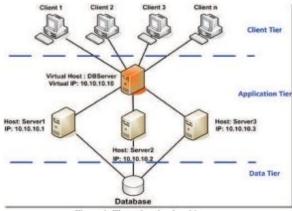


Figure 1. Three tier cloud architecture

A. Load balancing in cloud

The load balancing in cloud computing is dynamic i.e cloud cannot rely on the prior knowledge whereas it takes into account run-time statistics. It is complex to maintain the stability of processing so many jobs in the cloud computing environment. The cloud provider installs heterogeneous resources. The resources are flexible to users in dynamic environment. In this scenario the requirements of the users are granted flexibility (i.e. they may change at run-time). Algorithm proposed to achieve load balancing in dynamic environment can easily adapt to run time changes in load. Dynamic environment is difficult to be simulated but is highly adaptable with cloud computing environment.

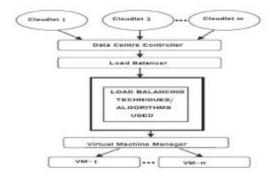


Figure 2. load balancing in cloud

Figure 2 shows the load balancing in cloud where the load balancer schedules tasks(cloudlets) to the corresponding virtual machines(VM-1...VM-n) using the appropriate algorithm such that the cost of the processing

should be minimized and servicing the number of users should be maximized. Here the virtual machine manager is responsible to allocate and monitor the virtual machines. Data center controller is processing the tasks(cloudlets) using the load balancer algorithm. In designing this paper the optimum load balancing algorithm to minimize the cost is discussed.

II. RELATED WORK

A. Cloud Service Scheduling

Scheduling of cloud services can be categorized at user level and system level. User level scheduling deals with problems raised by service provision between providers and customers. The system level scheduling handles resource management within data center. Data center consists of many physical machines. Millions of tasks from users are received and assignment of these tasks to physical machine is done at data center. This assignment or scheduling significantly impacts the performance of cloud. In addition to system utilization, other requirements like QoS, SLA, resource sharing, fault tolerance, reliability, real time satisfaction etc, should be taken into consideration.

B. User Level Scheduling

Market-based and auction-based schedulers are suitable for regulating the supply and demand of cloud resources. Market based resource allocation is effective in cloud computing environment where resources are virtualized and delivered to user as a service. Service provisioning in Clouds is based on Service Level Agreements (SLA). SLA represents a contract signed between the customer and the service provider stating the terms of the agreement including non-functional requirements of the service specified as Quality of Service (QoS), obligations, and penalties in case of agreement violations. Thus there is a need for scheduling strategies considering multiple SLA parameters and efficient allocation of resources. The focus of model is to provide fair deal to the users and consumers, enhanced quality of service as well as generation of optimal revenue.

C. System Level Scheduling

System level scheduling is scheduling virtual machines to the corresponding physical machines. While scheduling virtual machines, the scheduler needs to consider the capacity of each physical machine and some threshold value must be chosen for each physical machine depending on the capacity. The load of each physical machine must be updated for every assignment and when the load reaches the threshold value, The migration or transfer of virtual machines must take place. The transfer may be static or dynamic. Static transfer considers the transfer of volume only where as dynamic transfer has to consider the state of virtual machine along with volume. Downtime of virtual machine is important to be considered to improve the performance of cloud. Dynamic transfer is complex to

implement with no or less downtime but static transfer have more downtime. This needs to be considered in server scheduling.

III. MATHEMATICAL MODEL

A. Hungarian Method

The Hungarian method is a combinatorial optimization algorithm which was developed and published by Harold Kuhn in 1955. This method was originally invented for the best assignment of a set of persons to a set of jobs. It is a special case of the transportation problem. The algorithm finds an optimal assignment for a given "n x n" cost matrix. Assignment problems deal with the question how to assign n items (e.g., jobs) to n machines (or workers) in the best possible way [...]. Mathematically an assignment is nothing but a bijective mapping of a finite set into itself [...]"

The Hungarian algorithm can also be used for a maximization problem in which case we first have to transform the matrix. For example a company wants to assign different workers to different machines. Each worker is more or less efficient with each machine. The efficiency can be defined as profit. Higher the number, is higher the profit.

For Solving the assignment problem create one table based on the value of data, we call it as cost matrix. With the determined optimal solution we can compute the maximal profit.

- Worker1 => Machine2 9
- Worker2 => Machine4 11
- Worker3 => Machine3 13
- Worker4 => Machine1 7

Steps

- Find the minimum from each row and subtract the minimum from all the rows.
- Find the minimum from each row and subtract the minimum from all the rows.
- 3. Assign one zero ("0") to each row and column.
- 3. Cover all zeros with a minimum number of lines.
- 4. Create additional zeros if required.
- 5. Map all zeroes then this will give the minimum cost.

Existing work was using balanced assignment i.e the assignment was square matrix, the number of sources and destinations are equal. This type of assignment problems can be considered as balanced assignment. This can be represented as a square matrix, but in cloud environment this may not work as the cloud is servicing number of requests with minimum resources compared to the requests.

The following table gives the general Hungarian assignment, where number of tasks(souces) are equal to the virtual machines(destinations) so that this can be represented as a square matrix. The servicing time is represented as the cost matrix.

B. Hungarian Method for load balancing in cloud

Load balancing problem can be represented as a two dimensional cost matrix. Resources are represented in a column and tasks who need resources are represent in a row.

The hungarian method can be used for assignment of tasks to virtual machines. Based on the virtual machine's current load and capacity the tasks are to be assigned to the corresponding virtual machines dynamically. Whenever the cost matrix of an assignment problem is not a square matrix, that is, whenever the number of sources is not equal to the number of destinations, the assignment problem is called an unbalanced assignment problem. In such problems, dummy rows (or columns) are added in the matrix so as to complete it to form a square matrix. The dummy rows or columns will contain all costs elements as zeroes.

Periodically checking the availability and load on each virtual machine by a load balancing algorithm then assigns the tasks to the corresponding virtual machine if its capacity is more than the required capacity to process the request and its availability status is free.

repeat {

Step 1: Initialize the capacity(VC[i]) of each virtual machine(VM).

VC[i] = VM Capacity in MIPS

Step 2 : Initialize the Length of each Task TL[j] = Length of Request in MI

Step 3: Initialize the availability status of each VM=available, Vm_a[i]=available

Step 4: Find Execution Time for each Request to VM if VM_a[i]=available

Ex_Time[i][j]= TL[j]/VC[i] Seconds

Step 5 : Construct Expected Cost Matrix ECM[V,R]

Step 6: Find out Minimum Execution Time from each row and subtract it from entire row.

Step 7: Find out Minimum Execution Time from each column and subtract it from entire column.

Step 8 : Cover all zeroes with minimum number of lines.
If , No.of zero = number of resources then go to step 9,
Else, go to step 8.

Step 9: Find minimum value which is not covered by any row and column and Subtract it from uncovered row and add it from value which is twice covered by line.

Step 10: This matrix and original matrix are to be compared and choose best resources(VM) for the assignment of tasks and update the assignment status of VM as busy.

} until there is no job left unassigned

Step 11: The above process should be repeated infinitely.

As the cloud is providing service based computing for n number of users for all the time until there is no resource available, but ideally the resource must be available all the time as the cloud is a collection of enormous pool of resources as per definition. And once after the request is serviced again the availability status of the virtual machine must be updated to be available, so the load balancer algorithm should update the availability status and load on each resource (virtual macine) periodically.

IV. IMPLEMENTATION AND RESULTS

When we apply the above algorithm on the test data it shows the following results.

Steps 1&2: According to the considered capacities and task lengths, the following assignments were taken

VM capacity (MIPS)	Task Length(MI)
120	9000
150	8000
180	6000
200	5000

Steps 3&4: According to the estimated execution times calculated on the corresponding virtual machines, The following Execution time matrix is formed. Here there are four tasks and three vms, so it is an unbalanced assignment

Task/VM	Task1	Task2	Task3	Task4
VM1	30	40	50	40
VM2	40	30	25	30
VM3	40	35	45	40

Step 5: Add a dummy row as the number of resources(VMs) are less than the number of Tasks to be processed

Step 6 Now Apply Hungarian for finding optimum assignment, subtract min cost value from each row.

Task/VM	Task1	Task2	Task3	Task4
VM1	0	12	6	16
VM2	15	5	0	8
VM3	0	5	18	11
Dummy VM	0	0	0	0

Step 7: Here column wise reduction is not required as each column contains zero, draw minimum number of lines to draw all zeroes.

Task/VM	Task1	Task2	Task3	Task4
VM1	0	12	6	16
VM2	15	5	0	8
VM3	0	5	18	11
Dummy VM	0	0	0	0

Step 8: Number of lines !=order of the matrix, Hence not optimal, again choose minimum for uncovered elements

Step 9: Here it is 5, subtract 5 from all uncovered elements

Task/VM	Taskl	Task2	Task3	Task4
VM1	0	7	1	11
VM2	10	0	0	3
VM3	0	0	13	6
Dummy VM	0	0	0	0

Step 10: Cover all zeroes with minimum number of line

Step 11: Number of resources=Number of lines, Then compare this matrix with original matrix and choose optimal assignment

	Task1	Task2	Task3	Task4
VM1	30	42	36	46
VM2	40	30	25	33
VM3	30	35	48	41
Dummy VM	0	0	0	0

According to hungarian methods the above assignment gives the optimum assignment so that the overall cost can be minimized.

V. CONCLUSIONS

This work is applying the hungarian algorithm for load balancing in cloud environment. As the cloud resources are dynamic in nature and tasks are also dynamic, the existing hungarian algorithm is extended by adding availability status for each resource periodically and the available resources may not be equal to the required tasks to be completed so the problem can be formulated as unbalanced assignment.. In this algorithm expected matrices(ECM) are generated and based on the results of the hungarian algorithm the load balancer knows about which task have to schedule by which VM. Here the priorities of tasks are not considered. Using extended hungarian method we can allocate resources dynamically for huge amount of tasks dynamically and also the hungarian method is simple to implement and works in balanced as well as in unbalanced conditions.

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Performance Analysis of Load Balancing Queues in User Level Runtime Systems for Multi-Core Processors

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Abstract: The speed of single processors is limited by the speed of light or speed of electron. Hence, processor manufacturers are packing multiple low speed processors or cores on to the same chip which are called multi-core processors. The number of processors on single chip is gradually increasing. Though multi-core processors are similar to Symmetric Multi-Processors (SMP), there are notable differences between them like shared last level cache. Operating systems consider these multi-core processors as SMP, and apply the suitable methods for task-scheduling and load balancing. But these strategies cannot fully explore the details of multi-core processors. The software also must be written to take the advantage of these multi-core processors. In this context, user level runtime systems evolved with a task as primitive concurrency construct. These tasks created by the program during runtime are added to the queues at user level runtime.

In this paper, we analyze the performance of various user level queues and their contention using Java.

Index Terms—Concurrency, Task, Work stealing, Centralized queue, Multi queue Double ended queue.

I. INTRODUCTION

The goal of parallelism is to maximally exploit the number of CPU cores present at hardware level. The goals of parallelism are:

- · Increasing throughput
- Reduce latency
- · Reduce power consumption
- Scale depending on number of cores (CPUs).
- Prevent loss of data locality.

Since the operating systems consider multi core processors as SMPs, the user level scheduler has to take care of scheduling the tasks created by the user to schedule in an optimal fashion [1]. The common practice by popular operating systems in case of multiprocessors is maintaining a single queue or multiple queues per processor. The processes or threads get added to these queues dynamically during the runtime and are scheduled on to the CPUs. Rear end of the queue is used for adding work load and front end of the queue is used for popping the work load and be executed. But the smallest execution unit in operating systems like Linux is a process or a thread (in Linux, process and thread are created using fork() and pthread_create() respectively). But both of these calls involve clone() system call of kernel. Using clone system call involves much overhead making it heavy weight. Though thread creation is of less overhead than a process creation overhead, it is still considerable load on performance involving:

- · system call overhead involving trap
- kernel level data-structure access on every operation.

Because of the above mentioned disadvantages of native thread API, modern approach of parallel programming runtime systems evolved from kernel level to user level.

These user level runtime systems are popular and became a De-facto standard for parallel programming [1]. Popular parallel runtimes such as Open MP, Cilk and TBB follow this approach for their runtime implementation. These runtime systems introduce a new scheduling entity called task which is considered to be even lighter in weight than thread since it is completely maintained at user level.

These runtime systems, provide API calls to create and maintain tasks. The programmer has to follow a sequence of API calls to implement parallel programs.

- 1. init():Initialize the runtime
- spawnTask(): Create tasks where ever parallel activity is to be done
- 3. join(): Wait for the tasks to complete.
- 4. release():Free the runtime.

init(): During the initialization of user level runtime system, a pool of native threads(pthread on Linux) is created and a single queue or multiple queues are created. These threads which get created during initialization of runtime are called worker threads or workers. Since it being a one time duty, during the initialization of runtime, every time a parallel execution entity is to be created, we need not enter the kernel level

spawnTask(): spawning a task allocates enough memory for task body and its parameters and this task object is added to the queue.

join(): All coarse grain or fine grain tasks have to wait until all the remaining tasks of that level have been completed at the joining points.

release(): It is the last call to the runtime which does join operation on native threads of thread pool and deallocation of queue objects which were created during the init().

In this paper, our focus is on studying the impact of the queue data structures which are used by worker threads to queue the tasks created by the programmer. We implemented three types of queues:

- Centralized or single queue
- Multiple queues without work stealing
- Multiple queues with work stealing

In this paper, the load balancing strategies are implemented and evaluated their performance by using a Matrix multiplication benchmark. To the best of our knowledge this is not ever studied in previous literature. Section II describes various types of queues used in user level runtime systems. Section III describes the experimental setup and result analysis.

II. TYPES OF LOAD BALANCING QUEUES

A. Single Queue

In this approach, during the initialization of runtime system, a single global queue data structure is created. This global queue is responsible for queuing the tasks created using taskSpawn(). This global queue is shared among all worker threads. Every worker thread is bound to a hardware level core or processor. If hyper threading is enabled at BIOS setup, the number of worker threads can be equal to the number of hyper threads. All these worker threads attempt to perform a dequeue operation on this global queue to get a task object when a worker becomes available. Once it is successful in dequeue operation a worker gets a task object and worker invokes its task body execution on its associated core.

Single queue approach is the simplest mechanism of implementing user level runtime system. When a worker thread is ready to execute a task, it attempts to dequeue a task from the global queue. This operation is a critical section and the worker must acquire a lock before this operation and release the lock after the operation. But it may suffer from the following disadvantages which may effect the overall performance of the parallel application.

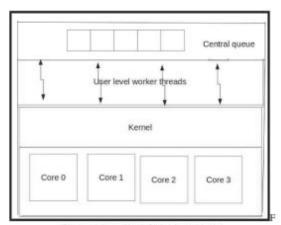


Figure 1: Centralized Queue Architecture

- Since all workers access a single queue worker threads may suffer from contention.
- It being a centralized approach, if worker threads become available at same instance, they have to compete to access the global queue. This may effect overall throughput of parallel task.

 Locality of the queue may cause cache performance isolation problem and false sharing.

B. Multi Queue

To overcome the main disadvantage of single queue approach, if a separate queue is associated with every worker thread, that is multi queue approach. Hence it is the first step for distributed load balancing. The tasks created by the programmer are added to separate queues associated with individual worker threads [2]. This approach guarantees transparent load balancing with the constraint that all the tasks are of equal duration. Since individual worker thread has access to its own queue, they need not contend on dequeue operation.

But this multi queue approach is not effective when all tasks are of variant duration. If tasks are of different

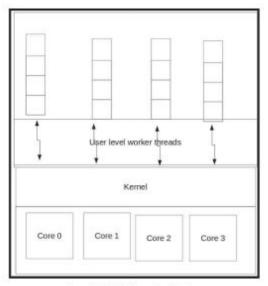


Figure 2: Multi Queue Architecture

durations, a queue associated with short duration jobs may become empty where as a queue with big duration tasks is overloaded.

C. Work stealing Queue

Work stealing is a distributed dynamic load balancing technique [3]. In this strategy, the thread pool maintains separate work queue per worker thread with stealing ability. When a work queue becomes empty it can attempt to steal a task from other queues. Since one end of the queue is accessible by its worker thread and other end is to add tasks. These queues need an additional feature of dequeuing from both ends in case of stealing by other worker. Double ended queues are used to implement this feature since it allows task deletion from both ends [4]. One end is accessed by the associated worker thread and other end open for stealing by other worker threads when they become empty. The tasks are created by application during runtime using the taskSpawn() or similar construct. The task gets added at the tail of a queue associated with each

processor. When execution reaches a fork point such as a spawn or parallel loop, one or more new tasks are created and put on a queue. The main strategies by which idle workers find new tasks are:

- Find a task from its own work queue
- Distributed work queues with randomized stealing

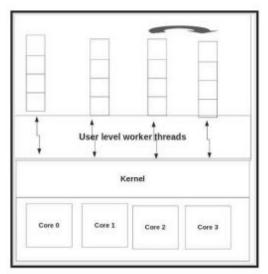


Figure 3: Work Stealing Queue Architecture

Since work stealing queues allow balancing of load across queues, it is more effective than multi queue approach.

III. EXPERIMENTAL RESULTS AND ANALYSIS

To illustrate the performance of different queue approaches at user level runtime systems, we implemented different types of queues in Java. The worker threads are plain Java threads which implement java.lang.Runnable interface. Three types of worker queues are implemented as blocking queues. Task construct is provided to the parallel programmer simply in the form of an interface. If the programmer has to implement his task body he can simply implement the interface and override the run() method of the interface. To make the job of testing different types of workloads, the user can choose an option at command line interface. The relationships among the classes are presented in Figure 4.

To evaluate the performance of the above mentioned three approaches, we implemented Square Matrix multiplication benchmark program. In this parallel implementation each task is created to find a single element of the product matrix (i.e. if the given two matrices A and B are 512 X 512 matrices, a total of 2¹⁸ tasks are created during execution. The intension behind taking large sized matrices is to overload the queues with task objects and test

how effectively load balancing is done across the queues. The benchmark is executed on

IBM x3400 server with 4 core (8 cores if hyper threading is enabled) Xeon E5-2401 and Linux kernel version 3.16.2.200. The number of worker threads taken in our experimental set up is equal to the number of cores (4) by disabling hyper-threading.

It can be observed from the execution times presented in Table1 that work stealing queue approach gives better performance than Centralized queue and Multi worker queue approaches. Though the difference of execution times between multi worker queue approach and work stealing is little, the difference is gradually significant for bigger matrix size inputs. The main difference is due to the stealing approach to balance the load across queues which is not addressed in plain multi queue approach. As stated in introduction section, centralized queue approach gives poor performance due to contention among the worker threads to access the single global queue. The difference of execution time is spent on saving the critical section code to access the global queue.

TABLE I

EXECUTION TIMES OF VARIOUS WORKER QUEUE APPROACHES

Matrix Size	Execution time in milliseconds				
	Centralized queue	Multi queue	Work stealing queue		
128	2	1	1		
256	7	6	5		
512	15	14	14		
1024	22	21	20		
2048	53	47	42		
4096	153	150	141		

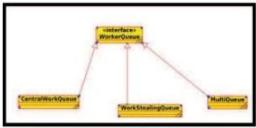
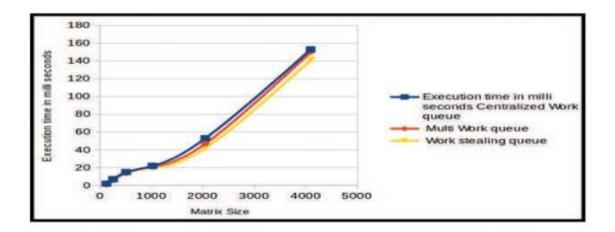


Figure 4: Class diagram of different approaches



IV. CONCLUSIONS

In this paper, we the effect of different load balancing queues on performance of task parallel applications. It is observed that work stealing queue approach performs better when compared to centralized queue approach and multi queue approach.

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Implementation of Orthogonal Frequency Division Multiplexing for SDR using MATLAB

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Abstract: Wireless Communication system is the emerging field of research. Users need to do many changes in the hardware to obtain high data rate less latency for less cost. To avoid Inter Symbol Interference (ISI) in a single carrier system, delay time must be very less compared to the symbol period. The data rate is inversely proportional to the symbol period. The low data rate is, due to the long symbol period. System with long symbol period h is not considered as an efficient communication system. The multi carrier system like Frequency Division Multiplexing (FDM) technique, the available bandwidth is used for multi carrier transmission by dividing the total bandwidth to sub bands. To obtain high data rates, the multiple carriers can be placed closely in the spectrum. But due to the less gap between multiple carriers in the spectrum, there is a chance of having Inter Carrier Interference. To avoid this interference guard bands need to be inserted which in turn results in low data rate. This paper focuses on the Orthogonal Frequency Division Multiplexing (OFDM) system implementation for testing purposes and its verification. Most of the stages in a communication system can be replaced by the software. For this process a new system called software defined radio came to exist. SDR is a radio which can be used for signal processing with minimum cost. The main goal is to create an OFDM signal using MATLAB for signal processing, synchronization, equalization, demodulation and detection. The paper also gives the design of an OFDM transmitter and receiver for Software Defined

Keywords: FDM, OFDM, ICI, Software Defined Radio and MATLAR

I. INTRODUCTION

The requirement for high speed data transmission has increased due to the rapid growth in the area of digital communication. To keep up with demand, a new modulation technique such as Orthogonal Frequency Division Multiplexing (OFDM) is currently being implemented. Now-a-days all the processor's power, has increased where the capability of handling the speed has become big task. A new multiplexing technique i.e. OFDM has become more important as it can have high speed with low interference. By studying the multi carrier system OFDM in many books and journals, it is clear that there will be a very good impact of OFDM in future communication system.

The main problem found in any communication system for high datarate is Inter Symbol Interference (ISI)[1]. ISI means the interference when a transmission interferes with itself and at receiver side it becomes difficult to decode the transmission correctly. As the receiver receives the signal from many obstacles by taking many reflected paths, the received signal will have many delayed versions of the original signal along with the actual one. This effect is called multipath. These delayed copies may cause interference at the receiver called ISI.

Main objective of any multi carrier system is efficient usage of spectrum, power consumption, robustness of multipath propagation and implementation complexity. Every objective with one or other may conflict, so implementations or techniques are selected which offer the best possible trade off between them. The best means of reducing the gap between the performance and channel capacity is OFDM modulation which combats multipath fading.

In addition to error correction coding techniques like turbo, spherical and Low density parity check codes, advanced OFDM is the good choice against multipath[2]. Fading effect can also be reduced to a certain extent. And to improve the efficiency of the spectrum the best method is to increase the capacity of the channel, which can be easily done with the new multi carrier system, OFDM.

In OFDM method, many orthogonal signals, which are overlapping are transmitted. It divides the available spectrum bandwidth into sub-channels. The gap between the sub-carriers is minimal theoretically such that a channel bandwidth is utilized. The main reason to opt OFDM is, it can handle the effects caused due to the multipath fading. Multipath causes mainly two problems - frequency selective fading and inter symbol interference. The achieved flat narrow band overcomes the frequency fading and modulation at low symbol rate removes the ISI by making long symbols than the channel impulse response. Using better error correcting methods along with frequency and time interleaving, more robustness can be achieved against frequency selective fading. And by inserting the required amount of guard band between the symbols of an OFDM signal, the effects of interference can be reduced even more so that at receiver, equalizer can be removed.

As the system increases information rate, the time required for each transmission becomes less. As there is no change in the delay time caused by the multipath, ISI is the main problem in a high speed communication. The new modulation method that is OFDM can avoid this problem by transmitting many low speed signals in parallel. Observe the below Figure.1 which shows two ways of transmitting the same data. If this transmission takes four seconds then each data will have duration of one second. But OFDM can send all the data in the same period simultaneously.

A Software Defined Radio (SDR) is a system where it uses software methods on digital signal. In a communication system after doing hardware related processing, the signal is converted into digital form as and then it is sent as input to the software system. The main aim of SDR is "to turn hardware problems into software problems" [3], so that radio engineers can handle the problems in more convenient domain. But everything cannot be converted into software, so SDR has two main sections: Software defined sub-system and Hardware defined sub-system. But this separation is not fixed. In general the antenna and the Analog to Digital Convertor (ADC) are of hardware defined and remaining system is of software. For this SDR we need software which can easily change the parameters like modulation type, signal to noise ratio, noise level, signal strength etc. which can be adapted to any other type of communication. That is hardware problems are converted to software problems.

II. ORTHOGONAL FREQUENCY DIVISION MULTIPLEXING

Mathematical Description

The OFDM Signal is given as

$$\nu(t) = \sum_{k=0}^{N-1} X_k e^{j2\pi kt/T}, \quad 0 \le t < T,$$

where Xk is the number of symbols, the number of sub carriers is denoted by N and T is the total symbol time of OFDM. The spacing of 1/T makes the OFDM signal orthogonal for every symbol.

$$\frac{1}{T} \int_0^T \left(e^{j2\pi k_1 t/T} \right)^* \left(e^{j2\pi k_2 t/T} \right) dt$$

$$= \frac{1}{T} \int_0^T e^{j2\pi (k_2 - k_1)t/T} dt = \delta_{k_1 k_2}$$

To avoid interference in channels due to multipath fading guard interval is included during this period a cyclic prefix is inserted before the OFDM block. OFDM with cyclic prefix is given as

$$\nu(t) = \sum_{k=0}^{N-1} X_k e^{j2\pi kt/T}, \quad -T_g \le t < T$$

Finally the transmitted signal is represented as

$$\begin{split} s(t) &= \Re \left\{ \nu(t) e^{j2\pi f_c t} \right\} \\ &= \sum_{k=0}^{N-1} |X_k| \cos \left(2\pi [f_c + k/T] t + \arg[X_k] \right) \end{split}$$

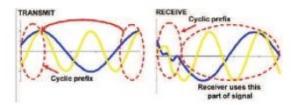


Figure 1. Signal with cyclic prefix

III. SOFTWARE DEFINED RADIO

SDR is a radio platform which uses software methods on digital radio signals. That is at receiver the signal is digitized and given as input to the software domain. The main objective of SDR is to convert hardware related issues into software related issues so that the engineers can work in a software platform. In general, an SDR is divided into two parts: the hardware system and the software system.

For big requirements like designing and handling receiver with multiple FM channels at the same time, we need wide spectrum and powerful system to process all the data. The system based on OFDM has a wide band application and so it is more suitable system for SDR.

IV. ARCHITECTURE OF ORTHOGONAL FREQUENCY DIVISION MULTIPLEXING

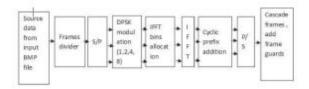


Figure 2. OFDM transmitter

A. Frame Guard

The main block in the OFDM transmitter is the modulator. Modulator modulates the input data .This modulated digital data stream is divided into frames based on variable symbol-per-frame, which gives the number of symbols per frame for a carrier.

Here in this paper the data is taken from an image file. Image pixel data is converted into matrix and then the matrix data is chunked based on the modulation type choosen. Here the number of symbols per frame is decided using modulation type If the number of symbols to be transmitted of a data stream, is less than a number of symbols per frame then the data is not converted into frames. And also if there is no data stream sufficiently long to divide it into multiple frames, then zeros are padded with two guard interval at either of the ends of the signal. This is used to find the starting point of substantial portion of the signal.

B. OFDM Modulator

The modulator generates a PSK signal matrix composed of complex numbers where the phases are the translated phases and all the magnitudes are considered as ones. For the remaining processing these complex numbers are converted into rectangular form[4].

Orthogonality between carriers must be maintained by controlling all the carriers and then OFDM process is done. OFDM signal is generated by taking input data like modulation type and signal power and then it chooses the spectrum based on its input. Each carrier to be produced is assigned some data to transmit. The required amplitude and phase of the carrier is then calculated based on the modulation type. The spectrum is then converted back to its time domain signal using an Inverse Fourier Transform.

Before differential or PSK modulation, encoding can be applied on each carrier (column of the matrix), and an extra row of reference data must be added to the matrix. The modulator then creates a row of random numbers within an interval defined by the symbol size (order of PSK chosen) and appends it on the top of the matrix. For every column, beginning from the second row (the first actual data symbol), the value is converted into the remainder of the sum of its previous row values and the value itself, over the size of the symbol (power 2 of the PSK order).

C. IFFT- Spectral Space to Time Signal

Each column of the DPSK matrix represents a carrier, their values are stored to the columns of the IFFT matrix at the locations where their corresponding carriers should reside. Their conjugate values are stored to the columns corresponding to the locations of the conjugate carriers. All other columns in the IFFT matrix are set to zero. To obtain the transmitting time signal matrix, Inverse Fast Fourier Transform (IFFT) of this matrix is taken. Only the real part of the IFFT result is useful, so the imaginary part is discarded.

D. Cyclic prefix insertion

A copy of the last 25% portion of every symbol period (I.e. row of the matrix) is included in the beginning of a row. This is the periodic time guard which keeps the receiver to synchronize while demodulating each symbol period of the received signal [5]. The matrix is now a modulated matrix. The modulated matrix is converted into serial data and it is considered as a modulated signal for a frame.

E. Communication Channel

The channel simulation allows finding common wireless channel characteristics such as noise, multipath, and clipping. To the transmitted signal random data is added, which is considered as a simple noise and simulated. For multipath simulation, attenuated and delayed copies of the transmitted signal is added to the original signal which reflects the problem in wireless communication for multipath fading. After adding the attenuated and delayed signal ,it is sent to the receiver and simulated.

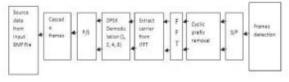


Figure 3. OFDM receiver

F. Frame detector

A trunk of received signal in a selective length is processed by the frame detector in order to determine the start of the signal frame. For only the first frame, this chosen part is comparatively large for taking the header into account [6]. The selected portion of received signal is sampled to a shorter discrete signal with a sampling rate defined by the system. A moving sum is taken over this sampled signal. The index of the minimum of the sampled signal is approximately the start of the frame guard while one symbol period farther from this index is the approximate location for the start of the useful signal frame [7].

The frame detector will then collect a moving sum of the input signal from about 10% of one symbol period before the start of the frame guard to about thirty percent of symbol period farther than the assumed start of the useful signal frame. The first portion, with a length of one less than a symbol period of this moving sum is discarded. The first minimum of this moving sum is the detected start of the useful signal frame.

G. OFDM Demodulator

Received OFDM signal is demodulated frame by frame. The total number of frames may vary by a wide range depending on the total amount of information transmitted through the OFDM System.

It is a reverse process of OFDM modulation. And like its modulator, the OFDM demodulator demodulates the received data frame by frame.

H. Guard Time removal

After converting a frame of discrete time signal from serial to parallel, a 25% length of a symbol period is removed from all rows. The remaining length of the symbol from all discrete signals is then lined up in parallel.

I FFT

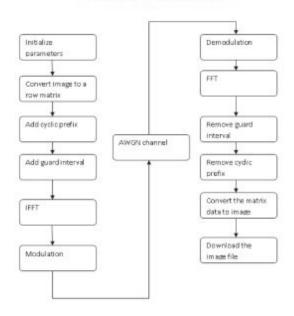
To the received signal is a Fast Fourier Transform (FFT) is applied which gives the spectrum of the received signal. The carriers are extracted to get the complex matrix of the received data.

J. Phase Shift Keying (PSK) Demodulation

The phase of each element in the matrix is changed and converted as a value within the size of the symbol.

On this new matrix differential operation is performed to get the demodulated data. This differential operation is used to calculate the difference between adjacent symbols in a column of the matrix. Then this parallel data is converted to serial and the demodulated stream of data for this frame is obtained. The series of zeros are appended to the data while transmitting to maintain the same symbol size for each carrier. With the help of number of symbols in a data and number of carriers the total number of appended zeros can be calculated. Similarly, for any type of PSK demodulation corresponding operation is performed to retrieve the original data. Here are the results shown for BPSK, QPSK, 16PSK and 256PSK.

V. SOFTWARE ALGORITHM



VI. RESULTS

A script file to invoke the OFDM parameters is simulated first, which invokes all the parameters of OFDM and initializes all the variables to start the simulation. Some variable values are allowed to the user to enter. The other variable values are obtained from the input variable data.

Please enter the data:

- 1) Image file name- an 8-bit grayscale (256 levels) bmp file:
- 2) IFFT length (power of two);
- total number of carriers less than [(IFFT size)/2 – 2];
- 4) Modulation type PSK;
- 5) Clipping of peak power in dB;
- 6) SNR in dB.

Following figures are the resultant images for different types of modulation methods.

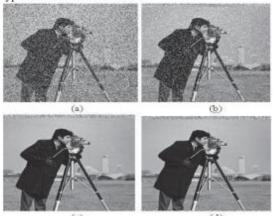


Figure 4: Images received at the OFDM receiver with BPSK technique for (a) SNR=0 (b) SNR=5 (c)SNR=10 (d)SNR=20

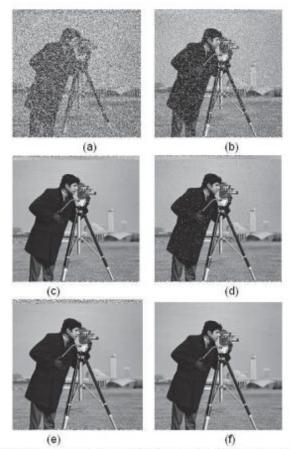


Figure 5: Images received at the OFDM receiver with QPSK technique for (a) SNR=0 (b) SNR=5 (c)SNR=10 (d)SNR=15 (e)SNR=20 (f)SNR=25

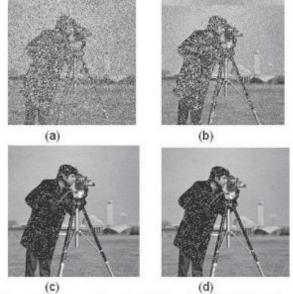


Figure 6: Images received at the OFDM receiver with 16PSK technique for (a) SNR=0 (b) SNR=10 (c)SNR=35 (d)SNR=40





Figure 7: Images received at the OFDM receiver with 256PSK technique for (a) SNR=20 (b) SNR=50

Table shows comparison of different parameters for PSK, QPSK,16PSK and 256 PSK modulation techniques for the following input data. It is clearly observed that in any modulation technique as signal to noise ratio increases the error rate decreases. Transmission time and receiving time decreases as number of bits increased for PSK.

TABLE I. COMPARISON TABLE

Modulation	SNR	BER(%)	Average phase error (degree)	% pixel error
BPSK	0	14.745	48.21	70,77
	5	1.61	25.1	9.045
	10	0.701	14.31	1.626
	15	0.648	8.33	1.58
	20	0.669	5.236	1.588
	25	0.000	2.299	0.000
QPSK	0	42.98	48.31	89.10
	5	16.07	26.39	47.85
	10	3,375	16.04	8.222
	15	2.485	12.11	3.919
	20	2,634	9.929	3.822
	25	0.000381	7.196	0.0015
16PSK	0	83.99	48,609	97.41
	5	71.71	27.39	91.91
	10	53.87	17.37	78.00
	35	17.00	6.53	31.04
256PSK	20	93.15	9.79	93.15
	50	93.76	7.32	93.76

Table 1. Shows comparison of different parameters for PSK, QPSK, 16PSK and 256 PSK modulation techniques for the given input data. It is clearly observed that in any modulation technique as signal to noise ratio increases the error rate decreases. And Transmission time and receiving time decreases as number of bits increased for PSK. As signal to noise ratio increases pixel error also decreases

VII CONCLUSIONS

An OFDM modulation and demodulation is successfully simulated using MATLAB in this paper. All main components of an OFDM system are implemented. Some of the problems faced while developing the OFDM simulation program are, mapping the modulation and demodulation and also maintaining the data format throughout the process.

Possible future works are adding a feature to accept the data in word size rather in bits, and including many other modulation techniques other than PSK like QAM, implementing multiplexing for OFDM for multiple inputs; that is even increasing the data rate. With increase in data rate performance of the system may degrade which can be still enhanced by including the diversity methods. So to overcome this, Forward Error Correction can be implemented

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Efficient Design Methodologies for Optimizing the Leakage Power in FPGAs

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Abstract: The scaling of the CMOS technology has precipitated an exponential increase in both sub-threshold and gate leakage currents in modern VLSI designs. Consequently, the contribution of leakage power to the total chip power dissipation for CMOS designs is increasing rapidly, which is estimated to be 40% for the current technology generations. In FPGAs, the power dissipation problem is further aggravated when compared to ASIC designs because FPGA uses more transistors per logic function when compared to ASIC designs. Consequently, in the nanometer technology, the leakage power problem is pivotal to devising power-aware FPGAs. This paper focuses on the architectural techniques for leakage power reduction in FPGAs. In this paper the multithreshold CMOS (MTCMOS) techniques are introduced to FPGAs to permanently turn OFF unused resources of the FPGA to reduce the power dissipation and the leakage power reduction technique in FPGAs on the use of input dependency is developed. This paper focuses on the reduction of leakage power with respect to CAD tools for the implementation of FPGAs.

Index Terms—CMOS, FPGA, CAD, MTCMOS, leakage power, power dissipation.

I INTRODUCTION

The continuous scaling of the CMOS process has attracted FPGA vendors to integrate more and more devices on the same chip to increase the chip functionality. As a result, the power dissipation of modern FPGAs increased significantly. Much of this increase in power dissipation is attributed to the increase in leakage power dissipation which is expected to exceed 50% of the FPGA power dissipation as modern FPGAs start using the 65nm CMOS process. In addition, the excessive scaling of the MOS gate oxide thickness t_{ox} resulted in a significant increase in the gate oxide tunneling current, thus exacerbating the leakage problem. In recent experiments, it was found that both the sub-threshold and gate leakage power dissipation increase by about 5X and 30X, respectively, across successive technology generations [1].

This paper will provide architectural modifications to FPGA designs to reduce the impact of leakage power dissipation on modern FPGAs. Firstly, multi-threshold CMOS (MTCMOS) techniques are introduced to FPGAs to permanently turn OFF the unused resources of the FPGA. The FPGAs are characterized with low utilization percentages that can reach 60%. Moreover, such architecture enables the dynamic shutting down of the FPGA idle parts, thus reducing the standby leakage significantly. Employing the MTCMOS technique in

FPGAs requires several changes to the FPGA architecture, including the placement and routing of the sleep signals and the MTCMOS granularity.

Secondly, a new technique for leakage power reduction in FPGAs based on the use of input dependency is developed. Both sub-threshold and gate leakage power are heavily dependent on the input state. In FPGAs, the effect of input dependency is exacerbated due to the use of pass-transistor multiplexer logic, which can exhibit up to 50% variation in leakage power due to the input states.

II FPGA OVERVIEW

Generally, FPGAS consists of logic blocks, routing resources and input-output pads. However, the advancement in FPGAs including of embedded memory Phase Locked Loops (PLL), DSP blocks, embedded processors and special feature blocks. The complete architecture is shown in the figure.1 Based upon these features the FPGA is considered as attractive design method.

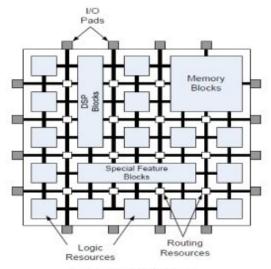


Figure 1: Modern FPGA fabric.

A) CAD for FPGAs

Generally, all the FPGAS are implemented by huge number of programmable switches. By using those switches only logic functions are designed and implemented. The Computer Aided Design tools of FPGAs transform the design in to stream of binary bits 1's and 0's only. The design is either schematic entry or a hardware description language. These binary streams of 0's and 1's are used to program the FPGA by proper configuration. The Figure 2 represents the flow diagram of the CAD tools for FPGA design.

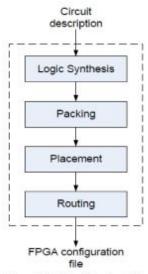


Figure 2: CAD tool flow for FPGA..

III LEAKAGE POWER REDUCTION IN FPGAS USING MTCMOS TECHNIQUES

In this section, the different supply gating methods using Multi- threshold CMOS techniques for FPGA are presented. These are mainly used to reduce sub- threshold leakage power in FPGAs. For leakage reduction a modified architecture of FPGA using sleep transistors and corresponding CAD algorithms are proposed. In the CAD flow, a new activity profile phase is introduced to identify the blocks of FPGA exhibiting the similar idleness. During the idle times, those idle blocks are turn off by this activity profile algorithm. Next, some new packing methods are introduced to pack the idle blocks with same activity profiles for turning to off them.

In FPGAs, the crucial one is leakage power reduction compared to Full-custom and Semi-custom ASIC designs because in FPGAs the unused resources are more. This standby leakage power is almost 40% due to unutilized resources, thus 60% of resources are only utilized in FPGAs [2]. For wireless communications, the idle mode period is very long [3]. In such FPGA applications, some utilized blocks are forcibly put into standby mode during the idle time and then leakage power is reduced.

In an MTCMOS implementation of FPGA, the sleep transistors are designed by high threshold voltage (HVT) devices. These transistors are connected to the pull-down network. This pull-down network is designed by low threshold voltage (LVT) devices, to which circuit is connected to ground as shown in the figure 3(a). When the sleep transistor is turned off, the leakage current of the circuit is reduced, but has very low saving. Hence, the circuit gets benefit from the Low VT pull down network when the sleep transistor is on, otherwise the sub threshold leakage current is limited, because sleep transistor is turned OFF.

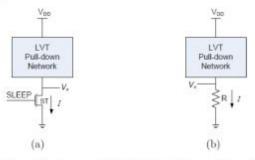


Figure 3: Architecture of MTCOMS. (a) Architecture of general MTCOMS, (b) Equivalent ST circuit in the active mode.

In the above figure.3, the equivalent circuit for the sleep transistor was shown as a finite resistance 'R' between the ground in the case of the sleep signal is high with a small voltage at the virtual GND line Vx. However, the sleep transistor finite resistance R incurs a penalty of performance due to the reduction of driving potential in the circuit VDD-Vx [3]. If the sleep signal of the sleep transistor is low, the entire circuit goes into a standby mode. In this case, the voltage Vx rises to 0 Volts and VDD Volts. Next, the sleep transistor acts as a very high resistance. This resistance is used to reduce the subthreshold leakage current. In FPGAs, sleep transistor circuits can reduce sub-threshold power leakage by (i) Power down the unutilized resources of the chip during configuration permanently (ii) turning off and on the unused resources of the chip dynamically based upon the activity of the circuits, and (iii) powering down the entire FPGA during the idle time.

In this paper, the changes at the CAD level were developed for FPGA design using the MTCMOS technique to get the full advantage of leakage power saving. All these changes are integrated into the Versatile Place and Route (VPR) flow [4]. The figure 4(a) and figure 4(b) shows the flow diagrams of the typical VPR CAD tool and proposed modifications respectively.

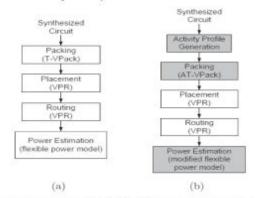


Figure 4: Process flow of CAD in FPGA (a) flow chart for VPR conventional method. (b) Proposed CAD flow diagram included in the VPR flow.

The Figure 4(b) shown as the considering the activity generation phase. In this stage, the identification of unutilized blocks with same activity is taken place. Blocks with similar activity profiles are forced into a standby mode together. The next stage is T-V Pack algorithm, which is used to integrate with activity profiles generation method and packing algorithm resulted algorithm is AT-V Pack as shown in figure 4(b). Finally, a modified power estimating model is introduced to properly calculate the power savings in this proposed MTCMOS FPGA architecture.

The conventional FPGA architecture is used in most of the modern FPGAs. This FPGA architecture consists of logic blocks, which are implemented by a four input Look Up Table (LUT), a Flip Flop and a 2X1 multiplexer as shown in figure 5.

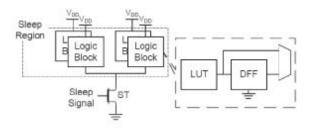


Figure 5: The MTCMOS type FPGA Architecture.

The logical blocks connected to one sleep transistor are called as sleep regions. The sleep signal controls each sleep region. Deactivation of the sleep signal moves the N clusters into low power mode during the inactive times. The output of the each logic block is stored in the Flip-Flop, before entering the sleep mode so it can recovered when the corresponding sleep region wakes up again. The sleep signals of the unused blocks or resources of the FPGA are deactivated during the OFF time permanently. In Modern FPGAs, during the runtime the sleep signals are dynamically generated using the partial reconfiguration logic [5], thus providing minimum area overhead. If the design is well- known in advance, the sleep signals easily can be generated [6].

The no. of clusters that can be determined by the size of the sleep transistor, leakage power savings area over head and the maximum permitted ground bounce about virtual ground lines. For this performance large sleep regions employ few number is larger transistors. As a result, the control circuitry needed to produce the less complex sleep signals. These signals consume less power and occupy less area when compared to small sleep regions.

The figure 6 shows the proposed FPGA fabric, in which the sleep transistors are pre-fabricated with fixed size in the FPGA Architecture. This figure shows the placement information. It provides the full connectivity between the sleep transistors and logic blocks and also provides minimum area overhead. During the FPGA fabrication, the sleep control signals of the each and every sleep transistor are hardwired [7]. As shown in the figure, the virtual ground V_{GND} line is connected to the pull-down networks of the logic blocks to the sleep transistor. The Virtual ground

V_{GND} lines are hardwired to their corresponding sleep transistors. Many research methods are proposed to optimize area [8], and the average overhead of the MTCMOS architectures using fine granularity in FPGAs is around 5% [9, 10]. For sleep transistor implementation, two types of devices are considered: header or footer devices. The Pmos transistors are used as header devices to block the current path from the supply line and pull down network. Footer devices are implemented by Nmos transistors to block the ground path, as shown in figure.7.

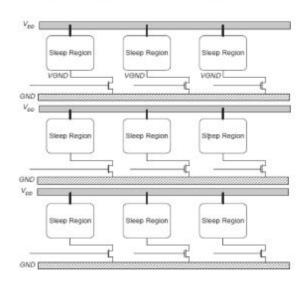


Figure 6: MTCMOS-based FPGA fabric with sleep transistors.

The header- PMOS approach has the drawback of area penalty when compared to the footer- NMOS approach. This is due to the low driving current of PMOS transistors because of low mobility of holes. Consequently, only NMOS footer sleep transistors are used in this work.

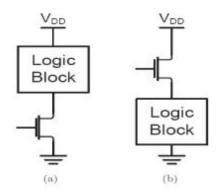


Figure 7: (a) NMOS footer sleep transistor implementation. (b) PMOS header sleep transistor implementation.

There are two types of sleep transistor architectures used in this paper. Those are local sleep transistors and global sleep transistors. The local sleep transistors are used at the logic block level, these are independently idle. Second, the global sleep transistor architecture consists of a single sleep transistor for entire large block that consists again many local blocks [11].

IV LEAKAGE POWER REDUCTION IN FPGAS THROUGH INPUT PIN REORDERING

In FPGAs, the power dissipation is state dependent as the i/p signals are forced into substantial leakage power reduction technique. This happens due to the pass transistor logic in the design.

In this section, a new methodology is introduced, which is based on reordering of the i/p pins reordering to decrease the leakage power dissipation in all blocks and resources of the FPGAs without any performance penalties. This proposed methodology handles the logic and routing resources differently to achieve more leakage reductions. Next, a new method with some modifications is proposed and implemented to increase the performance along the critical path [12].

The proposed pin reordering algorithm consists of two phases: (1) Logic pin reordering (LPR)- it targets leakage power reduction in the logic blocks of FPGA and(ii) Routing pin reordering (RPR)- this phase targets the routing switches. Right after the synthesis the LPR phase is performed and previous to the Packing stage. The RPR phase is performed next to the routing stage only. This process stages are shown in the figure 8. The CAD flow corresponding to these pin reordering methodologies are changed. The T-V Pack is used for packing and VPR CAD tool for placement and routing [13].

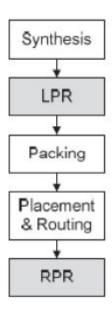


Figure 8: The proposed pin reordering algorithms with VPR CAD flow.

Figure 9 shows the different leakage savings due the LPR Phase. From the figure, we can understand the maximum power savings are generated due to the input swapping phase. The very small leakage power saving is due to the unutilized block into a low leakage mode because of the absolute minimum unutilized logic blocks or resources.

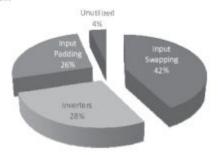


Figure 9: Leakage savings breakdown in logic blocks.

Figure 10 represents the RPR breakdown leakage power savings in the FPGAs. It can be understood from the figure that the average power savings of the unused routing resources is more than the unused logic resources. This is due to the percentage of unutilized routing resource is greater than that of the functional blocks. One more observation is that the leakage power savings in the inverters circuits is larger in the routing resources, which can be justified by the fact that the inverter circuits used in routing resources are of bigger in sizes than those used in the logic blocks. Hence the routing resources consume large leakage power [13, 14].

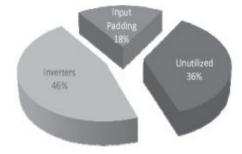


Figure 10: Leakage savings breakdown in the routing resources.

V CONCLUSIONS

This paper proposed several methodologies for leakage power reduction in modern nanometer FPGAs. The use of supply gating using Multi-Threshold CMOS (MTCMOS) techniques was proposed to enable turning OFF the unused resources of the FPGA, which are estimated to be close to 30% of the total FPGA area. Moreover, the utilized resources are allowed to enter a sleep mode dynamically during run-time depending on certain circuit conditions. Several new activity profiling techniques were proposed to identify the FPGA resources that will share common idleness periods, such that these resources will be turned OFF together.

Another technique proposed in this paper for leakage power reduction in FPGAs is the pin reordering algorithm. The pin reordering algorithm makes use of the input state dependency of leakage power to place as much as possible of the FPGA circuits in a low leakage mode without incurring and physical or performance penalties. The guidelines for finding the lowest leakage power dissipation mode were derived and it was shown how they vary with every process node depending on the relative magnitude of sub-threshold and gate leakage power components. The proposed pin reordering technique was applied to several FPGA benchmarks and resulted in an average of 50% leakage power savings. Furthermore, another version of the proposed algorithm is also developed that results in a performance was improved by 2.5%, while achieving an average leakage power reduction of 48%. This paper presented new CAD methods for the reduction of power dissipation in FPGAs.

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Analysis of Industrial Parameters for Chemical Combustion Process in Rotary KILN using LabVIEW with Wireless Technology

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Abstract: Analysis and control of Industrial parameters is of importance for most of the process control applications. But deploying cables from various transducers and final control elements to monitoring and controlling stations becomes costly and complex. This problem calls for wireless implementations for monitoring and control applications. This paper dispenses a low cost wireless combustion process parameters Analysing system based on ZigBee communication protocol. This system contains Rotary KILN unit ,sensors, ZigBee device ,PIC-Micro-controller, and PC (LabVIEW).The system uses Microchip PIC16F72 controller as signal processing unit in the field of combustion process and NI LabVIEW interface as the Analysing unit. It utilizes a precision temperature sensor, outlet pressure sensor which being a low cost sensors provides a authentic output within its operating range. The system follows a request response methodology, where the field unit responds to the request made by the Analysis unit of LabVIEW.

Index Terms— LabVIEW, ZigBee, PIC-Micro-controller, Rotary KILN.

I. INTRODUCTION

The measurement and Analysis of Rotary KILN combustion parameters are very crucial in order to optimize the performance of combustion process. Moreover, reliable data acquisition determines the accuracy of the Analysis algorithm [1]. In a field of industry, a plant may be having a host of independent processes consist various control objectives, and analysis of all these processes prove the conclusive factor in a process performance and safety. The interfacing of sensors in the field of process to the central analysis unit results in high installation and preservation costs, and make the system susceptible to wear tear, thereby reduction of its reliability. Whereas, wireless network communication offers lower set- up and maintenance costs with better flexibility to re-build and update the wireless network. Further, sensors of a wireless sensor network can also be installed in hazardous and secluded environments like nuclear power plants. The quick improvement in wireless system has resulted in a vast number of possibilities in different commercial environments and applications. In the past days various methods for industrial control over wireless sensor networks have been designed and implemented. But, industrial and commercial adaptations of most of these

methods are yet to be realized, principally due to the deployment and complexity costs involved. Wireless High Way Addressable Remote Transducers based methods prove to be most encouraging for chemical process control applications, but requires huge investments for deployment.

The prototype distillation column system adopts the ZigBee wireless communication protocol to acquire real-time data, and cool down the high temperature of a communication room. The system is designed to be simple, highly reliable and cost effective. In this system ,the measured parameters from Rotary KILN of chemical process can be processed by Microchip PIC16F72 –controller and the processed data is transmitted by ZigBee transmitter module to ZigBee receiver module, which is interfaced with PC –LabVIEW software through RS-232 communication. The received data from ZigBee module can be processed or analyzed by graphical Terminals Units of LabVIEW programming.

This idea represents low cost system to design wireless analysis of the Rotary KILN temperature and pressure suitable for small-scale industrial applications. The fundamental aim of this paper is to develop a system to design a wireless Rotary KILN combustion [2] parameters Analyzing system which enables to analyze the Rotary KILN combustion process parameters using ZigBee technology and analyses the parameters on the front panel of LabVIEW software on PC screen.

The system mainly contains two parts One is the Rotary KILN combustion unit [2] along with ZigBee transmitter node and another is the receiver node. The transmitter part consists of physical variable sensors, microcontroller and ZigBee. Receiver consists of a PC interfaced with ZigBee through a serial port. Here the parameters like temperature, steam pressure are detected by the sensors given to the microcontroller and transmitted to the receiver part through the wireless medium ZigBee.

II. SYSTEM DESIGN AND ARCHITECTURE

Fig.1.represents the system design and architecture, which incorporates two stand-alone units: one is the field unit and second one is the analyzing unit, where thermocouple senses the temperature of Combustion Product at Rotary KILN Junctions [3]. The analyzing unit is in wireless synchronization with the combustion unit. It shows the

updated process status of Rotary KILN and accepts reference point changes by the operator.

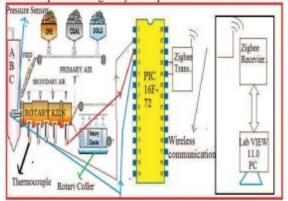


Figure 1. System Design and architecture

Field and analyzing unit have a separate display on A ZigBee trans-receiving module. ZigBee is wireless network system based on the IEEE 802.15.4 standard, which dispenses advantages of being power efficient, low cost, increased network capabilities along with high data transfer rate .So ZigBee network protocol sufficient for measurement and control applications.

The Rotary KILN unit is connected with thermocouples, which are in contact with the combustion product of sponge Iron. The unit Microchip PIC16F72 -controller, continuously gains the voltage from the sensor .Here voltage is proportional to temperature. The pressure sensor is connected at KILN Outlet Door(KOD), which produces output voltage proportional to KILN Outlet Pressure[3] Moreover, the received data from sensors is amplified from milli-volts to volts and is given to Microchip PIC16F72 -controller, which processes the signal and transmits the Rotary KILN combustion process parameters wirelessly the requested data to the analyzing unit.

Signal conditioning circuit is required for temperature and pressure sensing elements, it is designed with 741 IC circuit [4] and has a greater advantage of high CMRR ratio, high input impedance, and low output impedance. Signal conditioning circuit for temperature and pressure sensor is shown below Figure.2

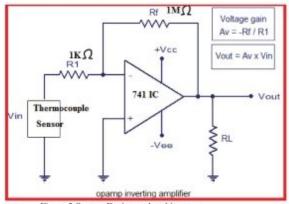


Figure 2.System Design and architecture

The analyzing unit mainly consists of ZigBee Receiver module and labview11.0 software installed PC. The unit receives the data from Rotary KILN[3]combustion unit(field unit)and received data is communicated with LabVIEW11.0 software installed PC through RS-232 Communication. Here com-port configuration settings is to be done in MAX(Measurement and Automation Explorer)after getting configuration setting ,the data from ZigBee Receiver module can be achieved in Labview11.0 using VISA read and write configuration setting through com-port communication. The received data can be analyzed using LabVIEW graphical programming.

In the rotary KILN combustion process, the quality of sponge iron product depends on combustion temperature and pressure levels. So temperature and pressure data to be analyzed in order to get desired quality of product .The relationship among temperatures and pressure can be analyzed from LabVIEW front panel diagram.

III. I/O FIELD DEVICES AND SYSTEM HARDWARE

This system is mainly designed with system hardware integration of LabVIEW software .System hardware mainly consists of following components

A. ZigBee module

B.PIC micro chip IC 18f458

C.K-type thermo couple

D. Pressure sensor

E. Rotary KILN

A. Zigbee module

This system is designed with wireless network communication using ZigBee module. Two different ZigBee modules are used, one is ZigBee transmitter and another is receiver. ZigBee transmitter is used at Rotary KILN combustion process to transmit the measured data to LabVIEW through wireless communication range of 30-40 meters. The ZigBee communication network protocol supports different network topologies like mesh, tree, star etc. This communication support is needed for interfacing more number of sensors module from different field stations of the process.

Type of network topology can be selected based on requirement of interfacing of sensors and actuators at the field of process. If the number of fields of process is more, then suitable network topology is to be selected for better communication [6]. This ZigBee network layer is applicable for network sans high power transmitter. Huge number of nodes can be handled by this ZigBee network layer. Here RS-232 –Recommended standard is used to make the communication between ZigBee Receiver module and LabVIEW installed PC.

B. Microchip PIC16F72 controller:

Microchip PIC16F72 is a CMOS -flash based 8 bit microcontroller. It has a great feature of 200ns instruction execution speed, It has 5 channel of 8 bit analog to digital converter, which can be more flexible for interfacing analog sensor from the field of process. In this system two analog sensors are interfaced to microchip PIC16F72 controller and the sensing signal is processed through micro controller program; processed data is transmitted to ZigBee receiver module through wireless communication

This micro chip has a high performance RISC CPU [6]. This can be operated at industrial temperature and the wide operating voltage range is from 2.0 v to 5.5 v. One more important thing of micro chip is 'it has inbuilt PWM module'. So it can be used for control of industrial field devices along with suitable signal conditioning circuit[7].

C.K-type thermocouple:

K-type thermocouples can be used for industrial applications. Here, these are used for the measurement of combustion temperatures, its temperature ranging from -200°c to 1350°c.Rotary KILN combustion temperature is changing from 750°c to 1200°c.So k-type thermocouples are suitable for the measurement of combustion temperature. K-type thermocouple [8] produces the output voltage in the range of milli-volts with respect to change of temperatures. So thermocouples require signal conditioning circuit for interfacing of sensor with PIC16F72 microcontroller. Thermocouple input and output relationship and K-type thermocouple are shown in the below Figure 3.

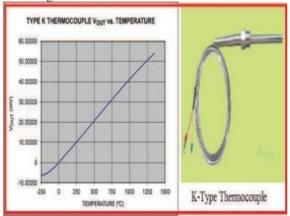


Figure 3. K-type Thermocouple input and output relationship

D. Pressure sensor:

In this system, high resolution Bar-600 relative pressure sensor is used for the measurement of outlet door pressure at Rotary KILN. If the operators are unable to maintain sufficient level of pressure at KILN OUTLET-DOOR, it causes blasting of the chamber. KILN produces 30-150PSI ranging pressure at KOD chamber. This sensor is sealed from water. In this prototype system, SIKA make product is used for pressure measurement of KILN outlet door pressure. It's pressure temperature is operating from 0°c to 80°c.Here pressure sensor produces analog output voltage proportional to KILN outlet pressure changes. This voltage is in the range of volts, so we can directly interface this signal to PIC-microcontroller without any signal conditioning circuit and easily process the signal through micro controller programming .Pressure sensor, used in proto type system is shown below Figure.4.



Figure.4. High Resolution 600-Bar relative pressure sensor

E. Rotary KILN:

Rotary KILN is like a furnace chamber or Reactor, which is used in Steel, Pharmaceutical, Fertilizer and cement industries. Entire production manufacturing process is going inside of the Rotary KILN. Industrial rotary KILN is shown below Figure.5



Figure 5. Industrial Rotary KILN

Reduction of Iron in Rotary KILN is completely temperature dependent process. If the operator is able to control temperature and pressure level in the Rotary KILN, it produces high quality product. This paper completely analyses the relationship among temperature, pressure and product quality. In this process Iron-ore raw material is converted into sponge iron by the combustion process at different temperatures. Generally Rotary KILN has seven junctions; operator needs to maintain suitable temperature at every junction in order to maintain perfect chemical reactions. If the chemical reactions are perfect, then product grade or quality is good. Different chemical reactions take place at KILN junction are shown below.

In this process, operators need to maintain different levels of temperature of bed, gas and reduction .The temperature profile along the length of the rotary KILN of sponge Iron process can be adjusted to heat the raw material iron ore to the reduction temperature with in short time and maintain this bed temperature levels to carry out the reduction to achieve the desire level or quality of Ferrous (Fe). In general the temperature profile is different for various iron ore depending upon the reduction bility characteristics. The typical temperature ranges to be maintained at 100TPD KILN is shown in below table, 1

TABLE I ROTARY KILN JUNCTION TEMPERATURES

TEMP	T1°C	T2°C	T3°C	T4°C	T5°C	T6°C	T7°C
REC	750	860	960	1020	120	1030	1030
GAS	930	1030	1080	1080	1090	1100	1120
BED	850	980	1020	1030	1040	1050	

Quality of the product of sponge iron not only depends on the temperature, pressure levels at combustion process, it also depends on the size of raw material of iron core. If the temperature levels at junction of Rotary KILN is controlling perfectly then the resulting Ferrous % at different iron core sizes is shown in the below table.2. This paper completely describes the range of temperature to be maintained at combustion process of reduction of iron ,and also describes how grade levels are changing with respect to unwanted change in reduction of iron.

TABLEII
FERROUS QUALITY LEVELS AT DIFFERENT SIZES OF IRON ORE

IRON ORE	+16mm	+12mm	+10mm	+4mm
Fe%	90.0	91.31	92.51	95.55

IV. SYSTEM SOFTWARE

Different configuration settings are required at field point and analyzing unit. Initially Rotary KILN combustion process parameters to be interfaced with PIC-microcontroller through signal conditioning circuits. These parameters are processed through micro-controller program and transmitted through ZigBee wireless technology. Data communication between ZigBee transmitter and receiver can be made success by suitable software configuration settings.

A. Configuration settings of ZigBee module:

ZigBee both transmitter and receiver modules are operating at 2.4 KH frequency. These two modules need to be configured through PC programming (or) the unit microcontroller. Before the system is setup, for this existing system, these two modules were configured through personal computer to have the same personal area network ID and bit rate by configuration of two ZigBee modules have been done using configuring software, TMFT V2.6 by module manufactures.

B. Rotary KILN configuration unit:

In this application; rotary KILN combustion unit produces sponge iron as a final product with respect to raw material iron ore. Quality of product depends on temperature of the junction and size of the iron ore; here production quality is analyzed by considering necessary parameter like temperature and pressure. Three temperature sensors are used to measure the temp- of bed, gas and rec. This K-type thermocouple (temperature sensor) produces output signal in the range milli-volts, which is amplified to volts. "this voltages signal is calibrated into temperature by using micro-controller programming" which is displayed on LCD as field unit and it transmitted to analysis unit. Pressure sensor output system is processed like temperature signal. Prototype of this Rotary KILN combustion unit is shown below Figure.6. The microcontroller 10-bit analog to digital converter to update by read the signal from temperature sensor and pressure sensor and store it into the memory for transmission purpose and historic al report.



Figure.6 Prototype Rotary KILN combustion unit

C. Analyzing unit

Lab-VIEW front panel is acting as analyzing unit to this application here LabVIEW front panel was designed to analyzing the quality of product (sponge iron) with respect to change of three temperature levels (bed, gas and rec).

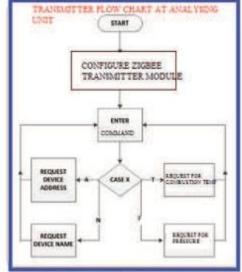


Figure 7. Logical flow diagram of Transmitter module at analyzing unit

In this system field unit continuously sends the measured signal through ZigBee communication to analyzing unit. At this analyzing unit ZigBee receiver module is communicated with PC- LabVIEW through RS-232 communication. The measured parameters at the combustion process are achieved by entering the commands 'T' in the "ENTER REQUEST" input control. Figure.7 and Figure.8 shows the logical flow diagram of Transmitter and receiver at Analyzing (monitoring) unit.

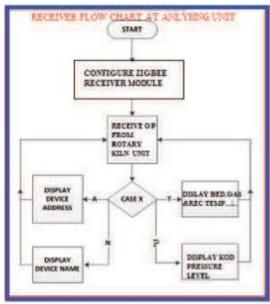


Figure 8.Logical flow diagram of Receiver module at analyzing unit

Communication between ZigBee Receiver and LabVIEW is configured in Measurement and Automation Explorer (MAX) of LabVIEW. The data from communication parts of PC can be received at the block diagram of LabVIEW by using VISA read and write commands.

After receiving data into the block diagram of LabVIEW [9]; dataflow programming to be written for the relationship between the temperatures (KILN combustion) and the quality of sponge iron product. Entire result of this system is monitored (or) analyzed on front panel of lab view through unique graph models. Analysing unit of this application is shown below figure.9:

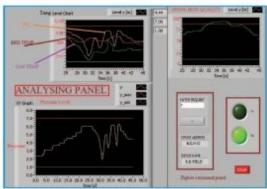


Figure.9. Analyzing Unit at Front panel of LabVIEW

V. CONCLUSIONS

This paper discusses designs and developed of a temperature and pressure analyzing system in chemical combustion process on Rotary KILN. This system is based on the ZigBee wireless communication protocol. The implementation has been done for point to -point system that has only one field unit analyzing two parameters. But given the user friendliness of ZigBee technology the system can be upgraded for analyzing several field units with different process field parameters. It achieves a line-of-sight range of 30 meters and a range of 15 meters with obstructions. The developed system is economical, reliable and accurate for processes, where temperatures are within 1100°C. Finally sponge Iron product quality is analyzed with respect to BED,GAS and REC temperature Levels.

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A Brief Overview on Conservation of Lakes in India

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Abstract: Aquatic ecosystem like lakes worldwide are being severely altered or destroyed at a rate greater than that at any other times and far faster than they are being restored. This article focuses on the restoration and conservation measures to be followed for the management of lakes which are facing the problem of environmental degradation due to population explosion, urbanization, industrialization, discharge of domestic sewage, industrial effluents, chemical intensive agriculture, dumping of municipal solid waste, idol immersion etc. These measures should be strictly followed by the people and the government because lakes and their surroundings are unique assets and valuable ecosystems for both society and nature. Lakes have social, cultural, aesthetic and economic values and it is our responsibility to retain the glory and pristine beauty of the lakes.

Index terms-Lakes, Degradation of lakes, Urbanization, Eutrophication, Siltation, lake pollution, lake conservation, Dal lake, Hussain sagar lake.

I. INTRODUCTION

Water is the source of life on earth and earth is known as the 'Watery Planet' because it is the only planet in the solar system with the abundant source of water. About 97 percent of earth's total water supply lies in oceans which is unsuitable for human consumption due to its saline content, 2% percent is frozen in the polar ice caps and the remaining 1% percent is available in lakes, rivers and groundwater (Table 1) which is suitable for human consumption. Lakes are the best available fresh water resources on the earth's surface as we can freely access only the water in lakes. Lakes have traditionally served the function of meeting water requirements of the people for drinking, household uses like washing, for agriculture, for fishing and also for religious and cultural purposes. Apart from these functions, lakes are known to recharge ground water, controls runoff, moderate the hydrological events drought and floods, host variety of flora and fauna and provide a wide array of recreational activities and aesthetic benefits for humans to

With rapid urbanization and expansion of city boundaries, a number of lakes in urban areas are facing issues of over exploitation, encroachment, pollution etc. Therefore, it is needed to initiate efforts to restore and conserve the lakes.

TABLE 1 DISTRIBUTION OF WATER ON EARTH

Percentage of total water		
97.3		
2.14		
0.61		
0.017		
0.0001		
0.001		

II. CAUSES FOR DEGRADATION OF LAKES

For mankind, water is a basic need. It influences and alters the social, cultural, political and religious heritages of different communities. The need for plentiful supply of water is universally demanded. However, much importance is not given to the quality of water. All over the world, the first victims of water pollution are the water bodies like lakes so that even one time drinking water resources are facing the crisis. In the last half of the 20th century, lakes underwent unprecedented environmental degradation. The major factors that lead to the degradation of lakes are

- Rapid urbanization and encroachment
- Continuous flow of untreated sewage
- Intensive agricultural runoff
- · Discharge of industrial toxic effluents
- · Dumping of debris and garbage
- Heavy siltation and pollution due to idol immersion.



Figure.1. Encroachment along the lake boundary



Figure.2. Disposal of garbage in the lake

III. IMPACT OF URBANIZATION ON LAKES

Various problems are associated with urban water bodies. Human settlements and effluent geneses from various sources are the chief factors for the degradation of lakes. The anthropogenic pressure has also resulted in degradation due to deforestation, extensive agricultural use, flow of slit and harmful chemicals. The tourists who come for visiting the lakes pollute the lakes by throwing harmful waste and polythene bags. Increasing encroachment on the bank of the lakes causes deterioration of water quality and disturbs the biodiversity of the lake, all these cause an impact on climate change also.

Rapid urbanization has following impacts on lakes:

A. Eutrophication

Lakes in the urban areas receive enough nutrients like nitrates and phosphates from sewage, industrial effluents and fertilizer and pesticide rich run-off from agricultural fields which promote the rapid and lush growth of oxygen consuming algae especially blue-green algae and aquatic weeds like water hyacinth. This growth deoxygenates water and the depleted levels of oxygen in water leads to a situation where aquatic life forms cannot survive. The dead organisms undergo anaerobic decomposition releasing anoxic gases like methane, hydrogen sulphide and carbon dioxide which makes the lakes stink emitting foul smell. This process of nutrient enrichment of the lakes leading to excessive plant growth is called Eutrophication and the lakes are termed as Eutrophic lakes.



Figure. 3. Eutrophication infestation with water hyacinths

B. Siltation or Sedimentation

Siltation is a form of water pollution where water flowing into the lakes brings sediment which is either silt or clay and settles at the bottom of the lakes. Activities like deforestation, intensive agricultural cultivation and land clearances for construction loosen the top soil, which finds its way into the lakes.

IV. IMPACT OF LAKE POLLUTION

Lake pollution has the following effects:

A. Toxic chemical effects

Chemical toxic substances like heavy metals and pesticides in sewage, industrial effluents and agricultural run-off pollute the lakes affecting aquatic organisms and humans. Pesticides like DDT and heavy metals like lead, mercury and cadmium which are not water soluble are absorbed into the tissues of the organisms from the polluted water and accumulate in the organism's body. This process is called Bioaccumulation. The concentration of these toxic substances build up at successive levels of food chain. This process is called Biomagnification. These phenomena cause various types of diseases in humans effecting different body organs.

B. Water borne diseases

Waste water especially sewage that is discharged into lakes contain pathogenic (disease causing) organisms like bacteria, virus and parasites that are capable of transmitting water borne diseases in humans. Some of the water borne diseases are diarrhoea, cholera, typhoid, dysentery, jaundice, gastroenteritis etc.

V. NEED FOR LAKE CONSERVATION

Lakes when restored and conserved have the following environmental and ecological benefits:

- · Harvest rainwater and recharge ground water.
- · Reduce water logging and flood risk
- Increase economic activities through ecotourism and recreational activities.
- · Enhance biodiversity in and around the lakes
- Improve the health conditions of the people living in the lake surroundings.

VI. LAKE CONSERVATION STRATEGIES

A. Lake protection steps:

- Preventing encroachment of lake surroundings for different activities.
- The shore line of the lakes must be properly fenced to protect from encroachment.

B. Lake management steps:

- Construction of sewage treatment plants for treating sewage and letting the water into the lakes.
- · Separating waste water from the storm water.
- The inlets and outlets of the lakes should be identified and need to be monitored at regular intervals.
- Encouraging management and handling of municipal solid waste.
- Beautification of lake bund by landscaping and plantation.
- Plantation on the lake surroundings to prevent soil erosion.
- · Increasing community participation
- Reducing pollution through idol immersion by following Green Ganesha drive i.e., making use of environmentally friendly idols.
- · Environmental education and awareness

C. Lake restoration steps:

- · De-silting the lake bed by dredging
- De-weeding
- Removal of floating aquatic plant species.

VII. LEGAL FRAMEWORK FOR LAKE CONSERVATION IN INDIA

The lakes and water bodies of India are directly influenced by a number of legal and regulatory frameworks. The fundamental duties enshrined in the constitution of India Article 51A (g) states "It shall be the duty of every citizen of India to protect and improve the natural environment including forests, lakes, rivers and wildlife and to have compassion for living creatures."

MoEF (Ministry of Environment and Forests) plays an important role in the restoration and conservation of lakes/water bodies in India. MoEF has implemented NLCP (National lake conservation plan) in 2001 for conservation and management of polluted and degraded lakes in urban areas. The major objectives of NLCP include encouraging and assisting state governments for sustainable management and conservation of lakes.

Acts for the conservation of water bodies:

- Water (Prevention and Control of Pollution) Act, 1974. This act was introduced to ensure domestic and industrial effluents are not allowed to discharge into water courses without adequate treatment. Contravention of this law will lead to punishment for a period not less than six years with fine.
- Environment Protection Act, 1986. This is an umbrella act under which the central government can notify steps to be taken by states for ensuring protection, conservation of the environment, including lakes and other bodies.

Authorities for conservation of lakes:

- · Ministry of environment and forests
- · Ministry of water resources
- · Agriculture ministry
- Other local authorities i.e. Municipal corporations, Water supply boards, Tourism department etc.

VIII. PRESENT STATUS OF SOME OF THE LAKES IN INDIA

A. Dal lake

Dal lake, the jewel of Kashmir valley attracts a number of tourists due to its exotic natural scenic beauty and hundreds of house boats which facilitates tourists in enjoying the peace and tranquility of the whole Kashmir valley. Dal lake is one of the most beautiful lakes of the world and is a home for a variety of flora and fauna. However, this lake is suffering from problems like discharge of sewage and effluents which led to growth of aquatic weeds and water hyacinths due to eutrophication, dumping of garbage from hotels, human settlements, siltation and uncontrolled tourists pressure. A large number of commercial buildings including hotels, restaurants and house boats have reduced the size of the lake.

Dal lake conservation

Under the National lake conservation plan of the Ministry of environment and forests of the Government of India, the restoration and rehabilitation measures undertaken to bring the lake to its original eutrophication free status are construction of siltation tanks, mechanical de-weeding, regrouping of house boats and reforestation of catchment area to reduce erosion and movement of silt.



Figure.4. Excessive Eutrophication infestation by aquatic weeds in Dal Lake



Figure.5. Eutrophic Dal lake with house boats

B. Hussain sagar lake

Population growth and industrialization lead to encroachments and shrinking of lakes in Hyderabad. The famous Hussain sagar was built during 1562(450 years old) which served as a source of drinking water during the Nizam's time was completely polluted. In the last 30 years, the lake shrank more than 50% of its original size. The quality of water in the lake has gradually deteriorated mainly due to the continual entry of untreated domestic sewage and industrial effluents which is the reason for eutrophication. The other reasons of pollution are dumping of solid waste as well as immersion of large number of Ganesh and Durga idols during festivals.

Impact of Idol immersion on lakes

The traditional mud idols have been replaced by plaster of paris statues. Plaster of paris contains gypsum, phosphorus, sulphur and magnesium which do not degrade and forms an impermeable layer at the bottom of the lakes. Particularly, the colours used in making the idols contain the heavy metals mercury, lead and chromiumwhich are potential causes of developing cancer. These materials poison water bodies by increasing the chemical and organic load affecting the aquatic organisms in large numbers, blocking the natural flow of water and causing stagnation and siltation. Due to the concern raised by the environmentalists regarding the pollution of the lakes due to immersion of idols, environment friendly idol immersion is followed which can reduce the pollution load and restore the pristine beauty of the lakes. Immersion of idols in artificial ponds is



Figure.6. Pollution details of Hussain sagar lake



Figure.7. Immersion of idols during festivals in Hussain sagar lake



Figure.8. Disposal of solid waste in Hussain sagar lake

also one of the ways to reduce lake pollution. Artificial or temporary ponds are constructed near the surroundings of the lakes exclusively for immersion of idols. Continuous fresh water supply should be ensured into the ponds to avoid turbidity where the supernatant water overflows through the holes provided to the artificial pond.

Hussain sagar lake conservation

HMDA (Hyderabad metropolitan development authority) has started HCIP (Hussain sagar lake and catchment area improvement project) to improve the quality of Hussain sagar lake.

The following measures are being followed to improve the quality of the lake under HCIP.

A. To prevent encroachment

- · Fencing and bund road formation
- · Plantation on the surroundings

- B. To improve lake ecosystem
 - Installation of fountains to increase dissolved oxygen.
 - · Desilting by dredging
 - · Removal of aquatic weeds

C. To improve recreation activities

- · Beautification around lake
- · Discharge of treated water in the lake

D. To prevent lake pollution

- · Setting of sewage treatment plants
- · Organizing public awareness campaigns



Figure.9. View of Sewage treatment plant at Hussain sagar lake



Figure 10. A Deweeding machine removing aquatic weeds



Figure 11. Beautification around Hussain sagar lake

IX. CONCLUSIONS AND SUGGESTIONS

Urban lakes or water bodies are the first victims of urbanization and their conservation is a sign of healthy and sustainable urban development. Lake conservation strategies if followed strictly by the government and the people will have environmental and ecological benefits.

People should be made aware of importance of lakes and then the laws should be implemented for punishing those who pollute the lakes. There is also need of setting up courts dealing only with environmental issues. Nature has enriched us with a number of resources and it is our duty to do every possible thing to restore it. The same duty is recognized under Article 51A (g) of constitution of India.

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In the next issue (Vol. No.12, June 2017)

- Behaviour of Magnetised Water Concrete Under Different Curing Conditions
- 2. Flexural Behaviour of Reinforced Concrete Beams Using ANSYS
- 3. Response of Reinforced Concrete Structural Components Subjected to Blast Loading
- 4. A Study of Corrugated GFRP Composite subjected to Transverse loading
- Power Saving and Delay Analysis of Adder Circuits using Adiabatic Logic
- 6. Analysis for the Implementation of Capacitive Couple Readout Circuit for Contact-less ECG and EEG
- 7. Cloud Armor: A Trusty Supporting Reputation-based Management for Cloud Services
- Contextual Customisation of Reusable Components for High Cohesiveness in Robust Software Development

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Abstract: These instructions give you basic guidelines for preparing camera-ready papers for CVR College journal Publications. Your cooperation in this matter will help in producing a high quality journal.

Index Terms: first term, second term, third term, fourth term, fifth term, sixth term

I. INTRODUCTION

Your goal is to simulate the usual appearance of papers in a Journal Publication of the CVR College. We are requesting that you follow these guidelines as closely as possible.

A. Full-Sized Camera-Ready (CR) Copy

Prepare your CR paper in full-size format, on A4 paper (210 x 297 mm, 8.27 x 11.69 in). No header or footer, no page number.

Type sizes and typefaces: Follow the type sizes specified in Table I. As an aid in gauging type size, 1 point is about 0.35 mm. The size of the lowercase letter "j" will give the point size. Times New Roman has to be the font for main text. Paper should be single spaced.

Margins: top = 30mm (1.18 in), bottom, left and right = 20 mm (0.79 in). The column width is 82mm (3.23 in). The space between the two columns is 6mm (0.24 in). Paragraph indentation is 3.7 mm (0.15 in).

Left- and right-justify your columns. Use tables and figures to adjust column length. On the last page of your paper, adjust the lengths of the columns so that they are equal. Use automatic hyphenation and check spelling. Digitize or paste down figures.

For the Title use 24-point Times New Roman font, an initial capital letter for each word. Its paragraph description should be set so that the line spacing is single with 6-point spacing before and 6-point spacing after. Use two additional line spacings of 10 points before the beginning of the double column section, as shown above.

Each major section begins with a Heading in 10 point Times New Roman font centered within the column and numbered using Roman numerals (except for ACKNOWLEDGEMENT and REFERENCES), followed by a period, two spaces, and the title using an initial capital letter for each word. The remaining letters are in SMALL CAPITALS (8 point). The paragraph description of the section heading line should be set for 12 points before and 6 points after.

TABLE I.
Type Sizes for Camera-Ready Papers

Type	Appearance					
size (pts.)	Regular	Bold	Italic			
6	Table caption, table superscripts					
8	Section titles, tables, table names, first letters in table captions, figure captions, footnotes, text subscripts, and superscripts					
9	References, authors' biographies	Abstract				
10	Authors' affiliations, main text, equations, first letters in section titles		Subheading			
11	Authors' names					
24	Paper title					

Subheadings should be 10 point, italic, left justified, and numbered with letters (A, B, ...), followed by a period, two spaces, and the title using an initial capital letter for each word. The paragraph description of the subheading line should be set for 6 points before and 3 points after.

For main text, paragraph spacing should be single spaced, no space between paragraphs. Paragraph indentation should be 3.7mm/0.21in, but no indentation for abstract & index terms.

II. HELPFUL HINTS

A. Figures and Tables

Position figures and tables at the tops and bottoms of columns. Avoid placing them in the middle of columns. Large figures and tables may span across both columns. Leave sufficient room between the figures/tables and the main text. Figure captions should be centered below the figures; table captions should be centered above. Avoid placing figures and tables before their first mention in the text. Use the abbreviation "Fig. 1," even at the beginning of a sentence.

To figure axis labels, use words rather than symbols. Do not label axes only with units. Do not label axes with a ratio of quantities and units. Figure labels should be legible, about 9-point type.

Footnotes: 8-point Times New Roman font; copyright credit, project number, corresponding author, etc.

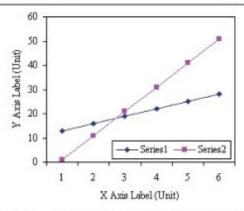


Figure 1. Note how the caption is centered in the column.

Color figures will be appearing only in online publication. All figures will be black and white graphs in print publication.

B. References

Number citations consecutively in square brackets [1]. Punctuation follows the bracket [2]. Use "Ref. [3]" or "Reference [3]" at the beginning of a sentence:

Give all authors' names; use "et al." if there are six authors or more. Papers that have not been published, even if they have been submitted for publication, should be cited as "unpublished" [4]. Papers that have been accepted for publication should be cited as "in press" [5]. In a paper title, capitalize the first word and all other words except for conjunctions, prepositions less than seven letters, and prepositional phrases.

C. Footnotes

Number footnotes separately in superscripts 1, 2, Place the actual footnote at the bottom of the column in which it was cited, as in this column. See first page footnote as an example.

D. Abbreviations and Acronyms

Define abbreviations and acronyms the first time they are used in the text, even after they have been defined in the abstract. Do not use abbreviations in the title unless they are unavoidable.

E. Equations

Equations should be left justified in the column. The paragraph description of the line containing the equation should be set for 6 points before and 6 points after. Number equations consecutively with equation numbers in parentheses flush with the right margin, as in (1). Italicize Roman symbols for quantities and variables, but not Greek symbols. Punctuate equations with commas or periods when they are part of a sentence, as in

$$a + b = c \tag{1}$$

Symbols in your equation should be defined before the equation appears or immediately following. Use "(1)," not "Eq. (1)" or "equation (1)," except at the beginning of a sentence: "Equation (1) is ..."

F. Other Recommendations

Use either SI (MKS) or CGS as primary units. (SI units are encouraged.) If your native language is not English, try to get a native English-speaking colleague to proofread your paper. Do not add page numbers.

III. CONCLUSIONS

The authors can conclude on the topic discussed and proposed. Future enhancement can also be briefed here.

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ABOUT THE COLLEGE

CVR College of Engineering (A UGC Autonomous Institution) was established in 2001, and its twelfth batch of students graduated from the College. CVR is preferred as the No. 1 college among more than 600 colleges in Telangana and AP that started since the year 2000 and was also rated as the #1 coeducational college in pass percentage among nearly 300 colleges under JNTU, Hyderabad for three consecutive semester examinations. It is the expectation of the academic community that CVR is on the successful path to be in the TOP-5 amongst all colleges in Telangana in the next few years.

The College was the first college in Telangana that was promoted by NRI technology professionals resident in the US. The NRI promoters are associated with cutting-edge technologies of the computer and electronics industry. They also have strong associations with other leading NRI professionals working for world-renowned companies like IBM, Intel, Cisco, Motorola, AT&T, Lucent and Nortel who have agreed to associate with the College with a vision and passion to make the College a state-of-the-art engineering institution.

The College has been given Permanent Affiliation by JNTUH and is accredited by NAAC with 'A' grade and also by National Board of Accreditation (NBA). It has also been accorded AAA+ status by Careers 360 on par with decades old institutions in the states of Telangana and Andhra Pradesh.

In keeping with the current global emphasis on green and eco-friendly energy generation, 360kW Solar PV plant has been installed in the campus to meet the power requirements of the college to a significant extent.

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