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EDITORIAL

We are happy to bring out the Volume – 13 of the Biannual journal of our college, CVR Journal of Science and Technology. This Volume is brought out in the first week of December 2017 itself, with the co-operation of all the contributors and the editorial team. We are thankful to the Management for supporting this activity, by encouraging us to publish the journal in colour print. This will enable to decipher the graphs, pictorial representations etc with more clarity. We are sure that researchers will appreciate this.

In this issue the first article is on GAN, the latest area in Deep Learning Networks of Computer Science field. Other areas covered are: SoC Implementation of AES 128 bit Algorithm for IEEE 802.6e, Vehicle Collision Avoidance System, Colour recognition Device for visually impaired persons, SPMSM Drive Control, Crash analysis using ANSYS workbench etc. We have received contributions from other institutes like Osmania University and Madawalabu University, Ethiopia. Copies of the Journals are being distributed to reputed institutions like IITs, NITs and Technical institutes. We expect contributions from these institutes also.

We are very happy to share with our readers that CVR College of Engineering is ranked **among the TOP 5 institutions**, **in the State of Telangana**, as per the **NIRF MHRD rankings**. It is ranked in the **101-150 band** of rankings by the **NIRF**. For a college which is about 16 years old, it is remarkable achievement. This made the management of the college to launch Mission 100, to be among the top 100 institutions in the country. Research activity plays an important role in this aspect. Hope the Journal and the contributors will help in improving the ranking of the institution. We are also happy to share with the readers that the college is **Accredited by NAAC with 'A' grade.** It is expected that the contributors will further enhance the reputation of the college through this Journal.

We have received good number of research papers for review, from our own faculty and from outside our institution also. A rigorous filtration process is done, anti plagiarism check using software, and review by experts are done. Finally research papers were selected for publication in the present volume.

This volume covers research articles in the branches of engineering, Humanities and Social Sciences. The breakup of the papers among the various branches is:

CSE – 3, ECE – 7, EEE – 4, EIE – 1, IT – 1, MECH - 3, H & S- 1.

The management is supporting the research and Ph.D Programmes by liberally sanctioning study leave for the faculty of this college. Faculty members working for Ph.D and on research projects are expected to contribute for the journal. Management is also encouraging the authors of research papers with incentives, based on merit. Some of the research articles accepted for publication in the forth coming Volume 14 are listed in Page No. 111.

I am thankful to all the members of the Editorial Board for their help in reviewing and short listing the research papers for inclusion in the current Volume of the journal. I wish to thank **Dr.S.Venkateshwarlu, HOD EEE and Associate Editor**, for the effort made in bringing out this Volume. Thanks are due to **HOD, H & S, Dr. E. Narasimhacharyulu** and the staff of English Department for reviewing the papers to see that grammatical and typographical errors are corrected. I am also thankful to **Smt. A. Sreedevi**, DTP Operator in the Office of Dean Research for the effort put in the preparation of the papers in Camera Ready form.

For further clarity on waveforms, graphs, circuit diagrams and figures, readers are requested to browse the soft copy of the journal, available on the college website **www.cvr.ac.in**, wherein a link is provided.

Prof. K. Lal Kishore
Editor

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Generative Adversarial Networks (GAN) Review

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Abstract: **Latest research in Deep Learning Networks (DLN), the frontier of machine versus human, is making fast strides into harder problems of learning and cognition. Generative Adversarial networks (GAN) are the state of the art learning networks showing promise in this direction. GANs are actively researched and pursued both in academics as well as business enterprises. An understanding of this new machine learning technique (GANs) and their possible usages are discussed in this paper. Results from a representative problem of one dimensional data are presented.**

Index Terms: **Generative Adversarial Networks (GAN), Convolution networks (CNN), Multilayer perceptron (MLP), Generator, Discriminator, Log likely hood function, statistical distributions and sampling of distributions.**

I. Introduction

With advent and success of artificial neural networks, artificial intelligence (AI) landscape has regained momentum in solving real world problems. Figure 1 shows the landscape of AI in relation to learning networks. Deep Learning is at the center of this momentum.

Human brain being massively parallel in structure and also hierarchical is probably capable of continuous activation both with current as well as future perceptions. Neuronal activations in human brain are influenced by incoming sensory information as well as top-down projections. Top down projections, probably, indicate expectation about future incoming information, which is typical of generative modeling[1]. However, this is different from bottom-up learning models, also called as feed forward learning deep neural networks (DNN). These feedforward learning machines are greatly successful in classification problems which have become important tools in decision making. However, it is difficult to figure out the source of classification errors in these feedforward networks which rely on sensory-input->learn->classify paradigm. Top-down learning, on the other hand, has the potential of explaining the information from sensory inputs by subtracting its predictions from sensor input. However, human brain is not confined to either of the approaches, but presumably a combination of both. From the motivation of the top-down approach of human brain, latest research is focused on Generative Adversarial networks (GAN) which fall in the area of deep learning. Following sections review some of the latest research publications on GAN and bring out an understanding of underlying learning algorithm through one dimensional data. Many of the research publications are still under review.

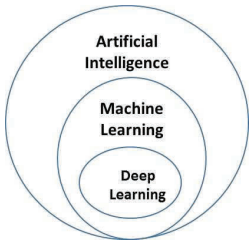

Figure.1 AI landscape

II. Generative Adversarial Networks (GAN)

Learning machines can broadly be categorized as discriminative and generative. While the goal of the former is to be able to classify information (objects in a limited definition) as precisely as possible, the later focusses on understanding the underlying distribution in the input information. Generative modeling attempts to mimic a known input. As an example, it is possible to create a mimicked version of handwritten symbols from the knowledge of a given symbol set or to create new images given a set of images. It would be difficult to distinguish between original and mimicked version of these objects. These Generative models are a kind of unsupervised learning machines. Unsupervised learning initially started with Kohonen feature maps, also called Self Organizing Maps(SOM) and progressed to recent Autoencoders (AE) which have become popular in Deep Learning (many publications on both SOM and AE are available in WEB). Unsupervised learning discovers the structure of the input space. Both deterministic networks based on back propagation (BPN) and probabilistic networks like Restricted Boltzman Machines (RBMS) are examples of unsupervised learning machines. However, these are still limited in the sense they are not completely generative models. Generative Adversarial networks (GAN) are introduced by Ian Goodfellow[2] and are currently being actively researched. Figure 2 describes a general architecture of GAN.

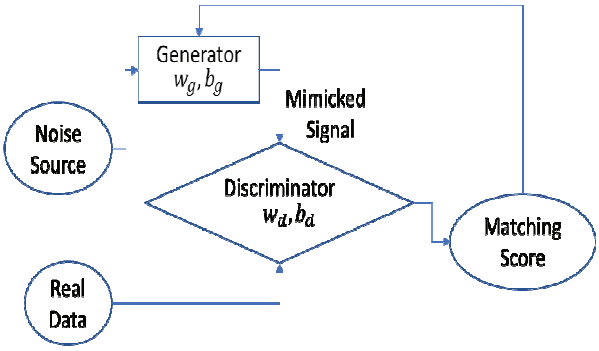

Figure.2 General of a GAN

GAN has two networks, Generative and discriminative, which are simultaneously trained. Generative network tries to discover the underlying distribution in real data without really having seen this data and Discriminative network attempts to estimate the probability that its input is real data and not from Generator. Both the networks can be of any type i.e. multilayer perceptron (MLP), Restricted Boltzmann Machine (RBM), Convolution Neural Network (CNN) etc. Generator objective is to mimic the underlying distribution in real data without really having access to this data. Discriminator tries to distinguish between real and mimicked data. Unlike in single network configuration, learning happens in two networks simultaneously with different objective functions. Training results in arriving at network parameters like (w_g,b_g) and (w_d,b_d) for generator and discriminator. While Generator's objective is to maximize its capability to mimic real data, the discriminator tries to maximize its ability to distinguish between data produced by generator versus real data. Equations 1 to 3 summarize this twin objective in terms of loss functions of Generator network, Discriminator Network and overall Adversarial Network.

Loss Function of Generator : $L_g = -\log(D(z))$ (1)
Loss Function of Discriminator : $L_d = -\log(D(i))$ (2)
Overall Loss Function = $L_g + L_d$ (3)

A tutorial on GAN is presented by Goodfelow[3] and Lili[22]. Following sections review the current literature followed by understanding of GAN using a one-dimensional simulated data implemented in Tensorflow.

III Literature Survey of GAN

Research publications on GAN have started in 2016 and gained momentum in 2017. Alec Redford[4] proposed convolution nets, as used in deep learning, both for the generator as well as the discriminator and applied for image representations. The claim in this paper is centered on using CNNs which are used in supervised learning, for unsupervised learning tasks. Model instability while training for longer epochs is observed. Paulin[5] used GAN based approach for semantic segmentation of images. This paper proposes for the first time a hybrid loss term consisting of (a) multi-class cross-entropy term and (b) adversarial CNN output. Loss term is a function of two parameters belonging to segmentation and adversarial models. Results on PASCAL VOC 2121 data sets indicate improved semantic segmentation accuracy using adversarial model. Arna Ghosh[6] applied GAN for handwriting profile in which deep convolution GAN (DCGAN) are used. The results of experiments are yet to be published. However, work in this area can become useful for detecting forged documents and signatures. The work related is in initial stages. Han Zhang[7] used stacked GANs to generate images from text descriptions. The task of creating photo realistic images from text is divided into two stages (1) sketching the primitive shape with basic color attributes with background generated from noise generator (2) correcting the low resolution image in text description and improving the background. Separate GAN is used for the two stages. Loss functions are similar to what is proposed[2]. Claim is on improved text to photo realistic image generation to other methods like variational auto encoders. Xun Huang[8] uses stacked GAN with pretrained discriminator and hierarchical arranged GANs. Each of the GANs has a loss function consisting of adversarial, conditional and entropy loss terms. Entropy loss term is a contribution in this publication. An interesting application of preserving original identity in an image after aging of person, is studied by Grigory Antipov[9]; this is in contrast to the approach of generating characteristics of a given image of a person. First a GAN is trained to generate good quality images with age characteristics while an optimization is used to improve the image while preserving the aging. Yet another application in the field of entertainment and art, cartoon image is presented by Yifan Liu[10]. In this GANs are used for auto painting (colorization) a given sketch. Pixel-to-pixel model constraints are added to loss function of GAN to better coloring. Marco Marchesi [11] investigated DCNNGAN for generating high quality mega pixel images. Limited data is used as opposed to thousands of images used by the other researchers. Interestingly, an application of GANs for cosmological data is reported by Mustafa Mustafa[12] and the area is gravitational lensing to sense dark energy in galaxies. Standard normal distribution of 64 dimension is used for generator. Network architecture follows DCGAN. Zhigang Li[13] addressed the problem of preserving identity in human faces using GAN with a generator to create faces and FaceNet as discriminator. This is a typical application of generating different facial orientations of a criminal with available frontal view (only front view); Hamid Eghbal-zaseh[14] introduced a general likelihood estimation for assessing the quality of generated images using GAN. The advantage of this method is that it is independent of GAN architecture as well as method of training. Jerry Li[15] brought out the theoretical basis of GAN and explained the collapse of discriminator with a proof. The difference between optimality of discriminator dynamics and first order dynamical systems is compared. Michael O.Vertolli[16] introduced a method of training and evaluation of GAN generated images. Auto Encoders are used in AE-GAN. It is shown that different distance metrics in loss function capture different parameters in images. Chan Shing[17] applied GAN to generate Geological data in sub-surface fields. It is concluded that the flow physics generated by

GAN closely resembles the reference data. Also, PCA performance was observed to be not accurate. Chao Shang[18] has handled one of the important topics in data science i.e. imputing the missing data using GANs. Imputation of missing data of health care dataset as well as MISNST are demonstrated using CycleGAN. It was reported that imputing multimodal data in large data sets was not possible. Compressed sensing MRI, a recent technique to reduce time of acquisition of MRI images, is presented by Tran Minh Quan[19]. Loss function contains not only the regular GAN term but terms containing frequency and amplitude terms. Daniel Mischesanti[20] studied GANs for speech denoising and enhancement and it is compared with classical approach based on STSE-MMSE algorithm and reported better SNR. The above research effort is diverse and indicates that loss function originally formulated by Ian Goodfellow[2], needs modification to suit training and domain requirements. Jaime Deverall[21] presented an interesting application of designing shoes using conditional GAN. The difficulties in training CGAN is attributed to dataset; many ambiguous comparisons are reported. By the time of writing this article more than 100 publications are added in just one year. GAN being very nascent, this paper focusses on bringing an understanding of their architecture and training using a one-dimensional data and single layer perceptron networks both for generator and discriminator networks.

IV ARCHITECTURE OF GANS

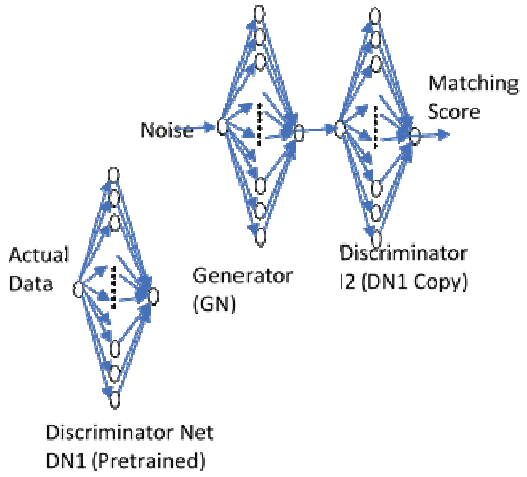

Figure.3 1-D Single layer perceprtron GAN

Figure 2 shows typical building blocks of a simple GAN using single layer perceptron networks for both generator as well as discriminator. Major components of GAN are (a) Generator (GN) and Discriminator (DN) networks (b) noise generator and (c) Optimizer. GN and DN simultaneously perform the tasks of mimicking and recognizing. The learning parameters in this simple network are weights, biases of both the generator as well as discriminator. However, both the generator as well as discriminator networks can be any networks like RBMs and CNNs. The learning function for input to hidden layer is selected as ReLu, but can be anything whereas, the function from hidden layer to output is chosen as sigmoid for discriminator network. Noise source is selected as random sample of random distribution and real data is a randomly sampled Gaussian distribution. Gradient descent algorithm is chosen as optimizer.

Initially discriminator is trained with actual data and part of artificial data. During this phase of training back propagation is applied to discriminator only and generator just generates data based on random sampling of noise source. The learning parameters of discriminator are frozen in this phase. In the second phase, complete adversarial network is trained with generator trying to improve its output based on error reported by discriminator. For demonstration of GAN, an open source code, suitably modified, is used and actual data and corresponding noise are shown in figures 3 and 4.

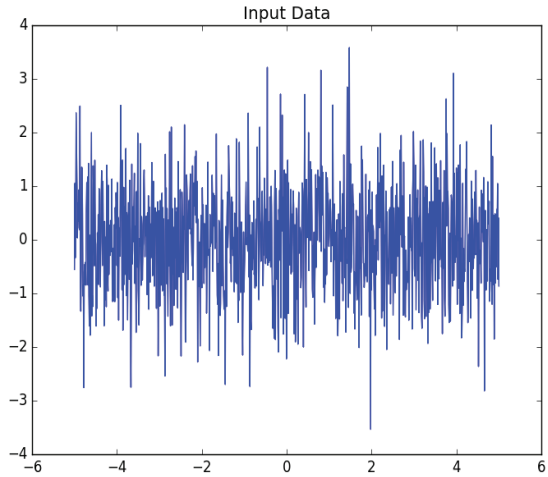

Figure.4 Actual Input to discriminator

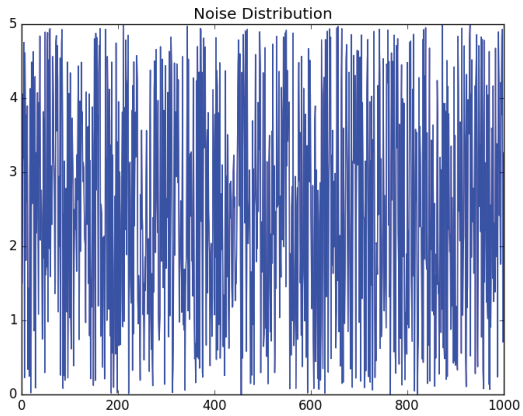

Figure.5 Noise data input to Generator

Figures 6 to 10 describe different outputs of GAN using simulation code. Each figure shows decision boundary of discriminator, real data and generator created mimicked data for different combinations of learning functions of GN and DN. Figures also show performance of GAN with different number of neurons in the hidden layers. Results are produced with 1000 iterations to understand the performance of GAN. It can be seen that for the chosen network, the learning function combination with changing number of hidden layer neurons, the decision boundary

(green line) changes. Some combinations of learning functions fail to discriminate the data. Desired decision boundary is to have probability of 0.5 i.e. the DN should not be able to clearly discriminate between real input and mimicked input.

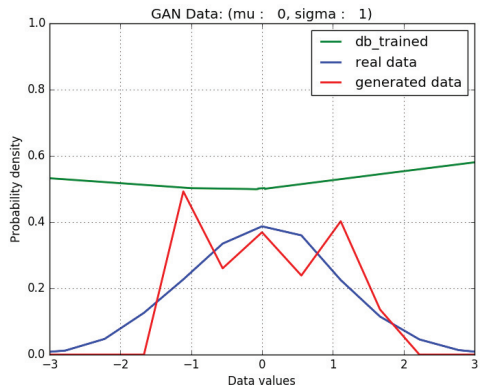

Figure.6 GAN outputs with sigmoid learning function (GN&DN) 32 neurons in hidden layer

Figure.7 GAN outputs with sigmoid learning function (GN&DN) 256 neurons in hidden layer

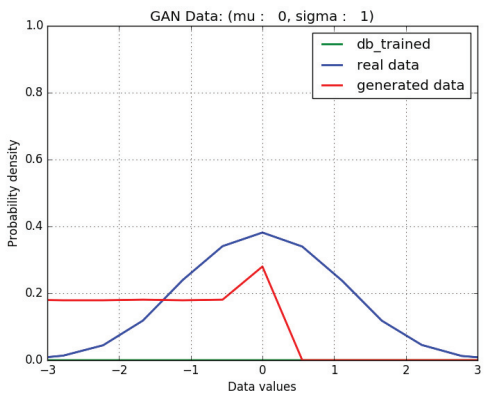

Figure.8 GAN outputs with ReLu learning function (GN&DN) 32 neurons in hidden layer

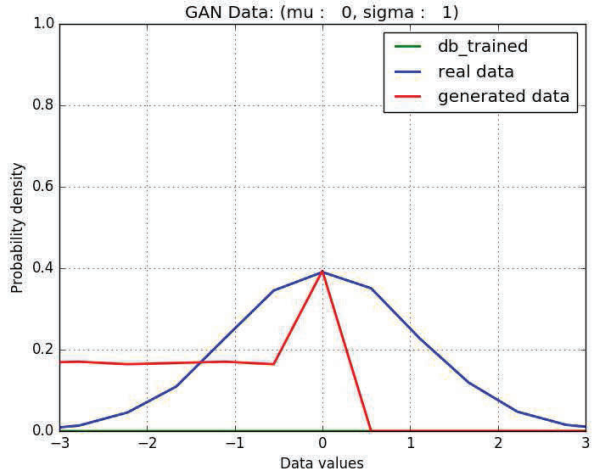

Figure.9 GAN outputs with ReLu learning function (GN&DN) 256 neurons in hidden layer

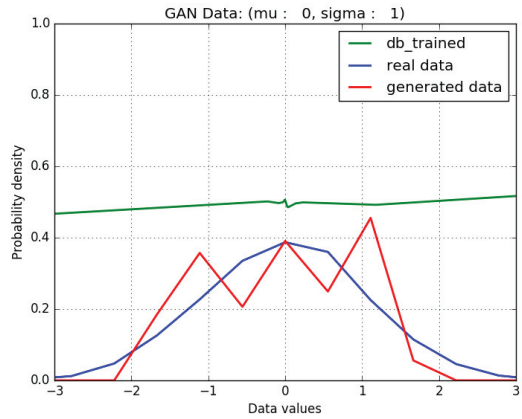

Figure.10 GAN outputs with mixed Sigmoid and ReLu learning functions and 32 neurons in hidden layer

V. Conclusions

GANs are the most recent machine learning algorithm and they are based on two player game theory. The research in this area started very recently [2016-17] and application areas include medical imaging, art, forensic sciences, industrial processes and power plant real time simulation etc. It is seen that considerable effort is required to arrive at an optimum architecture of Generator and Discriminator networks. And the selection of an optimizer for training is a serious issue. There is scope of introducing different loss functions for different applications. It is expected that good amount of research reporting will come up by 2018. The success of GAN as a possible disruptive technique largely depends on (a) simple and robust optimizer (b) easy rules to decide overall GAN architecture for different applications. The authors conclude that GANs offer a good scope for both academic and industry application development in the immediate future.

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MUTAWEB-Mutation Testing Tool for Servlet based Web Applications

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Abstract: **Mutation testing of web applications requires more sophistication and newer operators for greater efficiency to detect defects early in the testing cycle. A plethora of mutation testing tools are available for performing mutation testing. However for performing mutation testing of web applications there is only one tool available which is also available for web applications developed using Java Server Pages. The tools are also not addressing defects related to session management, cookie management while the logical, relational, operators and their corresponding mutant code are being tested. In the current work, an endeavour to implement some novel mutation operators pertaining to servlet based web applications has been made and a simple tool to implement some of the novel operators has been made successfully. This work will certainly assist the web application testers in quickly realising some key defects pertaining to session management and cookie management which might have been otherwise overlooked by the developers given the faster release cycles of the web applications.**

Index Terms**: mutation testing, web applications, testing tool, session management, cookie management.**

I. Introduction

Mutation testing is one of the testing techniques which is based on seeding mistakes into the code at known points and thereby observing the results of the test cases run. If the output is as expected with the original code, then it is indicative of a slip in the original code as the output is supposed to deviate from the expected result. If the output does not deviate from the expected result, then the mutated code which is called the mutant is said to be live otherwise dead. Dead mutants direct us towards a flawless code whereas a live mutant signifies a buggy code. To assure that the code is buggy, a retest of the code with an increased input sample data is performed, of which the results are further analysed. Suppose the results are found deviating from the expected results despite the increased sample data, then a back tracking is performed to analyse the buggy code and derive at the root cause for the defect [1].

Mutation testing can also be employed in testing the web applications, which are difficult to test in contrast to the standalone applications given the aspects of web application development like heterogeneity of development environment, cross platform deployment, browser incompatibility et.al. [2]. For performing mutation testing of web applications defining some operators for various possible defects that can be unearthed is done in earlier works where approximately 150 operators are proposed in various works for testing of applications [10]. Around 5 operators are implemented in the current work for testing of web applications.

There are many tools which perform mutation testing on various standalone applications. Applications like MuClipse, PIT, Jumble, etc., perform mutation testing on Java programs and applications like Cosmic ray and Mutpy does the same on python programs. But there are less number of tools which apply mutation process on web based applications .A tool which performs mutation testing on Java based applications (Servlets and JSPs) was proposed. This tool checks the status of mutation process by comparing log files which are generated by the tool. However, not all mutation operators generate log files. After applying mutation and running the updated application, the difference can be directly seen on the output (Webpages). For applications where applying mutation does not show any difference in the output, then log files before and after mutation are generated and both log files are compared to tell whether the mutant is live or not.

Section II provides a discussion on some of the existing mutation testing tools and their key features. Section III discusses the five novel mutation operators implemented as part of this MUTAWEB for testing web applications. Section IV provides conclusions and a peek into the future enhancements possible with this work.

II. Related Work

Various tools were earlier proposed and implemented for mutation testing of different applications [2, 3, 4, 5, 6, 7, and 10]. A total of 6 tools were taken into study for the development of MUTAWEB, the summary of which is presented here.

A. MuClipse tool

It is a mutation testing tool for java language. It can only mutate java based classes. It is a plug-in .To use this tool first it should be installed in eclipse. It provides a user interface in which different mutation operators are displayed in the form of check boxes. After choosing them, these operators will be applied on the existing java code (this is called mutating code). Junit is used here to run the tests on original code and mutated code. Muclipse compares both the results and if the results are same then the mutant is alive or else mutant is killed. Muclipse maintains the mutant score and displays them to the tester [5].

B. Judy tool

It is a mutation testing tool that supports only java language. It is a command line tool. This tool also covers all the branches in a given lines of code. From generation of byte code to execution of mutants, all can be done by this tool. Junit is used to run the tests for both original and mutated code. This was developed by Madeyski and Radyk [6].

C. WebMuJava

It is web mutation testing tool. It is an extension to Mujava. This tool was developed by Upsorn Praphamontripong, Jeff Offutt, Lin Deng, and JingJing Gu. This tool mutates Servlets and jsps. The mutated files are compiled and included in webapp and then the web app is tested. The tests for normal testing are completely different when compared to this mutation testing. Here the tests are created manually in the form of requests and these were stored using htmlunit, selenium, jwebunit. After that, these tests are applied automatically on the web application and the output is compared every time to generate the mutation score (Which is no of mutants killed to the total no of mutants inserted) [3].

D. Cosmic-ray

It's a mutation testing tool in python. It is an Open source command line tool which is not fully developed, and contributions through GitHub are in progress. This tool mostly mutates the code at AST (Abstract Syntax Tree) level. Developed by Austin Bingham, a founding director of Sixty North, a software consulting, training, and application development company Mutpy offers a new range of mutation operators for the testing of python programs in an efficient manner [9].

E. Mutpy

It is a mutation testing tool in python desktop applications and also web applications (DJANGO WEB DEVELOPMENT FRAMEWORK FOR PYTHON). This tool supports unit test module, and generates reports which can be human readable format. This Mutpy tool does not provide any user interface. It is a command line based tool. At present this tool supports 27 mutation operators [7].

F. Jumble tool

It is a mutation testing tool which mutates the code a byte code level. This tool works faster as it will work under bytecode level. This tool supports JUnit to perform tests on java classes. This tool returns mutation score and no of mutants for which the tests failed for the user for analysis. This tool does not return the mutants for which the tool passed. Jumble was developed in 2003-2006 by a commercial company Reel Two [4].

G. PIT tool

It is a mutation testing tool developed by Coles. It is open source tool. This tool generates mutants quickly. There are 4 phases: mutant generation, test selection, mutant insertion, and mutant detection. Like jumble tool pit also performs mutation at bytecode level. Tool is used as a command line tool as well as an eclipse plugin. The latest version of PIT released is 1.1.4 [8].

A summary of the tools under study is presented in the Table 1 highlighting the language in which each tool is developed and the languages supported by each tool.

TABLE 1
SUMMARY OF TOOLS UNDER STUDY

S no.	Tool Name	Language Developed	Language Supported	references
1	MuClipse	Java	Java	[5]
2	Judy	Java	Java	[6]
3	WebMuJava	Java	Web applications	[3]
4	Cosmic-ray	Python	Python, Django	[9]
5	Mutpy	Python	Python	[7]
6	Jumble	Java	Java byte code	[4]
7	PIT	Java	Java	[8]

III. IMPLEMENTATION

In the present work, 5 operators have been incorporated and tested with mutating the web application to demonstrate the error discovery.

Initially, the web application under test should be placed in the folder where the testing tool is present. Its web.xml is updated with the files of the application. The main page of the application is executed. Here, the file to be mutated is given as input and the type of mutation operator is to be selected. Some operators require generation of log file before mutation and a section for doing the above process is provided. The log file generation code is inserted into the file and the updated application has to be executed in order to write log code into a log file. Then another section which

also takes input as a file name and type of operator is provided which now applies mutation and also modifies the logger code inserted previously. The application is executed again in order to generate another log file. A point to be noted is that the file name and the type of operator selected before and after applying mutation must be the same. After both the log files are generated, a servlet code which compares the contents of both log files is executed. The status of the mutation is displayed (Live or dead). After this, the contents of both log files are cleared. Before mutation is applied, a copy of that file is created and after executing the log checking servlet, the contents of mutated file are updated with its original contents.

Some operators do not require log file generation and the results of mutation can be seen in webpages. The application where the change is likely to be seen is to be noted down manually. Then after applying mutation operator, the updated application is re executed and the differences are written to a log file. Comparing both those web pages manually, we can say whether the mutant is alive or not. Again, the mutated file contents are updated with its original contents. This is the basic and overall working of MutaWeb tool.

A. DSID: Session Invalidation Function Deletion

When a user logs out from an application, the session information of the user has to be destroyed. So if anyone tries to open the profile url even after logging out, the server will redirect the user to the login page. This operator will delete the method which performs the session invalidation process. This is a security constraint where applications opened in public area networks are prone to these problems if the session operations are not handled correctly. Figure 1 shows the the rendering of profile page of a sample application under test. Figure 2 refers to the rendering of the profile page requesting the user to re login as the session is expired. Figure 3 refers to the rendering of the same page which is unexpected after the introducing the mutated code.

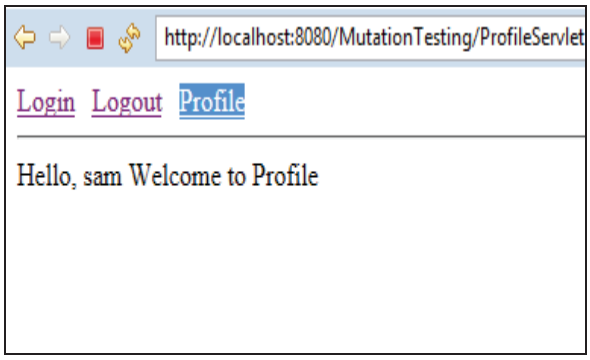

Figure 1. Profile before logout and before applying mutation

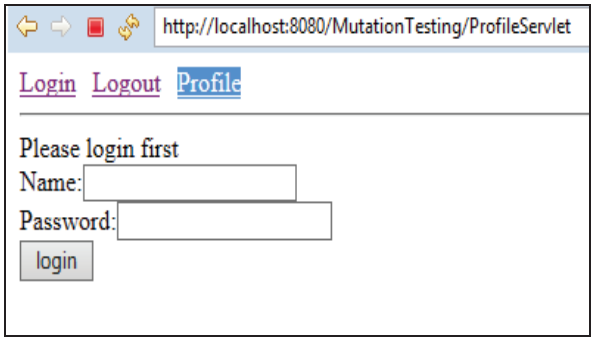

Figure 2. Profile after logout and mutation applied

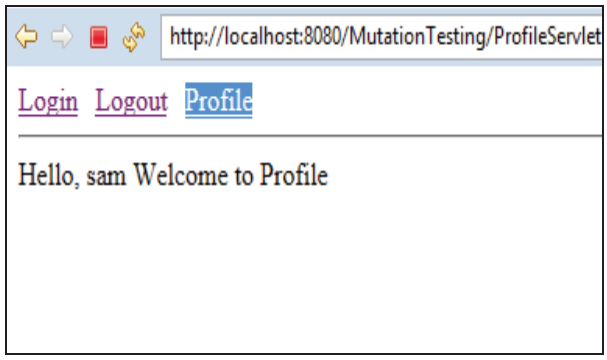

Figure 3. Profile after logout and after applying mutation

B. DACD (AddCookie Method Deletion):

Cookies are used for storing information like username, password, session ID, etc. All these are stored in the form of key value pairs. Once a Cookie table is created, objects of any name can be created and that can modify, add and delete cookie table contents. So an operator which deletes a method which adds cookie information into cookie table is implemented.

Usually cookie information is not displayed on the webpages. The user of that web application might not the difference in the content displayed before and after applying this DACD mutation operator. In this case, log files are introduced. Two log files are created, one for storing information before applying mutation and the other one for storing information after mutation operation is applied. The contents of both the log files are compared and its status is displayed. If contents of both the log files are same then we say mutant is alive else mutant is dead.

C. DHBR (HTTP Boolean Replacement):

When a session is created, usually a session variable with the username or ID is set. After the user clicks logout, the session is destroyed and the session variable's value is set to null. The parameter to this session creation or accessing method is a Boolean operator. This operator will invert the Boolean parameter in the method and run the mutation process. In both the cases, this method will try to access the current session. The difference comes after this step. If the parameter is true, then it will create a new session if a current session does not exist. If the parameter is false, then it will not create a new session even if a current session does not exist.

In any part of the application, the session maybe accessed by using the session creation or accessing method. So when we modify the Boolean variable from false to true and if that session variable is accessed, then its value is set to null. Here, the difference can be seen in the output (webpages) and there is no need of any log file concept.

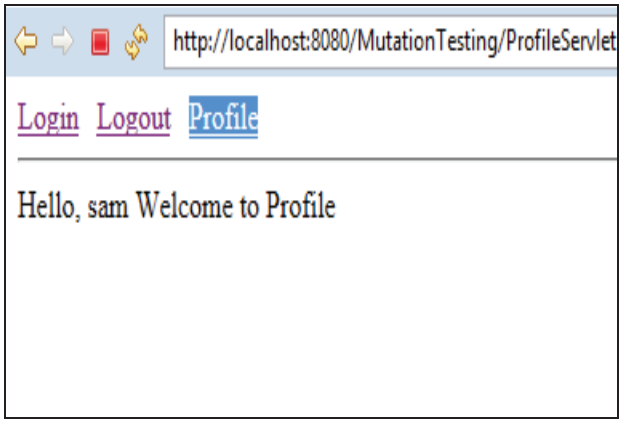

Figure 4. Profile before Mutation

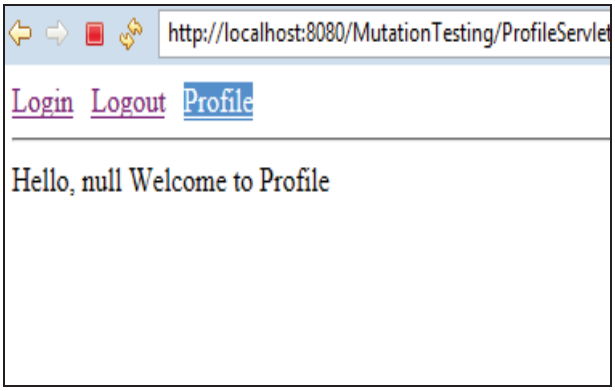

Figure 5. Profile after Mutation

D. DFIR (Forward Include Replacement):

In Web Applications, redirecting to other pages is a common feature. However, the control is not transferred to the redirected web page. Transferring the control feature is provided by the RequestDispatcher class in Servlets. When "include" attribute is used for redirecting to other webpage, and then the control is transferred to the called webpage and after its execution gets over, the control is returned back to the called webpage. So all the statements after the method call are executed. In the case of usage of "forward" tag, the control is not returned back to the called webpage but all the statements are after the method call are not executed. The statements related to response objects are not executed as control is transferred to the other webpage.

This operator will invert "include" to "forward" and test the application whether it is working well with the redirection of pages and transfer of control operations. Figure 6 and Figure 7 show the rendering of the login page with and without the mutated code.

Figure 6.Login before Mutation

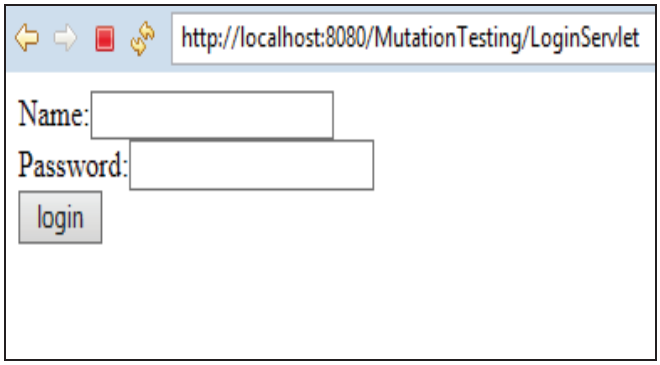

Figure 7.Login after Mutation

E. DRDUR (RequestDispatcher RLReplacement):

Like action string in html form tag and responseObject.sendRedirect method are used for redirecting to other pages, RequestDispatcher also does the same thing but provides an additional feature to transfer control to other webpage. However, the developer should also check whether the program sent a request to the correct expected webpage. So this operator will apply mutation in such a way that it will replace an existing URL in the RequestDispatcher with another URL. Figures 8 and 9 demonstrate the testing of requeste dispatches method.

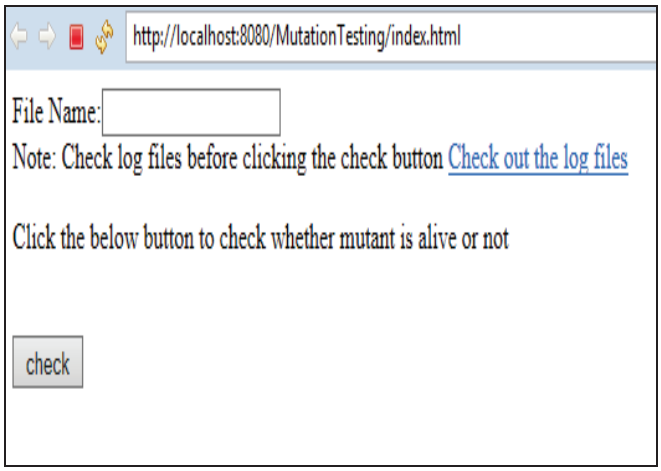

Figure 8. Servlet Redirection before Mutation

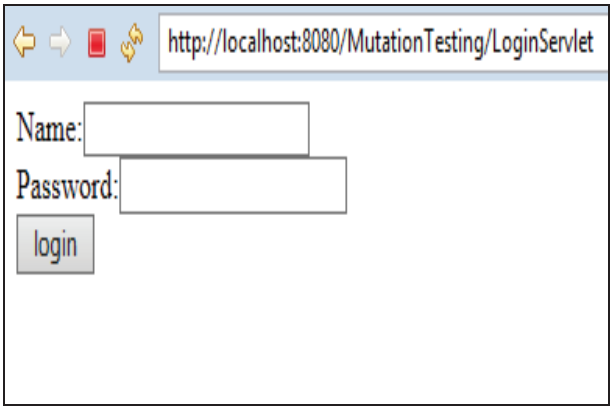

Figure 9. Servlet Redirection after Mutation

IV. Conclusions

The above mutation operators are focussed on the session and cookie management of servlets. The tool developed could serve as a first hand aid to showcase some of the overlooked errors in the code as soon as the testing commences. However there is scope for inclusion of some more operators pertaining to servlet based web applications and the efficiency of operators to be measured against conventional testing strategies.

There is a scope for improvement of the tool to make it working dynamically online rather than like a standalone tool which is currently the need of the industry.

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A Hash Map based Binary Matrix Approach for Text Document Classification

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Abstract: **The conventional model uses the sequential approach for classifying the text document. In this paper, a new approach for the text document classification is proposed. The proposed method preserves the sequence of words that are occurring in a document. The data structure that is used in this method to preserve the word sequences is called "Binary Matrix". A classification technique is also proposed for classifying the text document. To index the terms, it uses Hash Map and this is associated with the list of class labels of the document in which the word is present.**

Index Terms: **Text Document, Hash Index, Hash Map, Binary Matrix, Classification**

I. Introduction

The World Wide Web (WWW) is widely distributed and dynamic information gallery. The total number of websites have grown from 130 in 1993 to 1 billion in 2016. The number of search queries per day started to skyrocket. In 1998 Google saw 9800 queries per day which grew to 40,000 searches per second and amounts to 3.5 billion searches per day [1] and these numbers are increasing rapidly every day.

Internet and corporate, spread across the global produces textual data in exponential growth, which needs to be shared, on need basis by individuals. If the data generated is properly organized, classified then retrieving the needed data can be made easily with least efforts. Hence the need of automatic methods to organize and classify the documents become inevitable. Due to such exponential growth in documents, the increase usage of the internet by the individual takes place.

Automatic classification refers to assigning the documents to a set of predefined classes based on the textual content of the document.

The classification can be Flat (or) Hierarchical

Flat Classification: In this there is no structure defined that specifies the relationship between the different documents. When the number of categories increase, it becomes difficult to search the category. [3, 7]

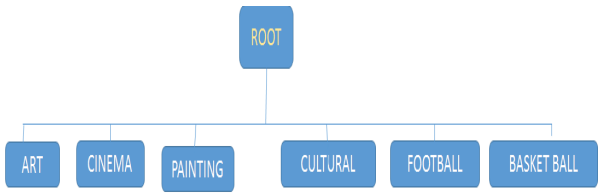

Figure 1. Flat classification

Hierarchical Classification: It uses Divide – and – Conquer approach. The classification can be repeated on the document in each sub category until it reaches to leaf and can be classified further. [3, 7]

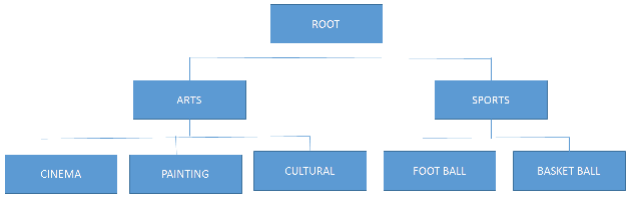

Figure 2. Hierarchical classification

Binary Classification: Initially Machine Learning is applied for binary classification where the classifier determines whether the document belongs to some pre – defined category or not. It is a kind of single label classification where the classifier decides whether the document belongs to a category or not. This kind of classification is useful to decide whether the mail received belongs to inbox or spam category. [6, 7]

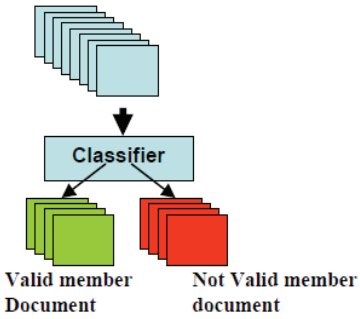

Figure 3. Binary classification

Single Label Multi Class Classifier: In some situations where there are more pre – defined categories present, the binary classifier needs to be modified for the classification of document into multi categories. [6, 7]

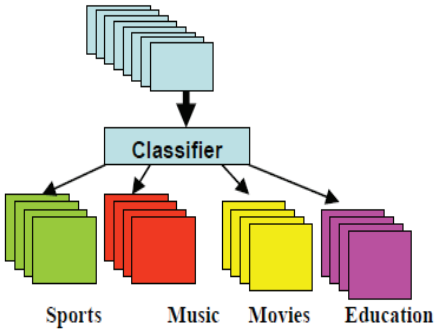

Figure 4. Multi-class single label classifications

Multi Class Multi Label Classifier: A single document may be classified into more than one class. This is called multi class or multi label classifier. [7]

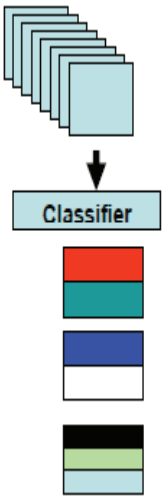

Figure 5. Multi-class multi-label classifications

II. Related Work

A. Representation Models

The representation model for the text classification can be classified into two categories: those based on endogenous information of the given corpus (i.e. Content – based models) and those exploiting additional, external information in order to get more on textual information (i.e. Content – aware models). [6]

Vector Space Model (VSM) is an algebraic model for representing text documents as vectors of identifiers, such as, index terms. The major limitation of the VSM is that the correlation and context of each term is lost which is very important in understanding the document. [11]

Ontology Model can be used as a conceptual model which maintains a dictionary like structure for retrieving the information from the text document. It basically describes the document as a multi-dimensional vector that would encompass not only words in the document but also concepts. [10]

N – gram is a sequence of terms, with the length of N. Mostly, words are taken as terms. Each word from the document is represented as a set of overlapping N – gram. If N – gram is found in all the document, it gives no information about the context between the documents.

Latent Semantic Indexing (LSI) is one of the most popular linear document indexing methods which produces low dimensional representations using word co – occurrence which could be regarded as a semantic relationship between terms. It minimizes the reconstruction error (the Euclidean distance between the original matrix and its approximation matrix). The deficiencies of LSI are, it include few negative values in the reconstruction matrix which is difficult to explain by the model. [12]

Locality Preserving Indexing (LPI) is proposed for document indexing. Each document is represented as a vector with low dimensionality. Unlike LSI, which determines the global structure of the document space, LPI discovers the local structure and obtain a compact document representation sub space that best detects the essential semantic structure. LPI is based on the manifold theory. It tries to find the linear approximation to the Eigen function of the Laplace Beltrami operator on the compact Riemannian manifold. It is capable of discovering non – linear structure of the document space to some extent.

After the representation is given to the document then the classification task is performed which can classify the document to predefined category. Many statistical computational models are available and are developed based on the Naïve Bayes Classifier [5], K-NN Classifier [8], Centroid classifier [9].

III. Proposed Method

The proposed text documentation classification system avoids sequential matching of terms during representations and proposes to index the term in hash map. An efficient index scheme for preserving the sequence of occurrence of words in a text document a “Binary Matrix” is used.

Let there be c – classes and each having n number of documents, extract the words from each document. After doing some text processing, each word of the text document is labeled with the class in which the word is present. If the word is present in the text document of more than one class the label consists of all class names using hash map. [2]

The input to the proposed classifier is a text document and knowledge base processing is done on the text document to extract the words from it and constructs a Binary Matrix to decide for which class the document belongs to. The output of the classifier is the class to which the text document belongs.

Limitations:

1. If the length of the sub substring is same in multiple classes, FCFS method is used to label the document with class.
2. The tolerance factor if the length of the sub string is differing by atleast one is not addressed.

IV. Approach

In the proposed approach, a large data set is being used to verify the classifier. The hash map is used for indexing the term present in the document. Hash indexes are basically very much useful than B – Tree because we need to go all the way to the leaf node while searching in B – Trees. A suitable size of hash table will give a complexity of O(1)

and is not the same with B – Tree where it is not a constant and has the complexity of O(log n). For representing the data in the proposed approach we use hash map with a key – value pairs where the key will be representing the terms present and value is corresponding to the class in which the document is present.

Let there be four classes C1, C2, C3 and C4 having documents. Assuming that, the following are list of terms extracted from all the documents of the different classes:

C1 = Brilliant, Performance, Excellent, Republican, Underdogs
C2 = Republican, Country, Excellent, Splendid
C3 = Technology, Contribute, Common, Champion, Lead
C4 = Quick, Champion, Excellent, Lead, Technology

Table I shows the hash map constructed for the above classes

TABLE I.
HASH MAP CONTENT

Key	Value
Brilliant	C1
Performance	C1
Excellent	C1, C2, C4
Republican	C1, C2
Underdogs	C1
Country	C2
Splendid	C2
Technology	C3, C4
Contribute	C3
Common	C3
Champion	C3, C4
Lead	C3, C4
Quick	C4

Once the knowledge base is ready, the system can be given the test document or the query document as an input to the classifier. The classifier then creates a Binary Matrix for the test document and the knowledge base present. Binary Matrix is the one that contains only 0's and 1's as its entries. It has the dimension C * T_q [4]

Where, C is the number of classes and
T_q is the number of terms in the query / test document after pre processing

The hash map is then accessed to search for the occurrence of each term in the test / query document. If a term T_i exists in a particular class C_j, then the entry into the binary matrix will be 1 otherwise it is set to 0. If M is a binary matrix, it will be given as [4]

$$M_{ij} = \begin{cases} 1 & if\ T_i \in C_j \\ 0 & otherwise \end{cases}$$

Let the test / query document containing the following terms after processing

T_d = Brilliant, Champion, Technology, Republican, Contribute, Quick

Table II shows the binary matrix with the entries for the test document words against the knowledge base.

TABLE II.
BINARY MATRIX STRUCTURE

	Brilliant	Champion	Technology	Republican	Contribute	Quick
C1	1	0	0	1	0	0
C2	0	0	0	1	0	0
C3	0	1	1	0	1	0
C4	0	1	1	0	0	1

Once the Binary Matrix is constructed it will be containing the value 1 for the terms that are identified in a specific class. These 1's are representing the substring available in the given test document.

In order not to lose the correlation and semantic of the sentence all the consecutive 1's i.e. the longest substring will be identified in the binary matrix. Once the longest substring is identified then the corresponding class in which the similar substring is present will be labelled as the class for the test / query document.

V. SYSTEM ARCHITECTURE

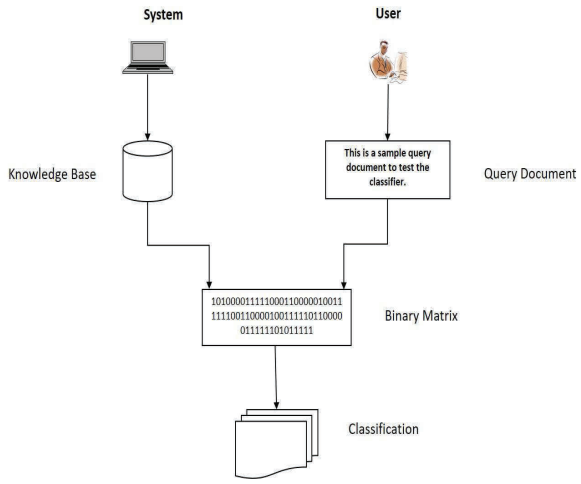

Figure 6. Architecture of Classifier

VI. Research Methodology

A. Knowledge Base Creation:

Let there be K number of classes (C1, C2, C3, . . ., CK), each containing n number of documents.

Step 1: Extract all the words from all the documents in the class
Step 2: After extracting the words from a class remove stop words and perform stemming to drop unnecessary words.
Step 3: Remove the duplicate words after Step 2.
Step 4: Store unique words into hash map with its class identification. i.e. <word – class> pair.
If the word already exists in the hash map, simply add a new class name to the <word – class> pair, otherwise add a new word and its class pair to the hash map for the first occurrence of the word.
Step 5: Repeat Step 1 to Step 4 to process all classes.

Algorithm 1. Knowledge base creation

B. Binary Matrix Construction:

After the knowledge base is created, it is accessed for constructing the binary matrix.

Step 1: Extract the words from the test / query document
Step 2: After extracting the words from a class remove stop words and perform stemming to drop unnecessary words.
Step 3: Binary Matrix is constructed with both knowledge base classes and extracted words of the test document.
Size of Binary Matrix = Number of Knowledge Base Classes * Number of Extracted Words in Test Document
Step 4: Depending on the occurrence of the word in a particular class place an entry into the binary matrix as 1 or 0

Algorithm 2. Binary Matrix Construction

C. Finding Class:

After the binary matrix is constructed containing 0's and 1's, identify the class for the test document. Each row of binary matrix will be representing a binary string.

Step 1: Look for a row with a longest substring containing only 1's
Step 2: Declare the corresponding class as the class the test document belongs to.

Algorithm 3. Finding a class for the test / query document

VII. Experimental Setup

The dataset that is used for the experiment is taken from BBC dataset. The test run was conducted using the data set against classifier. The test results are as shown.

A. Preprocessing:

Simple text processing is done on the dataset available to remove the stop words and perform stemming on the text documents.

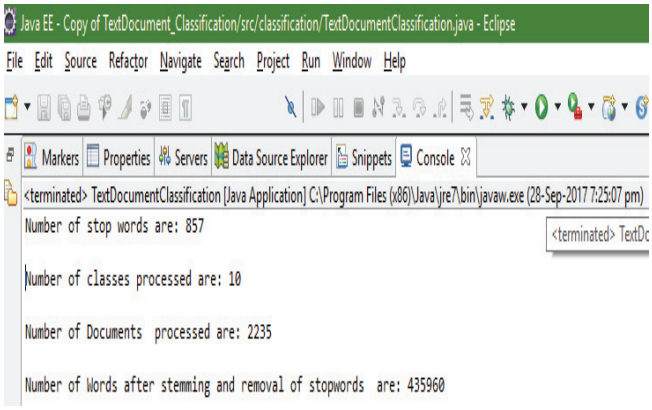

Figure 7. Pre Processing of the Classes

B. Phase 1: Knowledge Base Creation

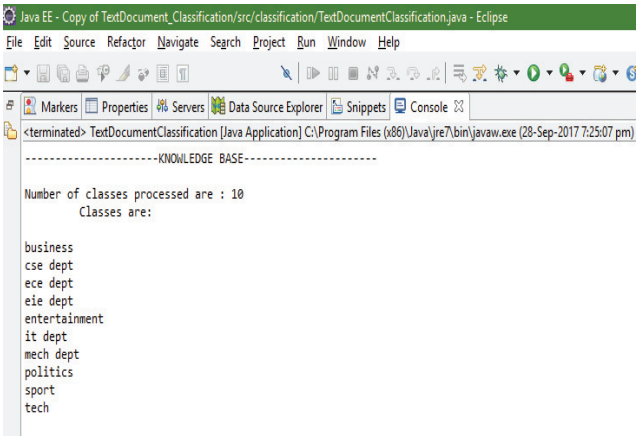

Figure 8. Knowledge representing no. of classes

C. Phase 2: Binary Matrix Construction

After the Knowledge Base is ready the classifier is given this and the test document as input. The classifier then extract the words available in the test / query document.

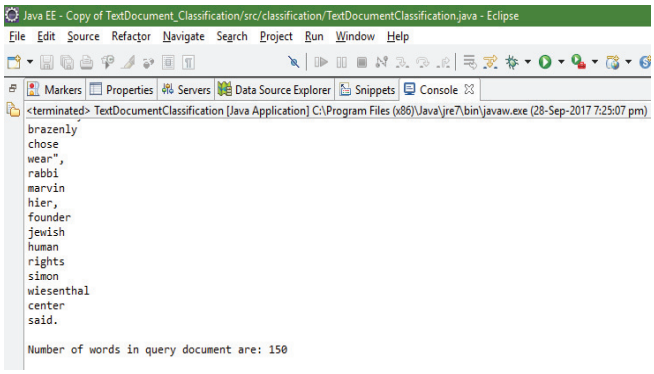

Figure 9. No. of words extracted from test document

Then after the words are extracted from the query document the Binary Matrix is constructed with the required dimension.

```
----------BINARY MATRIX---------

size of binary matrix is: 10*150

After Binary Matrix Construction:

0   1   0   1   1   1   1   0   1   0   0   0   1   0   1
0   0   0   0   0   0   0   0   0   0   0   0   0   0   0
0   0   0   0   0   0   0   0   0   0   0   0   0   0   0
0   0   0   0   0   0   0   0   0   0   0   0   0   0   0
0   1   1   1   1   1   1   0   1   1   1   1   1   1   0
0   0   0   0   0   0   0   0   0   0   0   0   0   0   0
0   0   0   0   0   0   0   0   0   0   0   0   0   0   0
1   1   1   1   1   1   1   1   1   1   1   1   1   1   1
0   1   0   1   1   1   1   0   1   0   0   1   1   0   1
0   1   0   1   1   1   1   0   1   0   1   1   1   0   0
```

Figure 10. Binary Matrix for the test data

D. Phase 3: Labeling the Class

Later the classifier will identify the longest substring from the binary matrix and assign the test/query document with the class label.

```
0   0   0   0   0   0   0   0   0   0   0   0   0   0   0
0   0   0   0   0   0   0   0   0   0   0   0   0   0   0
0   1   1   1   1   1   1   0   1   1   1   1   1   1   0
0   0   0   0   0   0   0   0   0   0   0   0   0   0   0
0   0   0   0   0   0   0   0   0   0   0   0   0   0   0
1   1   1   1   1   1   1   1   1   1   1   1   1   1   1
0   1   0   1   1   1   1   0   1   0   0   1   1   0   1
0   1   0   1   1   1   1   0   1   0   1   1   1   0   0

The query document is belongs to ->    politics
```

Figure 11. Class labeling

VIII. Conclusions

A new text document classification algorithm using hash indexing is proposed that basically makes use of a new data structure called "Binary Matrix" which is used to preserve the sequence of terms in the test document. Even though the term sequence of the test document is preserved the algorithm did not preserve the sequence of terms of the training data. In order to speed up the classification the representation model and the data structure are very useful. Addition of the new classes and deletion of the existing classes can also be performed easily using hash mapping.

The experiment is also performed on the New Groups articles where its results were accurate.

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SoC Implementation of AES 128 bit Algorithm for IEEE 802.16e Mobile WiMax Standards

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Abstract: **Wireless Technology plays a very vital role in data transmission process. The most widely used wireless technology standard is IEEE 802.16. Especially the basic standards like Zig-be, Li-Fi, Bluetooth and Wi-Max be the most widely used for connecting point to multipoint networks wirelessly in a secured environment. Security is the main issue of any transmission system in today's world. Many security algorithms were proposed for the MAC layer in Wi-Max but most commonly used is AES (Advanced Encryption Standard) algorithm. In this paper 128-bit AES algorithm is implemented in CTR mode. CTR mode is preferred compared to other modes because it avoids data dependency both in encryption and decryption process. All the Blocks were designed using Verilog HDL, simulated using ncvlog simulator, synthesized in cadence- RTL Complier and finally implemented in Soc Encounter using GPDK 45nm technology libraries.**

Index Terms**: AES Encryption/Decryption, Galois field, CTR mode, RTL Compiler, SoC Encounter.**

I. Introduction

Security is the main issue both in wireless and wired communication. Nowadays wireless communication is growing vast. Broadband Wireless Access (BWA) has been serving enterprises and operators for years, to the great satisfaction of its users. However, the new IP-based standard developed by the IEEE 802.16 is likely to accelerate adoption of the technology. It will expand the scope of usage i.e., the possibility of operating in licensed and unlicensed frequency bands and unique performance under Non-Line-of-Sight (NLOS) conditions. The most important features of Wi-MAX are Quality of Service (QoS) for real time video conferencing and orthogonal frequency division multiplexing in physical layer of Wi-MAX. Design similar to OSI model, Wi-MAX [2] uses two layers namely, physical layer and data link layer. MAC layer in Wi-MAX is nothing but data link layer in OSI model and is connection-oriented [2]. MAC layer mainly consists of three sub layer MAC CS, MAC SAP and MAC Common Part Sub Layer (MAC CPS) [3]. The main requirement of end user being the security of data and that service provider to view unauthorized network access. To solve many security issues, many protocols like wired equipment protocol (WEP), Li-Fi, Zig-be, Bluetooth and finally AES. WEP was widely used till 2009 but was broken by brute force attacks. Finally, Rijndael AES which assures more reliable and data authentication remains to be the main security issues which were offered by Rijndael AES in counter mode with Cipher Block Chaining (CBC- MAC) mode.

II. Wi-Max Layer Security

The link between upper layers and MAC layers used in Wi-MAX [1, 8] standard is shown in Figure 1**.** The security issues are handled in these layers. Being the core part of IEEE 802.16e, MAC-CPS defines all the processes required for the proper transmission such as bandwidth requirements, connection establishment and management. The connection between the MAC CPS and convergence sub layer (CS) is established by MAC service access point (MAC SAP). SAP also does other functions like carrying out the communication process, connection and transportation of data over the channel. Encryption and Decryption process are performed by privacy sub layer by receiving the data from higher layers. Processes like authentication and secure key exchange between base station and subscriber station are also performed by security sub layer [3, 5]. Encapsulation and privacy key management are two set of protocols required for the smooth condition of the processes performed by security sub layer.

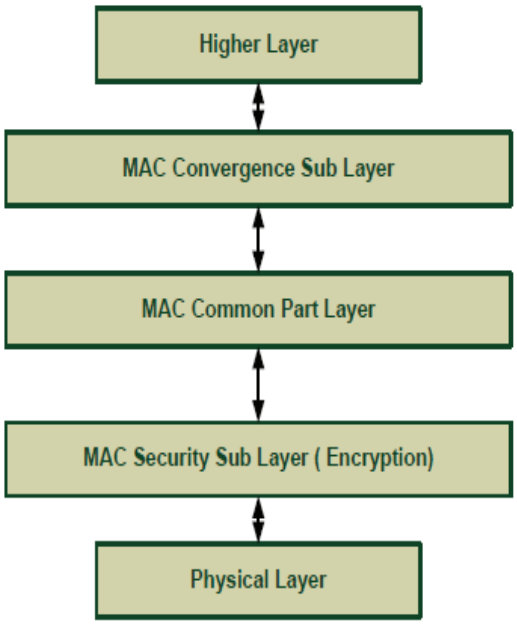

Figure.1. Overview of MAC layer

The process of sending the data packets across the fixed Broadband Wireless Access (BWA) is done by encapsulation protocol which also gives conditional access by the main station. The privacy key management mainly has two versions: PKM1 and PKM2 used in mutual

authentications. To refresh the key between main station and subscriber station is provided by PKM protocol. Traffic encryption keys (TEKs) are exchanged to secure subsequent PKM which is shared secretly. [8]

III. Advanced Encryption Standard

AES encryption and decryption [4] use same private key so it is called as symmetric key block cipher algorithm. For instance, if the block size is 128-bit i.e., it contains 128-bit information. Here, the input for encryption is the plaintext and output is cipher text which is generated by using ciphers and for decryption it is vice-versa. In this different sizes of keys are used depending upon the number of rounds for data abstractions which are required. The different sizes of keys used in AES are 128, 192 and 256 keys for 10, 12 and 14 rounds respectively [4]. Unlike DES, the entire block is used for each round of operations.

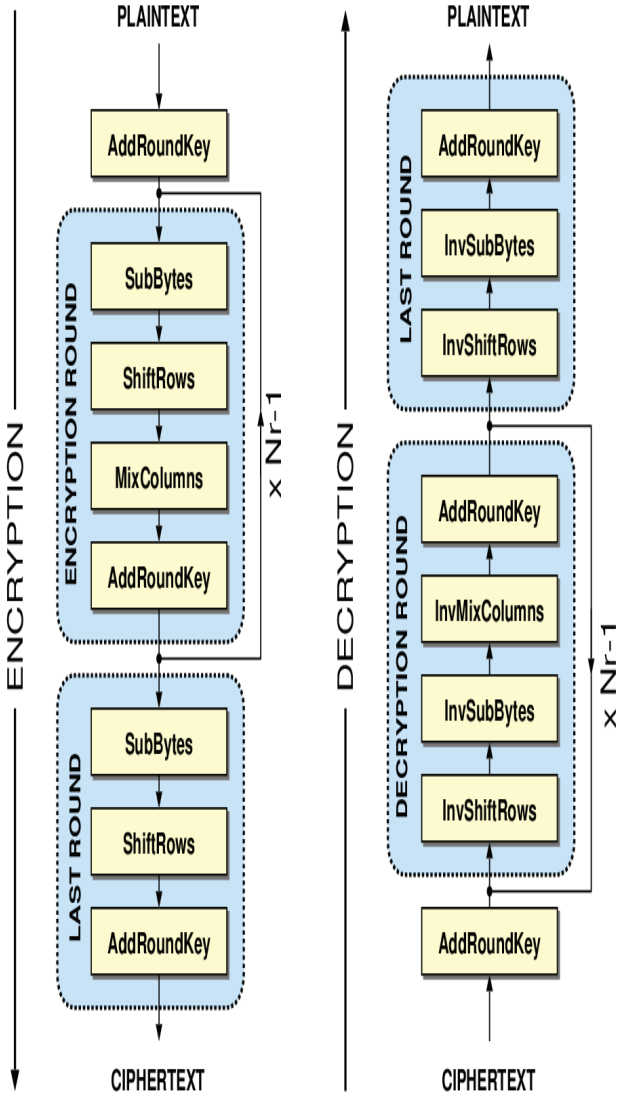

Figure.2. AES Encryption & Decryption Process

Rijndael AES algorithm [9] consists of four operations namely Sub Byte Transformation, Shift Row Transformation, Mix Column Transformation and Add Round Key in encryption. In decryption, the same operations are but each of the above operation takes its inverse form. For both encryption and decryption, key expansion units are used to generate ten different keys for ten rounds in the case of 128 bit. In every round a new key is generated from the previous key with the help of a key matrix and the primary key is referred as cipher. In this paper, AES is designed for 128 and 256 bit keys with 10 and 14 rounds of operations respectively [6]. In the first round, Add Round Key operation is solely performed and in the last round, all the operations except Mix column Transformation are performed in both encryption and decryption. The complete process AES encryption and decryption is explained briefly in the form of a flow chart as shown in Figure.2.

A. Sub Byte Transformation

The most important in Sub Byte Transformation is the S-Box. In this operation, the input byte is considered to be one of the elements of Galios field. The S-Box is implemented by passing the given input through multiplicative inverse and then affine transform. For performing this transformation all the S-Box values will be available well before hand and store in the memory. The 128 bit data is presented in 4*4 matrixes in byte format where in the mappings to S-Box replaces the original data byte [6, 7]. The mappings to S-Box are as shown in Figure 3(a).

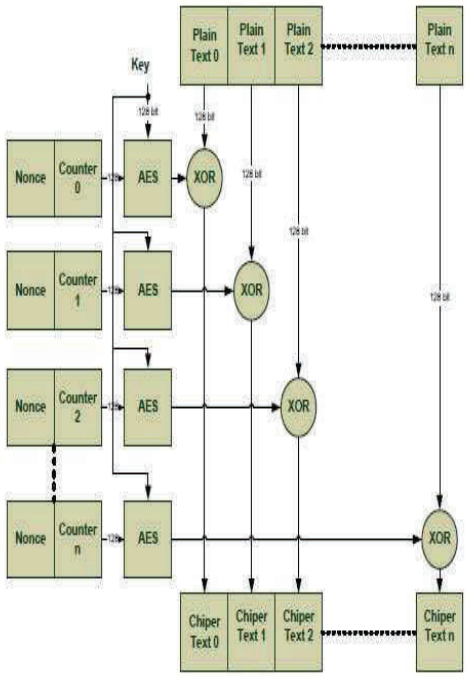

Figure.3 (a). Mapping to S Box

B. Shift Row Transformation

As its name suggests, the shift row transformation is done on 4*4 matrix row by row. In encryption the shift is towards left and the change in position of bytes depends on the row number. Elements in 0th row will not be shifted but in 1st, 2nd, 3rd rows, the elements are shifted by 1,2 and 3 times respectively. The shift row operation in encryption

performed as shown in Figure. 3(b).For decryption the shift takes place towards right [6].

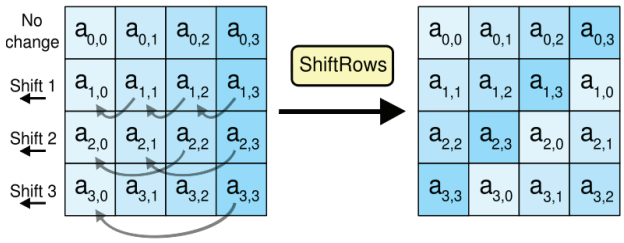

Figure.3 (b). Shift Row Transformation Process

C. Mix Column Transformation

Mix Column Transformation operation is one of the most power consuming operation in which the multiplication is carried out by galios field by inter byte mixing. Here, a constant 4*4 matrix is used for forward operation and another for reverse operation as shown in Figure.3(c). [6,7]

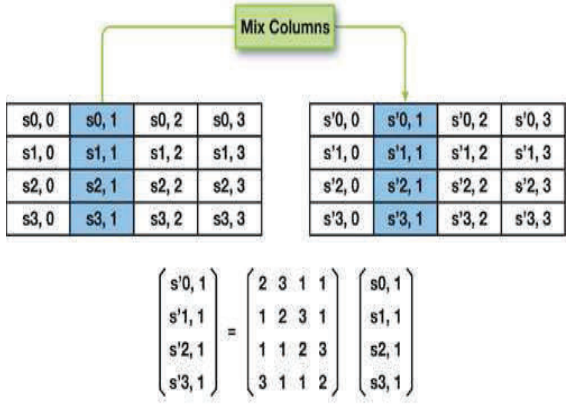

Figure.3(b). Mix Column Transformation Process

D. Add Round Key

In this operation, the Mix Column is XORed with the cipher key that is updated in each round using key expansion procedure to produce another 4*4 matrix and the output is given to next round [6] as shown in Figure. 3(d).

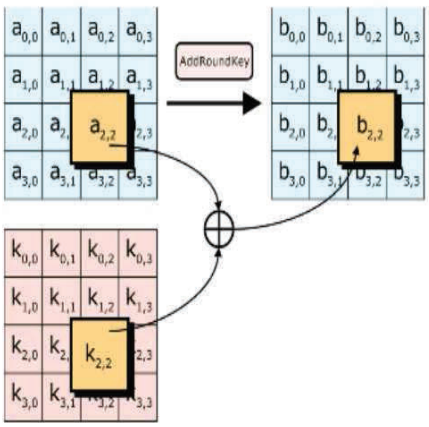

Figure.3 (d). XORed Operation Process Structure

E. Key Expansion

This unit takes a 128 bit cipher key, and perform a key expansion routine and generates a key schedule for every round. This unit contains Subword, Rotword and Rcon (i) where i represents round number. In every round Rcon (i) value is assigned and processed. In Subword operation, SubByte Transformation is applied to the word in that column. The function Rotword rotates the elements in the column by one shift from bottom to top. Then the byte is XORed with Rcon (i) to produce the corresponding column for the next round.

IV. AES Modes Of Operation

AES block cipher can be implemented in different modes of operation based on several implementation issues. Electronic Code Book (ECB), Cipher Feedback (CFB), Output Feedback (OFB), and counter (CTR) are the different types of modes in which AES operates for security purposes. In this paper, especially AES algorithm is implemented in CTR mode [9]. Data dependency of Cipher Block Chaining mode is avoided in the counter mode with the value of counter increasing by one in encryption and the same counter sequences are maintained in decryption process on the receiver side.

A. AES in CTR Mode

Prior to the encryption of plaintext, an arbitrary block called nonce and counter is encrypted, and then the result is XORed with plaintext to create cipher text. Due to the involvement of counter in encryption, the cipher block is not the same even if we have same plaintext. Due to non-linear concept of S-Box this mode avoids the attackers from predicting the patterns of repetition in cipher text. Further, this mode is more suitable for parallel encryption of various blocks. All these advantages make AES [4, 9] CTR mode be the best choice for AES implementation. The AES CTR model is same as shown in Figure.3 (a).

V. Implementation & Results

All the blocks are implemented using ASIC Cadence SoC Encounter [10] Tool with 45nm technology libraries. Figure.4 shows RTL Schematic of AES top module (which includes both encryption and decryption). Figure.5 shows RTL schematic of core structure of AES. Figure.6 shows RTL schematic of Encipher block, Figure.7 shows RTL schematic Decipher block. The timing of AES module with positive slack is 650ns. Figure. 8 shows the net power usage of AES. Table I and Table II, give the pre & post clock tree synthesis report in terms of nano seconds when routing is performed before special route and after nano route process. Finally, Figure.9 shows the IC chip Fabrication Layout structure which is named as GDS II file of AES top module.

Language Used - Verilog HDL
Simulator Tool - Ncvlog
Synthesis Tool - RTL Compiler
Implementation (Back-End Process) - SoC Encounter
Power Analysis n terms of nano watts

a) Internal Power - 0.650 (50%)
b) Switching Power - 0.62 (48%)
c) Leakage Power - 0.0006 (0.5%)

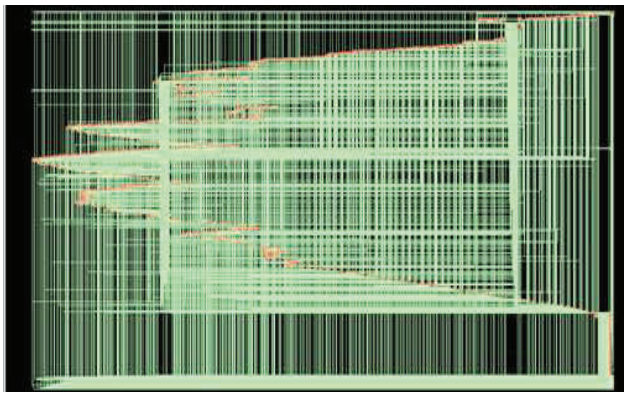

Figure. 4 RTL Schematic of AES Top Module

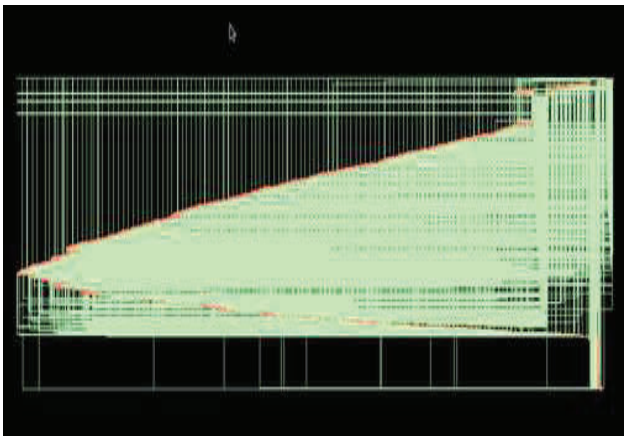

Figure. 5 RTL Schematic of AES Core Structure

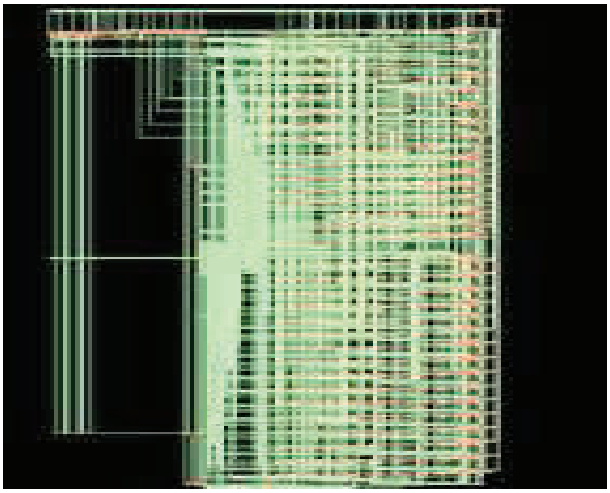

Figure. 6 RTL Schematic of AES Encipher Block

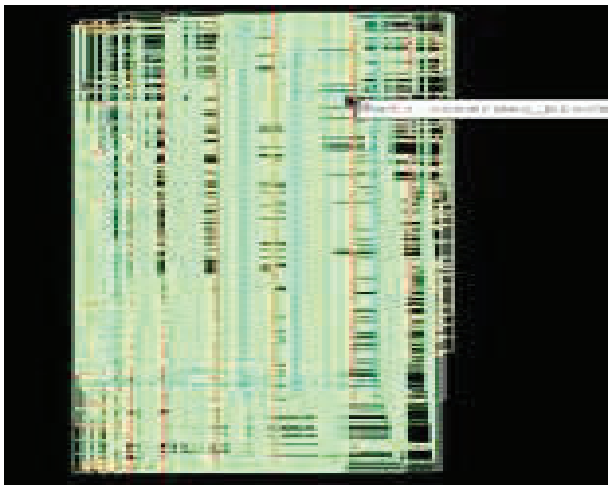

Figure.7 RTL Schematic of AES Decipher Block

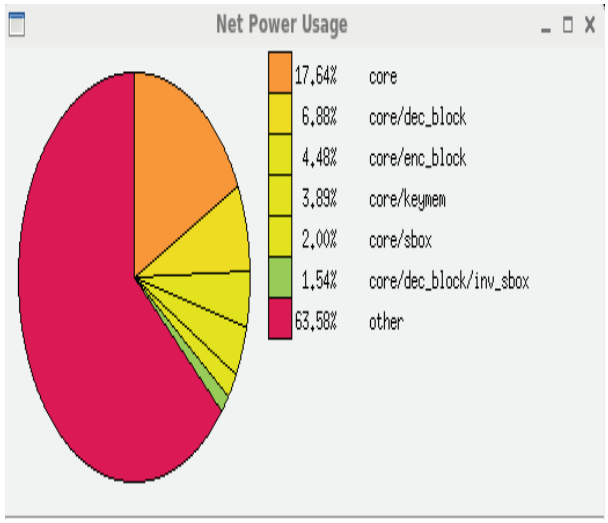

Figure. 8. Net Power Usage

TABLE I
PRE CLOCK TREE SYSTHESIS REPORT

Setup mode	all	reg2reg	default
WNS (ns):	0.464	0.464	5.894
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	2942	1071	1872

TABLE II
POST CLOCK TREE SYNTHESIS REPORT

Setup mode	all	reg2reg	default
WNS (ns):	0.390	0.390	5.713
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	2942	1071	1872

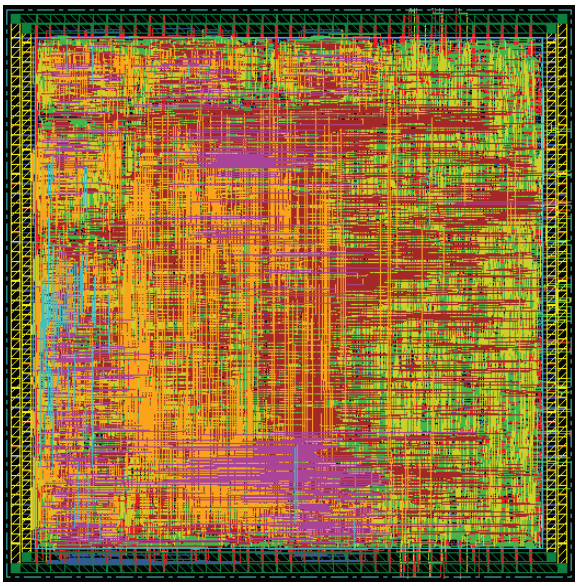

Figure. 9. GDS II of AES Top Module

VI. CONCLUSIONS

All the blocks are verified by ncvlog simulator and synthesis by using RTL complier and finally implemented in SoC Encounter and IC chip layout is obtained i.e., GDS II file. The top module consist of encipher and decipher blocks which is further designed by using inverse S-Box. The main advantage of AES algorithm in counter modes is, it consumes very less power as shown in figure 8 and as well as area occupancy on IC is also very less. These features play a prominent role for portable devices and have advanced improvements for Mobile Wi-MAX devices.

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Performance Analysis of Multi Carrier CDMA Transceiver System using a Novel Dynamic Decoding and Scheduling Procedure

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Abstract: **Wireless communications is a rapidly growing area of the communication, with high-quality and high data rate information exchange between mobile devices located anywhere in the world. Multi Carrier Code Division Multiple Access (MC CDMA) has emerged recently as a promising possibility for the next generation broadband mobile networks and it can cater to the needs of broadband mobile networks. The Transceiver proposed for a Multicarrier CDMA system is capable of achieving desirable performance with effective interference cancellation. Dynamic decoding algorithm with dynamic threshold determination and scheduling procedure is proposed to increase the system performance**.

***Index Terms*: Bit Error Rate, Signal to Noise Ratio, Multicarrier CDMA**

I. Introduction

The MC CDMA Transceiver provides the best form of communication in a noise and interference free system. Due to fading, the receiver experiences numerous copies of the transmitted signal and each of the signal takes different path.While traversing from transmitter to the receiver each signal suffers a delay and gets attenuated as well.

The interference cancellation procedures available in the literature cannot provide the required Bit Error Rate (BER) for MC CDMA system. To provide minimum BER, we have proposed a dynamic threshold determination and scheduling procedure to combat processing delay of the previous module, which is due to the fact that the system takes more number of iterations to reduce BER and improve signal quality [1],[2]. Another limitation of the previous module is that when the scheme is applied to a multiuser system, Multiple Access Interference (MAI) occurs which may increase the BER of the system [3]. A multiuser parallel scheduling scheme is proposed to combat MAI and increase the spectral efficiency of the system [4], [5], [6]. This system fails to maintain the Bit Error Rate (BER) of the system when number of users are increased. In a frequency selective fading channel, MAI degrades the performance of MC CDMA system. By appropriate usage of codewords , the system reduces BER in a multipath fading environment [7]. A hybrid subcarrier mapping scheme makes use of a superimposing common set of subcarriers [8], [9]. However, most of the work available in literature, fix the threshold value to determine the channel selection [10].

In order to overcome these limitations, the proposed algorithm reduces the number of iterations and at the same time improves BER and the number of scheduled users by varying the threshold in a dynamic manner and adopting an adaptive equalization procedure. The Dynamic Threshold determination for MC CDMA system is proposed to achieve Proper channel selection and estimation, reduce number of iterations to control the processing delay and to minimize BER to increase the performance of MC CDMA Transceiver. The paper comprises of following sections: section II explains the System Description, section III describes the Dynamic Decoding Scheduling Procedure, section IV explains Results and Discussion followed by Conclusion in section V.

II. System Description

The MC CDMA receiver calculates the summation of amplitude of signals that exists from different paths, the phase of the signal being significant. The signal strength of each signal varies depending on the nature of summation of signals. If all signals exists in-phase, they tend to add together. When the signals are out of phase, they tend to subtract from each other. However, this case does not happen, as some signals will be in-phase and others will be out of phase, depending on various path lengths, and therefore some will tend to add to the overall signal, whereas others will subtract. The mathematical model of multipath can be presented using the method of impulse response, from which multipath time can be calculated which defines the time delay between the initial and the last received impulses. After obtaining the channel transfer characteristics, coherence bandwidth decides the nature of the channel, but it is not very significant in deciding the error rate of the receiver over wide range of frequencies.

In the receiver, the signals are de spreaded after the recovery of subcarriers at the output of Fast Fourier Transform (FFT), by applying inverse code matrix. To optimize and mitigate the effects of the channel there arises a need to introduce weighing factor. A linear receiver is used in this case, which arrives at a decision based on linear combination of all subcarrier signals. The receiver should be provided with FFT that can be implemented efficiently using standard butterfly topologies, inverse code matrix c^{-1} and the weighing matrix W. Consider FFT and c^{-1} to b non-adaptive, and an implementation of simple linear receiver can be

performed. Inversion is needed to find the Minimum Mean Square Error (MMSE) of the signal in the presence of noise, MAI and Inter Chip Interference (ICI).

Consider a MC CDMA system with k transmitters generating independent data symbols $x_k = \{-1, 1\}$. The coded data $d_k = \{-1, 1\}$ is interleaved and spread by Direct-sequence spreaders

$$S_k = \left\{-1/\sqrt{N}, 1/\sqrt{N}\right\}$$

where N is the Processing Gain.

The received signal is given by

$$y = \sum_{k=1}^{K} S_k d_k + n \qquad (1)$$

Where n is AWGN with variance $N_o/2$.

The equation (1) depicts, that the received signal constitutes itself with the message and its unique code along with the noise component.

The amplitude $a_k(t)$ of the received signal at time 't' will be the same for all chip rate 1/Tc . The expectation of the received signal on to the spreading code of signal i after elimination of the signal (i-1) during the mth symbol interval is given by

$$I_{k,m} = \frac{1}{T_k} \int_{(m-1)Tk+tk}^{mTk+tk} r^{(k)}(t) a_k(t-\tau_k) dt \qquad (2)$$

Where $r^{(k)}(t)$ is the signal after cancelling users 1 through (k-1) which is used to detect data for user k of $T_k = N_k Tc$ for K^{th} user's symbol period and N_k is the spreading gain of user k and * represents the complex conjugate operation.

The SNR for signal k is given by

$$\Gamma_k = \frac{E^2\{R[I_{k,m}\gamma_k^*]/[I_{k,m}]\}}{Var\{R[I_{k,m}\gamma_k^*]/[I_{k,m}]\}} \qquad (3)$$

Where $E^2\{x/y\}$ is the square of expected value of x given y, $\gamma_k = \sqrt{P_k} e^{j\Phi k}$ is the complex channel gain and R[x] is the real part of x.

The variance of decision statistics, n_x is

$$n_x = Var\{ R[I_{k,m} \gamma_k^*]/ [b_{k,m}]\} \qquad (4)$$

thus

$$n_k = \frac{\sigma^2}{N_k} + \frac{\sigma^2}{N_k} \sum_{i=1}^{k-1} n_i + \frac{\sigma^2}{N_k} + \sum_{i=k+1}^{k} P_i \qquad (5)$$

Where σ equals 1 and 0.5.

The above equation depicts the way to determine SNR for a Multicarrier system. By using the unique code word, the desired pulse can be decoded and SNR is calculated. The SNR calculated is kept as threshold so that the Dynamic Decoding algorithm can efficiently recover the transmitted data to its best level.

Now we propose an algorithm that performs efficient decoding of the received estimate.

III. Dynamic Decoding Scheduling Procedure

This system works efficiently by adopting SNR as threshold. In a Multicarrier system, the information is conveyed via multiple carriers which have the same in-phase component but different quadrature phase components. In order to decode the desired information with optimum signal strength, Dynamic decoding schedule algorithm is employed. An optimum detector should have the capability of computing root mean square deviation instead of just reconstructing the received signal. The receiver should make a decision in favor of decoding a signal with least probability of error. In this sense, the receiver can surpass the distorted channel. Now the receiver will estimate the time response of the actual received signal and determine the most likely signal. In cases that are most computationally straightforward, criterion for the lowest error probability is achieved.

The transmitted carriers are to be discretized based on the threshold SNR. If the $(N-1)^{th}$ frequency produces a good SNR compared to $(N)^{th}$ frequency , the threshold will be updated (i.e.) SNR of $(N-1)^{th}$ frequency will be set as threshold, leaving SNR of $(N)^{th}$ frequency signal, so that the process continues for all different combinations of constellation levels of QAM as well as for different throughput levels so that the performance of receiver can be improved in the presence of noise and fading environment. Nu users are multiplexed by allocating M subcarriers in the available spectrum of width W = 1/T.

Each user is assigned a subset of subcarriers according to the prescribed allocation strategy. If the subcarriers Su are uniformly spaced, then

$$S_k = U/T_1 \quad \text{with } T_1 = MT,\ U = 0 \ldots\ldots\ldots\ldots M-1 \qquad (6)$$

Subcarrier allocation methods play an important role for optimization of Spectral Efficiency, the exploitation of Frequency Diversity, and the complexity of the detection algorithm.

Consider a system with K transmitters, each transmitting N subcarriers. Each subcarrier is allocated a different value of chip interval T_C.

(i) Initially 64-QAM modulation scheme is used for all the subcarriers.

(ii) Calculate E_r

$$E_r = E_{(M,i)} / \log 2 (M_i) \qquad (7)$$

Where i=1, 2 ….N, given the subcarrier SNR values using equation (6)

(iii) Set E_{Th} as threshold probability of Error and C_T bein their respective Constellation size.

(iv) Determine $\bar{E}_r$,the mean probability of error ,whose constellation size is $\bar{C}$.

(v) Compare $\bar{E}_r$ with E_{Th}. If $\bar{E}_r$ is less than E_{Th}, then current configuration is kept and algorithm ends.

(vi) Select the subcarrier with worst E_r and reduce the constellation size to 16-QAM and null the subcarrier.

(vii) Repeat the same procedure to compute E_i for all the subcarriers with changed allocation and return to step (v)

(viii) a) Determine the convergence point E_c, the SNR intersection with interference cancellation frequency.

b) Calculate the convergence by evaluating upper and lower boundaries of noise level , BER is calculated as

$$E^*=Q\ (SNR/N_0) \qquad (8)$$

c) Let i=1. Initialize path set to contain only one path $E_m\{(1)\}$ and corresponding metric set $\Upsilon_m=\{i_{infinite}\}$.

d) i =i+1. For each state 'n' extend E'_m-1 ending in state n' along the defined transition n'→n, producing the new path E_m in $E_{m,n}$ and update the metric in $E_{m,n}$ using $\vartheta_m=i_{inf}(\vartheta')$.

e) Remove all the paths with complexity greater than or equal to that of current optimal path.

f) Define a set of metrics for paths that have reached the target BER, the convergence point for receiver iterations.

g) D $(\bar{S},S_T)$ denotes the Euclidean distance between the signal constellation $\bar{C}$ and C_T.

Bit Error Rate can be expressed in closed form as

$$P_l.E_{EA} = \lim_{N_{EA}\to\infty} P_b^{QAM} = Q(\sqrt{\pounds}) = Q\ (\sqrt{2}\ E_b/N_0) \qquad (9)$$

which is the exact expression for BER in AWGN channel. Evaluation of BER, when coherent detection is applied in fading conditions requires the computation of an average over the fading distribution.

IV. Results And Discussion

In this section, we compare the proposed scheme with conventional Multiuser Scheduling and Parallel Scheduling to evaluate the number of iterations needed to obtain required minimum BER of the system. We exhaustively search all possible sub channel assignments as well as dynamic threshold determination. The simulation results focus on increasing number of scheduled users and minimize BER performance of the system.

Figure 1 and 2 compares the low complexity adaptive equalization and dynamic scheduling with Multiuser scheduling and parallel scheduling approaches. The number of iterations varying from 1 to 6 signifies variation of number of subcarriers from 64 to 2048.Since we need to exhaustively search all possible subchannel assignments as well as the corresponding BER of the system , the complexity grows exponentially. Results for minimum subcarriers 64 and maximum subcarriers 2048 is shown in figure 1 and 2.

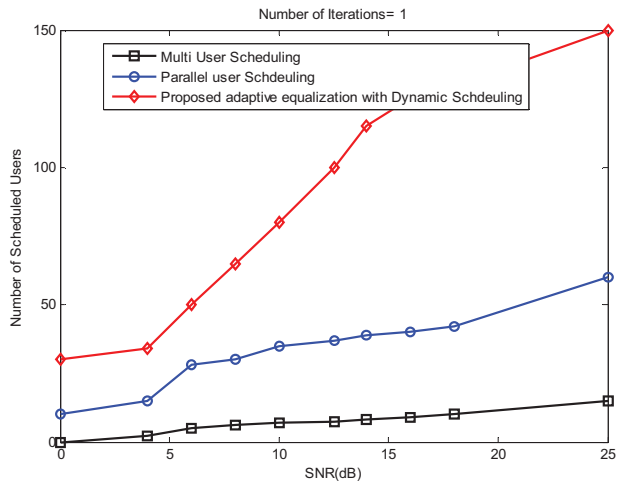

Figure 1. Performance of MC CDMA Transceiver with dynamic threshold determination with 64 Subcarriers

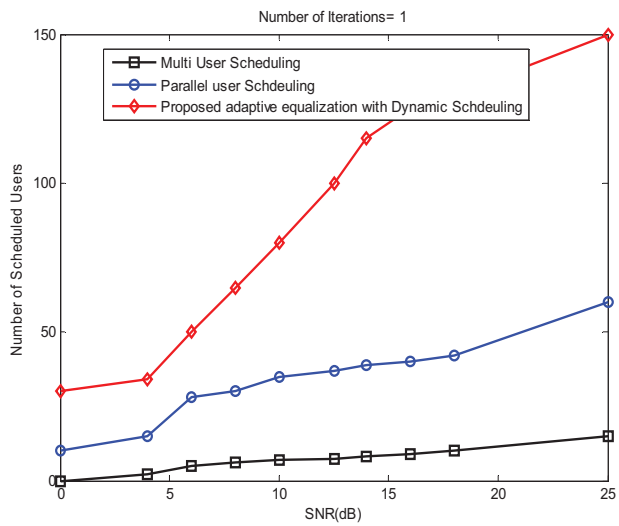

Figure 2. Performance of MC CDMA Transceiver with dynamic threshold determination with 2048 Subcarriers

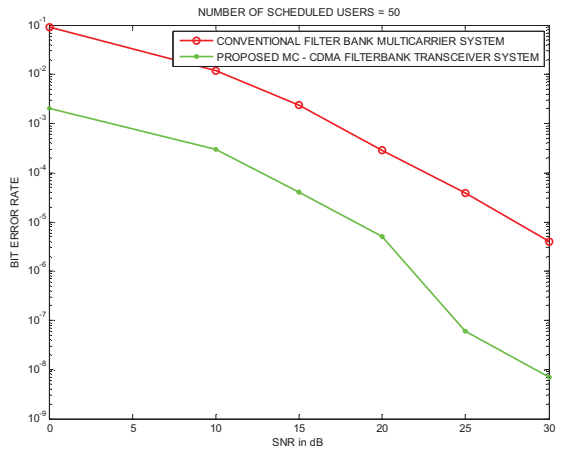

Figure 3. BER Performance of the MC CDMA system with Adaptive Equalization and Dynamic Threshold determination for 50 users

Figure 3 shows the comparison of the BER performance versus SNR of MC CDMA transceiver system employing adaptive equalization with dynamic threshold determination. The conventional system does not guarantee required BER when the number of users is increased.

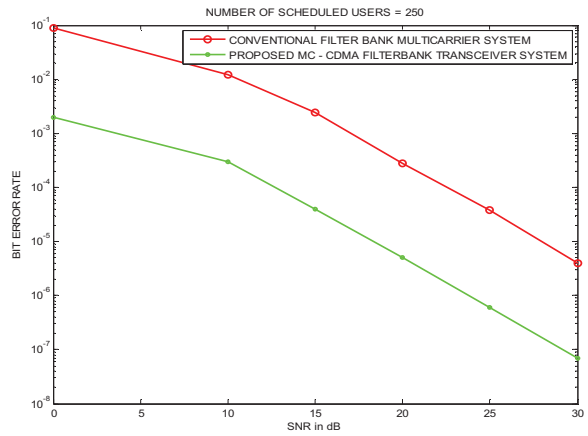

Figure 4. BER Performance of the MC CDMA system with Adaptive Equalization and Dynamic Threshold determination for 50 users

The figure 4 illustrates the operation of algorithm when the users are increased to 250. However, the proposed system requires less number of iterations to converge to minimum BER when compared with conventional techniques. For a low SNR of 10 dB, the proposed system yields a BER of 10^{-4} compared to the conventional techniques which provide a BER of 10^{-2}. When the SNR is increased to 30 dB, the proposed system yields a BER of 10^{-7} compared to the conventional techniques which provide a BER of 10^{-5}.

V. Conclusions

In this method, the dynamic determination of threshold was carried out including the fading scenario. The effective decoding procedure mitigates Inter User Interference (IUI) as well as Multiple Access Interference (MAI). This is evident from the fact that the number of scheduled users increase there by increasing the overall spectral efficiency of the MC CDMA system applying adaptive equalization. The Dynamic Decoding scheduling procedure increases the average throughput and minimizes BER to required level.

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Design and Verification of High Speed IO Transmitter in 14nm Technology

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Abstract: **For many years, parallel I/O schemes ruled the chip to chip, board to board or backplane communication. Parallel I/O had to experience performance issues like crosstalk, signal integrity and increased skew after passing certain I/O clock-frequency rates [1]. Also parallel I/O methods increased the complexity of the hardware (high pin count, more wires) and made bandwidth sharing inevitable. In many new communication protocols serial data transmission has become very common due to low pin count (reduced cost). Serial I/O methods can also transmit at much higher clock rates per bit transmitted, thus outweighing the parallel transmission method. High speed serialization with large bandwidth plays a major role in transmitter of high speed interfacing circuits such as PCIe, USB, and SATA. Various encoding schemes are used based on the protocols. Efficient equalizers with interface units are required to avoid ISI (Inter Symbol Interference) and to drive the back-panel line. This also makes the design complex, which in turn makes the design verification and validation more challenging.**

Index Terms: **PCIe, Serial I/O, USB, SATA**

I. Introduction

High-speed serial I/O standards require only a half or less pin and wire count for the transmissions unlike the parallel transmission schemes. Surprisingly serial transmission methods, which are being widely used today in many new communication protocols, are able to transfer data at rates higher than 8 Gb/s. In high-speed serial transmission, clock and data are combined in a single stream thus reducing the problem of bit-to-bit skew. High-speed serial I/O standards span in more than one communication scenario like, Fibre channel, InfiBand and Gigabit & 10-Gigabit Ethernet etc. Dramatic increases in processing power, fueled by a combination of integrated circuit scaling and shifts in computer architectures from single-core to a possible many-core systems. This has rapidly scaled on-chip aggregate bandwidths into the Tb/s range [1], necessitating a corresponding increase in the amount of data communicated between chips not to limit overall system performance [2]. Due to the limited I/o pin constraints, high-speed serial link technology is employed for this inter-chip communication.

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A. PCI Express overview

High-speed point-to-point electrical link systems employ specialized I/O circuitry that perform incident wave signaling over carefully designed controlled-impedance channels in order to achieve high data rates. General block view of High speed IO (Figure 1) divided into three sections namely 'Transmitter', 'Clocking' and 'Receiver' sections.

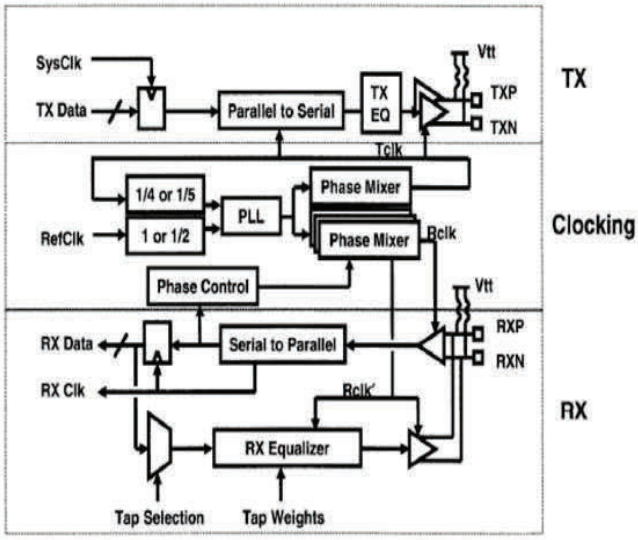

Figure 1. Block diagram of High Speed IO

Transmitter section contains encoding mechanism based on the protocol implementation, parallel to serial conversion (serializer), transmitter equalization circuitry and differential driver circuitry.

Clocking section is to control both transmitter and receiver contains phase lock loop, mixers, clock dividers and clock generator. This provides necessary clock required for transmitter and receiver sections.

Receiver section contains clock to data recovery, receiver equalizer circuit, decision feedback, error detection and correction, serial to parallel conversion (deserializer) and decoding scheme.

B. Electrical link system

Figure 2 shows the major components of a typical high-speed electrical link system. Due to the limited number of high-speed I/O pins in chip packages and printed circuit board (PCB) wiring constraints, a high-bandwidth transmitter serializes parallel input data for transmission. Differential low-swing signaling is commonly employed for common-mode noise rejection and reduced crosstalk due to the inherent signal current return path [7]. At the receiver, the incoming signal is sampled, regenerated to CMOS values and deserialized. The high-frequency clocks which synchronize the data transfer onto the channel are generated by a frequency synthesis phase-locked loop (PLL) at the transmitter, while at the receiver the sampling clocks are aligned to the incoming data stream by a timing recovery system.

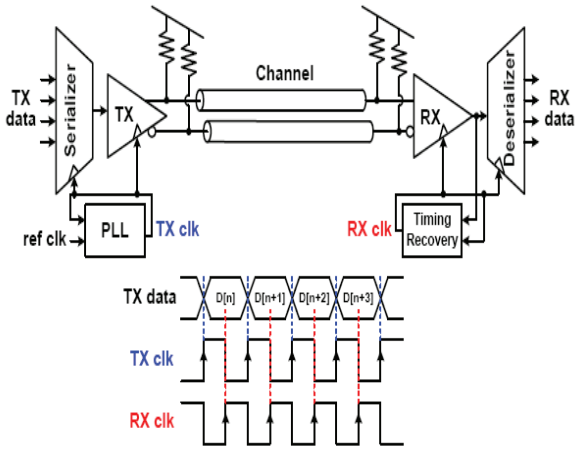

Figure 2. High speed electrical link system

C. Transmitter system

The transmitter must generate an accurate voltage swing on the channel while also maintaining proper output impedance in order to attenuate any channel-induced reflections. Either current or voltage-mode drivers, shown in Figure 3, are suitable output stages. Current-mode drivers typically steer current close to 20mA between the differential channel lines in order to launch a bipolar voltage swing on the order of ±500mV. Driver output impedance is maintained through termination which is in parallel with the high-impedance current switch. While current-mode drivers are most commonly implemented [8], the power associated with the required output voltage for proper transistor output impedance and the "wasted" current in the parallel termination led designers to consider voltage-mode drivers. These drivers use a regulated output stage to supply a fixed output swing on the channel through a series termination which is feedback controlled [9]. While the feedback impedance control is not as simple as parallel termination, the voltage-mode drivers have the potential to supply an equal receiver voltage swing at a quarter [7] of the common 20mA cost of current-mode drivers.

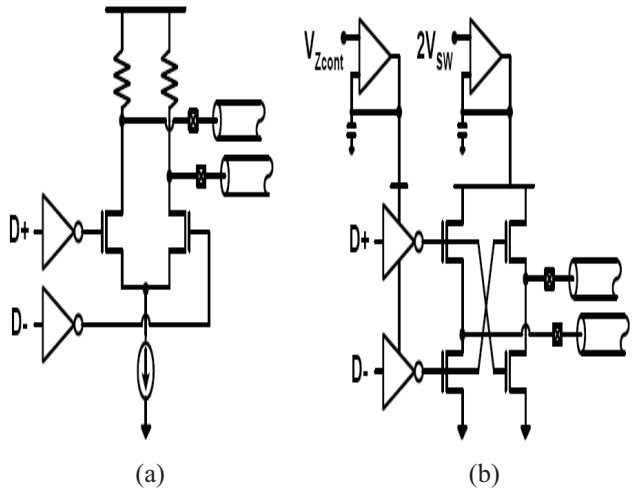

Figure 3. Transmitter output stages:

(a) current-mode driver, (b) voltage-mode driver.

D. Receiver system

Figure 4 shows a high-speed receiver which compares the incoming data to a threshold and amplifies the signal to a CMOS value. This highlights a major advantage of binary differential signaling, where this threshold is inherent, whereas single-ended signaling requires careful threshold generation to account for variations in signal amplitude, loss and noise [11]. The bulk of the signal amplification is often performed with a positive feedback latch [12,13]. These latches are more power-efficient versus cascaded linear amplification stages since they don't dissipate DC current. While regenerative latches are the most power-efficient input amplifiers, link designers have used a small number of linear pre-amplification stages to implement equalization filters that offset channel loss faced by high data rate signals [14,15].

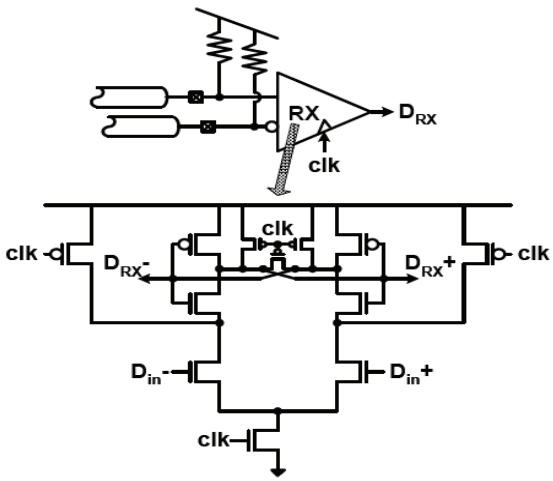

Figure 4. Receiver input stage with regenerative latch

One issue with these latches is that they require time to reset or "pre-charge". Thus to achieve high data rates, often multiple latches are placed in parallel at the input and

activated with multiple clock phases spaced a bit period apart in a time-division-demultiplexing manner (Figure 5). This technique is also applicable at the transmitter, where the maximum serialized data rate is set by the clocks switching the multiplexer. The use of multiple clock phases offset in time by a bit period can overcome the intrinsic gate-speed which limits the maximum clock rate that can be efficiently distributed to a period of 6-8 fanout-of-four (FO4) clock buffer delays [16,17], shown in [18]

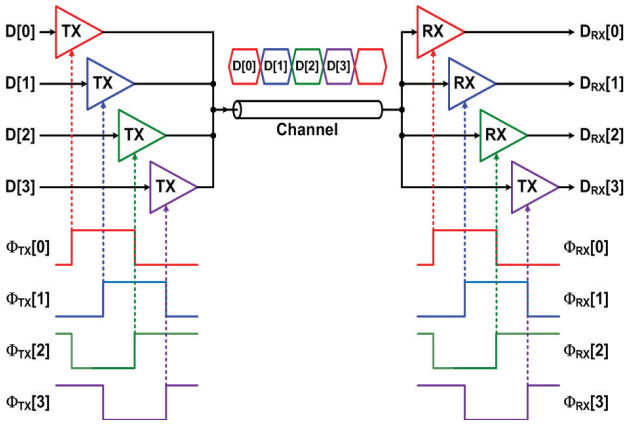

Figure 5. Time Division-Multiplexing link

II. PCIE TRANSMITTER BLOCK OVERVIEW

Figure 6 shows the block diagram of PCIe transmitter, depends on the input data PCLK will varies as stated in above section. Depending on the PCIe version encoding scheme varies as shown in table 1. In order to transfer data over a high speed serial interface, data is encoded prior to transmission and decoded upon reception. The encoding process ensures that sufficient clock information is present in the serial data stream to allow the receiver to synchronize to the embedded clock information and successfully recover the data at the required error rate. In addition, the 8b/10b or 128b/130b encoding improves the line characteristics, enabling long transmission distance and more effective error-detection at the receiver.

TABLE I
ENCODING SCHEMES IN PCIE

PCIe mode	Encoding scheme
Gen1	8b/10b
Gen2	8b/10b
Gen3	128b/130b
Gen4	128b/130b

Using the 8b/10b encoding algorithm adds 20% overhead to each character so the effective data-rate of PCIe Gen 1 becomes (1-0.20)x2.5=2 Gbps and for Gen 2 becomes 0.8x5=4 Gbps similarly by using 128b/130b encoding algorithm in Gen 3 and Gen 4 adds 1.538% overhead so the effective data of Gen 3 is 0.985x8=7.88 Gbps, for Gen 4 is 0.985x16=15.76 Gbps as shown in table 2.

TABLE II
ENCODING SCHEMES IN PCIE

PCIe modes	Operating frequency	Data rate	Bandwith
Gen 1	2.5 GHz	2.5 Gbps	2 Gbps
Gen 2	5 GHz	5 Gbps	4 Gbps
Gen 3	8 GHz	8 Gbps	~8 Gbps
Gen 4	16 GHz	16 Gbps	~16 Gbps

Parallel to serial conversion is done by using multiple stages in order to perform high speed operations without any data error in the serialized output, because using traditional FSM, built with multiple flops in the path will increase the overall path delay and may lead to race conditions with high speed input clock, leading to setup and hold violations.

In order to receive and recover the data coming from noise channel at receiver end, output at the transmitter end has to be differential so that channel noise can be compensated. Hence differential drivers are required to convert single ended data to differential data.

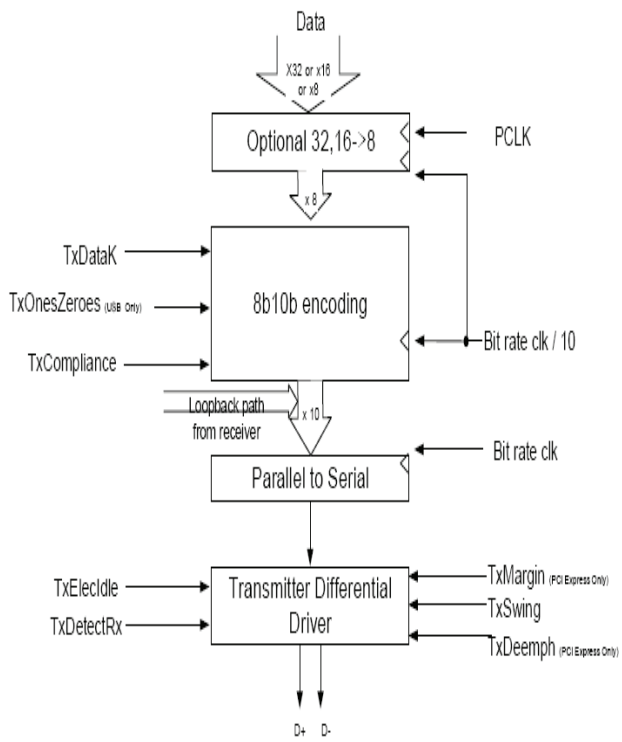

Figure 6. Transmitter Block diagram

III. CADENCE CONFORMAL

A systematic method that uses mathematical proof to check the design's properties is formally known as Logic Equivalence Checking (LEC). Verification starts writing systemverilog/verilog coding to mimic the behavior of

circuitry and compares the schematic with systemverilog code. Some of the advantages of Formal verification are:

- Enables "White box" verification
  This provides full controllability and visibility on internal structure
- No test vectors required
  - No input vector creation necessary
  - No test vectors for logical function
  - Testbench setup is not required
  - Easy debugging
- Exhaustive verification
- Find bugs earlier

This will help in finding bugs as early as possible and also in the progress of work, target a class of bugs typically found with simulation late in the design cycle

- Speed-
  Formal is magnitudes faster than simulation

It verifies the logical equivalence of RTL, gate or transistor level netlists to each other. But does not guarantee that the initial design meet the design specification. It also ignores timing information and performs only boolean equivalence checks.

Figure 7 shows the LEC Flow in the design cycle, LEC can be performed between RTL to RTL or RTL to pre-layout netlist or RTL to post-layout netlist or netlist to netlist. Figure 8 shows cadence conformal flow in ASIC design flow.

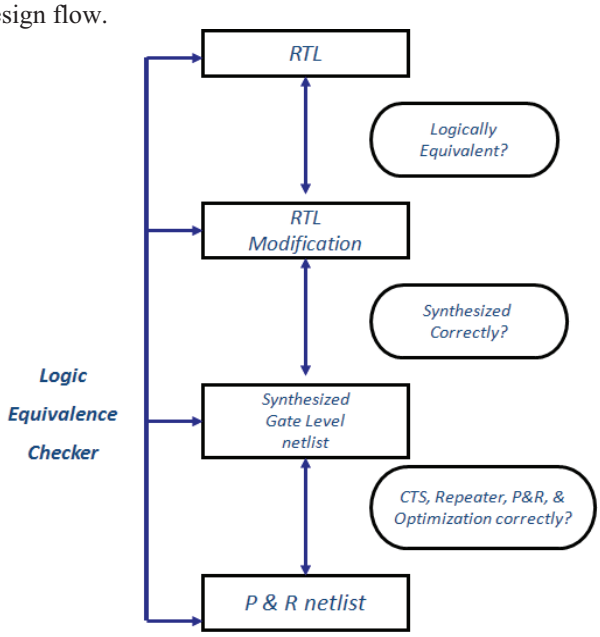

Figure 7. LEC in design flow

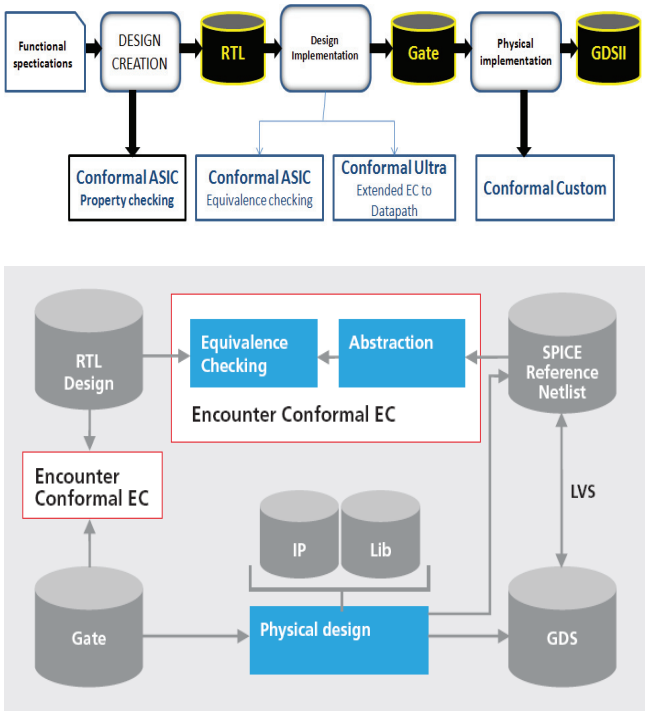

Figure 8. Cadence Conformal in design flow

Figure 9 shows the LEC tool flow, it contains two modes namely, 'setup' and 'LEC' , all the reading of systemverilog/verilog code, netlist is done in setup mode and mapping the instance to match the functionality, generation, comparison and debugging is done in LEC mode. This process repeats until schematic meets the functional/logical equivalence

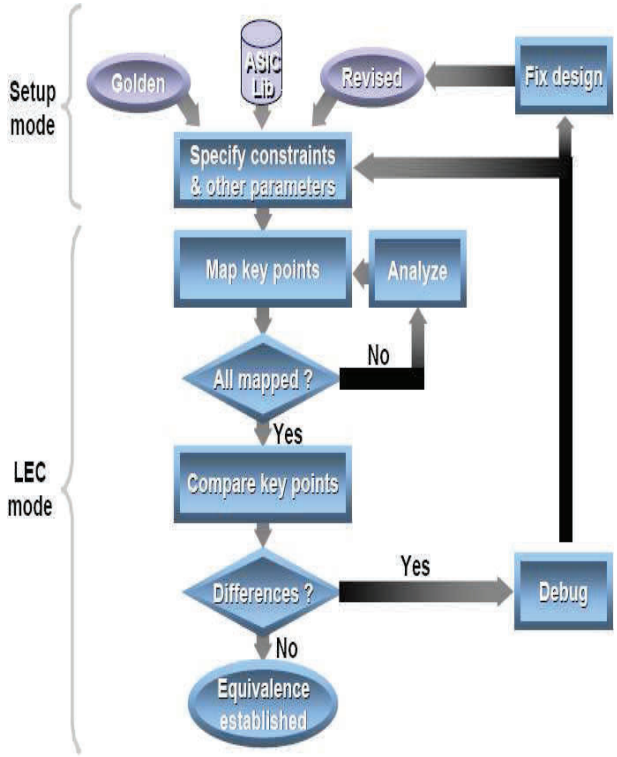

Figure 9. LEC Flow

IV. Proposed Design And Verification

A. Proposed verses existing

Existing High speed IO transmitters are suffering with ISI due to high frequency attenuation, behaves like low pass filter along the path and usage of CML logic leads to large number of transistor count in the design with low delay. Proposed method uses CMOS logic with custom D-Flipflop, latches, mux etc.. which provides high speed operation with full logic swing at high frequencies. This potentially eliminate requirement of equalizer with more number of taps at the transmitter. Existing design uses flatten design of serializer which increases possibility of risk during parallel to serial conversion. Proposed design divides the parallel to serial conversion into stages as 8bit user-interface (8UI) and 2bit user-interface (2UI) operating at different clock frequencies. This leads to clock domain crossing problem. This is eliminated by using feed-forward synchronization mechanism as shown in figure 10. Existing CML driver requires large tail currents. This is eliminated in proposed design by using digital driver with pull-up resistance and pull-down resistance same as line characterization resistance.

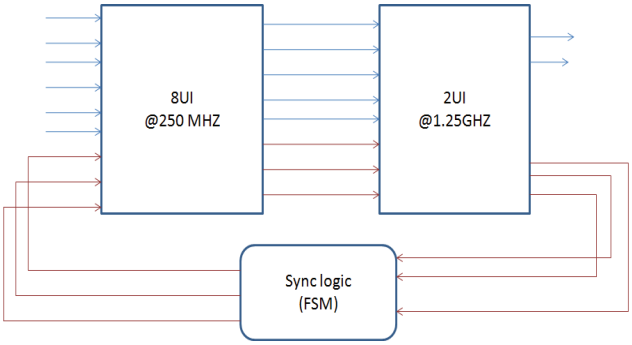

Figure 10. Proposed method of serailization

Figure 11 shows the block view of design. Parallel to serial conversion plays a major role in the Transmitter. Focusing on 'parallel to serial conversion' provides good insight on real need of equalizer at the transmitter, whether it is necessary or not. Encoding scheme just provides the data encryption at the transmitter.

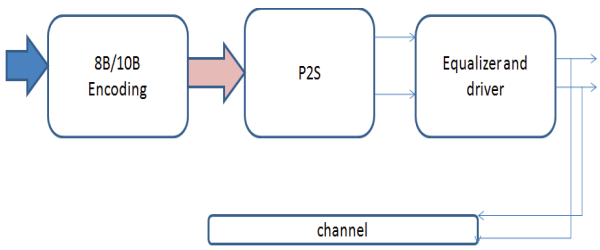

Figure 11. Block view of design

B. Design plan

Design contains 8b/10b encoding, parallel to serial conversion (P2S) block, followed by driver circuit connected to channel as shown in figure 20. 8b/10b encoding consist of disparity blocks to add two parity bits for every byte of input data from controller. P2S converts parallel inputs to differential serial outputs by converting 40bit input data to 10bit data using 8UI, 10bit output of 8UI connected to 2UI separates 10 bit data into 2bit even and odd stream. Finally this 2bits are converted to 1bit using MUX and D-Flipflop at output.

C. Verification plan

Verification is the act of testing a design against its specifications. This makes sure that the design is right. Verification is a quality control process. This is a repetitive process to make sure the design is right against its specification. Validation is the act of test system against its operational goals. This makes sure that it is a right design. Validation is a quality assurance process.

The proposed verification plan starts with writing systemverilog/verilog code to mimic the behavior of design. This code is simulated using VCS simulator to speed up the process once the required behavior is attained these RTL codes are used in formal verification using cadence conformal , which compares the schematic with RTL code for logic equivalence. Because of no test-vectors requirement, it is easy way of verification. It provides exhaustive verification and leads to finding bugs as early as possible in the design.

Figure 12 shows the proposed method of verification plan. Behavioral Models (BMODS) imitates the behavior of design using verilog/systemverilog and compares with the actually schematic level implementation using cadence conformal for Formal verification which verifies without simulation. Finally to make sure the design is working properly, use mixed signal validation by synopsys VCS-XA which rely on the stimulus. Hence the final simulation results makes sure of the assurance of quality in the design.

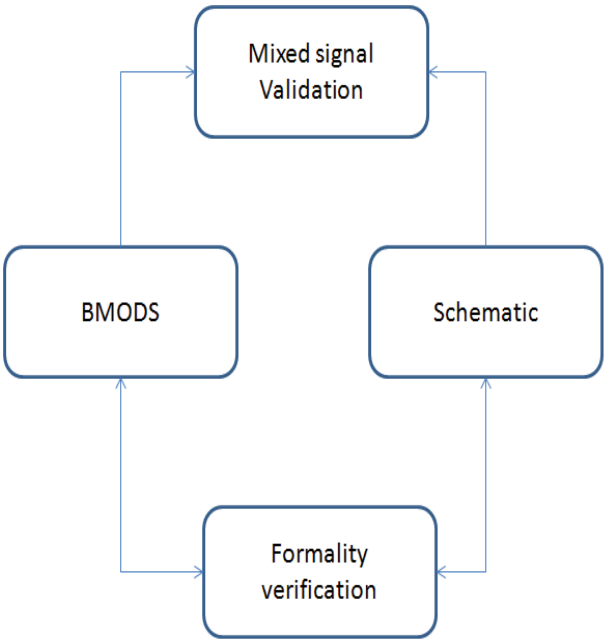

Figure 12. Proposed verification plan

V. Design Implementation

A. Schematic overview of Transmitter

Final schematic overview is as show in figure 13. And its symbol view in figure 14.

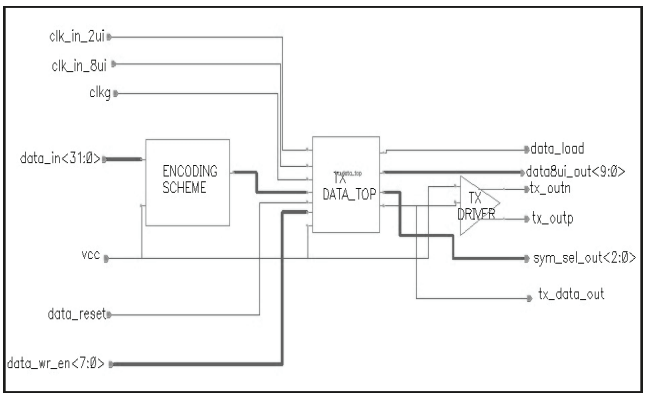

Figure 13. Transmitter schematic overview

Parallel to serial conversion is done in series of step by step conversion and also provides different level of user interface (UI) signals like 10bit interface output from data_8ui, 2bit interface output from data_2ui and 1bit interface output from TX_DATA_TOP. such that implemented design is compatible to both single and multi bit interfacing devices. Hence require multiple clock input signal in the design such as cllk_in_8ui for data_8ui operation, clk_in_2ui for data_2ui operation and clkg for final serialization, these clock frequency changes according to the PCIe mode as shown in table 3. data_wr_en input is used for output selection of data output for data_8ui and also for TX_DATA_TOP. data_in is the 32 bit input from PCIe controller to the transmitter for transmission, in order to clear the data. When power is just switched ON and for force reset of transmitter, data_reset is provided. Due to multi hierarchical design structure, it is complex to debug the failure occurred in the design, hence few signals such as data_load, sym_sel_out, data8ui_out, tx_data_out, are brought out to verify and debug the functionality of design,'tx_outp'and 'tx_outn' are dual outputs that are to be transmitted through the channel.

TABLE III.
OPERATING CLOCKS INFORMATION IN DESIGN

PCIe mode	clk_in_8ui	*clk_in_2ui*	Clkg
Gen1	250MHz	*1.25GHz*	2.5GHz
Gen2	500MHz	*2.5GHz*	5GHz
Gen3	800MHz	*4GHz*	8GHz
Gen4	1.6GHz	*8GHz*	16GHz

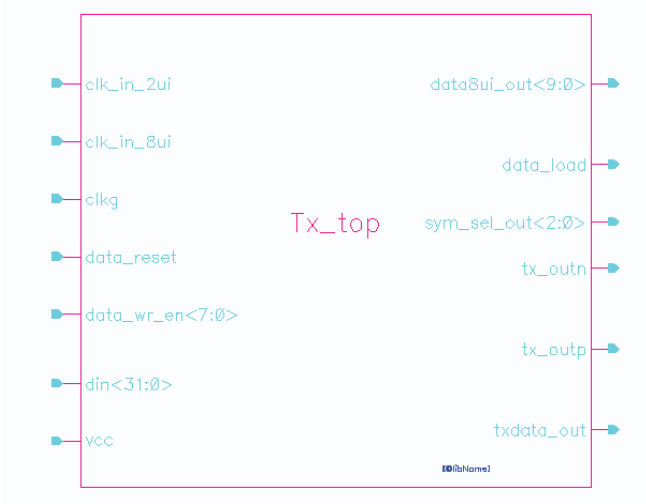

Figure 14.Tx_Top symbol view

VI. Results

A. Verification report

Design is Formal verified using Cadence Conformal. Conformal as capability of inspecting clock domain crossing. Figure 15. shows the hierarchical view of data_top in the design. Figure 16 shows the Verification Report of data_top.

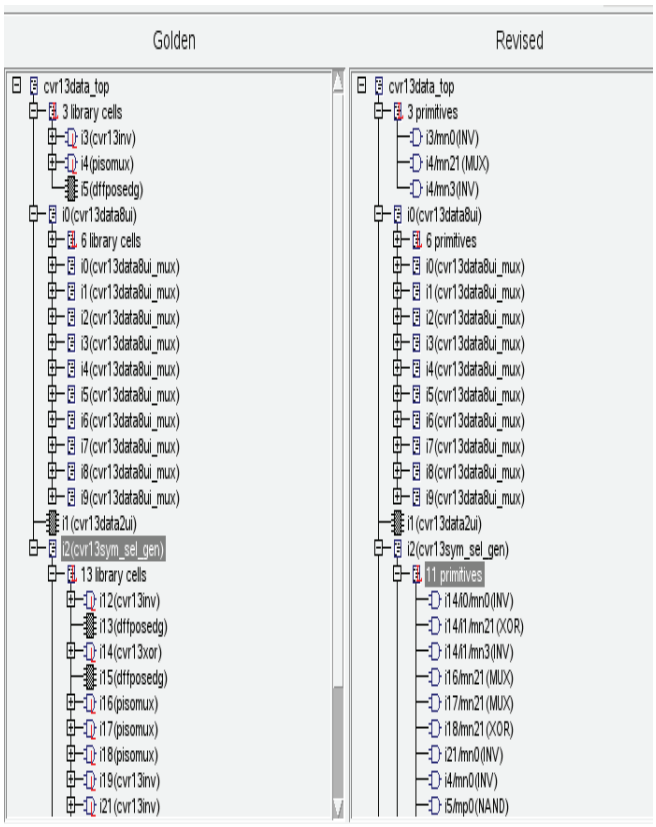

Figure 15. Hierarchical view of data_top

```
==========================================================================
                          Verification Report
..........................................................................
Category                                                          Count
..........................................................................
1. Non-standard modeling options used:                              0
..........................................................................
2. Incomplete verification:                                         2
     User added black box:                          yes
     Black box mapped with different module name:   yes
..........................................................................
3. User modification to design:                                     0
..........................................................................
4. Conformal extended checks recommended:                           0
..........................................................................
5. Design ambiguity:                                                0
..........................................................................
6. Compare Results:                                               PASS
==========================================================================
```

Figure 16. Verification Report of data_top

As the design is Formal verified, verification report in figure 16, ensures that implemented design is bug free without cross domain crossing violations and behavior of design is as expected. So this can be signed-off. Since we have not applied any stimulus some functionality may differ. To make sure the correct functionality, mixed signal validation is done and specter simulation is done for small blocks in hierarchy.

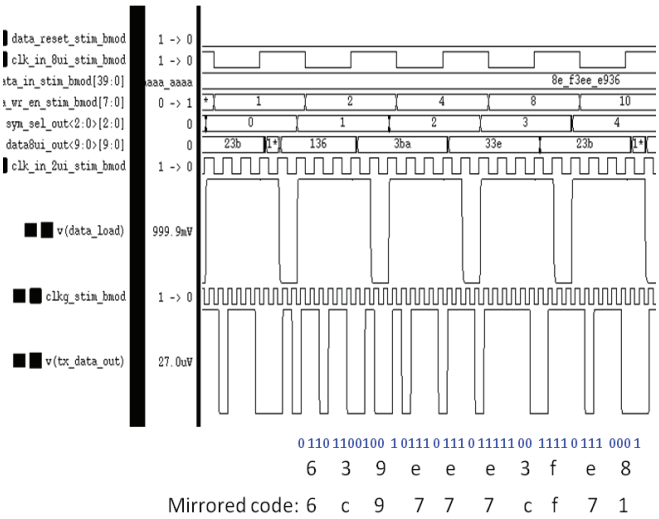

Figure 17. Mixed signal validation results of data_top

Figure 17 shows validation results of data_top with tx_driver for differential signaling. As the input 40bits parallel data feed to data_8ui, which slices 40 bit data into four slices of 10 bit each. Slices are selected using data_wr_en and sym_sel_out to provide output 10bit data parallel as 8UI interfacing at 250MHz in case of Gen 1, 500MHz in Gen 2, 800MHz in Gen 3 and 1.6GHz in Gen 4. data_2ui is separated, even and odd positioned bits of 10bits parallel data into 2 bit serial data at 1.25GHz in Gen 1, 2.5GHz in Gen 2, 4GHz in Gen 3 and 8GHz in case of Gen 4. Finally even and odd stream of 2bit data merged into one bit data tx_data_out using 2x1 mux with select line as the clock (clkg) as 2.5GHz in Gen 1, 5GHz in Gen 2, 8 GHz in Gen 3 and 16GHz in Gen 4. The output serial data tx_data_out in all generations is same as input 40bits parallel data.

VII. Conclusions

The designed high speed IO Transmitter provides high speed operation with less delay (1.81 ns) which is approximately two time faster than design implemented in 45nm technology (delay 4.45ns) and four times faster than design implemented in 90nm technology (7.23ns), with no data loss at the transmitter end. Equalizer is not required at the transmitter because no ISI occurred in the design. There were no Clock domain Crossing violations found which was fully verified using Cadence Conformal tool and validated using Mixed signal validation tool. But care should be taken to avoid ISI at receiver by placing equalizer with sufficient number of taps. Also, because of low pass effect of channel, signal gets degraded at the receiver's end.

The designed circuits are implemented in CMOS logic that can be replaced with CML logic to minimize power. Care should be taken on tail currents driving the logic through current mirror hence variations in the tail current in turn leads to glitches in the circuits. High capacitive loads formed at the current mirror may hold sufficient charge which may effect the operation.

For reducing ISI an efficient equalizer needs to be designed which may be linear or non-liner. Equalizer should be high pass because of low pass effect of routing channels so that it makes the overall response flat. Equalizer should provide sufficient gain at high frequencies. Liner equalizer such as Continuous Time Liner Equalizer (CTLE) or non-linear equalizers such as FIR filters with large or sufficient number of taps will provide the expected response at the driver output of the transmitter.

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Design and Verification of Impedance Matcher in a High Speed Serial IO Interface in 14-nm Technology

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Abstract: **A High Speed Interface corresponding to a PCIe (Peripheral Component Interconnect Express), DDR (Double Data Rate) or USB (Universal Serial Bus) suffices the need for speed, but it is important to eliminate the voltage reflections in the transmission line in the backplane and thus improve signal integrity. This is achieved by a Voltage-mode Impedance Matching circuit, connected to the differential channel of the High Speed Serial IO (Input-Output) Interface. A pair of Replica Circuits (shunt resistors) with switches, are used for calibrating the impedance to be matched with that of the effective resistance obtained at the channel. This is controlled by a Finite State Machine that takes the decision of switching the resistors, which help to match the voltage potential at their respective ends. This decision is made based on the feedback received from a pair of comparators, which are prereferenced with voltage levels, which are appropriate with equivalent voltages corresponding to the notion of effective resistance.**

Index Terms: **Pull-up Replica; Pull-down Replica; Impedance matching; Finite State Machine; Up-Down Counter; Comparators; Formal Verification; Voltage Reflections; MOS Switches; Calibration**

I. Introduction

Serial data communications systems have become increasingly common due to the high cost and synchronization difficulty of transferring parallel data. In a serial data communication system, the parallel data gets serialized in the Transmitting device and gets de-serialized in the receiving device. The Phase Locked Loops (PLLs) of the Transmitting device and the receiving device are used to synchronize data transfer. Serial Data transmission is a profitable means of transferring data. But, the characteristics of the channel and the potentiality of the transmitter and the receiver for sending and retrieving the data, limit the speed of the bit transfer rate. As data rates increase, transmitted signals are attenuated due to bandwidth limitations of the communications channels. Due to this, the phenomenon of Inter Symbol Interference (ISI) occurs, wherein the binary data will spread into the adjacent symbols, that adversely impact Bit Error Rate (BER).

The effect of ISI is reduced, by giving an extra amplitude to the transmitting signal during the transition, which amounts to a signal boost in high frequency. This process of conditioning the signal is called feed-forward equalization (FFE).

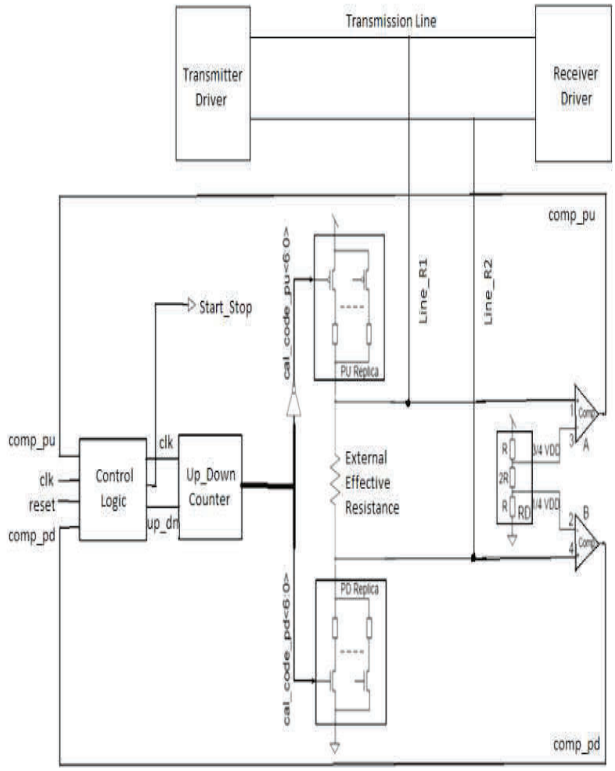

Figure 1. Block Diagram of the Impedance Matcher in a High Speed Serial Interface

It can have a frequency characteristic like a high pass filter. If the loss of the channel is greater than the signal boost, the signal transmitted will get under equalized at the receiver's end. Likewise, if the channel loss is less than the signal boost, the signal transmitted will be over equalized. In addition to the high frequency signal boost, for achieving good Return Loss, the transmitter impedance should be matched to the channel's impedance as predicted by Equation. (1).

From Equation (1), the single ended impedance of the transmission channel is represented by Zo and the differential impedance of the transmitter is represented by

Z_{TX},

$$\text{Return Loss}(dB) = 20 \log \left| \frac{2 \times Z_o + Z_{Tx}}{2 \times Z_o - Z_{Tx}} \right| \quad (1)$$

For maintaining the acceptable Signal Integrity, minimization of signal reflections is required for most of the communication protocols such as USB and DDR. A Characteristic Impedance, *Z*o of 50Ω is observed in many communication channels. Common Mode Logic (CML) based transmitter topologies are still common in recent works, because the transmitter impedance matching to 50Ω is achieved using linear resistors. Furthermore, for achieving signal conditioning capabilities, current steering techniques are used in the output stage.

Voltage mode drivers are more popular. Since FETs biased in the linear region are used as matching elements, it is challenging to match the impedance of a voltage mode transmitter to a line impedance. An FET can behave non-linearly and significantly change its impedance across PVT (Process, Voltage & Temperature) Variations. Since through FFE, signal conditioning is achieved by re-configuring the impedances of the FETs used, it is not as straight forward as the CML topologies.

A voltage mode driver is proposed that achieves a 20 Gbps operation, due to the absence of D [n-1] signal. High pass RC filters which are passive in nature, are used for achieving signal conditioning. In a hybrid approach, the main transmitter acts as a voltage mode driver, while current mode operation is used for realizing Equalization. An approach of programmable equalization current for generating a voltage boost during the transitions, simplifies the Equalization process.

Though the complexity of the Equalization technique offered by this approach is quite simple, it still uses analog supply voltage of 1.2V as the Current Mode Equalization circuit needs enough headroom for keeping the differential pair and current source in the saturation mode. Further, the power consumption increases as the equalization current increases and an increase in size of the Equalization differential transistors occurs for sustaining the current. For resolving this, a voltage-mode transmitter with a 2-tap topology is used.

Equalization is achieved through an impedance matching circuit, by integration of a replica circuit for the main driver, along with the same an auxiliary driver. 1.2V of analog supply is maintained for adjusting the impedance of the pull-up and pull-down paths of the main and auxiliary drivers, in an analog approach where four operational amplifiers are used.

This is a peculiar way to procure signal equalization and transmitter impedance matching in a power efficient feed-forward voltage-mode transmitter. A low frequency state machine along with replica circuit is used, that represents a mixed signal approach. All the components in the Impedance matching Circuit use a single, low voltage supply of 1.0V seemingly.

Signal is transmitted through a 10 inch lossy FR4 channel, by the driver. Impedance matching, signal equalization and voltage mode driver topology together help realize a mixed signal approach. The performance of the driver through analog and digital simulations is demonstrated, which includes Process, Voltage and Temperature (PVT) variations. Further sections present the outcome which recapitulates the performance of the new topology with that of the recent works

II. Transmitter Topology

Drivers based on CML topology require current sources that need a headroom voltage. Contrary to this, Voltage mode transmit drivers are more power efficient than CML based drivers and are hence more advantageous. The total current of a voltage mode driver is proportional to its load current, while it is four times the load current in case of the CML transmitter. The external load resistor R_L is driven by the current from the driver. This resistor represents 2*50 Ω, which is the differential line impedance. *R*pu and *R*pd are polysilicon resistors which help in reducing the non-linear resistance of the FET.

The total load current in this case flows, through P2 and N1. Both N2 and P1 are off and do not consume current. Yet, to match the transmitter's impedance to teat of the line impedance, which is 50Ω, calibration is required due to the non-linear nature of the resistances and corresponding variations pertaining to the FETs. The voltage amplitude (*V*o), becomes approximately VDD/2, if the transmitter and the line impedance are properly matched. There are a good number of proposals for impedance calibration schemes related to the conventional voltage mode transmitting devices. However, such schemes did not entirely account in considering the issues pertaining to the concept of signal conditioning.

III. Improved Topology Of Voltage Mode Driver

Illustration of the proposed voltage mode driver is presented in Figure 2. It consists of programmable pull up devices ranging from P1 to P4 and pull down units ranging from N1 to N4. For achieving high speed operation, low threshold NMOS and PMOS devices are employed. The overall speed versus power tradeoff is still favorable even though the low threshold devices result in very high power consumption.

Further, a sense circuit, integrated with replica circuit and a finite state machine that form a mixed signal block, set the programmability of the units. High frequency boost settings and the calibration code for impedance matching are also taken into account for all PVT conditions. The mixed signal architecture ensures that an impedance of 100 Ω is matched to that of the driver's differential impedance and thereby, we achieve the high frequency signal conditioning.

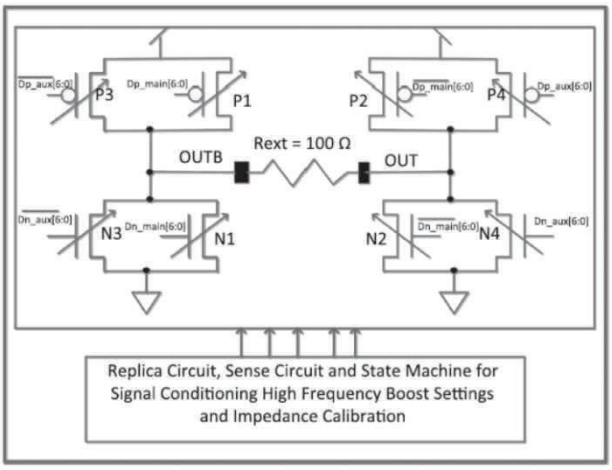

Figure 2. Simplified Schematic of Proposed Driver

IV. Measures For Signal Conditioning

Figure 2, illustrates the categorization of auxiliary and main units which are programmable. Their configuration is such that, maximum swing is totally achieved during signal transitions. The steady state ensures a lower swing. P1, P2, N1 and N2 for the main circuit components while P3, P4, N3 and N4 form the auxiliary circuit components.

If the data pattern is switching, like 1010, both main and auxiliary units are in sync, and the swing is maximum. The units are modeled as linear resistors when they are ON. The maximum swing is predicted by Equation (2). The Transmitting Driver's single ended output impedance becomes 50 Ω and the maximum swing becomes VDD/2, if all the units are properly matched.

$$Vo\_max = 100 \times \frac{VDD}{(RN1 \| RN3) + 100 + (RP2 \| RP4)} \cong \frac{VDD}{2} \quad (2)$$

The auxiliary units in steady state trigger the output contrary to that of the main units. This minimizes the output voltage swing.

The combination of main and auxiliary units is determined by how low the steady state output voltage swing is. For example, a lower steady state voltage requires more auxiliary units and less main units.

In this transmitter, four signal conditioning settings are available depending on the loss of the channel. Table 1 lists how the resistances of main and auxiliary units are set.

The determination of *V*o_min and *V*o_max is done accordingly. The equivalent output resistance of the single ended transmitting device is always matched to 50 Ω in all cases.

V. Implementation Of Impedance Calibration

A decent transmitter impedance is achieved by implementing a mixed signal approach for calibration. All pull-up units that are programmable and ranging from P1 to P4 along with the pull-down units ranging from N1 to N4, serve as the multiples of a unit pull-down and unit pull-up devices. The typical resistance formed for each unit is 3.2 KΩ.

Initially, the effective resistance of a single device is determined by the calibration scheme. The variations in Process, Voltage and Temperature (PVT) impact this effective resistance. This is done by using a transmitter replica circuit and adjusting the multiples of the pull-up and pull-down units until the transmitter is matched to 100 Ω, differentially.

At the instant where the main and auxiliary units have gained a maximum swing and are synced, the calibration is achieved. The values of P1-P4 and N1-N4 are evaluated from the boost setting selected through Table 1, when the signal unit impedance is determined.

Table I
Main And Auxiliary Units Resistances

R_MAIN RP1, RP2, RN1, RN2 (Ω)	R_AUX RP3, RP4, RN3, RN4 (Ω)	Vo_max (V)	Vo_min (Steady state) (V)	Signal boost (dB)
80	133	0.5*VDD	0.125 *VDD	12
67	200	0.5*VDD	0.250*VDD	6
59	350	0.5*VDD	0.350*VDD	3
50	open(∞)	0.5*VDD	0.500*VDD	0

The calibration system, shown in Figure. 3, consists of the following major components:

1. A Pull-up Comparator,
2. A Pull-down Comparator,
3. A Pull-up Replica unit,
4. A Pull-down Replica unit,
5. An Up-Down Counter,
6. A Control Logic (Finite State Machine),
7. A Voltage Divider,
8. A Transmitter Driver and
9. A Receiver Driver

A resistance variation less than or equal to 0.1% is allowed due to an external resistor, which is an on-board component.

Based on the target impedance values from the transmitting device, the appropriate value is chosen depending on the calibration. In this work with non-varying PVT conditions, the differential impedance is found to be 100 Ω.

The pull-up and pull-down replica blocks are connected in series with the external resistance similar to the voltage divider block. Blocks forming an Impedance Matcher.

A serial connection of three polysilicon resistors with nominal values set in proportions to R, 2R and R, forms a Voltage Divider circuit.

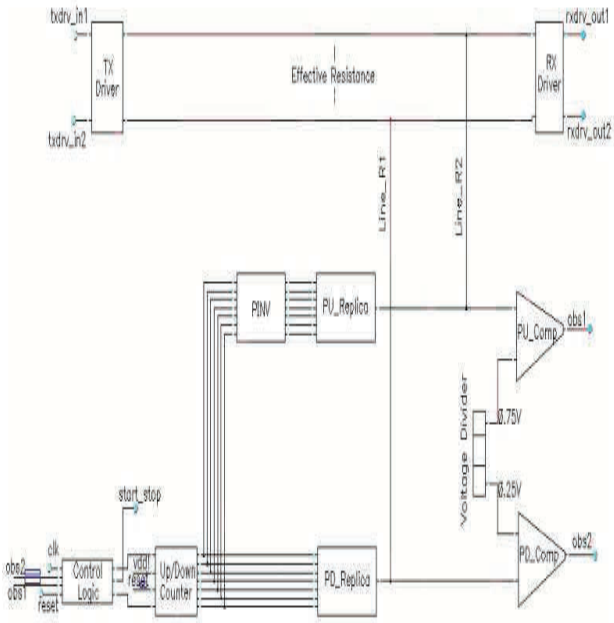

Figure 3. Integration of Analog and Digital

While VDD is the supply voltage, proportions of VDD/4 and 3VDD/4 are set as reference voltages for the comparators. VDD is the circuit supply voltage. The comparators, PU_Comp and PD_Comp compare voltage values between their respective differential input nodes.

The impedances of the pull-up and pull-down replica units are equal to the line impedance of the channel, when the voltage levels between the mentioned pairs get equalized at an equal instant of time. The impedances of the replica units are adjusted by the logic control module which resides in the feedback configuration with the comparators, till the acceptable ranges are achieved. Replica blocks denote the matrix sets of "binary weighted" impedances.

Each element is a serial connection of a MOSFET transistor and a poly resistor. The nominal value of replica impedance in typical PVT conditions is targeted to 50 Ω using the 1000000 control bit combination. In typical conditions, the replica circuit covers impedance range from 25 Ω–3.2 kΩ for the rest of the binary conditions.

The voltage levels of the inputs decide the input stages of the pull-up and pull-down comparators. Since impedance calibration is not mandatory to be a swift process, the designed comparators do not operate at high speeds. The Finite State Machine, which is apparently the Control logic block,takes the responsibility for the decision making of the calibration process. This is done by fetching the information from the comparators along with their respective commands, driven externally. This RTL code is synthesized with the help of the Design Compiler tool from Synopsys.

VI. Calibration Principles Of Operation

The positive edge of the "start" signal triggers System operation that forces the logic module to start calibration. At the initial calibration stage, pull-up and pull-down codes, cal_code_pu, cal_code_pd, are asserted to 1000000 which correspond to 50Ω pullup/pull-down impedance values in typical PVT conditions.

At the positive edge of the calibration clock signal, the PU_rep and PD_rep node voltages at the comparator inputs are compared to 3/4 VDD and 1/4 VDD threshold levels respectively. The comparator output information is fed back to the logic module. Subsequently, if comp_pu voltage is reported high, the comp_pd is checked. If it is detected to be high, the cal_code_pd code, which is the number of ON resistive blocks of the pull-down replica, is increased to decrease pull-down section impedance. Otherwise, cal_code_pu, which is the number of ON resistive blocks of the pull-up replica, and cal_code_pd are decreased together, and the logic cycle is repeated.

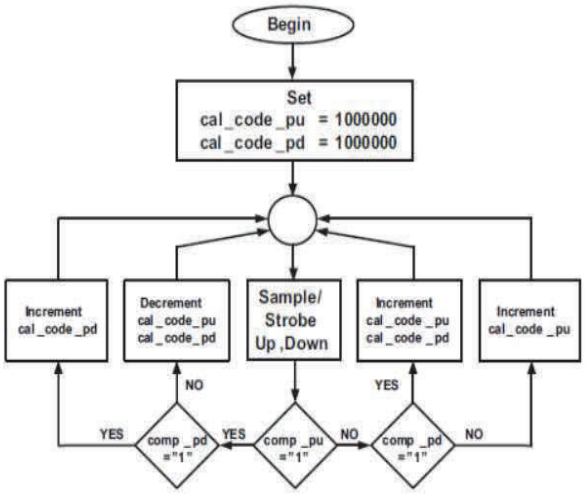

Figure 4. Impedance Calibration State Machine

The comp_pd signal level gets checked, if the comp_pu value gets reported as low. If it goes high, cal_code_pu and cal_code_pd are increased simultaneously. Otherwise, only cal_code_pu is increased. The calibration sequence logic diagram is shown in Figure 4. A positive ready signal is generated by the logic module, when the calibration gets completed. Also, registers are loaded with the binary codes, cal_code_pu and cal_code_pd for the usage of the output buffer residing at the transmitter.

VII. Procuring Signal Conditioning

Once the impedance calibration process is concluded, the transmitter pull-up and pull down units are set depending on the final values of cal_code_pu and cal_code_pd registers and the required signal boost setting. Both main and auxiliary units will present the proper transmitter impedance for any of the signal boost settings outlined in Table 1.

Figure 5 illustrates the process by which the main and auxiliary numbers of units are selected. The main pull-up units, P1 and P2, are set by register cal_code_pu_main. The auxiliary pull-up units, P3 and P4, are set by register

cal_code_pu_aux, and the auxiliary pull-down units, N3 and N4, are set by register cal_code_pd_aux. RTL code is used to implement the digital portion of the state machine.

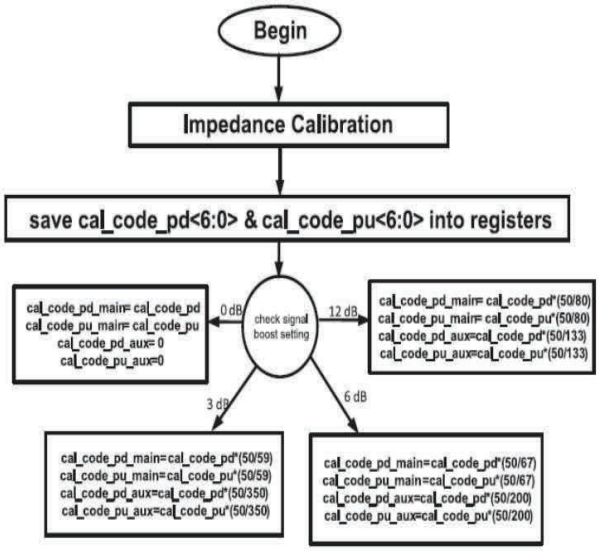

Figure 5. Signal Conditioning State Machine

VIII. Pull-Up Replica Unit

This replica unit consists of seven PMOS (P-type Metal Oxide Semi-conductor Field Effect Transistor) switches whose drains are connected to the weighted resistors ranging from 50 ohms to 3.2K ohms

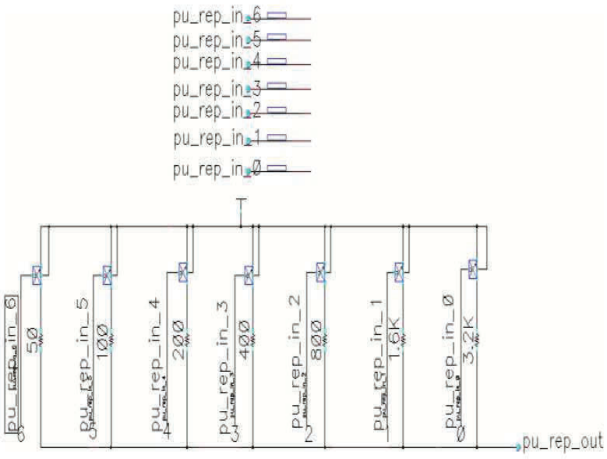

Figure 6. Pull – up Replica Unit

The switches are controlled by the Up_Down Counter whose outputs are connected to the Gate terminals of all the switches, as pu_rep_in_6, pu_rep_in_5, pu_rep_in_4, pu_rep_in_3, pu_rep_in_2, pu_rep_in_1 & pu_rep_in_0 respectively. The initial code programmed into the counter is to set the replica unit to 50 ohm resistance which corresponds to the decimal code of value 60, i.e., 1000000. In order to increase the equivalent resistance of the circuit, the number of switches to be turned on has to be minimal, which is no less than 50 ohms. In order to decrease the equivalent resistance of the circuit, the number of switches are to be turned on, so that the circuit's output potential matches with that of the effective resistance of the external load, i.e., the channel.

IX. Pull-Down Replica Unit

Similar to that of the Pull-up replica, the Pull-down replica unit consists of seven NMOS (N-type Metal Oxide Semi-conductor Field Effect Transistor) switches whose drains are connected to the weighted resistors ranging from 50 ohms to 3.2K ohms.

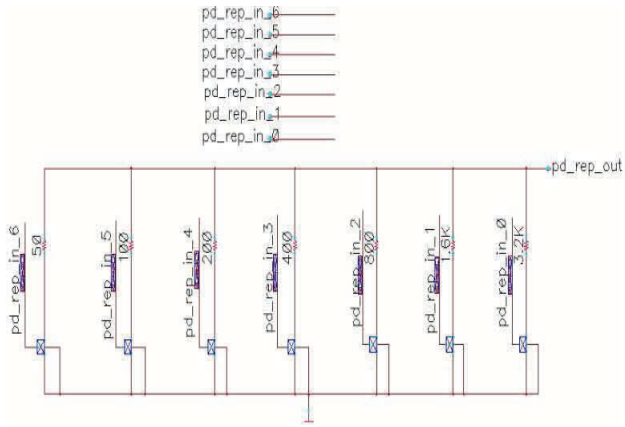

Figure 7. Pull-down Replica Unit

The switches are controlled by the Up_Down Counter whose outputs are connected to the Gate terminals of all the switches, as pd_rep_in_6, pd_rep_in_5, pd_rep_in_4, pd_rep_in_3, pd_rep_in_2, pd_rep_in_1 & pd_rep_in_0 respectively. The initial code programmed into the counter is to set the replica unit to 50 ohm resistance which corresponds to the decimal code of value 60, i.e., 1000000. In order to increase the equivalent resistance of the circuit, the number of switches to be turned on has to be minimal, which is no less than 50 ohms. In order to decrease the equivalent resistance of the circuit, the number of switches are to be turned on, so that the circuit's output potential matches with that of the effective resistance of the external load, i.e., the channel.

X. Finite State Machine

Figure 8 shows the key decision maker of the entire Impedance Matching circuit, whose prominence holds by the output, which drives the Replica units, in the way their output potentials match with the reference voltages at the differential channel termination ends, with respect to that of the reference voltages, 0.75V and 0.25V respectively. The crucial point being the outputs of the pull-up and pull-down comparator circuits, which are fed back as one of the primary inputs to the control logic, i.e., the illustrated Finite State Machine itself.

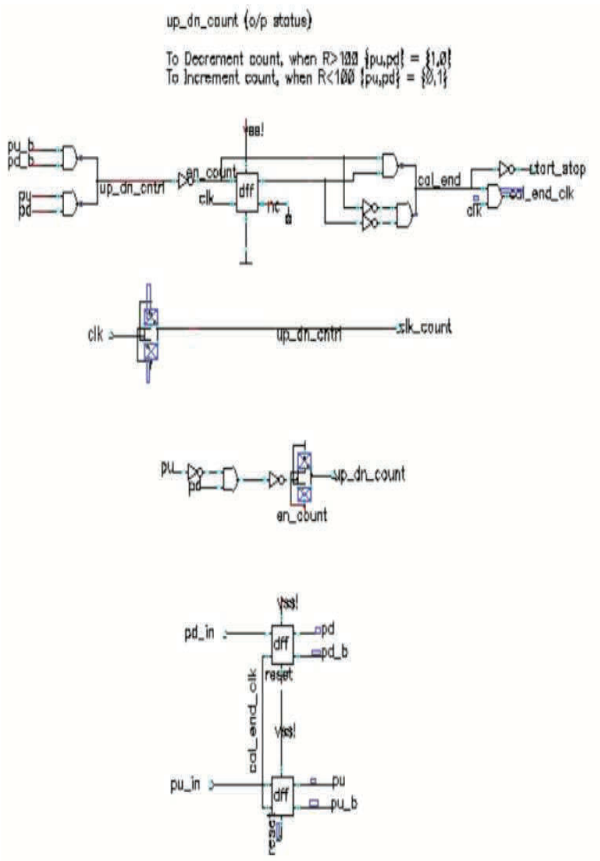

Figure 8. Finite State Machine (Control Logic)

A code of 01 to the input of the control logic, makes it enable the up count (increment) operation of the Up-Down Counter. A code of 10 to the input of the control logic, makes it enable the down count (decrement) operation of the Up-Down Counter.

XI. Up-Down Counter

As illustrated below, the Up-Down Counter has en_count as the control signal, to initiate and increment or a decrement operation of the circuit.

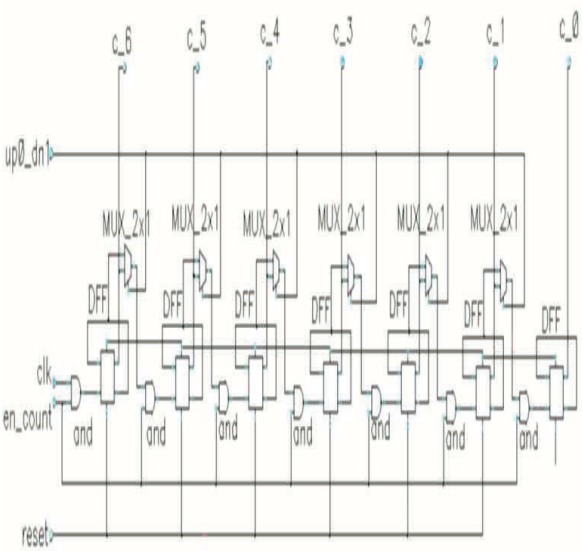

Figure 9. Up-Down Counter Implementation

When the count is enabled, another control signal, i.e., up0_dn1 will hold the charge of either of the two operations to be executed at a time. If a 0 is given to up0_dn1, then an increment of count is done. If a 1 is given to up0_dn1, a decrement operation is done. Usually, the range of value till the point that the counter has to either increment or decrement is decided and controlled by the feedback obtained at the Control Logic. The initial state of the counter is always set to a code of 1000000, which indicates an equivalent resistance of 50 ohms, where it is expected that the termination channel's effective resistance always varies in and around 100 ohms.

XII. Formal Equivalence Verification

Formal verification is a technique used in different stages in the ASIC project life cycle like front end verification, Logic Synthesis, Post Routing Checks and also for ECOs. But when you go deep into it, the formal verification used for verifying RTLs is entirely different from others. There are different formal techniques available as follows

1. Formal Equivalence Checking
2. Formal Property Checking.

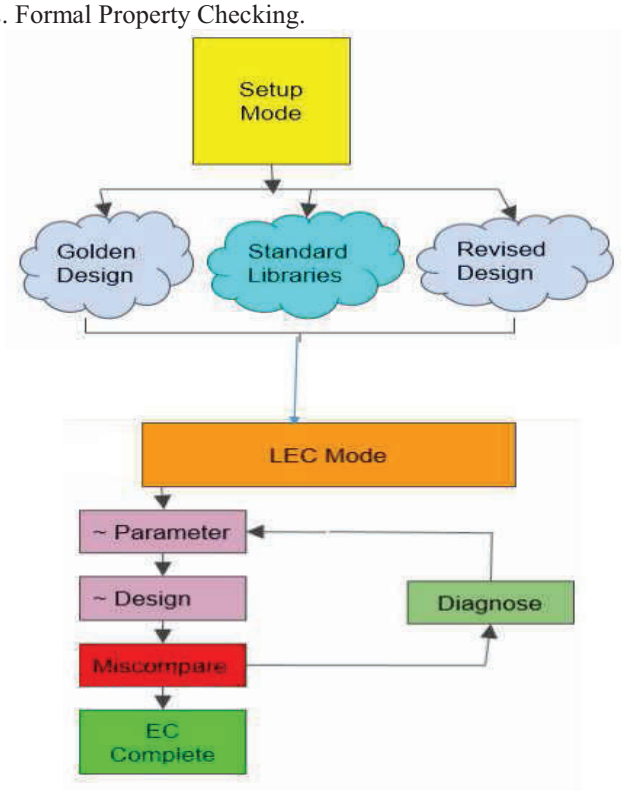

Figure 10. Cadence Encounter Conformal LEC tool flow

Mainly, there are two modes as shown in the figure 10, they are:

1. Setup mode &
2. LEC Mode

It is to be noted that, any changes that are to be made can only be done while in setup mode & the impact of the changes made can only be observed in the LEC mode, which abstracts the given inputs/commands and generates the results accordingly.

XIII. Simulation Results

A. Spectre Simulations

Outputs of Voltage Divider Circuit with 1/4VDD (0.25V) and 3/4VDD (0.75V) are as follows,

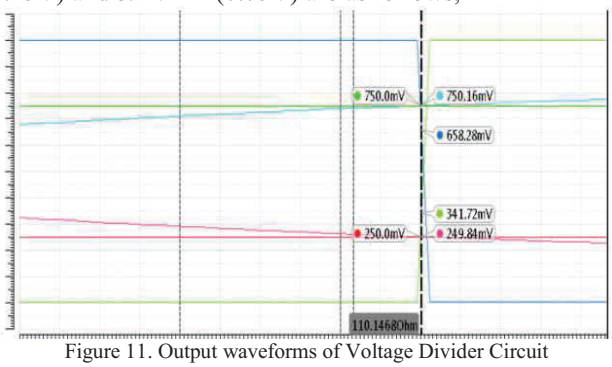

Figure 11. Output waveforms of Voltage Divider Circuit

Outputs of Counter in Incrementing mode from 0 to 127 are as follows,

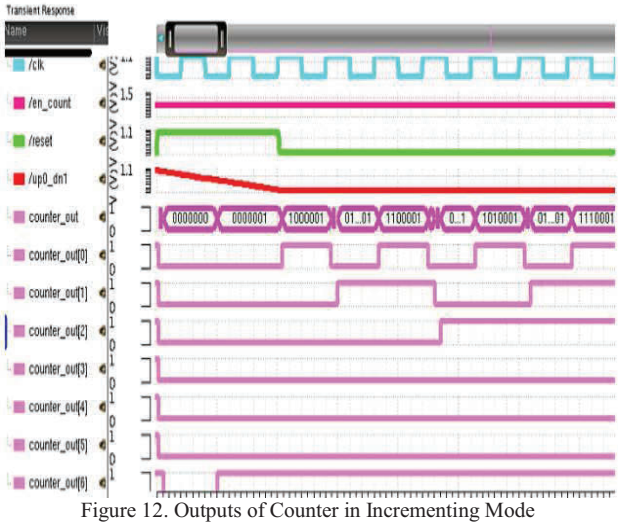

Figure 12. Outputs of Counter in Incrementing Mode

Outputs of Counter in Decrementing mode from 127 to 0 are as follows,

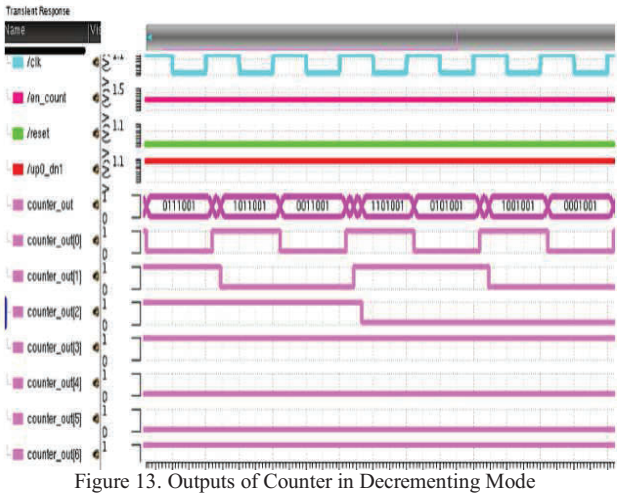

Figure 13. Outputs of Counter in Decrementing Mode

Impedance Matcher output for 80 ohm effective resistance, with the calibration code of approximately 40.5063291 is 1001111, is as follows,

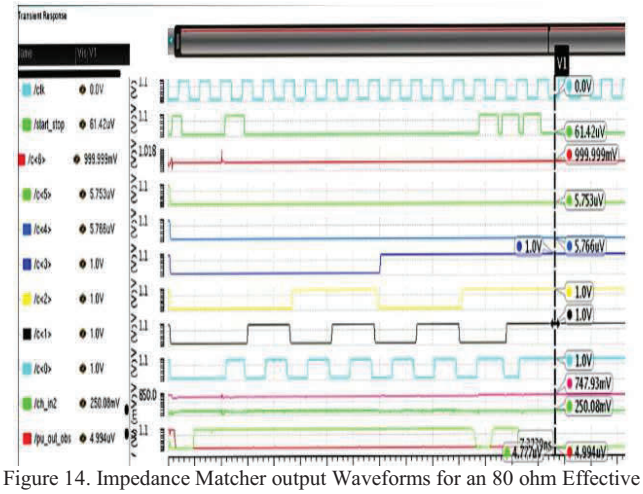

Figure 14. Impedance Matcher output Waveforms for an 80 ohm Effective resistance

Impedance Matcher output for 120 ohm effective resistance, with the calibration code of approximately 61.53846154 is 0110100, is as follows,

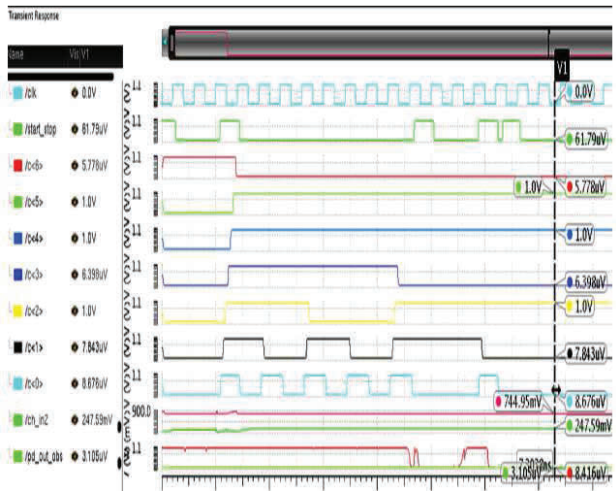

Figure 15. Impedance Matcher output Waveforms for a 120 ohm Effective resistance

B. RTL Simulations using Synopsys VCS

The RTL simulation of Impedance Matcher is illustrated in the following figure.

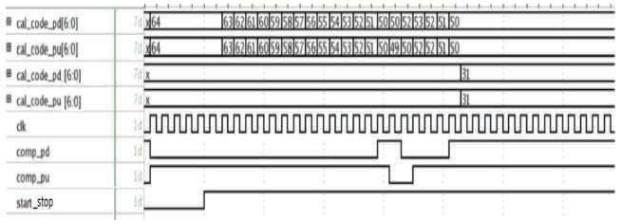

Figure 16. RTL Simulation output waveforms

It can be observed that, for an effective resistance of 100 ohms, when the cal_code_pu and cal_code_pd reach 50 ohms each, respectively, the calibration stops. The beginning and ending of the calibrations are indicated by the start_stop signals. The comp_pu and comp_pd are the outputs of the pull-up and pull-down comparators respectively.

C. *Formal Verification Report*

The Final Verification report corresponding to the Formal Verification of the Impedance Matcher circuit in a High Speed Serial IO Interface is as follows,

```
==================================================================================
                              Verification Report
----------------------------------------------------------------------------------
Category                                                                    Count
----------------------------------------------------------------------------------
1. Non-standard modeling options used:                                        0
----------------------------------------------------------------------------------
2. Incomplete verification:                                                   2
     User added black box:                                   yes
     Black box mapped with different module name:            yes
----------------------------------------------------------------------------------
3. User modification to design:                                               0
----------------------------------------------------------------------------------
4. Conformal Constraint Designer clock domain crossing checks recommended:    0
----------------------------------------------------------------------------------
5. Design ambiguity:                                                          0
----------------------------------------------------------------------------------
6. Compare Results:                                                         PASS
==================================================================================
```

Figure 17. Formal Verification Report on Impedance Matcher Circuit

XIV. Conclusions

Design and verification of an Impedance Matcher Circuit in a High Speed Serial IO (Input – Output) Interface has been implemented and verified successfully. The circuit encompasses the calibration of Impedances and capability of signal conditioning for high frequencies. A combination of the illustrated Pull-up and Pull-down Replica circuits, reference resistors, comparators and a digital state machine were used to form a mixed signal circuit. The calibration of impedance is accomplished with the detection of variations in resistance of pull-down and pull-up units used in the replica devices.

The Control Logic is used for settling the replica circuit resistances until the output stage is balanced to the impedance of the channel. The transmitter was designed in 14nm CMOS technology using a 1V nominal supply voltage. It is simulated using Synopsys VCS and mixed mode simulation tools. The at-speed power is 7.2 mW. This power is achieved at extreme process corners and maximum high frequency signal boost. The maximum impedance deviation from 50 Ω is 2.5% at all variations of process, temperature and voltage supply corners.

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BER Analysis of Digital Modulation Schemes using LabVIEW

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Abstract: **Since the last few decades there has been an abrupt rise in technology and all the communication devices of the new generation mostly rely on digital transmission of information. Thus, it has become necessary to give better and efficient services to users by employing better digital modulation techniques. This paper analyses the Bit Error Rate (BER) performance of different digital modulation schemes such as Binary Phase Shift Keying (BPSK), Quadrature Phase Shift Keying (QPSK) and Quadrature Amplitude Modulation (QAM) using LabVIEW. The Additive White Gaussian Noise (AWGN) channel is used for analysis and modulation. As LabVIEW is a graphical programming environment it gives good visualization of the results and it also allows us to design systems in an intuitive block based manner in short time as compared to other commonly used text based programming languages. Thus, it is concluded from the simulation results that BPSK outperforms QPSK and QAM in terms of BER.**

Index Terms**: AWGN, BPSK, QAM, QPSK**

I. Introduction

Communication is the process of conveying information from one entity to another in sending or receiving information between two or more people. The one who sends the information is called sender or source of information and the one for whom the information is destined is called the receiver or user. A Simple communication system consists of a transmitter, a channel and a receiver.

Conventional methods of communication use analog signals for long distance communication. But these systems suffer many losses such as interference, distortion, attenuation as well as other losses including security. To overcome these problems, the analog signals are digitized which allow the communication to be more clear and accurate without losses. Not only this, the digital system is more reliable, easy to design, cheap but also can be saved and retrieved more conveniently and above all the capacity of the channel is effectively utilized.

The process of digitization [1], [3] involves steps such as Sampling, Quantizing and Encoding which are performed in analog to digital convertor section. The receiver performs the reverse operations like decoding and reconstruction of the quantized pulse train which is then given to reconstruction filter to get the original signal.

Digital modulation [1] techniques provide more information capacity, high data security and fast system availability with a great quality of communication.

With tremendous development in digital communication systems it is very important to ensure the quality of service for real time transmission of video applications and provide user with more powerful and efficient services by using better modulation techniques.

The most commonly used digital modulation schemes are BPSK, QPSK & QAM as they offer the lowest bit error rate as compared to other digital modulation techniques like ASK, FSK, DPSK and other M-ary techniques.

In this paper BER [2] analysis is performed under AWGN channel using LabVIEW for modulation techniques i.e. BPSK, QPSK and QAM [10].

The paper is organized as follows:

- Section II discusses about the digital modulation schemes, BER and AWGN channel in detail.
- Section III describes the LabVIEW simulation and implementation of the generalized block diagram.
- Section IV gives the simulation results.
- Section V concludes the paper.

II. Digital Modulation Schemes

A. BPSK

It is one of the most commonly used digital modulation technique where in the phase of the carrier signal is varied according to the input bits at a particular time.

In this technique , the sine wave carrier usually takes two phase values such as 0^0 and 180^0.

B. QPSK

It is a variation of BPSK which sends two bits of digital information at a time. This results in the bit rate to half and allows space for other users. Since it transmits a combination of 1's and 0's, the generated bits are 00, 01, 10 and 11. Each of this combination of 2 bits is represented by a phase reversal such as 45^0, 135^0, 225^0 and 315^0.

C. QAM

It is a combination of both analog and digital schemes. It actually conveys two message signals or two digital streams by changing the amplitudes of two carrier waves using amplitude shift keying or amplitude modulation. These two carrier waves of the same frequency are out of phase with each other by 90^0 and are called as quadrature carrier or quadrature components.

D. BER

It defines the number of bits that are in error out of the total number of transferrable bits during an observation period. BER is evaluated using simulations assuming simple channel models usually AWGN channel without fading. If E_b is the energy of a bit and N_o is the noise power then BER is taken as a function of E_b/N_o and is expressed as

$$BER = \frac{1}{2}\, erfc\sqrt{(E_b/N_0)} \quad (1)$$

where erfc is the complementary error function of argument E_b/N_0. Plot of BER curves are used to describe the performance of a digital communication system.

In wireless communications, BER (dB) versus SNR (dB) is generally used.

E. AWGN chnnel

AWGN channel is one of the wireless communication [4], [7] channel model which considers a linear addition of white noise with a constant spectral density and a Gaussian distribution function of amplitude. It is a simple and tractable mathematical model which does not take into account fading interference, non linearity or dispersion but gives a useful insight to gain the underlying behavior of the system.

For AWGN channel model the channel capacity is given by the equation

$$C = B\log_2(1+S/N) \text{ bits/sec} \quad (2)$$

where B is channel bandwidth in Hz, S/N is Signal to Noise ratio in bits/sec

III. LabVIEW Implementation

LabVIEW (Laboratory Virtual Instrument Engineering Workbench) [5], [6], [8] is a graphical programming environment and has become prevalent not only in research labs but also in industries as well as in academia. It gives a powerful and versatile analysis for measurement and automation. The LabVIEW graphical programming language is called Programming and is performed using a graphical block diagram which compiles into machine code and eliminates many syntactical details. Since it is software based, it offers much flexibility than the standard laboratory instruments. It is possible to view and modify data and/or control inputs easily using LabVIEW.

As the appearance and operation imitate physical instruments like oscilloscope, the programs of LabVIEW are called Virtual Instruments (VI's). LabVIEW offers various display options and is designed to facilitate data collection and analysis.

LabVIEW contains with it the tools to help in troubleshooting the code and a comprehensive set of VIs and functions for acquiring, analyzing, displaying and storing data. LabVIEW has many built in features and may be used as a tool for simulation and control. It can be implemented on any of the platforms including Microsoft Windows, UNIX and LINUX. Other advantages of using LabVIEW is that it is possible to vary the input parameters and the corresponding results by making a change in the appropriate block in the front panel.

LabVIEW has built in analysis capability with functions to generate signals, analysis, visualization, and processing of standard and custom digital and analog modulation formats. All these are possible using the Modulation Toolkit which is available as a built-in with LabVIEW. The Toolkit helps to rapidly develop custom applications for research, design, characterization, validation, and test of communications systems and components that are used to modulate and demodulate signals. The various Modulation Toolkit applications include analog and digital modulation schemes like AM, FM, PM, ASK, FSK, MSK, GMSK, PSK, QPSK, PAM, and QAM. These modulation schemes are the foundation of many digital communication standards found in 802.11a/b/g/n, ZigBee (802.15.4), WiMAX (802.16), RFID, satellite communications, and commercial broadcast among others.

To work with RF signals, the Modulation Toolkit (MT) complements the PXI-5660 RF vector signal analyzer and the PXI-5671 RF vector signal generator. For low frequency signals like baseband and IF signals the Modulation Toolkit works with the 100 MHz mixed-signal test platform with digitizer, analog waveform generator, and digital waveform I/O products.

Figure.1 gives the block diagram of a digital communication system generated using LabVIEW. As shown in figure 1, all the three modulation techniques BPSK, QPSK & QAM are implemented in a single system. The system uses a PN sequence generator which generates a random signal and is applied to BPSK, QPSK and QAM blocks. Each of the blocks internally has its own communication system i.e. Modulator, AWGN channel and a Demodulator. The bits are modulated and demodulated in their respective blocks. The output from each block is given to respective constellation graphs as shown and is also applied as inputs to a single BER block which generates the BER plot for the three modulation schemes.

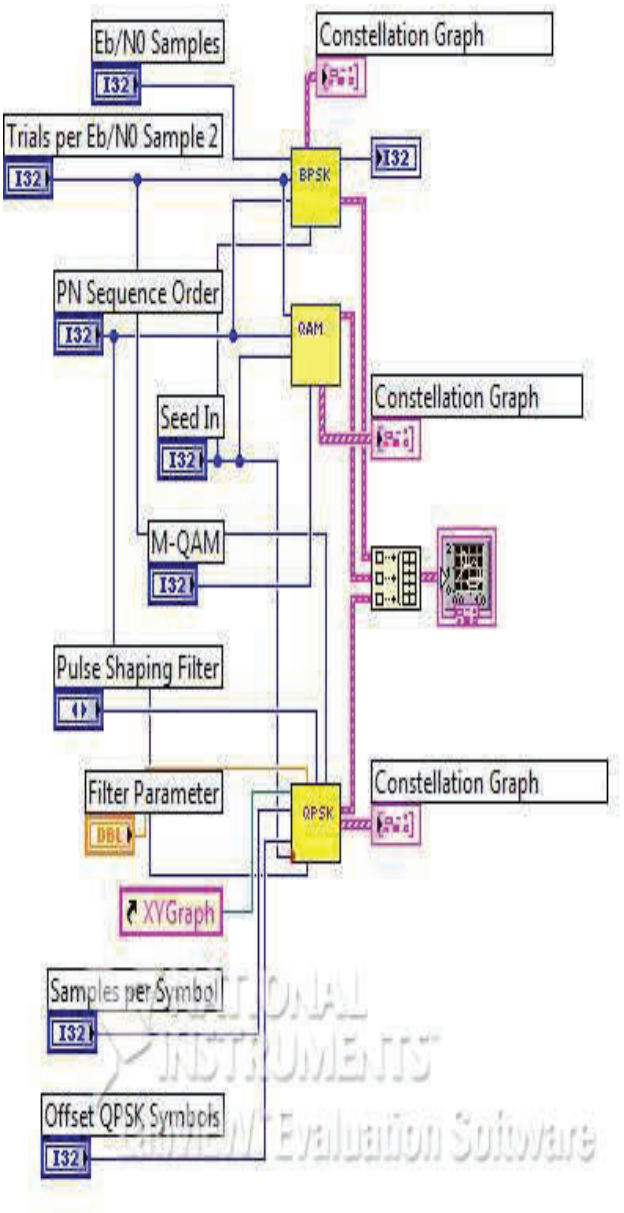

Figure 1. Block Diagram of a Digital Communication System generated using LabVIEW

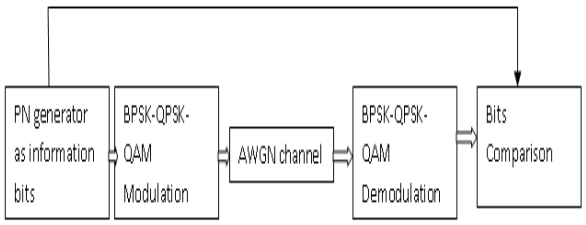

Figure 2. Communication System using LabVIEW

A. PN Sequence Generator

The PN sequence generator generates Galois pseudonoise (PN) bit sequences. The selected pattern is repeated unless the total number of bits that is specified is generated. Use this node to specify the primitive polynomial that determines the connection structure of the linear feedback shift register (LFSR).

The generated bits are applied as inputs to the modulator block. Figure 2 shows the block diagram of a communication system which implements all the three modulation schemes.

B. Modulator

The input bits from the sequence generator are mapped to symbols. Number of symbols indicates M-ary of the modulation scheme.

$$\text{Bits per Symbol} = \log_2(M) \quad (3)$$

For example, 16QAM has sixteen different combinations of amplitude and phase. Each is assigned a 4 bit sequence. These symbols are then passed through an AWGN channel.

C. AWGN Channel

The AWGN channel generates a complex Additive White Gaussian Noise (AWGN) with uniform power spectral density with zero mean and adds it to the complex baseband modulated waveform from the modulator block. The AWGN channel gives a signal-plus-noise waveform with E_b/N_0, where E_b represents the energy per bit, and N_0 is the noise variance.

D. Demodutor

At receiver side the received signal is down converted so that a constellation graph can be plotted. The signal is then re-sampled using MT fractional re-sampler as demodulator needs integer number of samples per symbol. This sampled signal is demodulated to give the output similar to input by removing frequency and phase offsets.

E. Comparator

The comparator compares the transmitted bit stream with the received bits from the demodulation process. These bits need not be synchronized if an MT calculate BER node (block) is used. The MT Calculate is used to calculate the average bit error rate for a Galois PN sequence. The two sequences i.e the PN sequence generated by MT Generate Bits (Galois, PN Order) with a matching PN order and the received sequence must be same.

IV. Simulation Results

In this paper, LabVIEW is used to design and implement the communication system block for modulation schemes – BPSK, QPSK & QAM and their performance is evaluated by finding BER versus SNR over AWGN channel.

Figure 3 shows BER versus SNR plot generated by the BER plot generator using LabVIEW. From figure 3 it is clear that BPSK has lowest BER compared to QPSK & QAM. For example at E_b/N_0 of 4dB, BER value in BPSK is less than 0.01 where as for QPSK it is greater than 0.01 and for QAM it is nearer to 0.1.

At SNR=6, BER value for BPSK is 0 whereas for QPSK it is 0.005 and for QAM it is 0.05.

At SNR=8, BER value for BPSK & QPSK is 0 where as QAM has a value of 0.01.

At SNR =10dB, BER value for BPSK & QPSK is 0 where as for QAM it is greater than 0.001.

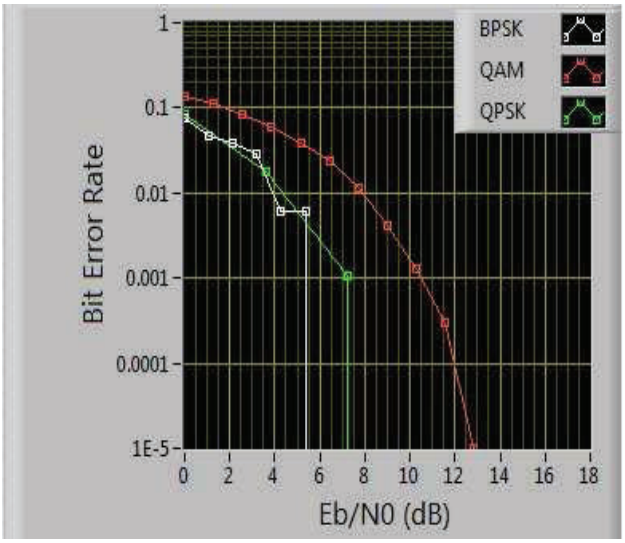

Figure 3. BER graph for BPSK, QPSK and QAM using LabVIEW

The BER value over AWGN channel for BPSK, QPSK and QAM is also given in tabular form in table1.

TABLE I.
COMPARISION OF BER VALUES

E_b/N_0 in dB	Digital Modulation Schemes		
	BPSK	QPSK	QAM
4	< 0.01	>0.01	~0.1
6	0	0.005	0.05
8	0	0	0.01
10	0	0	<0.01

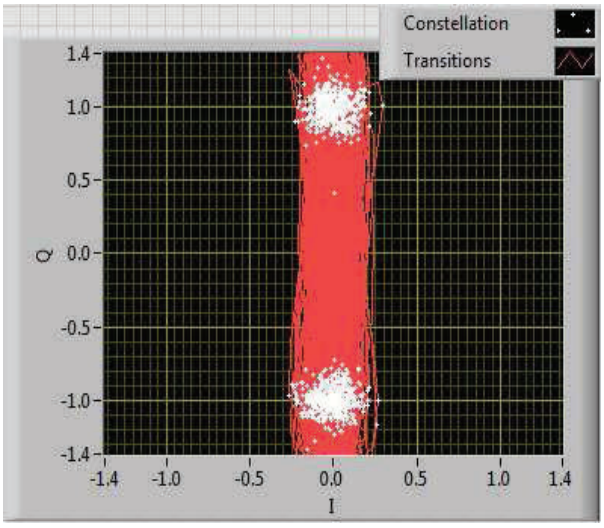

Figure 4. Constellation diagram of BPSK using LabVIEW

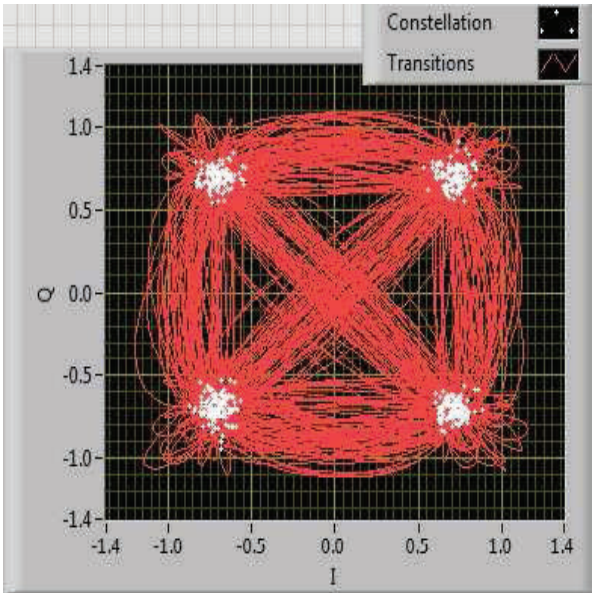

Figure 5. Constellation diagram of QPSK using LabVIEW

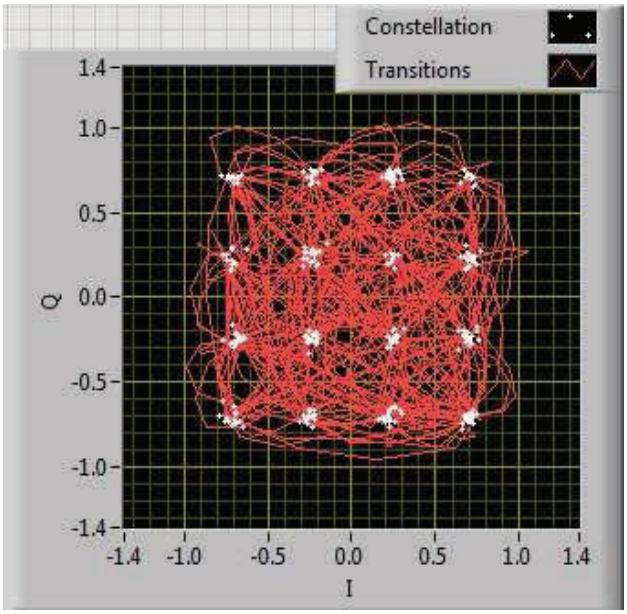

Figure 6. Constellation diagram of QAM using LabVIEW

Figure 4, 5, 6 gives constellation diagram of BPSK, QPSK and QAM as generated using LabVIEW. White dots in the constellation graph signify symbols and red lines give the transition from one symbol to another symbol. In figure 4, the constellation diagram of BPSK shows 2 bits each with a phase difference of 180^0. In figure 5, QPSK has four combinations of two bits and thereby each combination has a phase difference of 90^0. Figure 6 shows 16 QAM constellation diagram where 16 different combinations of amplitudes and phases are generated.

V. Conclusions

Commonly used digital modulation schemes like BPSK, QPSK & QAM are designed, implemented and their performance based on BER over AWGN channel is evaluated in LabVIEW. Through simulation results it is concluded that BPSK performs better compared to QPSK and QAM. The graphical environment of LabVIEW was easy to learn and simple to transform the concepts to a working program and it is also possible to continuously vary the input parameters and observe the corresponding results. In conclusion, the whole system is user friendly and BPSK gives the least number of bits in error for a given number of input bits compared to QPSK and QAM.

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Service Oriented Architecture based Embedded System Software Testing for Mobile Service

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***Abstract*: In recent years, for a range of mobile applications, the need for getting data or information from one place to another has been a driving force. There is huge demand for the usage of Service Oriented Architecture for different applications, if the number of embedded systems is increased. To distribute and estimate technical realizations of business tasks, embedded system provides a systematic way. But there are some limitations for embedded systems in computing environment- a mobile computer is equipped with more powerful capabilities. It maintains a small database, capacity of data processing, a narrow user input of user and small display. This paper presents how to overcome mobile limitation using embedded system software testing based on SOA. For further improvement of embedded system, it is first analyzing mobile application requirement, then write down the service specifications, enhancing the design providing extended use case specification which test use case testing and testing service test case which is derived from service specification.**

***Index Terms:* Service Oriented Architecture (SOA), Embedded system software, Testing, Business Process Execution Language (BPEL).**

I. Introduction

To connect different services, a new approach based on service is developed. The principle thought of SOA- Service Oriented Architecture is to give free-coupled segments between programming parts in a perspective of administration execution and to acknowledge business benefits in a perspective of objective of big business.

A service is a discrete unit of usefulness that can be gotten too remotely and followed up on and refreshed freely. For example, recovering a credit card record on the web [1]. There is a huge demand for the usage of SOA for different applications, if the number of embedded systems is increased. Even though embedded system gives a systematic way to distribute and estimate technical realizations of business tasks, there are some limitations for embedded systems in computing environment. To overcome the embedded system's limitations, this article presents embedded system and testing based on SOA [2]. To improve efficiency of embedded system, it will analyze mobile application requirement, writing service specification, optimizing design, and testing service test case which is derived from service specification.

A. Definition of SOA

A definition is provided below:

Oasis (www.oasis-open.org) defines SOA as -- "It is an architecture, which provides loose pairing among different services."

Arasanjani, Borges and Holley define SOA as follows: "It is an architecture, that backs loosely paired services to empower business adaptability in an interoperable, innovation skeptic way [3]. SOA comprises of a composite arrangement of business-adjusted services using interface-based service portrayals that support an adaptable and progressively re-configurable end-to-end business tasks."

B. *SOA Benefits and Implementation Principles*

SOA provides advantages in the following four basic classes:

- Decreasing integration cost
- Increasing reuse of resource
- Increasing agility of business
- Decreasing the business risk

These four core benefits actually offer return at many different levels and parts of the organization, depending on the set of business problems the company is applying SOA to. This research article consists of five sections [4]. In section 2, the related research which corresponds with embedded system testing is reviewed. In section 3, SOA based mobile interoperability testing is suggested. In section 4, design and test mobile SOA application is discussed. In section 5, the results are explained.

II. Literature Survey

In this section, the requirement of a Service Oriented Architecture (SOA) is reviewed, and requirements specification is obtained.

The following figure 1 shows the basic SOA architecture which operates from user interface to message channel.

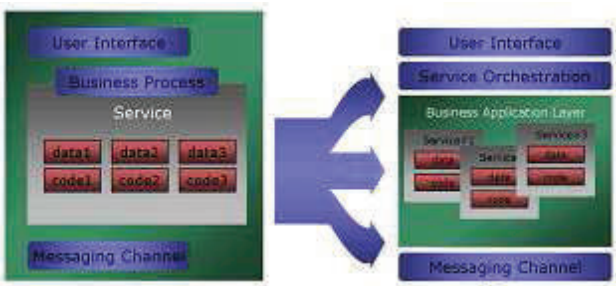

Figure 1. Basic System Oriented Architecture

A. Service Oriented Architecture Service Specification

Service specification of system of Architecture use MDA (Model Driven Architecture) [2] which realizes the model and UML (Unified Modeling Language). Unified Modeling Language specifies the requirement. System of Architecture service specification has two programs. They are system business driven specification and driven specification [4]-[9]. The UML modeling tool, which uses MDA modeling and unified modeling to integrate and to specify the service specification.

B. Designing of Mobile Service

As in this embedded system service design, Do Van Thanh [10] and Glaschick,R [4] has researched about mobile and embedded service. It proposes mobile agent Architecture which utilizes service in mobile. Mobile Agent architecture provides artificial and efficient mechanism using mobile device, but it does not lie at the origin in service [15]. We consider that we make analysis of mobile service from business requirement to user interface.

C. Testing of System of Arhitecture

As referring to Hans-Gerhard Gross [10], CBD testing (Component Based Development testing) in service has some trouble [11]. In CBD based service testing, there are two approaches which were 'interoperability testing' [12] and 'use case testing'. No proposed component based interoperability testing which behavior is modeling technique based on EFSM for interoperability testing [14]. We use EFSM approach to specify service test case generation. Extended Finite State Modeling based case specification includes some information about test case specification identifier, test items, input specification, output specification, environment needs, special procedural requirements and inter-case dependencies [15].

III. Testing of SOA based Embedded System Application

In this section, the process of testing of mobile service which origins from business requirements, service specification to service test case elicitation and testing is explained.

Whole process is:

- Analysis of Business model
- Identification and specification of Mobile service
- Application service identification and specification
- Testing design
- Test and Implementation

It starts from business model analysis which makes a service boundary from business requirement and makes initial business use case and actor [9]. Because a System Architecture's service providing mechanism is a loosely-coupled component and a form of service component, to analyze mobile service, it considers functional requirement as well as non-functional mobile restriction. Mobile service specification describes service details including main flow and restriction. This architecture is origin to test case design, implementation and testing. Using service specification, we define EFSM rule and design state transition diagram for service interoperability testing [8]. We design test case specification based on diagram which test service testing.

A. Business Model Analysis

Enterprise has a business model of its own. In business environment, It is analyzed both information architect view and business operator view with service expose and service consumer. It makes integrating view which between information and business in phases. It produce business context diagram between stakeholders.

Requirement analysis embodies business context diagram with system view. This approach derives basic foundation of functional business requirement, system requirement, non functional mobile restriction and deployment. It produces system level requirement and initial implementation context diagram.

B. Identification and Specification of Embedded System Service

Service identification and specification is made of use case, technical requirement, asset analysis, industrial standard analysis. SOMA (Service Oriented Modeling and Architecture) is proposed by alam [16]. We extend SOMA to adapt mobile service application. We propose a model which is a decompose model. It uses three approaches that is top-down approach, bottom-up approach and middle-out approach. In this paper we recognize sub systems, flow of subsystems and analysis messages and events. Service specification traverse requirements with consumer view which focus on consideration with traceable, stateless, discoverable, reusable and mobile restriction. In this process, it produces service specification.

C. Interoperability Testing of Embedded System Service Design

By using service specification, we design test case which is proposed by Noh [13].

Testing design steps are:

1. EFSM definition
2. Attribute identification table
3. Attribute value definition
4. State transition table
5. Test case specification

1. EFSM:

It characterizes EFSM (Extended Finite State Modeling) Control which expands FSM for testing of interoperability [13].

From state to state, following parameters may vary— {Input} {Output} {Predicates} {Actions} {Color}

2. Specify the table of attribute identification:

As following the EFSM rule, from utilize case to recognize service specification which puts forth interoperability test defense detail, it specifies table of attribute identification [12]. Following table I shows attribute identification table.

TABLE I
TABLE OF ATTRIBUTE IDENTIFICATION

S. no.	Corresponding	Behavior	Alternative circumstances	attributes

3. Attribute value:

It is defined from the above table of attribute identification. The following table II shows attributes, attributes values and service ID.

TABLE II
TABLE OF ATTRIBUTE VALUE

Service ID	Attributes		Values of attributes		
State No		S1	S2	S3	S4

4. Specify table of state transition:

This table is derived from EFSM specification. Table III shows the table of state transition.

TABLE III
STATE TRANSITION TABLE

S. no.	From state	Prerequisite	Input	Post-condition	To state

5. Test case specification:

Test case identifier, test item, state transition are shown here. Also it includes information of service use case ID, interoperability, behavior, I/O, procedural requirements and inter-case dependencies [14].

IV. IMPLEMENTATION AND TESTING

A. Implementation of BPEL

Embedded system is implemented by using web service and Business Process Execution Language.

```
< xml version="2.0" encoding="UTF-8"?>
<definitions
name="View
Reservation"...../ViewReservation"...">
<types>
:
.
<types>
<types>
</types>
<message>
name="viewreservationrequestmessage"
<partname='payload' element=" ">
<message>
<porttype name="viewreservation">
<operation name="initiate">
<input message="client">
.
```

Figure 2. Example of WSDL

Figure 2 WSDL descriptions which include type of service, message information, type of port, type of partner link, and so on [11]. Information of Business process execution is described by BPEL based on specification.

```
<task name="Viewreservation" targetnamespace=" "
">
<partnerLinks>          .......
<partnerLink name="Createreservation".....
partnerLinkType="client:ViewReservation"
Role=" " partnerRole="ViewReservationRequester"/>
<partnerLinkRole=""
name="System" partnerRole=" "
partnerLinkType" <partnerLinks>
<variable name="reservID" type="ns1:int"/>
.
:
<!-- COMPOSITIONLOGIC -->
<assign name="assign_uid_to_requestUid">
```

Figure 3. Example of BPEL

BPEL description includes task's namespace; business partner, variable, logic of composition and etc are shown in figure 3.

Figure 4 shows capture of mobile screen which displays the reservation service [10]. It displays functional requirements as well as nonfunctional requirements.

(a)

(b)

Figure 4(a and b) Capturing Mobile Screen

B. Embedded System Service Testing

Quality of test case depends on the completeness and optimization of the test case. Test case completeness is a method of test case measurement which indicates how many errors are detected with test case [16]. Test case optimization means how many test cases which are not expecting one is included during testing.

TABLE IV
RESULTS OF INTEROPERABILITY TESTING

Completeness	The number of methods which have Interoperability	The number of methods which include test case
	26	23
Test case optimization	Number of transitions before rule definition	Number of transitions after rule definition
	21	10

Table IV shows the results of interoperability testing. The result means highly completeness and optimization.

V. CONCLUSIONS

In this article the mobile service implementation and testing based on SOA to overcome embedded system restriction and to test service interoperability is presented. To improve the mobile efficiency, it is proposed that the service testing process use interoperability testing. The mobile application requirement analysis, service specification, optimize design are presented and test service interoperability which derived is from test case specification.

This article explains the implementation of embedded system service from business requirement to test case. It proposed a different type of mobile service testing process using test case specification. In this, service interoperability testing, results show high accuracy, completeness and optimization. Moreover, this approach of service interoperability test process can extend the application testing to develop cost efficient and optimized mobile services.

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Vehicle Collision Avoidance System by Blind Spot Monitoring and Drowsiness Detection in Automobiles

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***Abstract*: Driving a vehicle in the present traffic conditions is a great challenge for humans. So many automated techniques like auto braking, airbag exposure in case of collisions are introduced as vehicle safety systems. Driver's unawareness about the presence of a vehicle or obstacle in the blind spot area and distracted driving are the main reasons, which cause vehicle collisions in the present scenario. The aim of the project is to take preventive measures against the vehicle collisions using 1.Blindspot Monitoring and 2.Drowisiness Detection techniques. This system prototype is built on the base of embedded platform using RASPBERRY PI microcontroller with ARM11 processor.**

1. Blindspot Monitoring: This technique is used when there is an obstacle present in BSA and, during lane divergence; collision may occur in overriding situation. To avoid this phenomenon, ultrasonic sensors are used to detect the vehicles/obstacles in the blind spot region.

2. Driver Drowsiness Detection: The drowsiness of the driver is detected by capturing and processing image using MATLAB software. As soon as the driver feels sleepy, the microcontroller controls the DC motor connected to the wheels of the vehicle.

***Index Terms*: Blindspot area (BSA), drowsiness detection, Raspberry pi.**

I. Introduction

In the present scenario, the toll of road accidents has been in the increasing graph and many accidents are caused due to negligence of the driver. Most of the accidents also happen in the highway driving, where driver's have negligence during lane switching of vehicles. Thus, detecting the obstacle near the vicinity of our vehicle during lane switching or during highway driving is vital. The advanced automotive technology has been developing better systems to enhance the driver safety. The automotive technology is always on the thought of enhancing and, bettering the safety of the vehicles than their predecessors. Automobile manufacturers have proposed many safety schemes till date, like, collision forewarning technology, lane departure warning system (LDWS).

This paper describes about two vehicle collision avoidance techniques, which are as follows

1. Blind spot monitoring technique and
2. Drowsiness detection technique.

A. Blind spot monitoring technique

Blind spot[3] is the area where the driver cannot observe properly during driving, as mentioned in fig.1, due to many factors like head rest, pillar obstacle, passenger height etc., and many accidents occur due to sudden overriding of vehicles in the blind spot region. Hence this area needs to be monitored and obstacle needs to be detected.

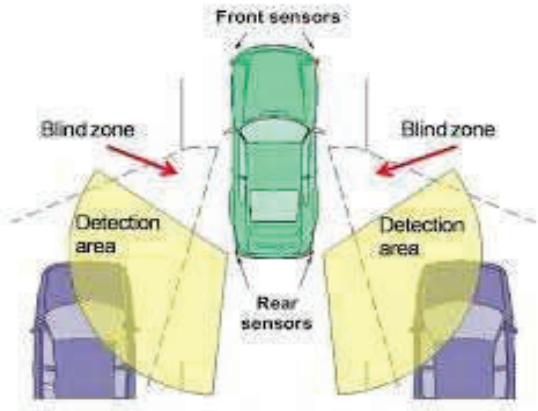

Figure 1. Blindspot Monitoring

Driver's negligence at the blind spot region needs detecting the obstacle and providing the image of the vehicle in order to warn and avoid the accidents. This system detects many obstacles, like pedestrian crossing suddenly, cars overtaking etc. and the driver is alerted. The system uses the ultrasonic sensor [3] to check the blind spot for an impending collision on the vicinity of the vehicle. The overtaking of vehicles is a big factor where accidents happen in the blind spot area. Mirrors become helpless during this situation and there could be a technology to avoid the collision on the blind spot during overtaking, lane switching etc. The system uses the ultrasonic sensors around the vehicle to detect the incoming obstacle in the specified range and sensor feedback is given to the raspberry pi microcontroller as to give the image of the vehicles to the driver, and warn by giving buzzer sound.

B. Drowsiness Detection Technique

Distracted driving as in fig.2 is one of the main causes of vehicle collisions. Passively monitoring driver's activities

constitutes the basis of an automobile safety system that can potentially reduce the number of accidents by estimating the driver's focus of attention[1].The driver's activeness will be detected by using MATLAB software[2] and the buzzer sound is produced as a warning to the driver by making the vehicle ignition system off.

The proposed system does not require any driver-dependent calibration or manual initialization, during day or night. We conducted a comprehensive experimental evaluation under a wide variety illumination conditions and facial expressions.

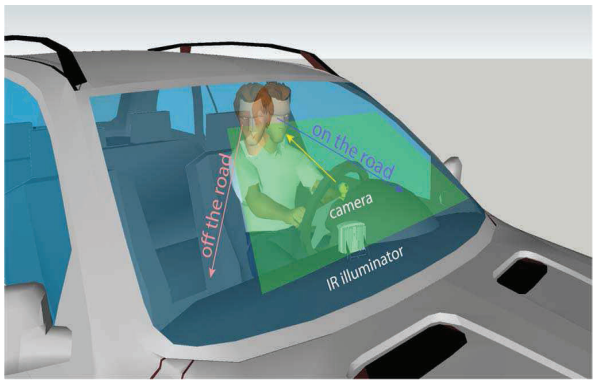

Figure 2. Drowsiness Detection

C. Block Diagram

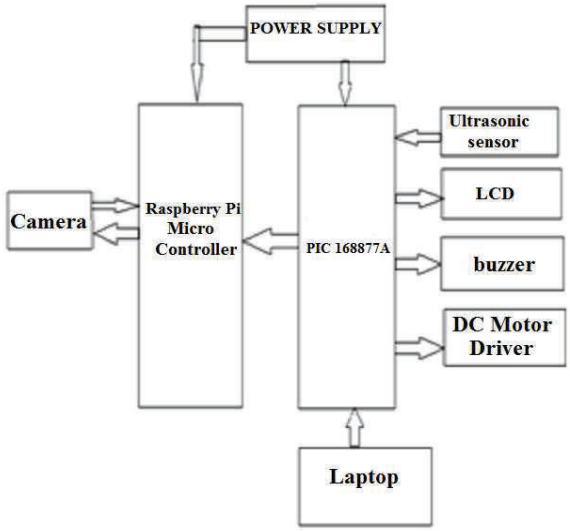

Figure 3. Block Diagram

The above fig.3 shows the block diagram[5] of the system prototype where the microcontrollers are interconnected to each other for communicating between themselves. Raspberry pi microcontroller is used to control the camera and to rotate it in the direction of the obstacle whenever, any obstacle is detected in the blind spot region.

II. Method

The schematic diagram fig.4 of explains the interfacing section of each component with PIC16F873A further to Raspberry pi and input output modules. PIC16F873A is used as the micro controller where it is interfaced with the ultrasonic sensor, crystal oscillator, IC L293D for controlling DC motor, buzzer, laptop, LCD, reset button, raspberry pi 3 B+ micro controller with ARM11 processor.

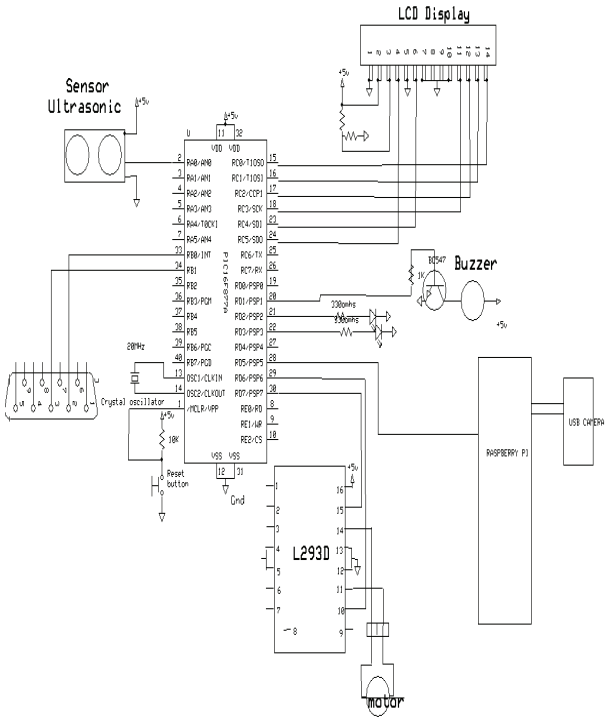

Figure 4. Schematic Diagram

A. Ultra sonic Sensor

It is connected to the pin2 (RA0) and works as input to PIC16F877A.When RA0=1 then, obstacle is detected.

B. Buzzer

Buzzer acts as the output module. It is connected to pin20 (RD1/PSP1) and works as output to PIC16F877A. When RD1/PSP1=0 buzzer gives sound indicating abnormal condition such as blind spot or drowsiness detected.

C. L293D

ICL293D acts as output of PIC Controller and as input for the DC Motors. It is connected to pins 29(RD6/PSP6) and 30(RD7/PSP7) works as output to PIC16F877A.It is used to control two motors where one for ignition system and the other for the camera rotation.

D. Laptop

Laptop acts as the input to the PIC Controller. Pins 2 and 3 of laptop are connected to the pins 33(INT/RB0) and 34(RB1) of PIC16F877A respectively. Laptop with MATLAB software is used to process the images of the face, detected by the camera, continuously in drowsiness detection system and to transmit information as 0 or 1 to controller.

E.LCD

Liquid Crystal Display acts as the output module. Pins 4, 6, 11, 12, 13, and 14 of LCD are connected to pins

15(RCO/T1OS0), 16(RC1/T1OS1), 17(RC2/CCP1), 18(RC3/SCK), 23(RC4/SD1), and 24(RC5/SD0) of PIC16F877A respectively. These pins act as outputs to display text on LCD.The texts are displayed as follows

1. "system ok vehicle moving" when the vehicle is in normal movement.
2. "blindspot detected vehicle stop" when the obstacle is detected in the blindspot area.
3. "drowsiness detected vehicle stop" when the system finds that driver is sleepy.

F. Raspberry pi

Pin28(RD5/PSP5) of PIC16F877A is connected to raspberry pi as input to capture image of the obstacle detected in the blind spot region and to send to the respective mail id.

G. Flowchart for Blindspot Monitoring

Embedded C language is used as programming language and simulated using the proteus7 software on LINUX operating system. The flow of software execution is as shown in fig.5. The ultrasonic sensor is assigned to the pin2 (RA0) which detects the obstacle and passes the information to the PIC controller as follows.

When,

1. RA0=1, the obstacle is said to be detected.

The motor driver gets off giving buzzer sound.

The rotating camera stops, captures the image of the obstacle and sends to the respective mail id.

Red led will glow, then text will be displayed on LCD as "blindspot detected".

2. RA0=0, the obstacle is not detected.

The motor driver remains ON.

Green led will glow then text will be displayed on LCD as "system ok vehicle moving".

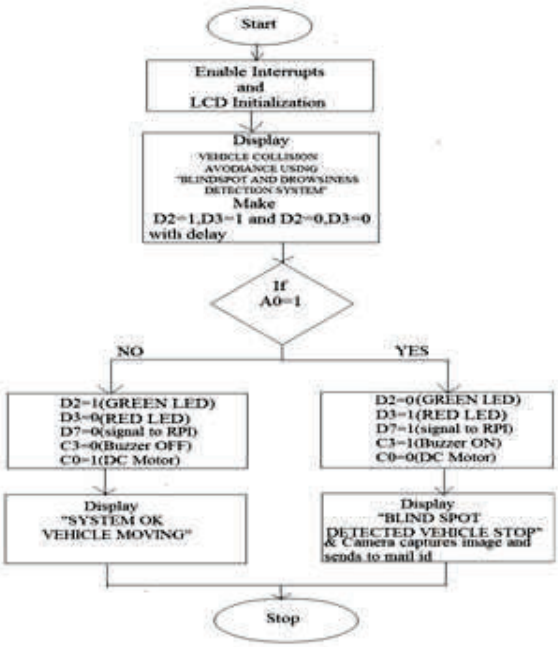

Figure 5. Flowchart for Blindspot detection

H. Flowchart for Drowsiness Detection

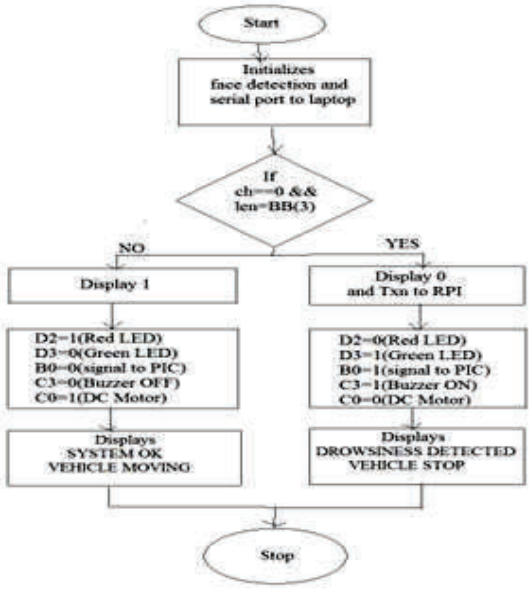

Figure 6. Flowchart for Drowsiness Detection

MATLAB software is used to implement the drowsiness detection method. The process of the face detection is as shown in fig.6, where the MATLAB programming is as follows,

1. Camera information[4] will be given as
Camera_name = winvideo,
Camera_id=1and
Format=YUY2_320X240.
2. Face detection with parameters as
Max size= [20 60]
Scalefactor=1.5 and
Merge threshold=10.
3. Initialization of serial with specified com port and checking for the condition of Ch==0 which indicates absence of face before camera to capture. This information is sent to raspberry pi to stop the motor driver.
4. The PIC controller takes the information as the external interrupt and stops the main programming execution and makes the ignition system off, since ch==o indicates the absence of driver before the steering.

III. RESULTS

The"Vehicle Collision Avoidance Using Blindspot Monitoring and Drowsiness Detection in Automobiles" is designed so that obstacles can be detected from distance and the presence of the driver while driving is observed to take preventive measures to avoid accidents. The project prototype is as below; when the system is normally moving then to indicate it text is displayed on LCD as "SYSTEM OK VEHICLE IS MOVING" as in fig.7.

Figure 7. System Prototype

A. Blindspot monitoring

When the obstacle is detected by ultrasonic sensor in the blind spot region, the buzzer sound is given as warning along with red LED, displays text on the LCD as "BLINDSPOT DETECTED VEHICLE STOP" and makes the DC Motor off as in fig.8.

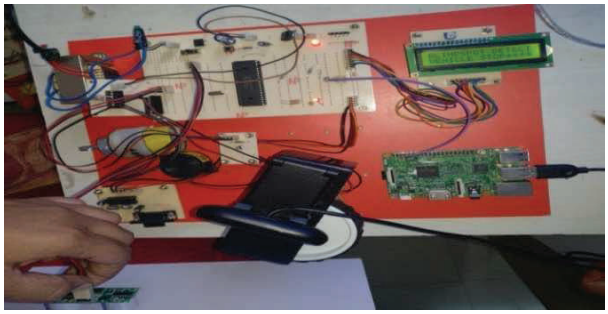

Figure 8. System when obstacle is detected in blindspot

Camera on RASPBERRY PI which is mounted on rotating DC Motor will rotate in the direction of the obstacle detected, and captures the image of obstacle and sends email successfully to the specified mail id as shown in fig.9, in order to make the driver aware of the obstacle in the blind spot.

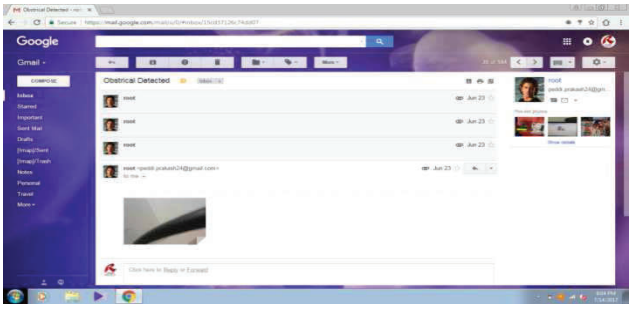

Figure 9. Captured image of obstacle in blindspot

B. Drowsiness detection

The USB camera keeps monitoring the face which is considered as the region of interest (ROI) and the image is computed using MATLAB to make sure about the presence of the driver in the position, indicating 1 when the face is found and indicating 0 when the face is not found, as shown in fig.10.

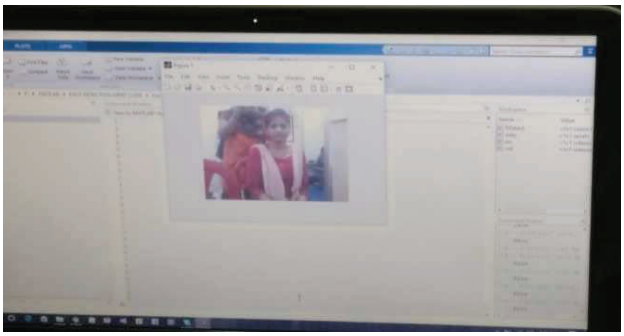

Figure 10. Image processing of face in matlab

When drowsiness of the driver is detected, the information from PC is sent to the controller through the serial communication; Then the driver is given buzzer sound as a warning and the DC Motor driver of vehicle will gets off displaying "DROWSINESS DETECTED VEHICLE STOP" as shown in the fig.11.

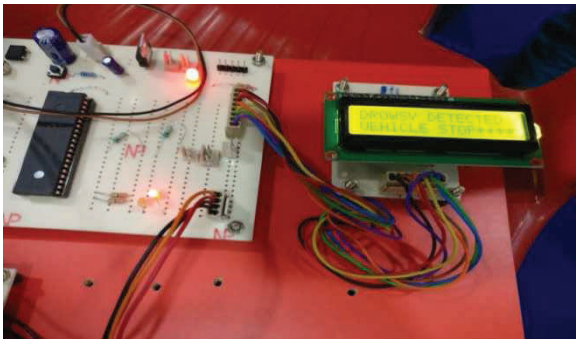

Figure 11. System when drowsiness is detected

In this paper "Vehicle Collision Avoidance Using Blindspot Monitoring and Drowsiness Detection in Automobiles" is mainly intended to control accidents using automated techniques with ARM11 processor. The project can be further extended by wireless modules using GPS.

The Blindspot monitoring is also made at night times using the night vision camera to capture obstacle at night times. The drowsiness detection could be extended as security system using the face detection technique in MATLAB software.

This paper can be extended using high efficiency GSM and GPS modules. We can find the location of particular object through SMS, so that sometimes we can easily identify the object time and place easily. And also by adding multiple sensors (like metal and obstacle sensors) to the system, we can use this moving robotic arm as multifunctional system used for finding the metal objects or bombs, further we can auto control robotic arm using obstacle sensor.

IV. Conclusions

In this paper we discussed the two automated preventive techniques to avoid the vehicle accidents with driver negligence while driving. The Blindspot Monitoring technique avoids accidents during lane divergences especially, for heavy vehicles like trucks and goods carrying

vehicles. The Drowsiness Detection technique uses MATLAB for processing and, makes sure that driver's eyes are on the road while driving, to avoid collision. Integrating features of all the hardware components used, have been developed in it. Presence of every module has been reasoned out and placed carefully, thus contributing to the best working of the unit.

Secondly, using highly advanced microcontroller i.e., Raspberry pi with the help of growing technology made our project highly reliable, the project has been successfully designed, tested and implemented.

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Diode Clamped Multilevel Inverter fed SPMSM

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Abstract: **This paper presents the control of SPMSM drive by using diode clamped three and five level inverters. The pulses are generated using Carrier Based Space Vector Pulse Width Modulation (CBSVPWM). Control technique like Field oriented control used for closed loop operation. Compared to conventional Space Vector Pulse Width Modulation (SVPWM), CBSVPWM is very fast and easy to implement digitally, which also reduces the complexity involved in calculation of angle and sector as in case of conventional SVPWM. It can also be extended to n-level.**

Index Terms: **Diode Clamped Multilevel Inverter (DCMI), Surface Mounted Permanent Magnet Synchronous Motor (SPMSM), Carrier Based SVPWM (CBSVPWM) and Filed Oriented Control (FOC).**

I. Introduction

Among AC motors the most prominent motor till date is the Induction Motor, however in current generation Permanent Magnet Synchronous Motors are gaining importance due to numerous advantages such as being light weight, gives high performance and have higher efficiency. The PMSM is an energy efficient motor operating at unity power factor. The advanced research in magnetic materials enables high flux densities to PMSM with good power density [1]-[3].

IPMSM and SPMSM are the two classifications of Sine PMSM. If the permanent magnets are buried inside the rotor core then they are treated as IPMSM and if they are buried on the rotor surface they are called as SPMSM. When air-gap torque is considered, IPMSM is better and when speed range is considered for the same voltage, then SPMSM is better. However, if the air gap power is considered, SPMSM is good compared to IPMSM [3]-[6].

The torque speed characteristics of any motor directly depend upon the type of modulation technique used. The modulation technique used in this paper for the analysis of SPMSM is CBSVPWM. This is based on the effective time calculation which is a simple and fast method to reduce the complexity involved in the calculation of angle and sector in case of SVPWM. The output voltage of the inverter is synthesized using effective time, and the gate signals are generated using effective time relocation theorem [7]-[9]. Multilevel inverters are used in wide range for high power and medium power applications. Among multilevel inverters, diode clamped inverters have their enormous advantages for high voltage and power applications [10]-[12]. With respect to the output voltage harmonics three level and five level inverters have significant advantages [13]. As the level increases the output voltage has less harmonics and gives the smooth operation for the SPMSM [14].

PMSM are generally used in application which requires high performance and high efficiency. The high performance of the motor can be obtained if the motor has smooth speed control for the entire range with full torque control even at zero speeds. In order to achieve such type of control, good control method should be used. The best method for PMSM control is the field oriented control. The principle of the FOC is to decompose the stator current into magnetic field component and torque generating component. These two components can be controlled separately like DC motor control. In this paper FOC for three-level and five-level diode clamped inverter is fed to SPMSM drive to analyze its performance using CBSVPWM [15]-[16]. Section II gives the mathematical modeling of SPMSM, Section III-Control methodology, Section IV gives the details of the modulation technique used and Section V gives the working of three and five-level diode clamped inverter.

II. Mathematical Modelling of Spmsm

The PMSM d-q axis voltage representation is shown below [1].

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} R+PL_d & -\omega L_q \\ \omega L_d & R+PL_q \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} 0 \\ \omega\varphi_a \end{bmatrix} \quad (1)$$

Where,
φ_a : Armature flux linkages
i_d, i_q : d-axis & q-axis component currents
V_d, V_q : d-axis and q-axis component voltages
Ld, Lq : d-ais and q-axis component inductances
R: Resistance of the armature
p: angular velocity

Equation (1) into α – β fixed coordinate, equation (2) is derived

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} R+PL_\alpha & PL_{\alpha\beta} \\ \omega L_{\alpha\beta} & R+PL_\beta \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + \omega_{re} K_E \begin{bmatrix} -\sin\theta_{re} \\ \cos\theta_{re} \end{bmatrix} \quad (2)$$

Where, $L_\alpha = L_0 + L_1 \cos 2\theta$ (3)

$$L_\beta = L_0 - L_1 \cos 2\theta \quad (4)$$

$$L_{\alpha\beta} = L_1 \sin 2\theta \quad (5)$$

$$L_0 = \frac{L_d + L_q}{2} \quad (6)$$

$$L_1 = \frac{L_d - L_q}{2} \quad (7)$$

The output torque equation of IPMSM is given by:

$$T = P_n \left\{ \phi_a i_q + (L_d - L_q) i_q i_d \right\} \quad (8)$$

$$T = P_n \left\{ \phi_a i_a \cos\beta + \frac{1}{2}(L_d - L_q) i_q^2 \sin 2\beta \right\} \quad (9)$$

For a surface-mounted PMSM $L_d = L_q$ rotor magnetic linkages is a constant, so the above Eq. (9) becomes

$$T = K_t i_q \quad (10)$$

The motor drive system dynamics is also represented by

$$T_e = T_L + B\omega_m + Jp\omega_m \quad (11)$$

Where T_L and ω_m are load torque and motor speed respectively [1]-[4].

III. Control Methodology

The main principle of the FOC is to control both the currents i_d and i_q independently to achieve the required torque. With this control maximum torque per ampere ratio for minimizing the current needed for the specific torque can be obtained by which the efficiency of the motor can be increased. FOC for SPMSM can be done equating $L_d = L_q$ which in turn gives Electromagnetic torque alone.

For SPMSM the torque equation is given as:

$$T_e = \frac{3}{2}\frac{p}{2}\left[\lambda_{pm} I_{sq}\right] \quad (12)$$

The maximum efficiency can be obtained by keeping d-axis current zero and the torque producing current is along q-axis.

The reference d and q axis currents for FOC are given as:

$$i_q^* = \frac{T^*}{\frac{3}{2}\frac{p}{2}\lambda_{pm}} \quad (13)$$

$$i_d^* = 0 \quad (14)$$

IV. Modulation Technique

CBSVPWM is a fast and efficient modulation techniques which limits the complexity involved in calculation of sector and the angle as in case of conventional SVPWM. In case of conventional SVPWM it is necessary to calculate the sector and the location of the voltage vector in the sector and also the angle of the space vector. These calculations make the system complicated as the level of the inverter goes on increasing. So, to simplify the analysis, a new technique is introduced called CBSVPWM. It is based on "effective time re-location algorithm" which is simple and easy and can be implemented for n-level inverters digitally. The switching states of the inverter are shown in the Fig. 1. The general formula for calculating the switching times is given as:

$$T_{xs} = \frac{T_s}{V_{dc}} V_{xs}^*, (x = a, b, c) \quad (15)$$

The difference between the maximum and minimum values of the times is called as effective time.

$$T_{eff} = T_{\max} - T_{\min} \quad (16)$$

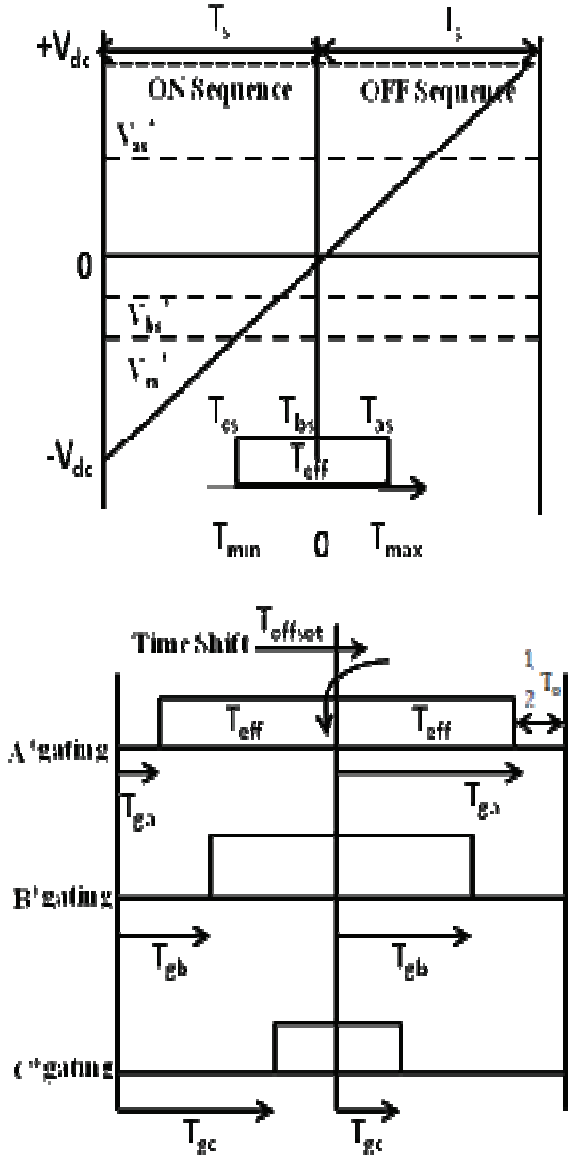

Fig. 1 Actual gating time generation for CBSVPWM

Where

T_{min} is the minimum value of T_{as}, T_{bs}, and T_{cs};

T_{max} is the max value of T_{as}, T_{bs} and T_{cs}.

The gating times can be calculated by adding the T_{offset}, the off-set time value to T_{as}, T_{bs}, and T_{cs}

The actual switching times for the two sampling patterns can be calculates by subtracting the gating times (T_{ga}, T_{gb}, T_{gc}) from the sampling times T_s,

V. Three and Five Level Diode Clamped Inverters

Multilevel inverters are popular for high power applications because as the level of the inverter increases the output voltage harmonics can be reduced to a greater extent, which gives the smooth operation for the motor connected to it. There are three topologies in multilevel inverters, among three diode clamped is the one which is widely used. In this topology for clamping DC bus voltage a diode is used and

the output of the inverter is the stepped waveform. For a m-level inverter, the number of switching devices are 2(m-1) and (m-1)*(m-1) clamping diodes with (m-1) DC link capacitors.

The three-phase three-level diode clamped inverter fed to SPMSM is shown in the Fig. 2. It consists of two capacitors to synthesize the DC supply voltage. Every leg contains four switches with four anti-parallel diodes. For positive $V_{dc}/2$ the top two switches of the each leg should be triggered and for the negative $V_{dc}/2$ bottom two switches of the each leg should be triggered. For the zero voltage one switch from top and one switch from bottom should be triggered. The maximum output voltage obtained in this case is half the DC source.

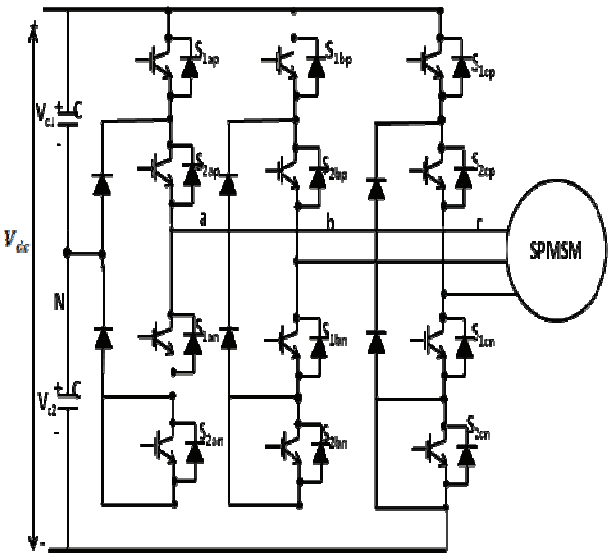

Fig. 2 Three-phae 3-level inverter fed SPMSM

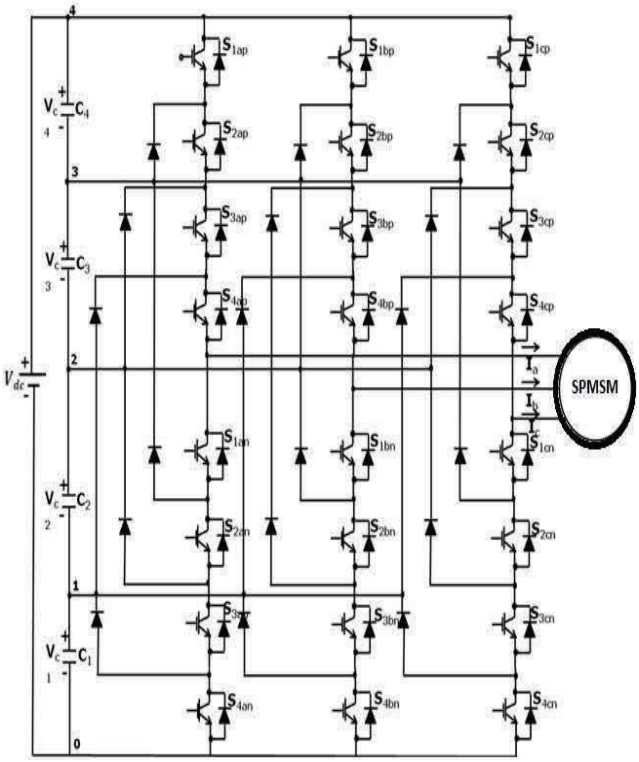

Fig. 3 Three-phase 5-level diode clamped inverter fed SPMSM

The five level diode clamped inverter fed SPMSM is shown in Fig. 3. In this case also one DC source is required and four capacitors are required to split the DC voltage. Each leg contains eight switches with eight ani-parallel diodes. The switching sequence of the five-level inverter can be explained as, to have an output voltage of $V_{dc}/2$ the top four switches from each leg should conduct. To have an output voltage of $V_{dc}/4$ the three switches from top and one switch from bottom should conduct. Also to have an output voltage of $-V_{dc}/2$, the bottom four switches should conduct at a time and to have an output voltage of $-V_{dc}/4$ one switch from top and three switches from bottom should conduct. To have a zero output voltage two switches from top and two switches from bottom should conduct. The anti-parallel diodes help us in clamping the DC voltages and to synthesize the output voltage into 5 levels. The output of the inverter with 5-level is given to the Surface Mounted SPMSM for the analysis. There are 27 switching states in 5-level inverter. The complexity increases if the SVPWM modulation is used. For this purpose CBSVPWM is used as the modulation techniques and the generated pulses are given to the switches. In this method there is no need to identify the sector and the angle of the voltage vector as in case of SVPWM. So, as the level of the inverter increase to get the smooth output waveform, the simple and easy modulation technique such as CBSVPWM is used. This modulation technique gives the same quality of the inverter output voltage as one get from the SVPWM technique.

VI. Results of DCML Inverter Fed SPMSM

The analysis of the SPMSM drive is done using MATLAB SIMULINK. The control diagram is as shown in the Fig. 4. The modulation technique used to generate the pulses for the inverter is the CBSVPWM and for closed loop control of the drive Field Oriented Control is used. The output speed, torque, line currents, three-phase currents, line voltages of the 3-level and 5-level inverter has plotted. Performance characteristics comparison is done between the 3-level and 5-level inverter fed to SPMSM drive. The drive is subjected to different loads and the change in the speed response is studied in both the cases. Fig. 5(a) & (b) shows the speed responses of the 3-level & 5-level inverter fed to SPMSM drive. Fig. 6. (a) & (b) shows the torque responses of the 3-level and 5-level inverter fed to SPMSM drive. Fig. 7(a) & (b) shows the SPMSM line current response when fed to 3-level & 5-level inverter. Fig 8 (a) & (b) shows the three-phase currents of the SPMSM drive when fed to 3-level and 5-level inverters. Fig. 9 (a) & (b) shows the 3-level and 5-level inverter output voltage waveforms. The parameters used in simulation while designing the SPMSM are

The d- axis Inductance is L_d=0.0058 Henry;
The q-axis Inductance is Lq=0.0058Henry;
The resistance value is 1.4 ohm and
The permanent magnet flux is 0.1546 webers.
The no. of poles is 6;
The value of F= 0.000038818.The value of J = 0.00176;

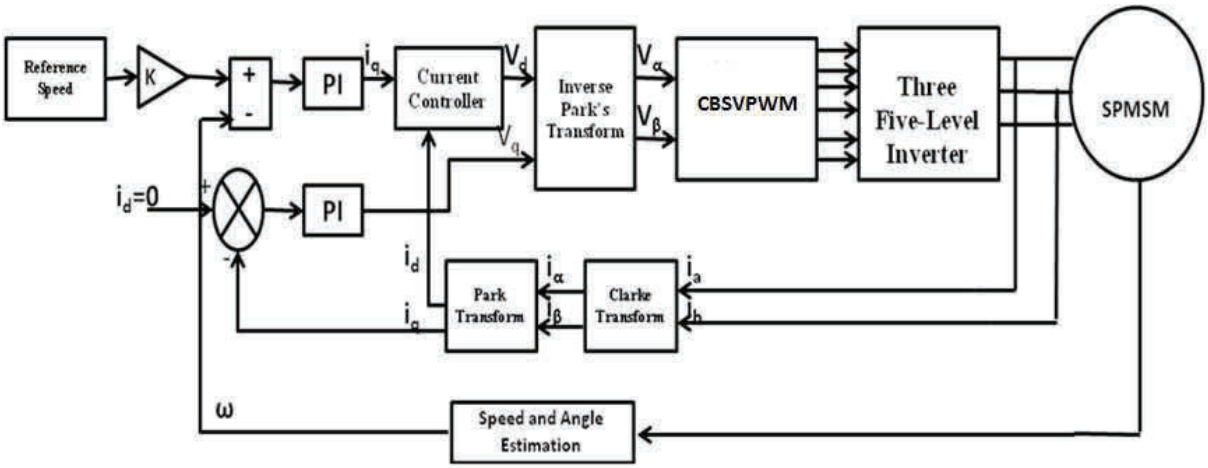

Fig.4. FOC of SPMSM using Diode Clamped Multilevel Inverter with CBSVPWM

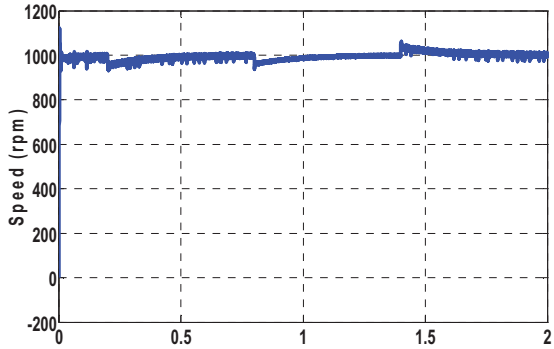

Fig.5.(a). Speed response of three-level DCI fed SPMSM drive

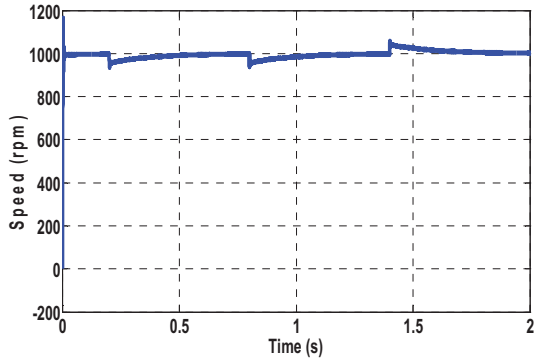

Fig.5.(b). Speed response of five-level DCI fed SPMSM drive

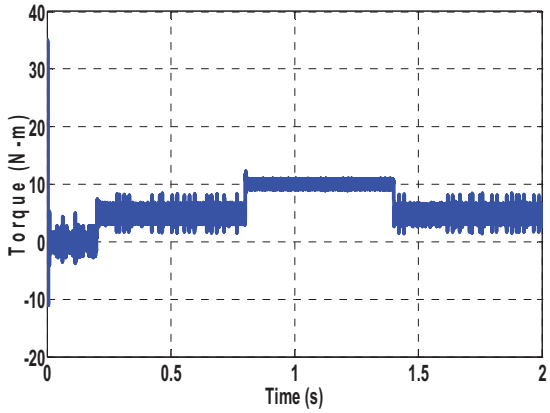

Fig.6.(a). Torque response of three-level DCI fed SPMSM drive

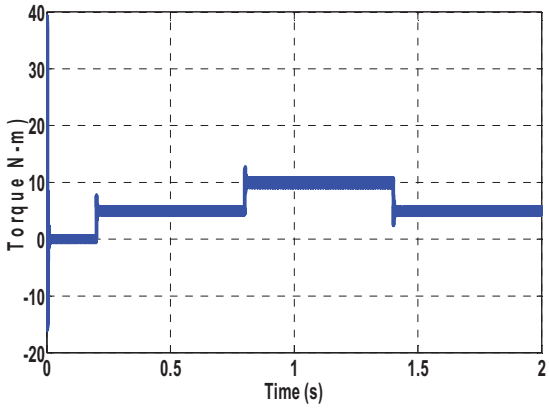

Fig.6.(b). Torque response of five-level DCI fed SPMSM drive

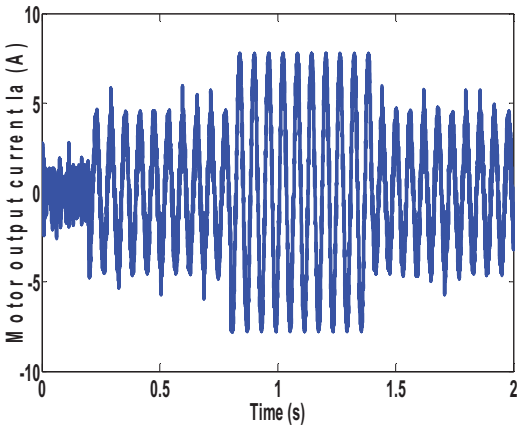

Fig.7. (a). Line current response of three-level DCI fed SPMSM

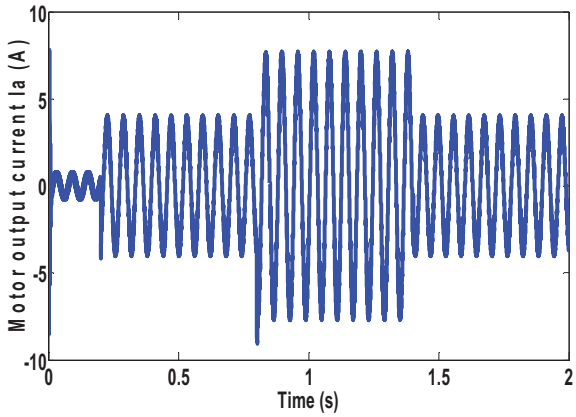

Fig.7. (b). Line Current response of five-level DCI fed SPMSM

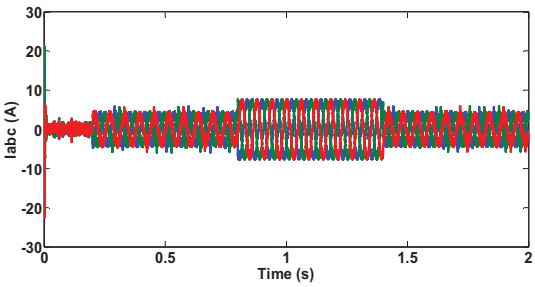

Fig.8. (a). 3-Φ current responses of three-level DCI fed SPMSM

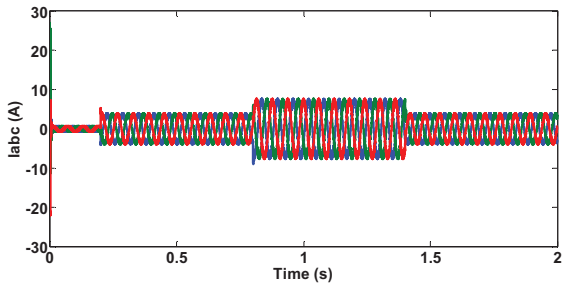

Fig.8. (b). 3-Φ current responses of five-level DCI fed SPMSM

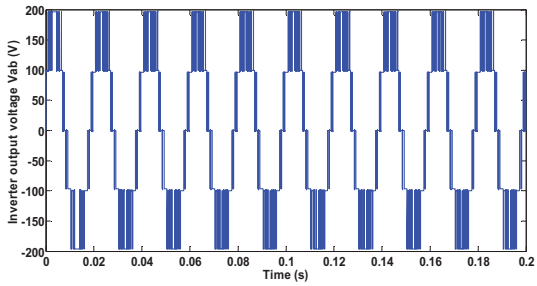

Fig.9.(a) Output voltage response of three level DCI fed SPMSM

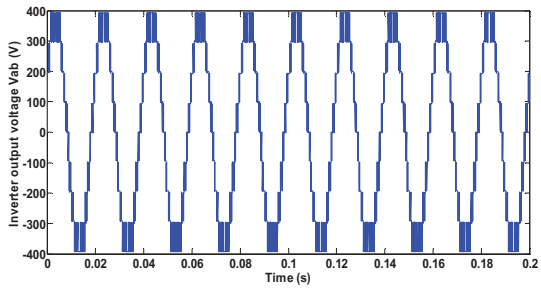

Fig.9.(b) Output voltage response of five-level DCI fed SPMSM

VII. Conclusions

In this paper, the analysis is done with 3-level and 5-level diode clamped inverter fed to SPMSM drive. The modulation technique use is CBSVPWM and the control technique is FOC. The inverter output is fed to the SPMSM drive and the speed-torque characteristics of the motor are studied at different load conditions. The load torque is changed to 5Nm, 10Nm & again 5Nm at 0.2, 0.8 and 1.2 secs. It has been observed that the change in speed at different loads is very less and remains almost constant and the response settles very fast in case of five-level inverter. The motor characteristics are very smooth and the speed changes with respect to the load changes are very fast as the level of the inverter increases. The modulation technique CBSVPWM is very fast and easy to implement digitally which can be extended to n-level.

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Study of Star Connected Cascaded H-Bridge STATCOM using Different PWM Techniques

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Abstract: **Two control algorithms are presented in this paper for STATCOM that meets the requirement of load reactive power and correspondingly voltage balancing of isolated dc capacitors for H-bridge Inverters used in STATCOM. The control techniques used for an inverter in this paper are Sinusoidal Phase Shifted Carrier (SPSC) PWM and Space Vector Phase Shifted Carrier(SVPSC) PWM. The STATCOM performance for the different load changes is simulated in MATLAB environment. The performance parameters such as balancing the DC link voltage, THD for the STATCOM output currents, voltages, and reactive components provided to the load by the STATCOM are compared for both these control strategies.**

Index Terms: **Cascaded Multilevel Inverter, SPSC, STATCOM, SVPSC.**

I. Introduction

Recently, attention towards the quality of electric power has enhanced due to more preventive guidelines on this area. This curiosity has led to the innovations of multiple equipment, which could progress the energy transmission ability and quality of the voltage in the point of common coupling. These innovative devices are popular as Flexible AC Transmission System (FACTS), which are inventions of modern-power electronics. Considerable work has been carried out using these FACTS devices for high-voltage transmission [1]- [2]. Innumerable FACTS devices, like Static Synchronous Series Compensators (SSSCs), Static Synchronous Compensators (STATCOMs) and Unified Power-Flow Controllers (UPFCs) are extensively used in power systems to stabilize transmission ability of the power system and to enhance power quality in distribution system. STATCOM technology is progressively applied to enhance power transfer ability and improve voltage stability [3].

A STATCOM is fundamentally one of the shunt-type FACTS device. It is one of the inverter with dc-link capacitors on its dc side with control technology, and this device is connected in parallel with the grid. The STATCOM regulates the reactive-power flow in the power line, either by absorbing or injecting it. This reactive-power flow is controlled by regulating the output voltage of the STATCOM [4].

The development of present static switches (IGBT, GTO) and the evolution of new switching devices (IGCT, IEGT, etc.), usage of novel inverter topologies, have facilitated the enhancement in power and voltage ratings of the electronic converters. Because of this, in few situations the inverter may be connected directly to medium voltage buses without coupling transformer [5].

Nowadays multilevel inverters are widely employed for STATCOM as it can enhance the power capacity of the compensator, to make it appropriate for high or medium-voltage bulk power applications [6-7]. There are several types of multilevel inverter topologies used for implementing STATCOMs such as diode-clamped inverter, neutral point clamped inverter, and cascaded H-bridge multilevel inverter. Cascaded H-bridge topology is widely employed due to its several advantages: (1) it can produce nearly sinusoidal voltage waveform and diminishes harmonics, (2) it can respond faster since the removal of the extra transformer to provide the necessary voltage levels, (3) due to modularity in circuit the design and construction is simple [8-9].

Now days the cascaded H-bridge converters in each phase is replacing many other configurations for medium-voltage three-phase multilevel conversion system [10- 11]. This multilevel inverter is preferred as a substitute to the three-level neutral point clamped inverter [12] for variable-speed drive and STATCOM applications.

All the cascaded H-bridge inverters used in STATCOM application are furnished with floating and electrically isolated dc-link capacitors without having any power source in the circuit. This eliminates a large and expensive transformer from the cascaded H-bridge STATCOM. As an example, a 6.6 kV and 1 MVA three phase transformer weights from 3000 to 4000 kg, whereas similar rating three-phase cascaded H-bridge inverter weights from 1000 to 2000 kg only [13].

The problem associated with cascade STATCOM is unequal voltage distribution among all the floating dc-link capacitors. Inappropriate conduction of semiconductor devices, the switching losses in the switching devices employed in the circuit, as well as signal disparity, the resolution issues in the control circuit, and presence of current/voltage sensors, may results into voltage imbalance in the dc-link capacitors.

The converter used in STATCOM acts as an inverter and all the H-bridges produce three different levels of output voltages with the control of four switches. By regulating the phase angle between line voltage and the voltages generated by inverter, results STATCOM to absorb or supply reactive power to the load. The power supplied to a cascaded STATCOM from the dc source should be maintained equal. Therefore, all the H-bridge cells in the inverter are similarly operated. But, due to the semiconductor devices of the inverter are not ideal and have dissimilar acceptance errors, each DC-link capacitor voltages might not be accurately balancing. It is the main drawback for the cascaded H-bridge inverters employed for STATCOM, so it is essential

required to use an extra control approach to equalize the DC-link voltages [14-17].

Numerous literatures have considered for the balancing of DC-link voltages of the cascaded H-bridge multilevel inverter. The distinct balancing control is combined with grouped balancing control for regulating DC-link voltages [18]. But, assigning appropriate values to gain parameters is not easy [18].

II. Modulation Strategies

Based on voltage control Cascade STATCOMs can be classified as pulse width modulation (PWM) and staircase modulation. More Investigations has been done in [17, 19-20] about the staircase modulation and PWM. Mostly PWM is chosen when a transformerless cascaded STATCOM is used. The foremost reason is that the 1.7 kV gate insulated bipolar transistors (IGBTs) may be functioned at a switching frequency higher than 1 kHz through a fewer switching losses. PWM is more advantageous for dynamic performance, more vigorous for line disturbances and faults, and more flexible in applications associated to staircase modulation.

A. Sinusoidal Pulse Width Modulation

Modulation process for multilevel inverters are based on carrier arrangements. The carriers shifted by horizontally is Phase Shifted Carrier PWM(SPSCPWM). Fig 1. Shows the arrangement of carrier and reference signals for the SPSCPWM technique. Mostly phase shifted carrier PWM is chosen for the cascaded multilevel inverters, due to this the power distribution among all the cells is uniform and this is easy to implement separately for any number of inverters. The PSCPWM technique results in the termination of all the carrier and connected sideband harmonics up to $2N^{th}$ carrier cluster, here N is the sum of H-bridges in each phase.

The Sinusoidal Phase-shifted carrier PWM having a carrier frequency of 1.2 kHz is applied to a group of two cascaded H-bridge inverters in each phase. Then, the output voltage of each group of H-bridges in a phase has 5-level line-to-neutral PWM waveform with the lowermost harmonic sideband centered at 4.8 kHz (= 1.2Khz x 2 x 2).

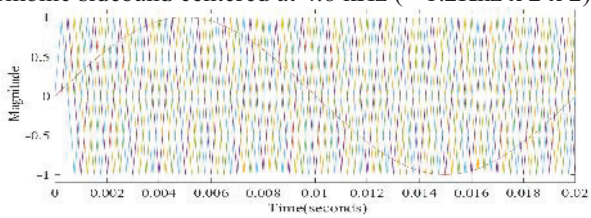


Figure 1. Carrier and reference waveform arrangements for a five level STATCOM with Sinusoidal Phase Shifted Carrier strategy

B. Modified Carrier-Based SVPWM

In the conventional SVPWM technique every outer sector must be mapped with inner sub hexagon sector to evaluate the switching time-period for multilevel inverters. The switching vectors related to the present sectors are turned on and the corresponding time periods are to be calculated from the mapped inner sectors. Because of the presence of more number of inverter sectors realizing this technique will be tough for multilevel inverters. The computational time-period is more in this method during real time implementation.

Before comparing with carrier signals, an appropriate offset voltage is to be added with sinusoidal reference to get the performance of SVPWM in the carrier based PWM technique [21-22]. The finding of offset voltage is contingent on modulus function which depends on the magnitude of DC-link voltage, the phase voltage magnitudes and the number of voltage levels.

A shortened method is defined, where accurate offset times periods are to be calculated for centering the time periods in a sampling interval for the middle inverter vectors. A technique is given in [23] for finding the maximum likely peak magnitude of the fundamental phase voltage in the linear modulation range. The subsequent equations are used to compute offset time $T_{offset.}$

$$T_a = \frac{V_a * T_s}{V_{dc}} \quad (1)$$

$$T_b = \frac{V_b * T_s}{V_{dc}} \quad (2)$$

$$T_c = \frac{V_c * T_s}{V_{dc}} \quad (3)$$

Here T_a, T_b, and T_c are the time periods of imaginary switching, related to the instant value of the reference phase voltages V_a, V_b and V_c.

T_s refers to the sampling time in the above equations.

$$T_{offset} = [\frac{T_0}{2} - T_{\min}] \quad (4)$$

$$T_0 = [T_s - T_{effect}] \quad (5)$$

$$T_{effect} = T_{\max} - T_{\min} \quad (6)$$

T_{max} = Maximum value of the three-phase reference voltages, in each sampling interval.

T_{min} = Minimum value of the three-phase reference voltages, in each sampling interval.

The switching vectors of the inverter are centered in a sampling time-period by the addition of offset voltage values to the reference phase voltages that equates the performance of SPWM technique with the SVPWM technique.

This proposed SVPWM signal generation does not involve look up table, identification of sector, angle information and voltage magnitude of space vector measurement for calculation of switching vectors for the conventional SVPWM technique for multilevel inverters. This technique is further effective when compared to conventional multilevel SVPWM technique. Fig. 2 shows the produced there-phase reference waveforms with the modified SVPWM technique. The generated reference waveforms are compared with triangular carrier signals to

produce switching pulses for the switching devices. Fig. 3 Shows the arrangement of carrier and reference waves for the modified Space Vector Phase Shifted Carrier PWM technique.

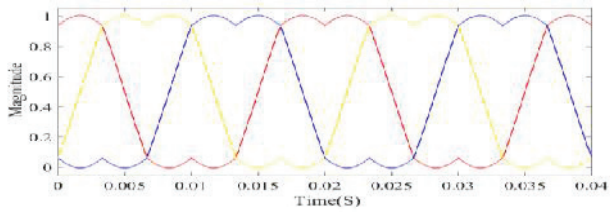


Figure 2. Reference signals for Modified SVPWM

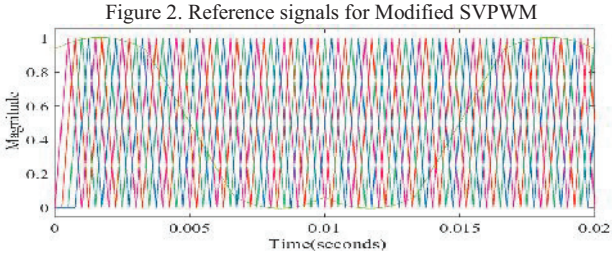


Figure 3. Carrier and reference waveform arrangements for a five level STATCOM with Space Vector Phase Shifted Carrier strategy

III. Control Strategy For Cascaded Five Level Inverter Based STATCOM

Fig. 4 shows the five-level cascaded H-bridge multilevel STATCOM. This STATCOM consisting of cascaded five level inverter, which is connected through coupling reactors to the grid. In this topology two single phase H-bridge inverter cells with capacitors as dc-link are connected in series to generate five levels of phase voltage. For an inverter, if N is number of H-bridges present in a phase and m is the number of voltage levels in a phase then the number of levels in phase voltage are 2N+1 and the number of levels in line voltage are 2m-1.

In the design of STATCOM, the three phase quantities v_a, v_b, v_c, i_{al}, i_{bl}, i_{cl}, i_{as}, i_{bs} and i_{cs} are source voltages, load currents and inverter currents, these are transformed in to v_d, v_q, i_{dl}*, i_q*, i_d and i_q in the synchronously rotating reference frame. The mathematical model of the cascaded inverter is transformed to the stationary rotating reference frame. Fig. 5 shows the control block diagram for the generation of reference voltages for various control techniques. The d - q axes reference voltage components of the inverter e_d and e_q are controlled as

$$e_d = x_1 + v_d - \omega L i_q \quad (7)$$

$$e_q = x_2 + \omega L i_d \quad (8)$$

Where v_d is the magnitude of source voltage component direct axis and i_d, i_q, i_{dl}*, and i_q* are d-q axes components of current of the inverter and load correspondingly.

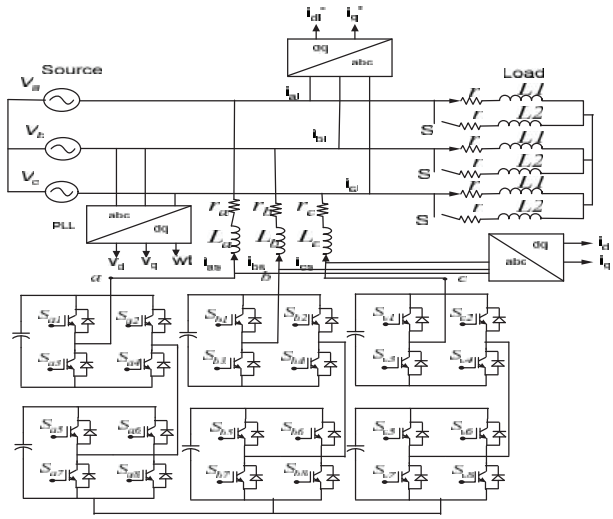


Figure 4. Cascaded multilevel STATCOM.

The synchronously rotating frame and source voltage vector are aligned together so that the q - component of the source voltage v_q is made zero. The control parameters x_1 and x_2 are controlled as

$$x_1 = (k_{p2} + \frac{k_{i2}}{s})(i_d^* - i_d) \quad (9)$$

$$x_2 = (k_{p3} + \frac{k_{i3}}{s})(i_q^* - i_q) \quad (10)$$

The d-axis reference current i_d* is

$$i_d^* = (k_{p1} + \frac{k_{i1}}{s})[(V_{dc}^*) - (V_{dc1} + V_{dc2} + V_{dc3} + V_{dc4} + V_{dc5})] \quad (11)$$

Where V_{dc}* is the reference DC-link voltage and V_{dc1} to V_{dc6} are voltages across the DC-link capacitors in each H-bridge. The unit signals sinwt and coswt are generated by using Phase Locked Loop (PLL) block from the source voltages. The stationary reference frame quantities are converted in to synchronous rotating reference frame as

$$e_{ds} = (\cos\omega t)e_d + (\sin\omega t)e_q \quad (12)$$

$$e_{qs} = -(\sin\omega t)e_d + (\cos\omega t)e_q \quad (13)$$

From these synchronous rotating reference frame signals, the reference voltages to control the inverter are generated as

$$v_{ar} = e_{ds} \quad (14)$$

$$v_{br} = -\frac{1}{2}e_{ds} + \frac{\sqrt{3}}{2}e_{qs} \quad (15)$$

$$v_{cr} = -\frac{1}{2}e_{ds} - \frac{\sqrt{3}}{2}e_{qs} \quad (16)$$

The switching frequency ripples in the inverter currents are removed by means of low-pass filter. From V_{dc}* and i_q* loops, the control block produces d-q axes reference voltages, e_d and e_q for the cascade multilevel inverter.

Fig 5. Shows the control block diagram to generate reference signals for the inverter. With these reference voltages, the inverter is controlled to supply the essential reactive currents to the load, and draws required active currents to control the dc-link voltage V_{dc}*.

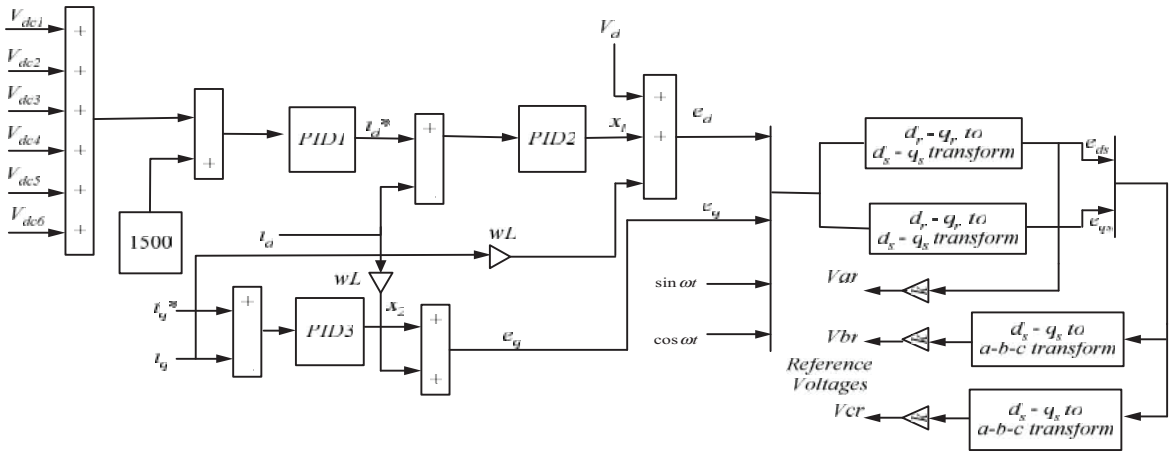


Figure 5. Control block diagram.

IV. Simulation Results

The five level Cascaded Multilevel STATCOM is considered for simulation. The simulation of STATCOM is carried out using MATLAB/SIMULINK for different load changes. The inverter is controlled by using Sinusoidal Phase Shifted Carrier (SPSC) PWM, and Space Vector Phase Shifted Carrier (SVPSC) PWM techniques. The system parameters and PI controller parameters for voltage control, current control loops are shown in Table I and Table II respectively.

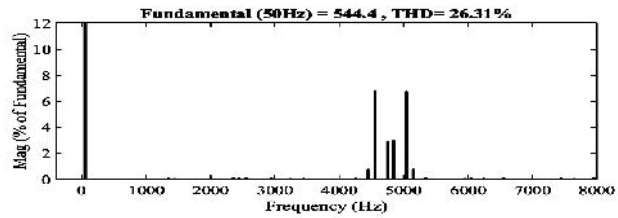
TABLE I
SIMULATION SYSTEM PARAMETERS

Supply Voltage	415 V RMS(Phase-Phase)
DC link voltage	250 V for both control techniques
Load Parameters	R = 4.6 Ω, L = 12.4 mH R = 4.6 Ω, L = 5.01 mH(for half load)
DC link capacitance	10 mF
Fundamental frequency	50 Hz
Switching frequency	1200 Hz
STATCOM Interfacing resistance	0.13 Ω
STATCOM Interfacing Inductance	2.19e-3 H

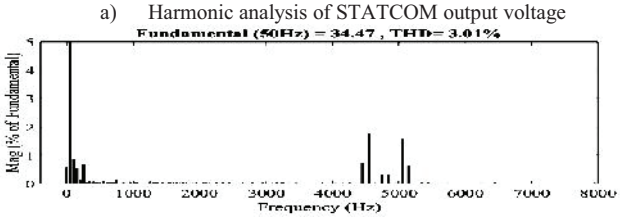
TABLE II
PARAMETERS OF PI CONTROLLERS

PI Controller	Control Variable	Proportional Gain	Integral Gain
PID1	Voltage	0.07	0.2
PID2	Voltage	0.08	0.2
PID3	Current	4	6

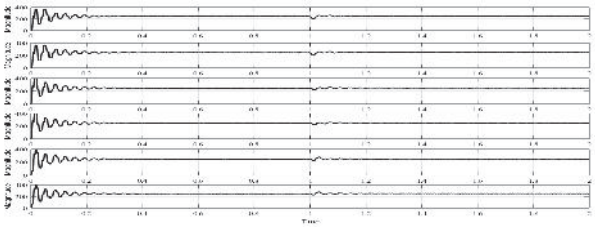
Fig. 6 shows the response of STATCOM for various performance parameters such as harmonic analysis of STATCOM output voltage and current, balancing the DC-link voltages for all H-bridges, Ripple content in DC- link voltage, comparison of reactive components required by the load and supplied by the STATCOM, and Phasor relations between Source voltage and STATCOM current for the variation of load from RL to RC at 1 sec by using Sinusoidal Phase Shifted Carrier PWM technique. It is observed that the STATCOM works perfectly for a reference DC link voltage of 1500 V, this voltage is equally distributed among all the DC-link capacitors of H-bridges and it is observed that the DC-link voltage is balanced for all types of load changes. Even if the load is changed suddenly also STATCOM supplies reactive components required by load. The ripple content in the DC-link voltage is low and it is around 9V. The harmonics in the output current is in the order of 3 % and in the voltage is 26.31%. And no harmonics observed below 4.8 kHz frequency due to SPSC technique. During the change of load from RL to RC the STATCOM currents is changed from lagging to leading with respect to source voltage. But during the change of load the inverter current magnitude values are almost double the normal value. After changing the load from inductive to capacitive at 1 sec, the reactive components supplied by the STATCOM changed from negative to positive, but to reach steady state it takes up to 3 sec.



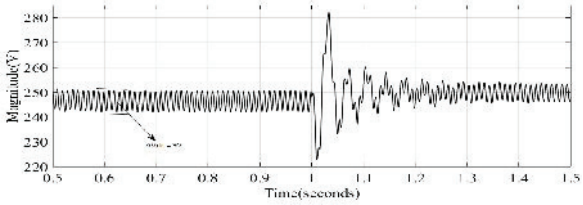
a) Harmonic analysis of STATCOM output voltage



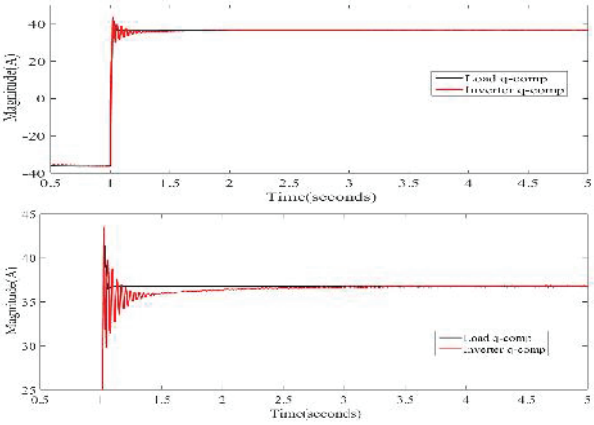
b) Harmonic analysis of STATCOM output current



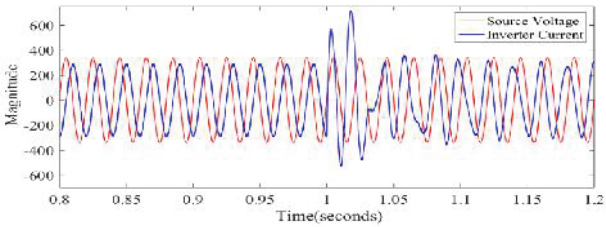
c) DC Link voltages



d) Ripple in DC link Voltage



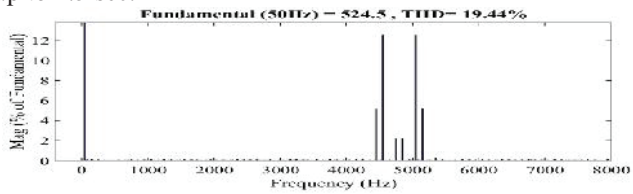
e) Comparison of load and inverter q-components of Currents



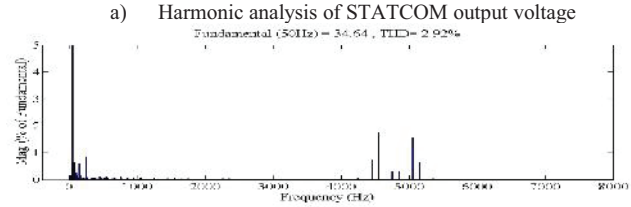
f) Source Voltage and STATCOM current

Figure 6. STATCOM response for variation of load from RL to RC at 1 sec with Sinusoidal Phase Shifted Carrier PWM

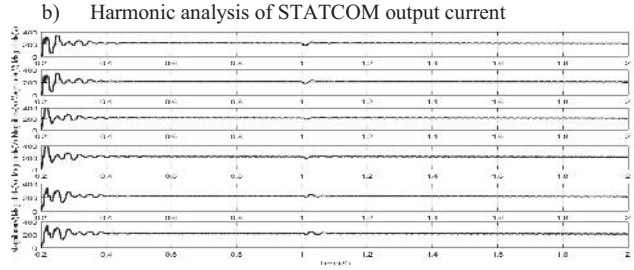
Fig. 7 shows the response of STATCOM for various performance parameters such as harmonic analysis of STATCOM output voltage and current, balancing DC- link voltages for all H-bridges, Ripple content in DC- link voltage, comparison of reactive components required by the load and supplied by the STATCOM, and Phasor relations between Source voltage and STATCOM current for the variation of load from RL to RC at 1 sec by using Space Vector Phase Shifted Carrier PWM technique. It is observed that the STATCOM works perfectly for a reference DC link voltage of 1500 V, this voltage is equally distributed among all the DC-link capacitors of H-bridges and the DC-link voltage is balanced for all types of load changes. If the load is changed suddenly also STATCOM supplies reactive components required by load. The ripple content in the DC-link voltage is low it is around 9V. The harmonics in the output current is in the order of 2.92 % and in the output voltage is 19.44%. And no harmonics observed below 4.8 kHz frequency due to Phase Shifted Carrier technique. After changing the load from inductive to capacitive at 1 sec, the reactive components supplied by the STATCOM changed from negative to positive, but to reach steady state it takes up to 2.5 sec.



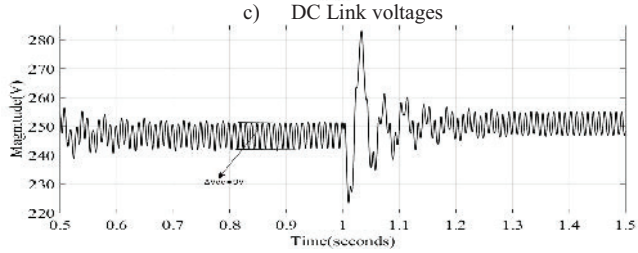
a) Harmonic analysis of STATCOM output voltage



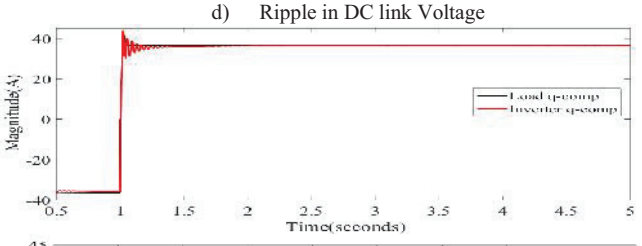
b) Harmonic analysis of STATCOM output current



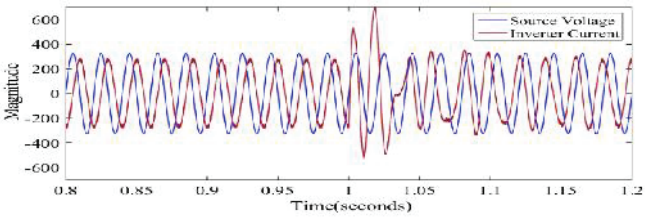
c) DC Link voltages



d) Ripple in DC link Voltage



e) Comparison of load and inverter q-components of Currents



f) Source Voltage and STATCOM current

Figure 7. STATCOM response for variation of load from RL to RC at 1 sec with Space Vector Phase Shifted Carrier PWM

V. Conclusions

The DC link voltage balancing is one of the major problems in cascaded multilevel STATCOM. In this paper, two control strategies are proposed for cascaded H-bridge five level based STATCOM. With these control strategies, the dc-link voltages of all the H bridges are balanced even if the STATCOM mode is converted from one load to another load. In all the circumstances, the reactive components required by the load are supplied by the STATCOM, and the harmonics in the inverter output current and voltage are reduced. The SVPSCPWM strategy gives 2.92% of harmonics in the output currents of the inverter and it gives 19.44% of harmonics in the output voltage which are less with respect to SPSCPWM technique. During the change of load the settling time required for the reactive components supplied by STATCOM is less in SVPSCPWM. Both methods give almost similar performance i.e harmonics in the output current, DC-link voltage balancing, and supplying of reactive components to load for different load changes.

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Simulink Modeling and Analysis of Grid connected PV System

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Abstract: **Due to lack of abundant availability of conventional energy sources, energy demand across the world met by renewable energy and is harnessed from natural resources such as sunlight, wind, rain, tides and geothermal heat which can be replenished. This paper gives the simulink modeling and analysis of grid connected Photo Voltaic (PV) system. Incremental conductance Maximum Power Point Tracking (MPPT) technique used to track maximum power from PV and is connected to boost converter to boost the voltage to maintain the voltage from PV. A two level inverter is used for DC to AC conversion with Pulse-Width Modulation (PWM) control. To synchronize the grid to solar PV at certain phase angle and frequency, Phase-Lock-Loop (PLL) technique used. Control circuit is designed to supply the power according to the load variations.**

Index Terms: **MPPT, Boost Converter, Two level Inverter, PWM, PLL.**

I. Introduction

The increasing energy demand and the less availability of conventional resources to meet the energy demand made a big focus on renewable energy sources .Renewable energy has a greater importance in the world because of the clean and environmentally safe energy, .besides classification of renewable energy based on the source of generation of solar Photo voltaic energy has become more popular as it is noise free and almost maintenance free. By arranging Solar cells in series -parallel fashion a PV module is designed which further connect series –parallel to form a solar . The maximum power can be extracted from PV panels which depends on temperature, irradiance and also on the non linear characteristics of the PV cell.

To obtain maximum power from the PV which is essential due to non linear characteristics of PV array Maximum power point Techniques (MPPT) are used. The different types of MPPT techniques are listed below [3].

1. Incremental Conductance MPPT
2. Perturb and Observe
3. Fractional open circuit voltage
4. Fractional short circuit current

In this paper incremental conductance technique is used to track maximum power for the Duty Cycle adjustment in modeling the system. A two stage conversion strategy is used to feed the supply to grid. First stage of conversion uses boost converter to boost the input DC voltage level. In Second stage two-level inverter is used to convert DC to 3-phase AC supply by pulse width modulation (PWM) control. For synchronization of the system to the grid PLL(phase lock loop) technique is used [6].

II. Solar Cell Modelling

A. PV CELL

A solar module is formed by connecting solar cells in series and parallel for required voltage and current. The equivalent circuit of solar cell has one current source where diode is connected parallel to it.

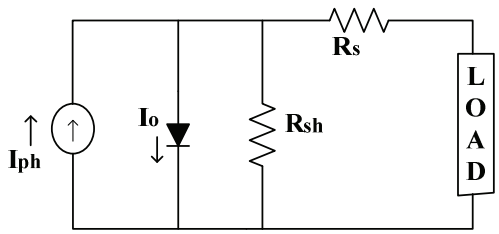

Figure. 1. Single diode solar circuit

The characteristic equation for a photovoltaic cell is given by

$$I_{ph} = [I_{scr} + \{k_i * (T_{ak} - T_{rk})\}] * \frac{s}{1000} \quad (1)$$

$$I_d = I_{rr} * \left(\frac{T_{ak}}{T_{rk}}\right)^3 * \exp\left[\frac{qe_g}{kA}\left(\frac{1}{T_{rk}} - \frac{1}{T_{ak}}\right)\right] \quad (2)$$

$$I_{rr} = I_{scr} / \exp\left(\frac{V_{oc}q}{kN_s AT_{rk}}\right) - 1$$

$$I_{pv} = N_p I_{ph} - N_p I_d \left[\exp\left\{\frac{q \times (V_{pv} + I_{pv}R_s)}{N_S AKT}\right\} - 1\right]$$

(3) & (4)

T : Temperature of the cell;
k : Boltzmann's constant, 1.38 * 10^{-19} J/K;
q : Electron charge, 1.6*10^{-23} C;
K_i : Short circuit current
I & V : output current and voltage;
I_{os} : Reverse saturation current;
I_d : Solar irradiation in W/m^2;
I_{scr} : Short circuit current;
E_{go} : Band gap;
A : Ideality factor;
T_r : Reference temperature;
I_{or} : Saturation current at Tr;
R_{sh} : Shunt resistance;
R_s : Series resistance

The characteristic equation of a solar cell is dependent on the number of cells in parallel and number of cells in series.

B. MPPT

In incremental conductance method the terminal voltage is controlled according to the maximum voltage which depends on the incremental conductance of the PV .For the change in output conductance if dI/dV is negative then the voltage is decreased and if dI/dV is positive then voltage is increased to track the maximum power at every instant..

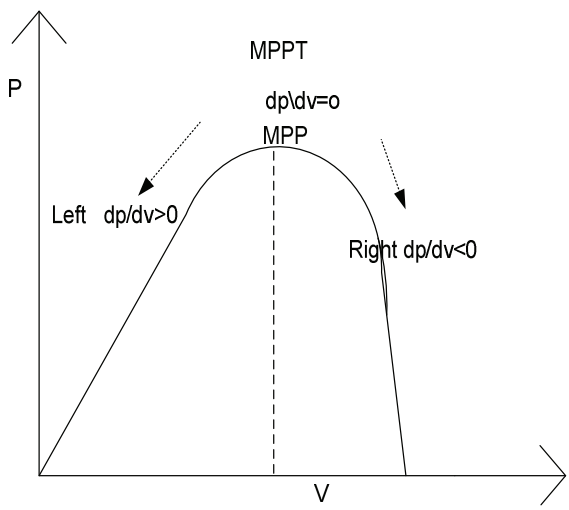

Figure.2. PV characteristics of a solar cell

Power=Voltage*current
By differentiating power with respect to voltage;
$dP/dV=(V*I)/dV$
$dP/dV = I + V*(dI/dV)$
For maximum power point is reached the slope $dP/dV=0$. Thus the condition would be;
$dP/dV=0$
$I + V*(dI/dV)=0$
$dI/dV= -I/V$

C. Boost Converter

Boost converter gives the output voltage greater than input voltage. PV cell DC voltage is necessary to step up for maintaining required rms AC Voltage using Boost Converter [8]. The Boost Converter consists of Voltage Source, Inductor, Switch (IGBT), Diode, Capacitor, Load. It involves two modes of operation [09].

Mode1: Switch is ON state, current flows through Inductor (L), Switch.
Mode2: Switch is OFF state, current flows through Inductor, Diode, Capacitor, Load.
The general circuit diagram of Boost Converter shown in Figure.3.

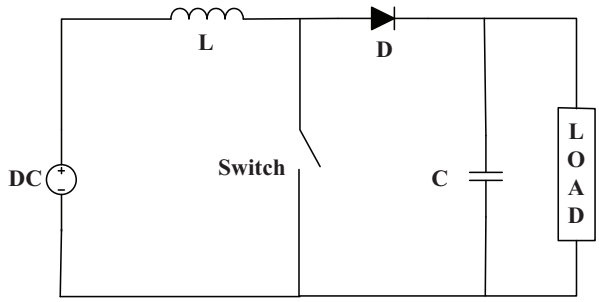

Figure.3. Boost Converter

The output of Boost Converter voltage is

$$V_o = \frac{V_s}{1 - Z} \quad (4)$$

Where,
V_o = Output voltage
V_s = Input voltage
Z = Duty cycle ratio

Duty cycle is extracted from MPPT and given to switch (IGBT) through PWM generator.

D. Inverter

A DC to AC conversion with desired output voltage for any frequency. The inverters can be broadly divided into

- **Voltage source inverter**
- **Current source inverter**

A two level Voltage Source Inverter (VSI) is fed with DC voltage which converts fixed DC voltage to 3-Phase AC voltage. Mostly these inverters are employed in machines and converter control. The VSI consists of three legs with two IGBT switches on each leg, DC Source and Load. General diagram of VSI is shown in Figure.4.

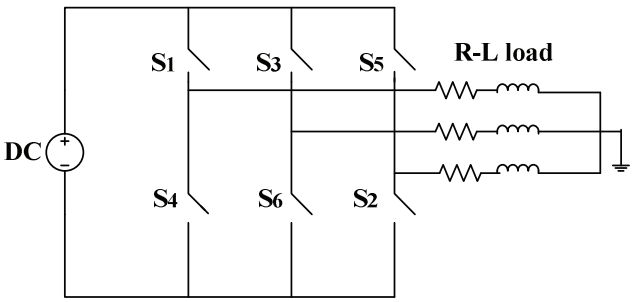

Figure .5. Three phase Voltage source inverter

Various controlling techniques are implemented out of which two most popular techniques are [10]

A. Pulse Width Modulation (PWM)
B. Space Vector PWM (SVPWM)

Switching purpose pulses of IGBT are driven by Pulse Width Modulation (PWM) Technique. In PWM triangular carrier Wave is compared with Sinusoidal reference wave of desired frequency. According to the condition ($f_r > f_c$) which provides switching instant pulses to IGBT. VSI is equipped with DC link of Capacitance bank which is used for grid synchronization purpose.

III. Grid Connected System

A. Phase Lock Loop

Phase locked loop is used to obtain the rotational frequency, direct and quadrature voltages. To interface the voltage source inverter with the grid phase angle information is necessary In PLL, Three-phase AC voltage (V_a, V_b, V_c) are transformed to two -phase stationary frame(V_α, V_β) using equation (1) and again two-phase voltage are transformed to rotating frame of d, q axis (V_{dr}, V_{qr})using equation (2). To transform from rotating frame to synchronous frame PI Controller and Integrator are used to estimate angular frequency and phase angle [6].

. In PLL, Three-phase AC voltage (V_a, V_b, V_c) are transformed to 2-phase stationary frame (V_α, V_β) using Equation (1) and again two-phase voltage are transformed

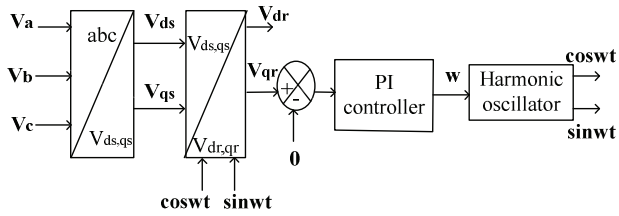

Figure 6.Phase Lock Loop

to rotating frame of d, q axis (V_{dr}, V_{qr}) using equation (6). To transform from rotating frame to synchronous frame, PI Controller and Integrator are used to estimate angular frequency and phase angle [8].

$$\begin{pmatrix} V_\alpha \\ V_\beta \\ V_o \end{pmatrix} = \frac{2}{3} \begin{pmatrix} 1 & -\frac{1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{pmatrix} \begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} \quad (5)$$

$$\begin{pmatrix} V_{dr} \\ V_{qr} \end{pmatrix} = \begin{pmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{pmatrix} \begin{pmatrix} V_\alpha \\ V_\beta \\ V_o \end{pmatrix} \quad (6)$$

If the estimated frequency (w^*) equals to actual frequency (w) at the estimated phase angle (θ^*) which is integral of (w^*), then rotating frame voltages (V_{dr}, V_{qr}) appear as DC Value [12]. These estimated values are feed backed as cos (wt), Sin (wt) to determine rotating frame voltages and PLL gets locked at ($\theta^* = \theta$).

B. Control

The PV real power output is given by

$P_s = 3/2\ V_\alpha\ I_d$ (7)

Where I_d proportional to real power

The reactive power is given by

$Q_s = -3/2\ V_\alpha\ I_q$ (8)

Where I_q controls Q_s

The above equations give the dependence of P_s and Q_s on I_d and I_q. The paper presents current-control scheme for controlling the voltage. So that I_d and I_q track their respective I_{dref} and I_{qref} . When I_{dref} and I_{qref} are limited then it is also used to protect the voltage source control against overload and faults. The current-control scheme is designed using the equations shown below.

$$L\frac{di_d}{dt} = L\omega i_q - Ri_d + m_d\frac{v_{dc}}{2} - v_{sd}$$

$$L\frac{di_q}{dt} = -L\omega i_d - Ri_q + m_q\frac{v_{dc}}{2} - v_{sq}. \quad (9 \& 10)$$

From the equations the state variables are I_d and I_q ; the control inputs are e_d and e_q and V_α, V_β, ω,and V_{dc} are the disturbances. Due to the presence of the factor Lω, dynamics of id and iq are coupled and are nonlinear. To decouple and linearize the dynamics, m_d and m_q are determined based on the control laws:[10]

$$m_d = \frac{2}{v_{dc}}\left(u_d - L\omega i_q + v_{sd}\right)$$

$$m_q = \frac{2}{v_{dc}}\left(u_q + L\omega i_d + v_{sq}\right) \quad (11 \& 12)$$

$$L\frac{di_d}{dt} = -Ri_d + u_d$$

$$L\frac{di_q}{dt} = -Ri_q + u_q. \quad (13 \& 14)$$

Equations 7 & 8 shows the dependency of u_d and u_q, respectively. Figure.7. shows the block diagram of the dq-frame current-control scheme. Similarly, u_q is the output of another compensator, kq(s), that processes $e_q = i_{qref} - i_q$. It should be noted that, to produce m_d and m_q, the signals $2/v_{dc}$, ωi_d and ωi_q are employed as feed-forward terms to decouple the dynamics of i_d and i_q from that of v_{dc}.

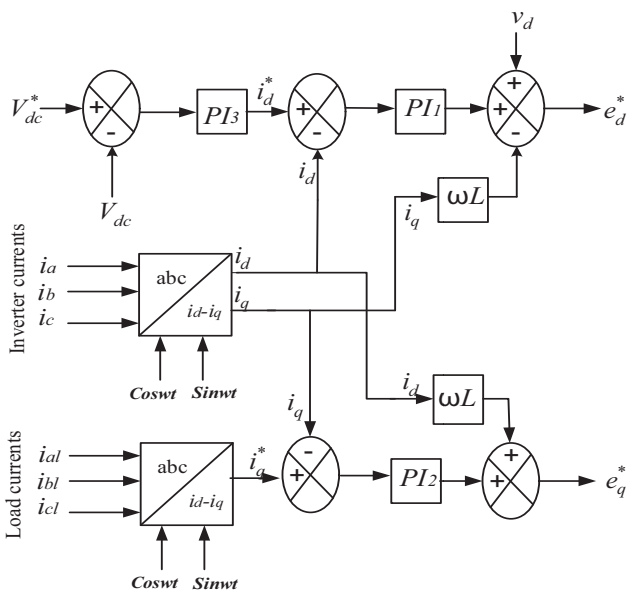

Figure.7.controlcircuit of inverter

The Pulse width modulation signals are obtained by the transformation of m_d and m_q into m_a, m_b and m_c, based on:

$$\begin{bmatrix} m_a \\ m_b \\ m_c \end{bmatrix} = \begin{bmatrix} \cos(\rho) & -\sin(\rho) \\ \cos(\rho - \frac{2\pi}{3}) & -\sin(\rho - \frac{2\pi}{3}) \\ \cos(\rho - \frac{4\pi}{3}) & -\sin(\rho - \frac{4\pi}{3}) \end{bmatrix} \begin{bmatrix} m_d \\ m_q \end{bmatrix} \quad (15)$$

m_a, m_b, and m_c are compared with a triangular PWM carrier signal, and the switching pulses are generated from the VSC valves. Since the d- and q-axis control plants are identical, the compensators kd(s) and kq(s) can be picked to be identical. Let the compensator be of a PI type as:

$$k_d(s) = k_q(s) = \frac{k_p s + k_i}{s} \quad (16)$$

Where the values are

$$k_p = \frac{L}{\tau_i}$$

$$k_i = \frac{R}{\tau_i} \quad (17 \& 18)$$

the closed-loop transfer-functions of the d- and q- axis current controllers assume the first-order form. where τ_i is the time-constant, usually selected in the range of 0.5 to 5 ms, depending on the desired speed of response. [7]

$$\frac{I_d}{I_{dref}} = \frac{I_q}{I_{qref}} = G_i(s) = \frac{1}{\tau_i s + 1} \quad (19)$$

IV. Simulation Results

In standalone system from the data values provided simulation study is done where the power from the solar is extracted and supplied to the 3 phase balanced load. Here the output voltage of the array is the input to the boost converter of (120v) is converted to 600v following the equation as calculated. The output voltage of boost appears to be dc as shown in Figure.9.

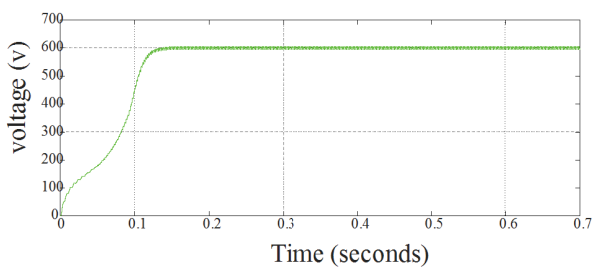

Figure 8. Boost converter voltage(Vdc)

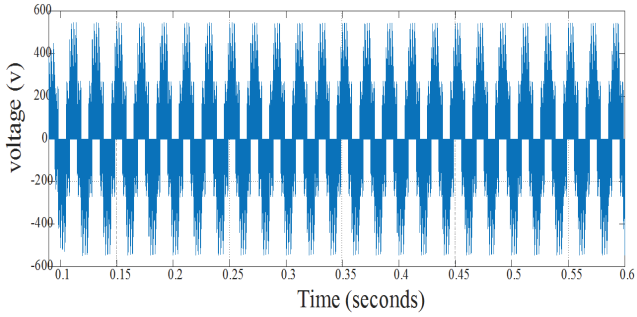

Figure.9. Inverter phase voltage V_a

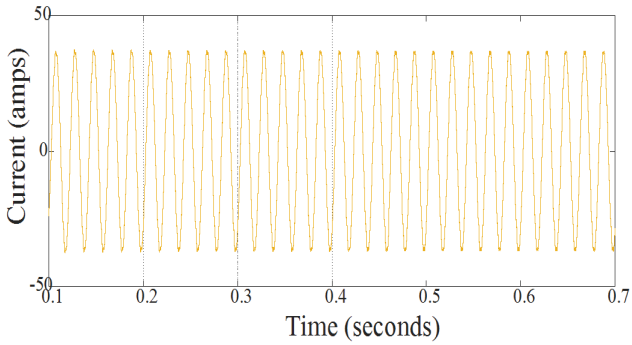

Figure.10. Inverter line current (I_a)

TABLE.I
PHASE LOCK LOOP PARAMETERS

Parameters	values
Source phase –phase voltage	440 v
Source frequency	50 hz
Load p-p voltage	1000v
Load frequency	50
Active power	$10e^3$
Reactive power	100
PI controller	P=5,I=10

A. Control

The PLL is used for the measurements of the frequency and phase-angle. It can estimate the real and reactive power flow to the load. PLL is a central component in a control structure. From the input signal phase values are detected for the source values as shown in Figure.11 where the phase values of inputs appears to be dc voltage of V_{dr}=340 v and V_{qr} = 0. The error signal in phase is passed through the loop filter which helps in determining the angular frequency (w) at the estimated value of (314) rad/sec as shown in fig 1.5 and phase angle is determined as unit vectors by the harmonic oscillator as shown in fig 1.6

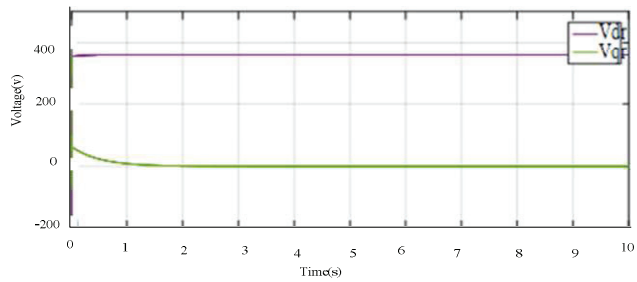

Figure.11. V_{dr},V_{qr} voltages

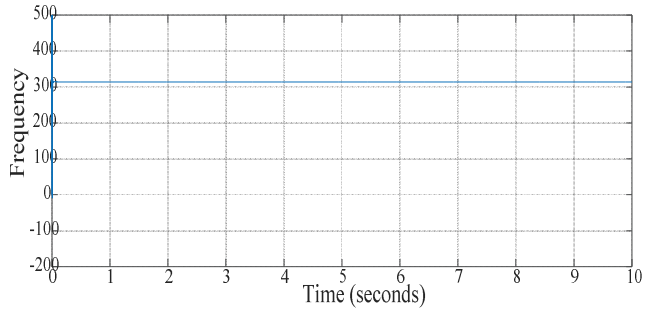

Figure.12. Angular frequency (w)

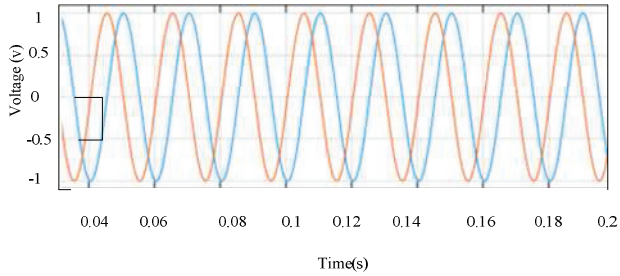

Figure.13. unit vectors

TABLE.II
GRID CONNECTED PV SYSTEM SIMULATION DATA

Parameters	Values
Grid voltage	400 v
Grid frequency	50hz
Load	R=4.6 Ω, L=0.0146H
Inverter capacitor	$60e^{-6}$
Pll PI control	P = 50, I= 100
Control PI	P = 0.1, I= 0.2
Filter	$5e^{-3}$

In this system solar system is interfaced to grid and load so that pv system supplies active power to the load where as the source supplies reactive power to load. such that I_{dinv} tracks the I_{dre}f as shown in Figure.14.

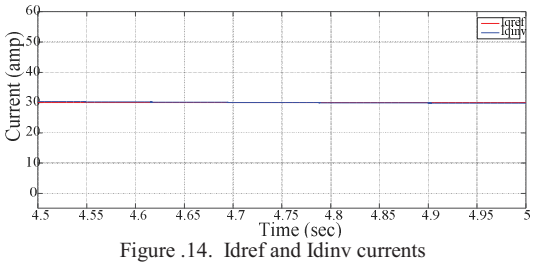

Figure .14. Idref and Idinv currents

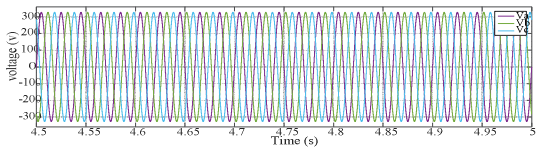

Figure 15. Grid voltage

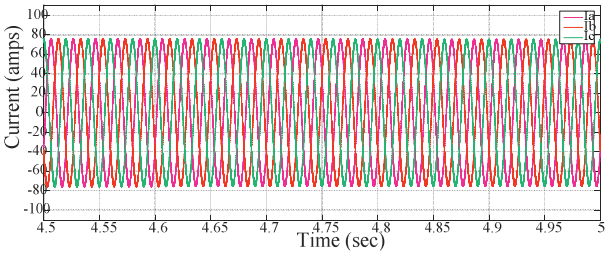

Figure 16. Grid current

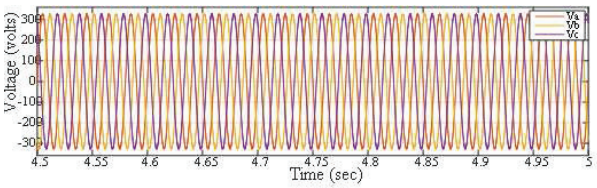

Figure 17. Inverter voltage

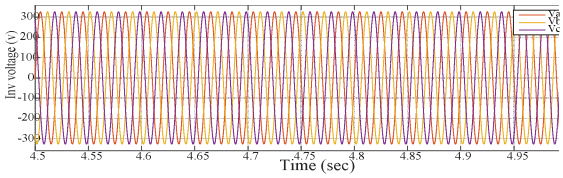

Figure 18. Inverter currents

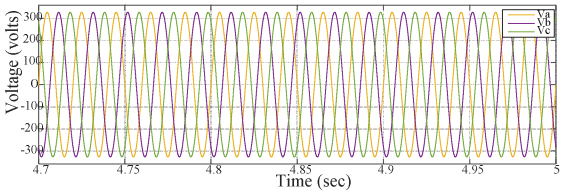

Figure 19. load voltage

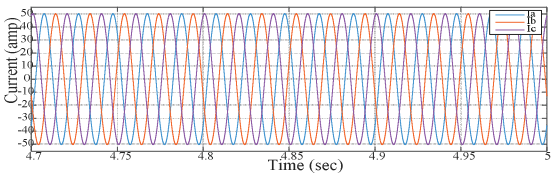

Figure 20. Load current

V. Conclusions

The grid connected PV system suffers form ground leakage currents by which distortion factor will increase during the operation which can be reduced by using transformer less inverters in the circuit.

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Design and Implementation of 3-Phase 2-Stage Grid-Connected Solar PV System

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Abstract: **Solar Photo Voltaic (SPV) system is categorized under Distributed generation to meet the demand of power for load variations, as it also helps in assisting the existing power system. In this paper, Standalone PV system is interfaced to three phase grid which includes PV array, Perturb and Observe (P and O) Maximum Power Point Tracking (MPPT) technique used to track maximum power from PV array and also for the adjustment of Duty Cycle for giving switching pulses to High level switch of Boost Converter. 2-level Inverter is used for DC to AC conversion with Pulse-Width Modulation (PWM) control. Phase-Lock-Loop (PLL) technique is implemented to synchronize the Standalone PV system with grid at certain phase angle and frequency. Control circuit is designed to supply active and reactive power to load by standalone PV system and grid according to load variations. The overall system is simulated in Matlab software for outputs.**

Index Terms: **MPPT, Boost Converter, 2-Level Inverter, PWM, PLL.**

I. Introduction

Renewable energy sources like solar photovoltaic cells, wind, biogas are mainly employed for generation of power locally at a distribution level of voltage known as Distributed Generation (DG). Commonly solar photovoltaic (SPV) systems are utilized as Distributed Generation (DG) source due to abundant solar energy availability, long life of the solar photovoltaic (SPV) system with less maintenance [1]. Earlier standalone photovoltaic (PV) systems were in use which involves battery usage for storage of energy to meet the peak power demand associated with system complexity, reliability and maintenance [2]. To avoid such problems Grid interface PV system came into existence to improve the efficiency as the generated power can be supplied to the grid without any storage.

At present scenario photovoltaic array are extremely safe and reliable with minimum power loss. Usage of solar array for power generation reduces fossil fuel deposits to the great extent. As photovoltaic array is the combination of modules, includes a group of individual solar cell which outputs the voltage and current according to the inputs (Temperature & Irradiance) having non linear characteristics [15]. Solar cell is the basic functional block in the entire solar photovoltaic system with low efficiency output, to increase the output solar cells are connected series or parallel forming PV module [16].

PV module applications may be on the field installation or on building top roofs, based on the locality PV module design depends on the properties such as resistance to bad weather conditions, ability of solar capture, shade conditions for adaptability working of the module under any circumstances [17]. However PV array is connected to grid involves certain impacts of phase unbalance, reactive power, stability and power quality [18].

To interface grid tracking maximum power from the array is essential due to non linear characteristics of array Maximum power point Techniques (MPPT) are used. A review of different MPPT techniques are listed below based on control and operation [3].

1. Incremental Conductance MPPT
2. Perturb and Observe
3. Fractional open circuit voltage
4. Fractional short circuit current

In this paper perturb and observe technique is discussed to track maximum power and for the Duty Cycle adjustment. From PV to grid connected PV system HAS 2 stages of conversion.

1. DC-DC Conversion
2. DC-AC Conversion

First stage of conversion is done by boost converter to boost the input dc voltage level. Second stage of conversion is done by 2-level inverter to convert into 3-phase AC supply by pulse width modulation (PWM) control.

For load sharing between standalone system and grid a control strategy is required, so PLL technique is considered. It plays a vital role in synchronization of standalone system with grid as it gives the information of phase values and frequency. As the phase of inverter and grid outputs are same then the load is connected to the system for active and reactive power flow supply to the load. Based on control procedure adapted to handle both the power flow important techniques are available

1. P-V Controlled inverter strategy
2. P-Q Control strategy
3. Current control scheme

In this paper active power control is done by adapting current control scheme. The block diagram of overall system is shown in Fig 1.

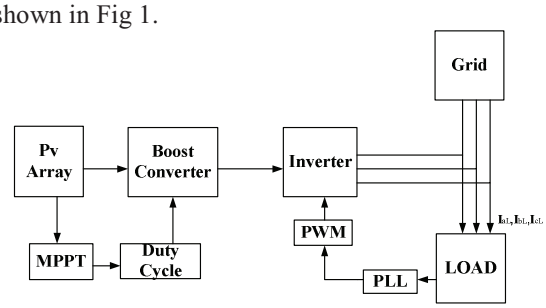

Figure 1. Block Diagram of grid connected SPV system

II. SPV SYSTEM DESIGN

A. PV Array

PV Array has number of solar cells connected in series and parallel for required voltage and current to obtain characteristic curves [4]. Equivalent circuit of single diode model of solar cell shown in Fig 2.

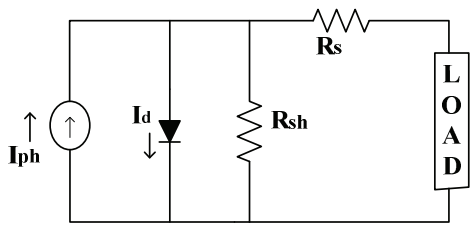

Figure 2. Single diode Circuit of solar cell

Output current of PV module is given by:

$$I_{pv} = N_p I_{ph} - N_p I_d \left[\exp\left\{ \frac{q \times \left(V_{pv} + I_{pv} R_s \right)}{N_S AKT} \right\} - 1 \right] \quad (1)$$

Where,

I_{ph} = Photo current

I_d = Module Saturation Current

N_p , N_S = Series and Parallel Cells Number

T = Temperature (Kelvin)

K = Boltzmen Constant (1.381×10^{-23})

A = Ideality Factor

q = Charge of e^- (1.602×10^{-19})

R_s = Series Resistance Ω

Another model is Two-Diode which as 2 diodes with better accuracy but complexity in modeling [5].

B. MPPT

In Perturb and Observe (P and O) MPPT Power and Voltage values are used for perturbation. P and O Control algorithm is designed in such a way that change in voltage measures the maximum power in forward direction, if power decreases for voltage change adjustment is done in backward direction for maximum Power [6]. The governing equations of ΔP and ΔV are

$$\Delta P = P_k - P_{k-1} \quad (2)$$

$$\Delta V = V_K - V_{K-1} \quad (3)$$

The conditions for perturb and observe MPPT are as follows [7].

$\frac{dp}{dv} > 0$ (+ve slope, left side of curve)

$\frac{dp}{dv} < 0$ (-ve slope, right side of curve)

$\frac{dp}{dv} = 0$ (At Maximum power point MPP)

The Perturbation Process shown in Fig 3.

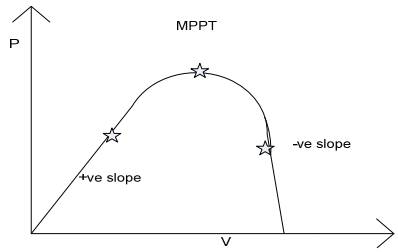

Figure 3. MPPT process

Due to perturbation it decides the Duty ratio to increase or decrease [7].

C. Boost Converter

PV Array DC voltage is necessary to step up for required RMS AC Voltage using Boost Converter [8]. The Boost Converter consists of Voltage Source, Inductor, Switch (IGBT), Diode, Capacitor, Load. It involves two modes of operation [9].

Mode1: Switch is ON state, current flows through Inductor (L), Switch.

Mode2: Switch is OFF state, current flows through Inductor, Diode, Capacitor, Load.

Here energy storage of Inductor flows through the circuit in mode2 operation. The general circuit diagram of Boost Converter shown in Fig 4.

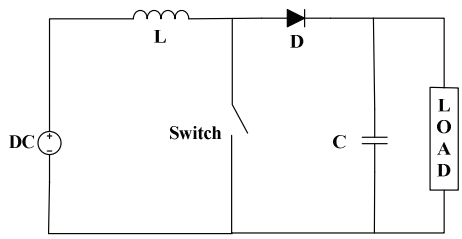

Figure 4. Boost Converter

The output of Boost Converter voltage is

$$V_{out} = \frac{V_{in}}{1 - D} \quad (4)$$

Where,

V_{out} = Output voltage

V_{in} = Input voltage

D = Duty cycle ratio

Duty cycle is extracted from MPPT and given to switch (IGBT) through PWM generator.

D. INVERTER

Two Level Voltage Source Inverter (VSI) is applied which converts fixed DC voltage to 3-Phase AC voltage. Mostly these type of inverters are employed in machines and converter control. The VSI consists of three legs with two

IGBT switches on each leg, DC Source and Load. General diagram of VSI is shown in Fig 5.

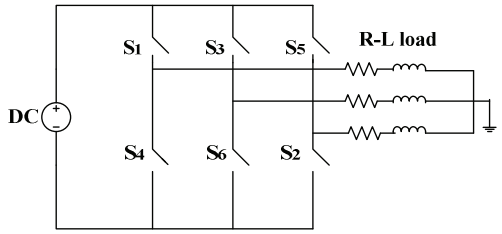

Figure 5. VSI

For controlling 2- Techniques are categorized [10]

A. Pulse Width Modulation (PWM)
B. Space Vector PWM (SVPWM)

In this paper switching purpose pulses of IGBT are driven by Pulse Width Modulation (PWM) Technique. In PWM Triangular carrier Wave (f_c) is compared with Sinusoidal Reference wave (f_r) of desired frequency. According to the condition ($f_r > f_c$) provides Switching instant pulses to IGBT. VSI is equipped with DC link of Capacitance bank which is used for grid synchronization purpose.

III. Control Design

A. Phase Lock Loop

To interface the voltage source inverter with the grid phase angle information is necessary. For obtaining accurate results of phase angle Phase Lock Loop (PLL) technique has been used. It estimates the phase and frequency values [11]. Besides interfacing phase angle parameter is necessary for active and reactive power flow control [12]. The block diagram of PLL is shown in fig 6.

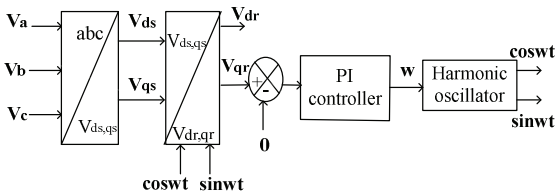

Figure 6. Phase Lock Loop

In PLL, Three-phase AC voltage (V_a, V_b, V_c) are transformed to 2-phase stationary frame (V_{ds}, V_{qs}) using equation (5) and again two-phase voltage are transformed to rotating frame of d, q axis (V_{dr}, V_{qr}) using equation (6). To transform from rotating frame to synchronous frame PI Controller and Integrator are used to estimate angular frequency and phase angle.

$$\begin{pmatrix} V_{ds} \\ V_{qs} \\ V_o \end{pmatrix} = \frac{2}{3} \begin{pmatrix} 1 & -\frac{1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{pmatrix} \begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} \quad (5)$$

$$\begin{pmatrix} V_{dr} \\ V_{qr} \end{pmatrix} = \begin{pmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{pmatrix} \begin{pmatrix} V_{ds} \\ V_{qs} \\ V_o \end{pmatrix} \quad (6)$$

If estimated frequency (w^*) equals to actual frequency (w) at the estimated phase angle (θ^*) which is integral of (w^*), then rotating frame voltages (V_{dr}, V_{qr}) appear as DC Value [12]. These estimated values are feed backed as Cos (wt), Sin (wt) to determine rotating frame voltages and PLL gets locked at ($\theta^* = \theta$).

B. Standalone PV System

Standalone PV System includes PV array, MPPT, Boost converter, Inverter, PWM, 3 phase load. Voltage (V) and currents (I) are sensed from PV array by MPPT for duty cycle adjustment in order to provide gate pulses to IGBT switch of Boost converter which boost up the DC voltage. Obtained DC voltage is supplied to dc link (capacitor) which acts as a source to the inverter (2-level) converting Dc to Ac. For conversion process in inverter switching pulses to IGBT switches are given by Pulse Width Modulation (PWM) technique. Three phase voltage and currents from inverter are provided to 3-phase load. The general block diagram of standalone PV system is shown in Fig 7.

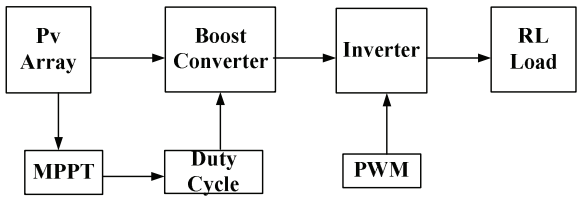

Figure 7. Standalone PV

C. Grid Connected PV System

In grid connected, standalone system and grid are connected to load as shown in Fig 8. For interfacing the both PLL technique is used to maintain at same phase angle and frequency at inverter and grid side [13]. According to the load standalone pv and grid supplies required voltage and current.

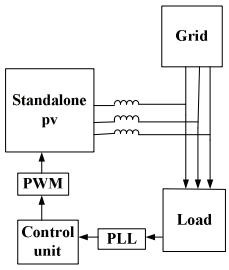

Figure 8. Grid side PV system

For sharing the load between pv system and grid a dq current control scheme is used as shown in Fig. 9.In this control reference signals are estimated according to the load demand. m_d and m_q are estimated voltages given by equation

$$m_d = u_d - \omega L i_q + v_d \quad (7)$$

$$m_q = u_q + \omega L i_d \quad (8)$$

Whereas U_d, $U_q$are specified as

$$U_d = (K_{p1} + \frac{K_{i1}}{s}) e_d \quad (9)$$

$$U_q = (K_{p2} + \frac{K_{i2}}{s}) e_q \quad (10)$$

e_d and e_q are refered as

$$e_d = i_{dref} - i_d \quad (11)$$

$$e_q = i_{qref} - i_q \quad (12)$$

Here i_{dref} and i_{qref} are reference d and q axis currents. Now estimated values of m_d, m_q are transformed to 3 phase reference values through inverse PLL which serve as switching pulse to the inverter [14].

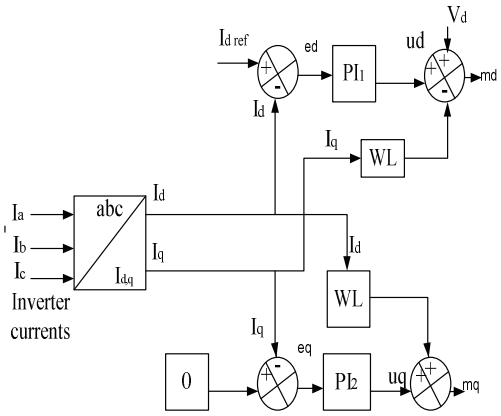

Figure 9. Inverter control circuit

IV. Simulation Results

A. Phase lock loop

In PLL the phase and frequency values are estimated for the input RMS value of voltage or current. At the rms value of voltage of 440 volts V_{dr} is calculated to 359 volts where as V_{qr} is calculated to zero by using the above phase lock loop equations (5, 6) as shown in Fig 10. To find the angular frequency of V_{qr}, it is calculated by 2πf where f is 50 hz which gives ω value as 314 rad/sec as shown in Fig 12. Unit vector of phase values are estimated by harmonic oscillator as shown in Fig 11.

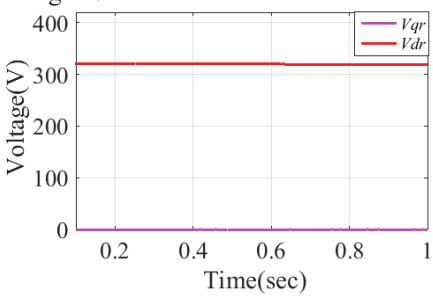

Figure 10. V_{dr} V_{qr} voltages

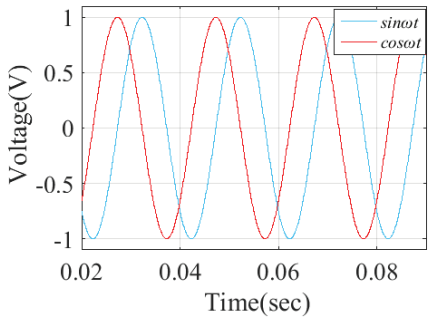

Figure 11. unit vectors

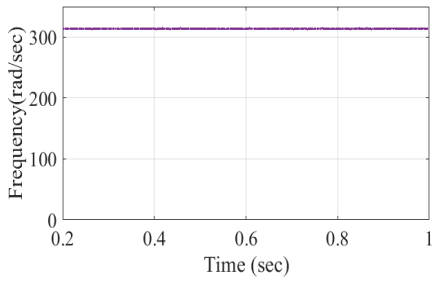

Figure 12. angular frequency

B. Standalone PV System

Standalone PV system simulation study is done based on certain data provided to the system for the block diagram shown in Fig. 7. The simulation data is provided in the table I.

TABLE I.
SIMULATION DATA OF STANDALONE PV SYSTEM

Array Irradiance	1000
Array Temperature	25 deg c
Maximum power(Pmp)	83.2 W
Maximum voltage(Vmp)	10.3 V
Maximum current(Imp)	8.07 A
Boost Inductor L	0.011 H
Capacitance	60 μ F

According to the data, array generates the voltage of 120 (volts). At the point of maximum voltage, maximum power is tracked by(P and O) MPPT maintaining the duty cycle ratio to(D =0.8). Boost converter increases the input voltage fed from array to 600v as calculated from equation (4). The output voltage of boost converter is shown in fig 15. as constant dc voltage.

$$V_{out} = \frac{V_{in}}{1-D}$$

= 120/1-0.8 = 600 V

Here single phase voltage and currents appears to be as step and sinusoidal waveforms are shown in the Fig 13, 14. The peak value of inverter voltage obtained is of dc voltage 600 volts and the sinusoidal currents draw the peak value of current 40 amp for the RL load impedance of 4.6+j0.00146 ohms.

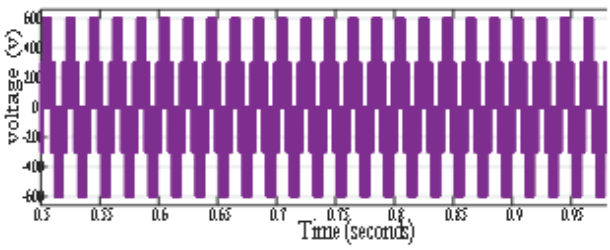

Figure 13. Inverter voltage(Va phase)

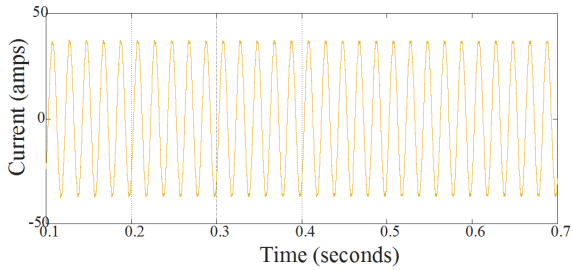

Figure 14. Inverter current (Ia)

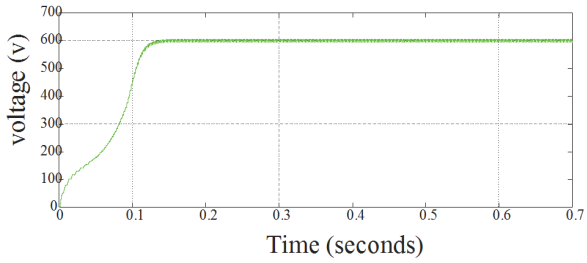

Figure 15. Boost converter voltage(Vdc)

C. Grid connected PV system

The simulation data for simulation study is shown in table II.

TABLE II.
GRID DATA

Parameters	values
Grid voltage	400 v
Grid frequency	50
Load	R=4.6 Ω, L=0.0146H
Pll PI control	P = 50, I= 100
Control PI	P = 0.1, I= 0.2
Filter	$5e^{-3}$

In grid connected PV system impedance of the load is taken as Z= 4.6+j0.0146 ohms, the load currents obtained are (30-j30) amps. To supply active component of current (30 amps) by the inverter, control is designed setting reactive component to zero. For active power control actual current of inverter matches reference current (I_{dinv}=I_{dref}) as shown in fig 16. Inverter supplies peak current of (30 amps) to the load which is active component fed into load as shown in fig 18. but the load demand is more of (50 amps) as shown in fig 19. The remaining power to the load is supplied by grid of current value of (78 amps) as shown in fig 20. as grid is both active and reactive source Here the voltages of grid, inverter and load are not influenced and maintained peak voltage of 330V as shown in fig (21,22,23). The dc voltage obtained ($2.3*10^4$) volts after interfacing with load and grid is shown in Fig 17.

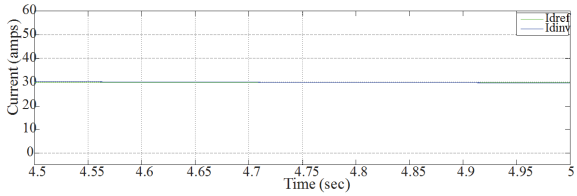

Figure 16. I_{dinv} and I_{dref} currents

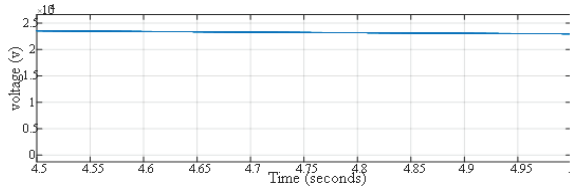

Figure 17. Dc voltage (V_{dc})

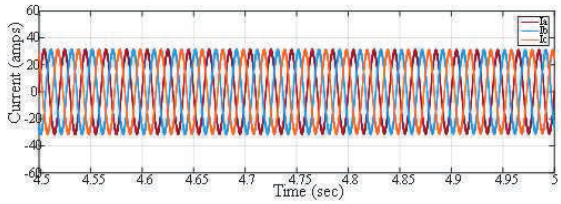

Figure 18. Inverter current

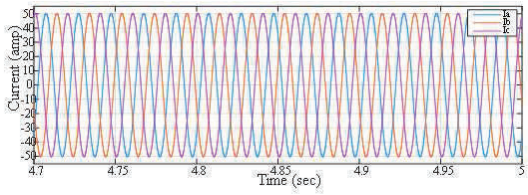

Figure 19. Load current

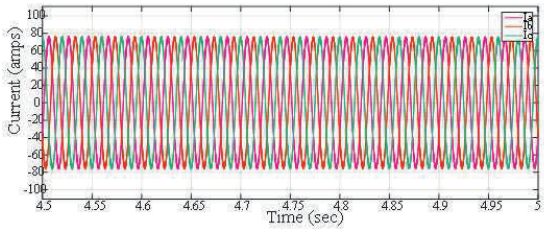

Figure 20. Grid current

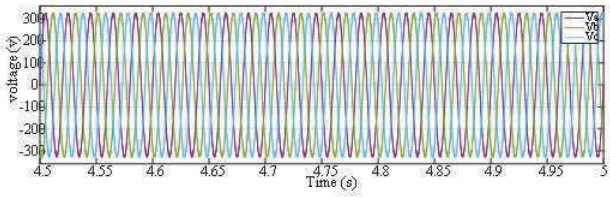

Figure 21. Grid voltage

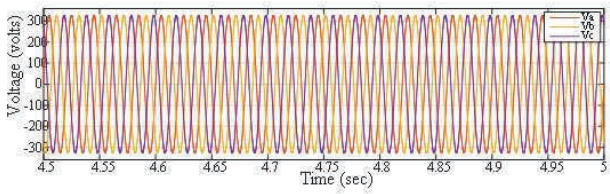

Figure 22. Inverter voltage

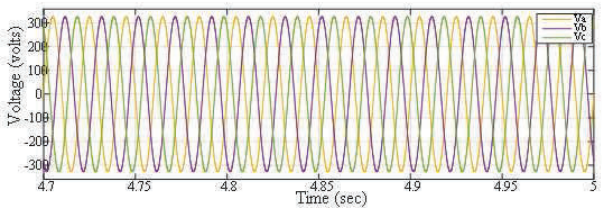

Figure 23.Load voltage

V. Conclusions

Solar cell is developed with the described equations which operates at an effective voltage and current by the inputs of temperature and irradiance. Standalone system study is done which supply power to the particular load, where it involves the MPPT technique to track maximum power. Phase locked loop plays a significant role in connecting a power electronic converter to the grid. In this paper, PLL is implemented in a grid connected system. The three phase voltages are converted into two phase voltages. The two phase voltages are transformed to synchronous rotating frame. The q-component of source voltage, v_q is made zero using PI controller, which ensures exact frequency information of source at any time.

In this paper power flow control is also implemented using control logic circuit for active power compensation. The control logic generates reference voltages and fed to inverter through PWM technique to supply active component of current for the load connected. The designed system is applicable for the load variations under balanced condition.

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LabVIEW based Greenhouse Automation

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Abstract: **The main aim of this paper is to control the basic parameters of greenhouse using LabVIEW. LabVIEW is an environment that consists of several components which are required for any type of measurement, test or control application. This involves development of a prototype model which mimics the greenhouse system. This prototype contains beds of soil which has seeds planted in it. Small pipelines are used for irrigation of the same. As irrigation needs proper humidity and temperature control, sensors are used to control these parameters. Also the prototype has a Door monitoring system which enables better ambient conditions control. Every parameter is monitored and controlled using LabVIEW software. Web service is used for the real time applications. This enables the monitoring and control from a remote place also**

Index Terms: **Greenhouse effect, LabVIEW, Front panel, Temperature sensor, Humidity sensor**

I. Introduction

Greenhouse is a place where plants are grown under optimal conditions. It includes ambient temperature, light intensity, soil fertility, water irrigation, and humidity. Different plants require different conditions for their growth which may not be possible at all times [1]. To overcome this and help the maintenance of optimal conditions inside a greenhouse, automation is done using LabVIEW [2]. By using Lab VIEW and Data Acquisition systems we can measure and monitor the parameters required inside a greenhouse. In this paper, humidity, door monitoring, water irrigation and temperature are monitored and controlled for the developed prototype. Different sensors are used for the measurement of the parameters which are then interfaced with DAQ and are controlled using LabVIEW.

A. Hardware

The prototype is constructed as shown in figure 1. Four beds of soils are made on a wooden plank. Seeds are sown in it. Four tubes are provided above the soil bed, to promote timely water supply. It is covered with a transparent sheet to provide sunlight. Sensors are used for measuring the parameters. These sensors are interfaced with DAQ and controlled using LabVIEW software. These sensors are run using external power supply taken from regulated power supply. Outputs from the DAC are very low mostly in milli volts. Low voltages and current may not run the motors and other devices used in the project, hence amplifier circuits and relays are used for the devices to run.

Figure 1. Prototype of the Greenhouse setup

B. Software:

National Instruments Compact Field Point (CFP) is used to interface the hardware with the digital controller developed in LabVIEW. LabVIEW is a graphical programming tool that enables the user to develop programs swiftly without worrying about the syntax.

II. Block diagram

The following are the technologies implemented for executing the project

- LabVIEW Graphical Programming
- High Speed Data Acquisition using NI CFP

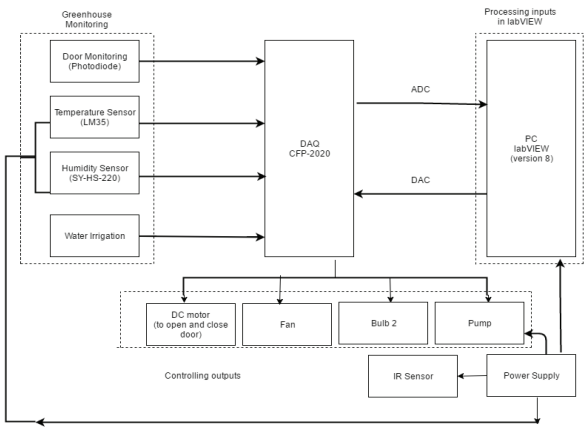

Figure 2. Block diagram

The block diagram shown in figure 2 illustrates the blocks of greenhouse monitoring and control set up. This is

divided into three sections comprising of a monitoring system, processing system and a feedback system. All programs which are written inside the LabVIEW version 8 environment are called VIs. A VI consists of a Block Diagram and a corresponding Front Panel. The Front Panel includes various controls and indicators while the Block Diagram contains various functions and other VIs that are inter wired among themselves.

III. Temperature Control

Temperature is one of the important parameters to be maintained in the greenhouse. Greenhouse is mostly constructed in the cold countries where temperature is very low and plants would get freezed in that climate [3]. If temperature is above the required point then fan should be turned ON. If the temperature is below the set point then bulb should be turned ON. This is all done using a feedback loop and continuous monitoring. The control system associated with this may appear as an open loop system and to reduce errors it is more common to use negative feedback. The diagram shown in Figure 3 represents the basic structure of a closed loop control system.

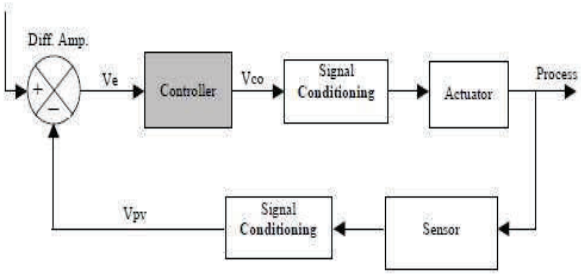

Figure 3. Closed Loop Control System

The Process block in the above diagram represents a physical characteristic. This characteristic chosen has to be maintained at the desired operating point. In this paper, Temperature is selected as the physical quantity. Hence it is to be maintained at the desired value. The feedback loop provides the current value of the process thereby enabling the generation of error signal. A solid state temperature sensor is used to monitor the temperature in this application [4]. It sends an output voltage that is very small for practical purpose, typically in the millivolt range. The signal is amplified by the signal conditioning block that follows it. The signal conditioning block may also be used for calibration purposes by scaling the voltage from the sensor to the corresponding temperature. The current value of the process variable is obtained from the signal conditioning block and it is designated as VPV. The data flow of the temperature control operation is shown in the Block Diagram panel. Figure 4 shows the details of the Front panel [5] which describes the operation of the ON/OFF controller of the process. The operation begins with a check on whether the Controller is ON or OFF. This is accomplished with VI 2 (AI Sample Channel.vi) and the comparator C1. The output of C1 is either TRUE or FALSE. If TRUE, then the Controller is OFF, and if FALSE then the Controller is ON. VI 2 takes its input from Channel 1 of Device 1 (DAQ Board number). Analog input Channel 1 is physically wired to DAC output Ch. 0 which controls the operation of the fan. Thus by testing the DAC output Ch. 0, one can determine whether the Controller is ON or OFF.

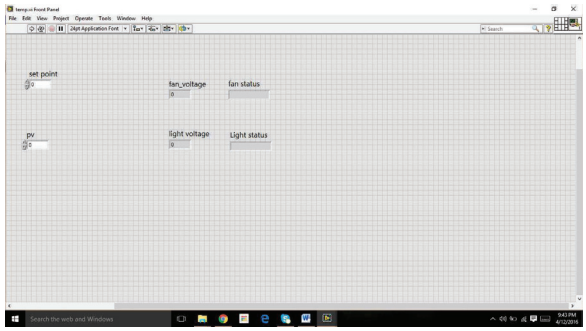

Figure 4. LabVIEW version 8 front panel for temperature measurement and control

IV. Humidity Control

The measure of the amount of water in the air is called RELATIVE HUMIDITY (RH). Relative humidity is the ratio of actual water vapour content to the saturated water vapour. RH is not a direct measurement as it is measured on a relative basis. Hence this may make Relative Humidity a little harder to understand unlike the measurement of temperature, pressure and other parameters. However the role of RH is extremely important in determining the plant health. To make the measurement of RH more user friendly to the plants, proper equipments have to be chosen. As the temperature of the air increases, its potential water-holding capacity also greatly increases. For example, air at 60ºF (~16ºC) can hold over five times as much water as the same air at 20ºF (~ –7ºC). As an example it can be seen that water or frost settles out on automobiles, grass and the rooftops of our houses during cool nights of even warm spring days. This is called DEW POINT where the warm air cools and reaches a point of SATURATION. In parts of the world where there is higher relative humidity, this is a common occurrence when there are marked temperature differences between day and night. But in many places where there is a wide temperature difference, infrequent dew formation can be seen if the place is less humid. The air holds so little water that it does not reach saturation even at the lower night temperatures. To measure humidity, a smart humidity sensor module SY-HS-220 is used for this design. The humidity sensor SY-HS-220 is shown in the Figure 5. It can be seen that the board consists of signal conditioning circuits along with the humidity sensor.

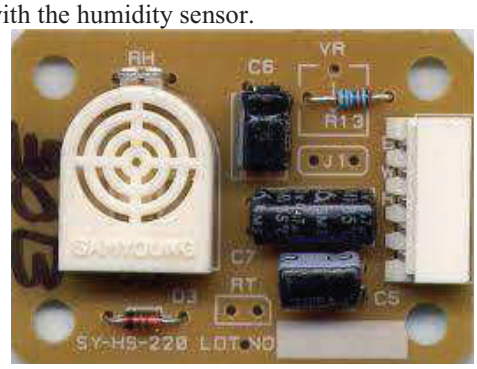

Figure 5. SY HS 220 humidity sensor

The humidity sensor used here is capacitive type. It consists of an on chip signal conditioner. The whole setup is mounted on a PCB (Printed Circuit Board) which enables markings for other stages. The sensor is pulsed with the help of CMOS Timers which provides the output voltage. The other units are frequency to voltage converter, AC amplifier, Oscillator and Precision Rectifiers. Incorporation of such stages on the board significantly helps to enhance the performance of the sensor. It also helps to provide great impediment to the noise. The humidity sensor is highly precise and reliable. The output of the sensor is in terms of DC voltage and it voltage is directly proportional to the humidity [6] and it decreases the need for conversion of voltage to RH%. This work with +5 Volt power supply and the typical current consumption is less than 3 mA. The operating humidity range is 30%.

The following code is written to measure the relative humidity and SY-HS-220 is used to measure the relative humidity .The output of the sensor is voltage .This code is used to convert the voltage to %RH and it is done by calculating the slope by taking into considerations the output voltage ratings of the sensor used. The code also indicates the status of %RH if it is within the sensor operating range or beyond. When the relative humidity falls beyond the sensor operating range then an LED will glow indicating to perform the necessary operations to maintain the humidity. If the humidity is less then humidifier then it must be turned ON and if the humidity is more than a small inlet, it must be opened until there is required humidity in the room. The front panel in figure 6 indicates the relative humidity after conversion using a numeric indicator and gauge. The status tab shows if the relative humidity is within the sensor operating range or
beyond.

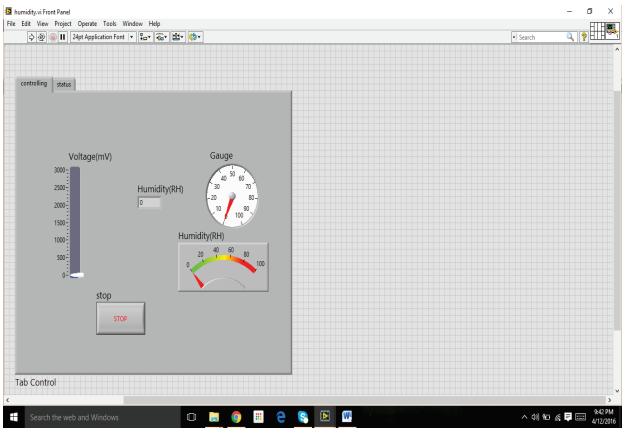

Figure 6. LabVIEW version 8 front panel for humidity measurement

V. Door Monitoring

The main aim to include door monitoring in our project is to maintain the required parameters [7] (ie. set conditions) in our greenhouse prototype. When the door is kept open the air may flow in and would disturb the temperature and humidity in the room. To prevent that we will be automatically closing the door after a certain time once it is opened .When a person arrives at the door he would sensed by the proximity sensor first and then the door gets opened by some mechanical function. The IR sensors follow a principle of using a specific light sensor which detects the IR wavelength in the electromagnetic spectrum. An infrared (IR) sensor is an electronic device, that emits light in the IR wavelength in order to sense some aspects of the surroundings. Applications of IR sensors involves motion detection and even thermal energy i.e heat variation of objects. This type of sensor is called passive IR sensor as it can measure only infrared radiation rather than emitting. Usually in the infrared spectrum, all the objects radiate some form of thermal radiations. These types of radiations are invisible to our eyes which can be detected by an infrared sensor. The emitter is simply an IR LED (Light Emitting Diode) and the detector is simply an IR photodiode which is sensitive to IR light of the same wavelength as that emitted by the IR LED. When IR light falls on the photodiode, the resistances and these output voltages change in proportion to the magnitude of the IR light received**.** When any object strikes the IR region then it produces the minimum amount of voltage which is given to the DAQ [8] and again from the DAQ input voltage it is given to the motor driver and from the motor driver, the motors operate. Figure 7 shows the block diagram of the door monitoring.

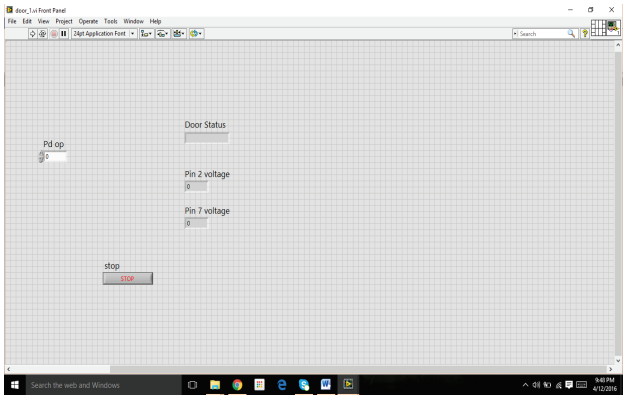

Figure 7. LabVIEW version 8 front panel for door monitoring

VI. Drawbacks

The two main drawbacks faced in the above setup are as follows. Appropriate sensor has to be chosen in temperature control as the output required was in centigrade. So a signal conditioning IC LM35 was used. The IC senses the temperature and gives an output in voltage. Later the voltage was calibrated to temperature and it was used for controlling. The second main drawback was that the sensor used for humidity measurement. It gave an output in terms of voltage which had to be converted to humidity (%RH) in order to monitor. Controlling humidity was big deal because humidity varies consistently and maintaining it was a tough task. Automatic controlling of humidity is more tedious as it involves huge hardware like humidifier etc.

VII. Conclusions

The main aim of this paper is to control and monitor the basic parameters of the green house using LabVIEW version 8. Different parameters like temperature, automatic door monitoring, water irrigation are studied, monitored and

controlled. Humidity is a parameter which is measured and indications are given accordingly. Problems faced in terms of interfacing, programming, circuitry and power amplifications are overcome. All these are done using LabVIEW and DAQ. A prototype has been designed to resemble the greenhouse and all the measurements are taken within the prototype. Hence by implementing this we are able to monitor and control certain parameters like temperature, humidity and able to meet the required optimal conditions for greenhouse. The door monitoring and water irrigation is also done.

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Predicting Student Performance using KNN Classification in Bigdata Environment

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Abstract: **The data mining techniques are widely used to run business in profits and also for analyzing the data for different business needs. The analysis of data has many advantages. The extraction of hidden trends in the large data is much helpful to make decisions. The data mining system also called as knowledge discovery from databases, helps to find useful predictions from the data. The patterns extracted from data mining techniques are beneficial to provide quality education in educational institutions. In this paper, the student performance is predicted by applying one of the classification algorithms KNN classifiers using the Hadoop platform, which aids to take decisions of knowledge workers such as academic council.**

Index Terms: **KNN Classifier, Data mining, Student, Big data, Academic performance.**

I. Introduction

The Datamining techniques are applied in various fields to extract the previously unknown patterns from the data. The patterns are helpful to gain knowledge by the decision makers. The decisions taken by knowledge worker are useful to improve the business process. The data mining algorithms have proved their usefulness in various application domains, a few to mention, Credit Card frauds, Sports, Health Care, Banking, and Insurance. The data mining techniques are used by researchers in the Educational domain [1] and it is known as Educational data mining. The classification or clustering techniques are used by most of the researchers to know the implicit patterns from the educational data. The Prediction of student performance [2] - [16] or predicting the grades in the subjects is helpful for stakeholders. The above-mentioned techniques are applied in the educational domain to know hidden patterns. Using the patterns, the academic committee can take decisions and implement new methods to improve the quality of education, as well as implement the best practices in the niche areas. The measures taken to improve the quality in academics will be helpful for the institute as well as the industry. The data mining consists of several algorithms for classification and clustering. Classification can be done by using the decision tree, Naive Bayes, support vector machine, neural networks, KNN algorithms. Similarly, clustering consists of different algorithms like Partition based, Density based, Hierarchical, Model-based [20], etc. In this paper, the authors used KNN classification technique for the student data implemented in big data environment using Hadoop and MapReduce.

The main motivation of the paper is to predict the student performance by knowing the grade of the student in Choice-Based Credit System (CBCS) using the KNN classification technique applied in Hadoop MapReduce Platform [22]. The model created by the authors will be of great help in the educational institutions to take appropriate measures to improve the quality of the institute.

Section II consists of Classification models, Section III includes Related work, Section IV consists of the Methodology, Section V consists of Experimental Results and Discussion and Section VI deals with conclusions.

II. Classification Models

The data mining [17] algorithms are broadly classified as supervisory and un-supervisory methods. The supervisory methods are also termed as classification. The classification is a two-step process. The first step is the learning phase of classifier model. The dataset used in the learning phase is called as training data. The training data consists of class label. The model will be built using the training data and one of the classifier algorithms. The model is applied to the test data to assign the class label. There are different classification methods used to compare the classifier accuracy. There are different classification algorithms used to build the model and classify the unknown sample. A few popular algorithms are decision tree induction, Naïve Bayes, Artificial Neural Network, Support Vector Machine, Bayesian Belief Networks, KNN, Rule-based and Regression Analysis.

The Decision tree classification algorithm can be constructed using several algorithms. One of the algorithms used to construct decision tree is C4.5. The C4.5 algorithm is an enhancement of Iterative Dichotomiser (ID3) algorithm to build the decision tree. The most popular Decision tree algorithm C4.5 divides the dataset recursively into subgroups until no subgroup can be divided further or remaining data samples belong to one group. This is the terminating criterion of the algorithm. For dividing the dataset into different subgroups, information gain is used as the measure. The information gain is the most popularly used measure. The other measures used to construct the decision tree are GINI index, Gain ratio, and Chi-square.

Unlike the Decision Tree, Support Vector Machine (SVM) divides [12], [21] the data using hyperplane to minimize the error and optimize the margin. So far, the above two techniques are linear classifier techniques, and there are nonlinear classifier methods, like the brain. Here, the researchers simulate the brain, because of this, it is called as Artificial Neural Networks (ANN). It consists of the learning phase and classification phase using weights, feedback, activation function.

K-Nearest Neighbor algorithm [18], [22] is a non-parametric method of classification. It is also called as instance based or lazy learning algorithm. The data sample can be assigned a class label by most of the nearest neighbors.

The Rule based classification uses IF-Then rules to make the classification. This is also called as antecedent and precedent.

Discriminant Analysis [19] is used to predict the categorical variable. It is useful for classifying the categorical variable. Here linear discriminant analysis is similar to principle component analysis.

III. Related Work

There is an increasing use of classification techniques in Education domain [1] in the last six years. Researchers are applying classification techniques to know the student performance. This study helps to compare the performance of the classification methods and the attribute measures they considered.

Ramaswami M, et.al [2] applied statistical techniques such as F-measure and Receiver Operating Characteristic (ROC) to find the minimum cardinality and high predictive probability by using six filter techniques and comparative study to find features which are more important.

Affendey L.S, et.al [3] collected 2427 data records and applied preprocessing, feature selection of 254 attributes and used different classification algorithms in WEKA data mining tool. They measured the accuracy of different classifier algorithms for the dataset they have considered.

Bhardwaj, K., Pal. S, [4] collected the data from the previous years and employed Bayesian classification algorithm on the student results and predicted student outcome in the examinations. The outcome of the prediction will help the institute to improve the pass percentage and also students' grades.

Bekele, R., et.al, [5] applied the Bayesian approach to predict the student performance of Ethiopian colleges. They have collected 574 samples by performing the survey, and finally, they considered 514 samples by taking the probability factor greater than 0.64. They formed Bayesian belief network to predict performance to improvise learning process.

Osmanbegovic E, et.al [6] applied three supervised algorithms such as Decision Tree, Naïve Bayes, Neural Network based algorithms to predict the student grades in the upcoming examinations and learning accuracy of the students. This helps to improve the results and help the faculty to take appropriate methodology to enhance the student performance. They have implemented the Decision tree algorithm for prediction of student performance such as grades or CGPA. Mladen D et.al [7] built another model to know about the student who completes the graduation.

Ogunde A.O., Ajibade D.A [8] used Iterative ID3 algorithm for student grades of the University of Nigeria. The accuracy of the algorithm is 79.556.

Romero, C, Ventura, S [9], have employed decision tree to find the academic performance and used Chi-square automatic interaction detection (CHAID) to perform the classification.

IV. Methodology

The students academic performance is given considerable importance by various committees inspecting the college, especially in technological institutions. The academic performance of the student is determined by the marks in the internal examinations and the end semester examination. The student performance in each semester is determined by the total marks obtained in each subject and, the cumulative total of subjects and labs in that semester. In the curriculum, there are two internal examinations. The internal examination marks are a combination of three components. These are mid marks, assignment, and attendance. There are two internal examinations and average of the two examinations is awarded as internal marks. The end semester examinations are conducted, and minimum marks must be obtained in the end examination to pass, but the overall marks for passing in each course is 40(internal plus external).

A. Data Preparation and Preprocessing

The data is of three academic years in a subject in the second year I semester of Department of Information Technology of CVR College of Engineering. The data consists of absents marked as AB but modified as zero for experimentation purpose. The data may contain an erroneous value. The incorrect value will be converted to either upper bound or lower bound as preprocessing step.

B. Data Selection

In Engineering, during each semester, the curriculum supports mostly six subjects and two labs with approximately 28 credits. The Object-Oriented programming through Java subject is considered out of the six different subjects. The subject is considered because of its familiarity. The above said subject internal marks are considered with Mid1, Assignment1, Mid2 and Assignment2. The sample training dataset is as shown in Table I.

TABLE I
STUDENT_TRAIN DATASET

Mid1	Mid2	Assign1	Assign2	Grade
12	3	10	10	C
13	13	10	10	B+
5	6	10	10	B+
1	7	10	10	B
9	13	10	10	B
14	13	10	10	A+
3	13	10	10	B
3	4	10	10	F
13	13	10	10	F
2	5	10	10	B
14	17	10	10	S
15	13	10	10	A
15	18	10	10	S
1	1	10	10	F
3	4	10	10	P
1	4	10	10	P
16	15	10	10	S
15	5	10	10	A
15	18	10	10	S
12	4	10	10	F
3	13	10	10	C
4	13	10	10	A
4	13	10	10	A
14	16	10	10	A+
18	16	10	10	S

The above data is sample data of student_train data. The data is useful to build the model. The test data does not contain class label, so we should assign the class label using the model built in the learning or training phase. Table II is the test data without class labels.

TABLE II
STUDENT_TEST DATASET

Mid1	Mid2	Assign1	Assign2
19	19	10	10
19	19	10	8
17	15	8	8
18	14	10	8
16	16	10	9
14	13	10	10
20	19	10	10
19	20	10	10
5	12	10	8
13	15	10	7

C. KNN Classification

The algorithm works by considering number of the class labels in the train data. The dataset that is considered has nine class labels namely, S, A^+, A, B^+, B, C, P, F, AB. So, 'K' is Nine. The nine class labels of the training dataset are used to build the model. The class labels are the grades of the students. The grades are assigned based on the percentage of marks obtained by the student in that subject. The grades are defined as follows:

Grade: – Final Marks obtained in the subject are split into 9 classes : S is > 80% , A+ is >75% and < 80% , A is >70% and <75% , B+ is >65% and <70% , B is >60% and <65% , C is > 50% and <60% , P is >40% and <50%, F is <40%, and AB for Absent.

Now, Euclidian distance is considered as a measure to calculate the distance of the test label with the centers and assign the class label to the test sample by majority voting or nearest neighbor. The test data sample will be assigned the class label by determining which center is the nearest one.

Generalizing Test Phase

1. Determine the value of 'k' (input)
2. Consider the training dataset by storing the model and class labels of the data points.
3. Load the sample of test data points from the testing dataset.
4. Calculate the Euclidian distance amongst the 'k' closest neighbors of the testing data point from the training dataset based on a distance metric.
5. Assign the class label which is nearest to the training dataset to new data point from the test data.
6. Repeat steps 3, 4, 5 until all the data points in the testing data are classified.

The formula to calculate Euclidean distance is as shown in (1),

$$\sqrt{\sum_{i=1}^{n} (xi - yi)^2} \qquad (1)$$

In this manner, it will assign the class label to all the test samples and measure the accuracy of the model.

The above algorithm is implemented in Hadoop Map Reduce environment.

The <key, value> pair of the dataset is assigned to mapper function. The mapper function computes the distance with each class and lists it out. Next in the reducer phase, the first 'k' neighbors in ascending order of the distance measured are considered and the majority vote is taken and the class label is assigned to the test data sample according to the majority vote.

The input and output directories are organized and they are named as traindatafile and testdatafile. Having the files, apply the K-Nearest Neighbor method in a distributed environment of Hadoop by following the algorithms given below to design the Map and Reduce methods for K-Nearest Neighbor.

Algorithm 1 for Mapper Function

- **Procedure** KNN MAPPER Design
- Create key-value pair list to maintain test dataset
- testlist = new testlist
- Load file containing test data file

- load testfile
- Update key-value pair in test dataset
- testlist <= testdatafile
- Open train dataset file
- Open traindatafile
- Load training data points one at a time and calculate distance measure with every test data point
- Distance (traindata, testdata)
- Write the distance of test data point from all the train data samples with their respective class labels in ascending order
- Compare testdatafile with testdata(dist., label)
- Call Reducer
- **End procedure**

Algorithm 2 for Reducer Function

- **Procedure** for KNN Reducer Design
- Load the center value of "k"
- Load testdatafile
- Open testdatafile
- Load testdatafile points one at a time
- Read testdatafile
- Initialize counters for all class label
- Set counters to zero
- Look through top 'k' distances to each data point and increment counter for each class label it belongs
- for i = 0 to k
    - counter++
    - Assign the class label to testdatafile point depending on the highest value
    - testdatapoint =classlabel($counter_{max}$)
- Update outputfile with class label for testdatapoint
- outputfile = outputfile + testdatapoint
- **End procedure**

Thus, the above algorithms, KNN mapper and KNN reducer will assign the class label to each test data point.

V. Results And Discussion

The K-Nearest Neighbor algorithm was implemented on Hadoop cluster Setup, consisting of 4 nodes in CVR College of Engineering lab. One node acts as Name Node and Job Tracker and other three nodes act as Task Trackers and Data Nodes. All the nodes are of Intel Pentium Dual Core G3240 4th Generation, 8GB DDR3 RAM. The operating system is Ubuntu 14.04.4 LTS. The programming for coding the MapReduce is JAVA 1.8.0. Apache Hadoop 2.7.1 and all the nodes are created as a cluster.

The training data points are stored in student_train, and test data points are stored in student_testdata. The data files are copied into the Hadoop Distributed File System (HDFS). The Hadoop MapReduce runs iteratively until all the data points of test file are classified. The process is started with the small dataset and increased to larger dataset and runs multiple times, so as to classify the data points more accurately.

Table III
Student_Outfile

Mid1	Mid2	Assign1	Assign2	Grade
19	19	10	10	S
19	19	10	8	A+
17	15	8	8	A
18	14	10	8	A+
16	16	10	9	A+
14	13	10	10	A
20	19	10	10	S
19	20	10	10	S
5	12	10	8	F
13	15	10	7	C
13	17	10	8	A
14	19	8	8	A+
13	16	10	8	B
13	15	10	8	A

Table III indicates the student grades obtained in the final examination by running the algorithm. Suppose a student gets a grade C or P or F as the class label. The academic council can take appropriate measure to improve the student's academic performance before the examination is really conducted.

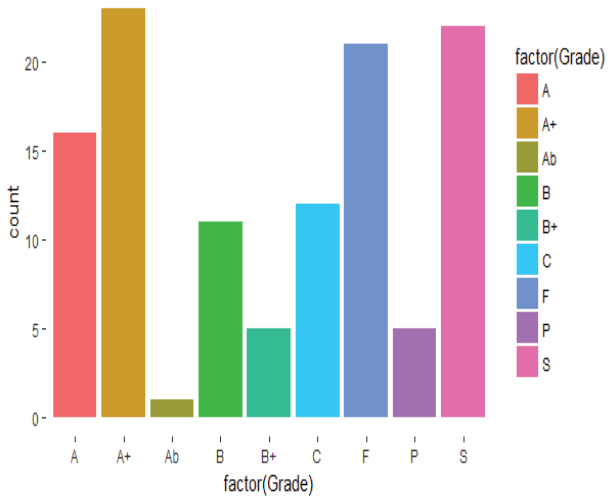

Figure 1. Grades and number of students in each grade

Figure1. indicates the student count in each grade. This also helps the academic council to assess the performance of a class. In the Figure1. the grade 'F' count is 22 and 'C' are 13 students. These grade students can be identified and implement appropriate methods to reduce the count and improve the students' performance.

VI. Conclusions

KNN classification technique is implemented in Hadoop MapReduce environment to classify or predict the class labels of the students appearing for the End Semester Examinations in one subject. By analyzing the result, we can improve the performance of the weak students by mentoring and conducting individual sessions, to pass in the examination, which in turn will help us to take appropriate steps to improve the quality of education in the Institution. The experiment is conducted for only one course of the Second year I semester OOPS through Java subject. But the analysis can be carried out for various other courses where there are more number of failures, as well as, to know the end semester cumulative grade obtained by the student.

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Design and Analysis of Four Stage Progressive Tool for House-wiring Wire Clip

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Abstract: **Progressive tool plays a vital role in sheet metal industries. It can perform various individual operations or combination of operations at two or more stations. In progressive tool design, strip layout design plays a key role. The design of strip layout should be in such a fashion that it can utilize more than 70% of total stock material. This paper describes the design of strip layout, actual cutting load required to perform the operations and based on this load calculation of press capacity and design of die element like thickness of die block, bottom bolster, top bolster and punch plate etc. The software used for modeling of die element is Creo 2.0 and for drafting of assembly drawing is AutoCAD 2016. ANSYS 17.2 is used to perform finite element analysis on blanking punch to ensure the working condition of tool within the limit.**

Index Terms: **Strip layout, progressive tool, press capacity**

I. Introduction

The popularity of Metal stamping process is due to its high productivity, ease in manufacturing of intricate shapes and low cost [1].

Progressive die is known for mass production. This tooling set up consists of one or more dies which can perform multiple operations in single stroke of the press machine. The work is carried forward in subsequent stations in the strip layout. Sheet metal products made by progressive tooling set up can be found inevitably in almost all household and/or industrial components and appliances. [2].

The essential prerequisites to execute first class press work are good operation planning, excellent tool design, accurate tool making and knowledgeable press setting [3].

Design of right tool holds the key to costing of the whole tooling set up. A costly tool will increase the cost of the manufactured component. It is important to keep the tooling cost low without sidelining the quality of the tool [4].

Progressive die design is an art rather than a science. The tooling design is decided based on individual designer's skill and knowledge which are acquired through working experience [5].

During the die design, the first step is to generate punch layout which indicates the optimum layout of the punches. This optimum layout is helping to avoid the clashes between punches and die buttons. None of the piercing operations can appear after scrap removal operation. The space between two punches should be enough to give die wall strength [6].

Wire clip has high consumption for demonstration to 1st year students in *'House wiring workshop' at CVR College of Engineering.* So, it produces a four stage progressive tool designed and analysis conducted on die elements like blanking punch. The 3D CAD model of the wire clip is shown in figure 1.

II. Component Details

The progressive die is to be designed for house-wiring wire clip of galvanized sheet. The following details shown in table 1 like area of component, volume of component have obtained from CAD software.

TABLE I.
COMPONENT DETAILS

Material	CPMnS based galvanized steel-Grade 33 [7]
Thickness	0.3 mm
Shear strength (kg/mm2)	35 kg/mm2
Area of the component	367 mm^2
Volume of the component	111 mm^3

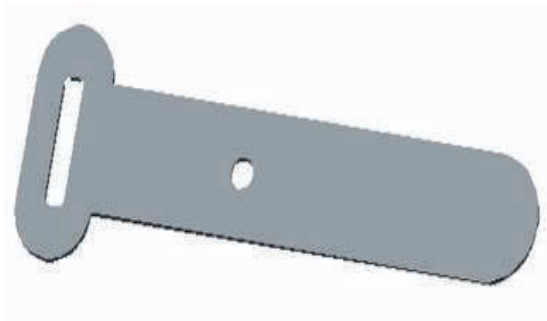

Figure 1. 3D CAD model of the wire clip

III. Strip Layout Development And Shear Force Calculation And Press Capacity

Development of strip layout is the primary task for designing of progressive tool. It represents the operations to be carried out at subsequent stations [8].

A. Strip Layout

A = Back scrap = Front scrap = sheet thickness = 1mm
B = Bridge scrap = 1mm
Width of the stock = 53mm
Pitch = Advance = B + L = 18 mm

Equation 1 shows the percentage utilization of the stock strip. The development of strip layout is shown in figure 2.

B. % Stock strip utilization (n)

Strip layout has to developed in such a way that stock strip utilization is maximum. It will save appreciable amount of stock material and tooling expenses.

$$n = \frac{Area\ of\ blanks\ X\ no\ of\ rows}{Area\ of\ strip\ per\ pitch} \times 100 \quad (1)$$

= Area of strip per pitch = Advance x stock width
= 18 x 53 = 954 mm^2
$= \frac{367\ X\ 2}{954} = 76.94\ \%$

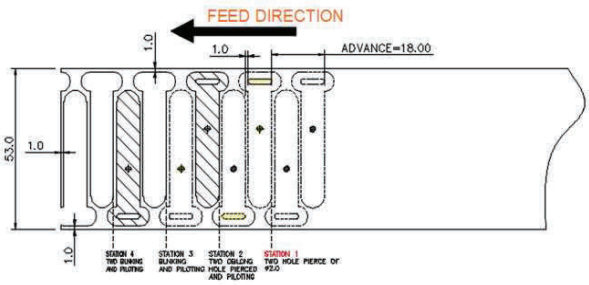

Figure 2. Development of the strip layout

As shown in figure 2, from the right hand side, at station 1 two holes are pierced. At station 2 oblong holes are pierced. Two blanking of two wire clip profiles are blanked at 3 and 4 station to have maximum stock utilization.

C. Shear Force calculation in Tons (T)

Equation 2 shows the shear force for cutting in tons (T) [8].

Shear force, $F_{sh} = \frac{K \times L \times t \times S_{sh}}{1000}$ T (2)

S_{sh}= Shear strength of the stock material = 35 kg/mm^2
Stock Thickness, t = 0.3mm
K= Factor of safety = 1.4
L = Total cutting perimeter in mm

A. Perimeters of the contours at each stage:

1) At station 1

The perimeter of the two piercing hole of diameter 2 mm is given by

Perimeter, P_1= 12.6 mm

2) At station 2

The perimeter of the two oblong hole is given by

Perimeter, P_2 = 31.6 mm

3) At station 3

The perimeter of the contour to be blanked is given by

Perimeter, P_3 = 98 mm

4) At station 4

The perimeter of the second contour to be blanked is given by

Perimeter, P_4 = 98 mm

Total cutting perimeter, L = $P_1 + P_2 + P_3 + P_4$
= (12.6 + 31.6 + 98 + 98)
= 240.2 mm

$F_{sh} = \frac{1.4 \times 240.2 \times 0.3 \times 35}{1000} = 3.54$ T

D. Press Capacity (Pc):

Equation (3) is for Calculating the press capacity which will be in Tons (T).

The Total press capacity is 25% more than the total tonnage calculated

Pc = Total Tonnage x 1.25 (3)
= 3.45 x 1.25 = 4.3 T

Since 4.3 T press not available in market, so 10 T press can be use for production of wire clip.

E. Ejection force (F_{ej})

After shearing, the sheet metal get stuck in the land provided in the die hole. The stuck material is called slug which has to be ejected by applying ejection force. Equation 4 shows the calculation for ejection force [9].

Ejection force, $F_{ej} = 0.1 \times F_{sh}$ (4)
= 0.1 × 3.54 = 0.36 T

IV. Development Of The Progressive Tool

A. Clearance (C)

Equation 5 shows the calculation for clearance to be given between die and the punch for shearing [8].

$C = 0.005 \times t \times \sqrt{F_{sh}}$ (5)
$= 0.005 \times 0.3 \times \sqrt{3.6}$
= 0.003 mm per side

B. Die Block Design

Equation 6 shows the thickness of the die which is also known as the female member of the tool [8].

a) Thickness of the die (T_D)in mm

$T_D = \sqrt[3]{F_{sh}} \times 10$ (6)
$= \sqrt[3]{3.6} \times 10$
$= 15.33 \approx 18.5$ mm

b) Land and draft

The straight portion of die opening is known land and the intentional amount of tapper in die opening immediate after the land in downward direction is known draft. If draft is not given, internal stress in the punch will cause crack in the die block. The standard value of land is
3 mm or three times of sheet thickness, when sheet thickness is less than 1mm then land is 3mm, while three times of sheet thickness is used when sheet thickness more than 1mm and draft angle is 1/2°.

c) Thickness of Bottom and Top Bolster

Equation 7 and equation 8 show the calculation for calculating the thickness of the bottom bolster and top bolster of the die set respectively [9].

Thickness of bottom bolster, $T_{BB} = 1.75 \times T_D$ (7)
$= 1.75 \times 15.5 = 27.125 \approx 28$ mm

Thickness of Top bolster, $T_{TB} = 1.25 \times T_D$ (8)
$= 1.25 \times 15.5 = 19.375 \approx 20$mm

d) Stripper plate design and Punch Plate

Scrap material cling to the punch and during return stroke it try to lift along with punch. Stripper plate is used to strip the scrap material from the punch.

There are two types of stripper plate i.e fixed stripper plate and floating stripper plate. When the stock thickness is less than 1 mm, floating striper is used which is holding the stock against die surface tightly during cutting.

Equation 9 and equation 10 show the calculation of the thickness of the stripper plate and punch plate respectively.

Thickness of the stripper plate, $T_{ST} = 0.5 \times T_D$ (9)
$T_{ST} = 0.5 \times 15.5 = 7.75 \approx 8$mm

Thickness of the punch plate, $T_{PP} = 0.5 \times T_D$ (10)
$T_{PP} = 0.5 \times 15.5 = 7.75 \approx 8$mm

V. Centre Of Pressure

During blanking of irregular shape, the summation of forces at both the side of the ram varies which results in bending moment in the pressing ram. This causes undesirable deflections and misalignment. It is predominant in progressive tool to find a point where the summation of forces is symmetrical. This point is called Centre of Pressure. It is important that the centre of pressure lies on the axis of the ram. This is also known as load centre where the shank is to be fitted [9].

Figure 6 is showing all the dimensions for load center of all cutting profile from X-axis and Y-axis. Equation (11) and equation (12) are showing the location of center of pressure from X-axis and Y-axis respectively.

Calculation of distance X in mm of the center of pressure from the axis Y-Y by the formula

$X = (L1 \times X1 + L2 \times X2 + L3 \times X3 + \ldots) / (L1 + L2 + L3 + \ldots)$

$$X = \frac{\sum Li \times Xi}{\sum Li} \quad (11)$$

Calculation of distance Y in mm of the center of pressure from the axis X-X by the formula

$Y = (L1 \times Y1 + L2 \times Y2 + L3 \times Y3 + \ldots)/(L1 + L2 + L3 + \ldots)$

$$Y = \frac{\sum Li \times Yi}{\sum Li} \quad (12)$$

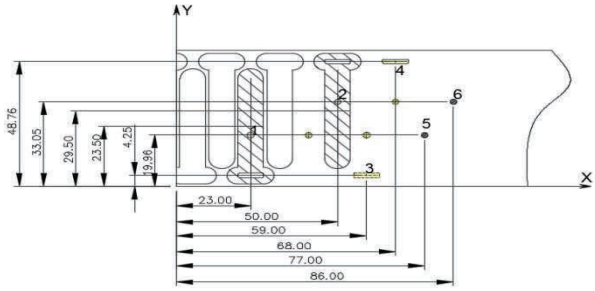

Figure 3. Co-ordinate dimension of cutting profile

Following equations (13), (14) and (15) are the load calculation according to serial number of figure (3) at different stations.

At 1 Load $L1 = \frac{L \times t \times S_{sh}}{1000}$ Tons $= \frac{98 \times 0.3 \times 35}{1000} = 1.1T$ (13)

Load at 2 is similar to L1, both have same profile.

At 3 Load $L3 = \frac{L \times t \times S_{sh}}{1000}$ Tons $= \frac{15.8 \times 0.3 \times 35}{1000} = 0.2T$ (14)

Load at 4 is similar to L3, both have same profile.

At 5 Load $L5 = \frac{L \times t \times S_{sh}}{1000}$ Tons $= \frac{6.3 \times 0.3 \times 35}{1000} = 0.1T$ (15)

Load at 6 is similar to L5, both have same profile.

TABLE II.
CALCULATION OF CENTER OF PRESSURE

Serial Number	Load, L T	Distance, X(mm)	Distance, Y(mm)	X_i x L_i	Y_i x L_i
1	1.1	23	23.50	25.3	25.85
2	1.1	50	29.50	55.0	32.45
3	0.2	59	4.25	11.8	0.85
4	0.2	68	48.76	13.6	9.752
5	0.1	77	19.96	7.7	1.996
6	0.1	86	33.05	8.6	3.305
Total	∑Li			∑(Xi x Li)	∑(Yi x Li)

From table 1, ∑Li, ∑ (Xi x Li), ∑ (Yi x Li) are 2.8, 122 and 74.203 respectively.

Distance of load from X axis, $X = \frac{\sum(Xi \times Li)}{\sum Li} = \frac{122}{2.8}$
$= 43.6$ mm

Distance of load from Y axis, $Y = \frac{\sum(Yi \times Li)}{\sum Li} = \frac{74.203}{2.8}$
$= 26.5$ mm

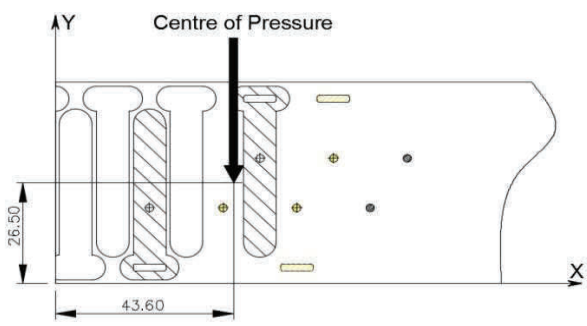

Figure 4. Location of center of pressure

Figure 4 represents the location of center of pressure for shank mounting.

VI. Finite Element Analysis Of The Punches

A. Results for Blanking punch

The stress, strain and total deformation of the blanking punch which is developed due to cutting force has found by the use of Finite element analysis (FEA). The type of element chosen is tetrahedron (10 nodes) and element size is 5mm shown in figure 5.

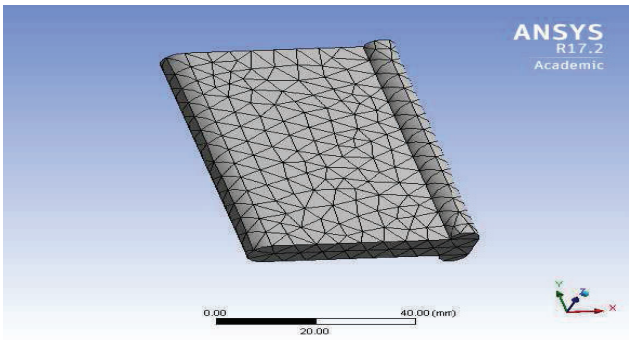

Figure 5. Meshing of the blanking punch (Tetrahedron 10-nodes)

The boundary condition and load application on blanking punch is shown in figure 6 and figure 7 respectively.

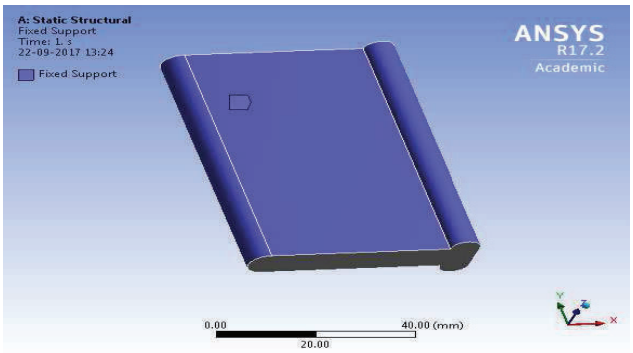

Figure 6. Constraint- fixed support

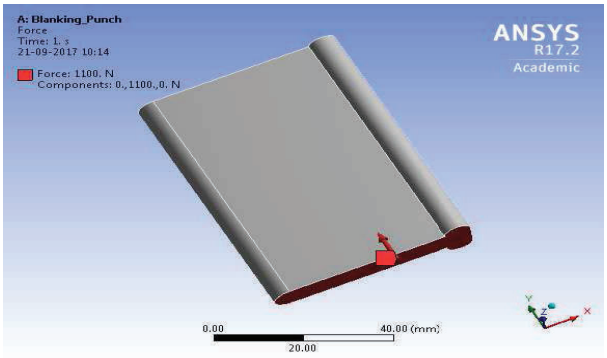

Figure 7. Cutting force applied on cutting face of blanking punch

The results of analysis for blanking punch are shown in figure 8 to figure 10.

Force required for blanking as calculated in equation (13) is 1.1T or 1100N.
Cutting area of the blanking punch = 252.82 mm^2 (Area obtained from CAD software)

The analytical calculation for the stress develop in the blanking punch is as follows

Stress developed (σ_1) in blanking punch in N/mm^2

$$\sigma_1 = \frac{Force\ required\ for\ blanking\ punch}{Cutting\ area\ of\ the\ blnking\ punch} = 4.351\ N/mm^2$$

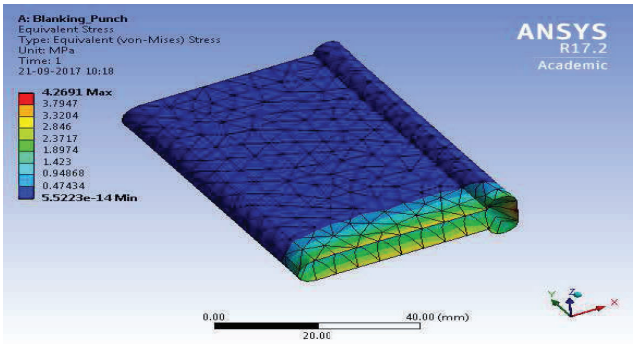

Figure 8. Von-Mises stress developed in the blanking punch

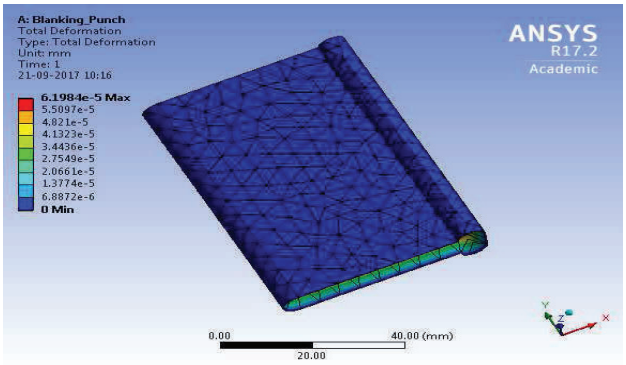

Figure 9. Total deformation occurred in the blanking punch

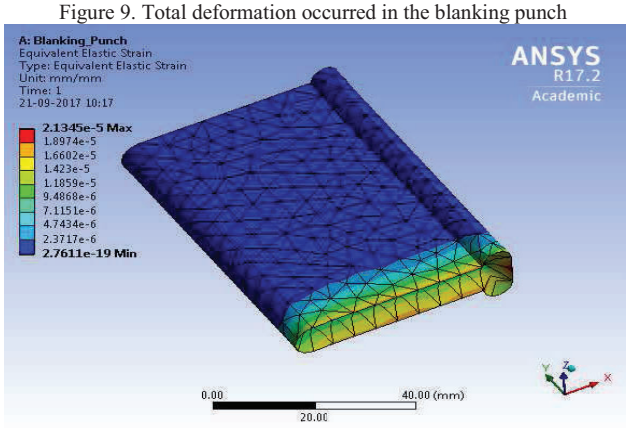

Figure 10. Equivalent Elastic (Von-Mises) strain in blanking punch

B. Results for Piercing punch

The type of element chosen for piercing punch and oblong punch is tetrahedron (10 nodes) and element size is 2.5mm shown in figure 11 and figure 17 respectively.

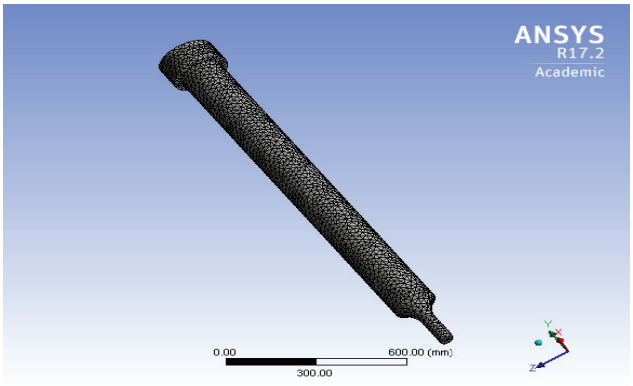

Figure 11. Meshing of the piercing punch (Tetrahedron 10-nodes)

The boundary condition and load application on piercing punch is shown in figure 12 and figure 13 respectively.

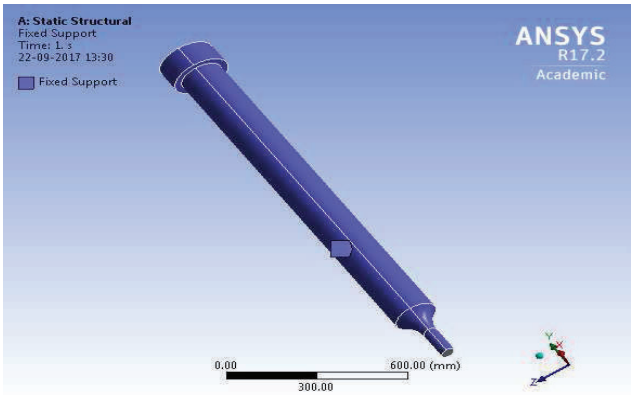

Figure 12. Constraint- fixed support

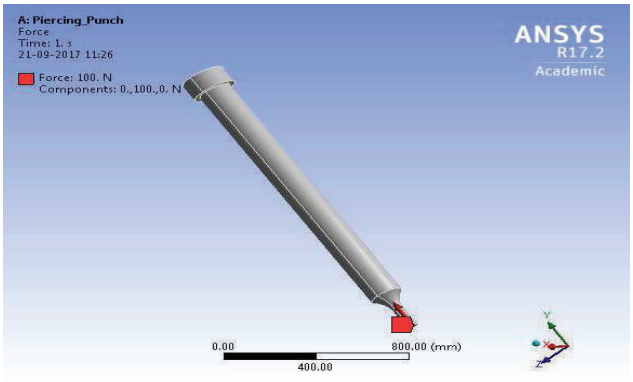

Figure 13. Cutting force applied on cutting face of piercing punch

The results of analysis for piercing punch are shown in figure 14 to figure 16.

Force required for piercing as calculated in equation (14) is 0.1T or 100N.
Cutting area of the piercing punch = 3.142 mm^2 (Area obtained from CAD software)

The analytical calculation for the stress develop in the blanking punch is as follows

Stress developed (σ_1) in blanking punch in N/mm^2

$$\sigma_1 = \frac{Force\ required\ for\ blanking\ punch}{Cutting\ area\ of\ the\ blnking\ punch} = 31.83\ N/mm^2$$

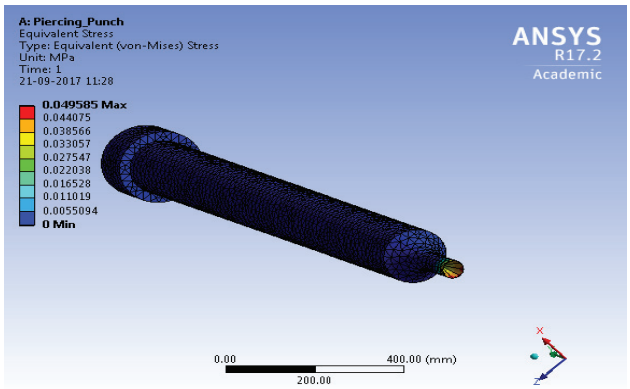

Figure 14. Von-Mises stress developed in the piercing punch

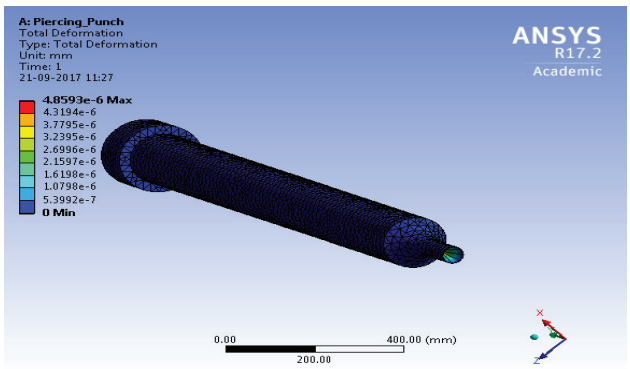

Figure 15. Total deformation occurred in the blanking punch

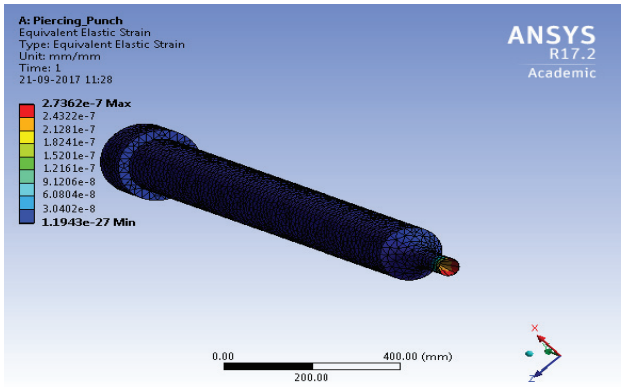

Figure 16. Equivalent Elastic (Von-Mises) strain in piercing punch

C. *Results for Oblong punch*

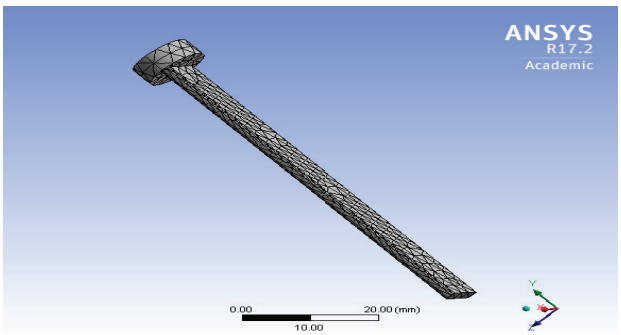

Figure 17. Meshing of the oblong punch (Tetrahedron 10-nodes)

The boundary condition and load application on piercing punch is shown in figure 18 and figure 19 respectively.

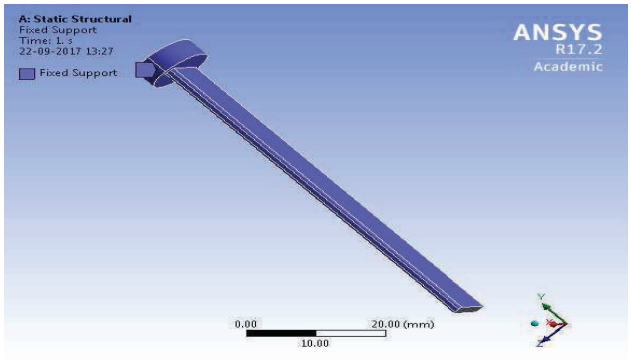

Figure 18. Constraint- fixed support

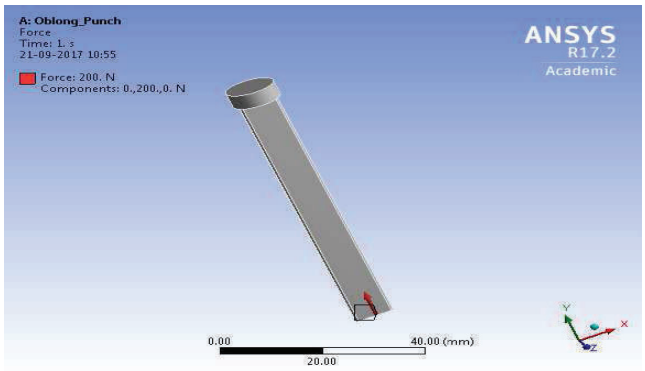

Figure 19. Cutting force applied on cutting face of oblong punch

The results of analysis for piercing punch are shown in figure 20 to figure 22.

Force required for oblong piercing as calculated in equation (15) is 0.2T or 200N.
Cutting area of the oblong punch = 11.89 mm^2

The analytical calculation for the stress develop in the blanking punch is as follows

Stress developed (σ_1) in blanking punch in N/mm^2

$$\sigma_1 = \frac{Force\ required\ for\ blanking\ punch}{Cutting\ area\ of\ the\ blnking\ punch} = 16.821\ N/mm^2$$

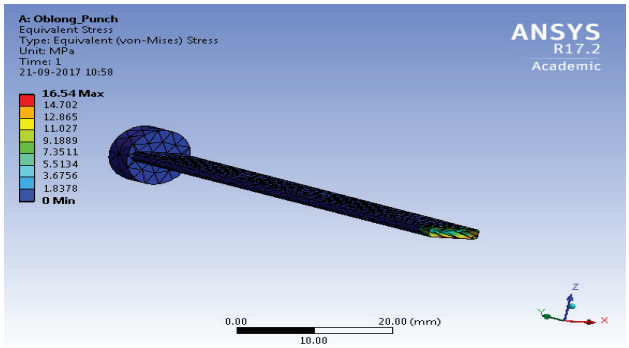

Figure 20. Von-Mises stress developed in the oblong punch

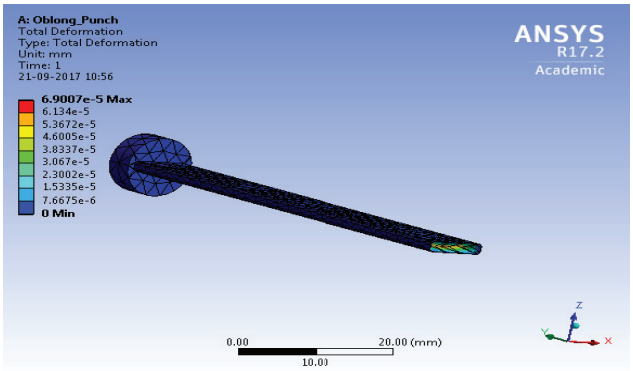

Figure 21. Total deformation occurred in the oblong punch

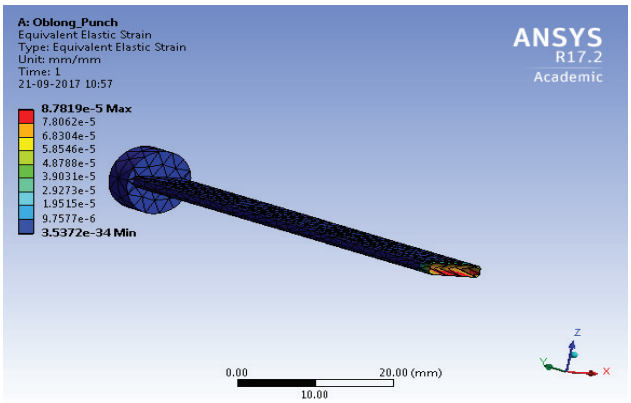

Figure 22. Equivalent Elastic (Von-Mises) strain in oblong punch

VII. Results And Discussions

The results of obtained from finite element analysis and analytical method is tabulated in table II.

Table III.
Results and Remarks

Serial number	Punches	Maximum Stress developed obtained through ANSYS	Total deformation obtained through ANSYS	Maximum strain developed (mm/mm) obtained through ANSYS
1.	Blanking punch	4.2691 MPa	6.1984×10^{-5} mm	2.1345×10^{-5}
2.	Piercing punch	0.049585 Mpa	4.8593×10^{-6} mm	2.7362×10^{-7}
3.	Oblong punch	16.54 Mpa	6.9007×10^{-5} mm	8.7819×10^{-5}

The material of punches is high carbon high chromium steel (D2 steel). Yield strength of D2 steel is 2200 Mpa [10] and the results obtained from both ANSYS is less than the yield strength of the material. Hence, the material will not fail in the required working condition. The centre of pressure for shank mounting is on X and Y axis 43.6mm and 26.5mm respectively.

This paper has completed most part for the design of a progressive tool. This tool has been designed for in-house manufacturing of tool for wire clip. Students can conduct experiments on same in production technology laboratory. The same components i.e. wire clip can be used by the

students for "house wiring" module in workshop practice session.

VIII. Final Assembly

The orientation of punches, pilots and final assembly of the progressive tool is shown in figure 23 and figure 27 respectively.

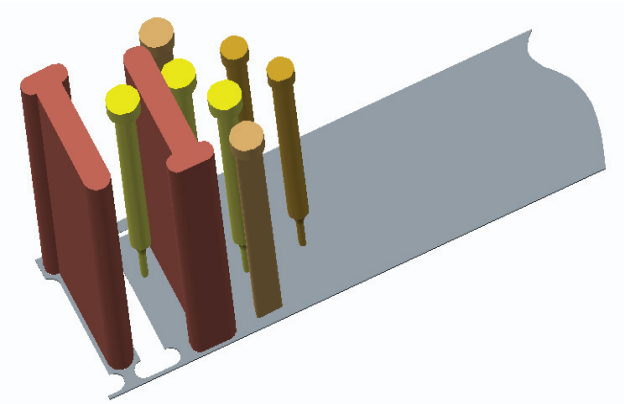

Figure 23. Orientation of punches and pilots for progressive tool

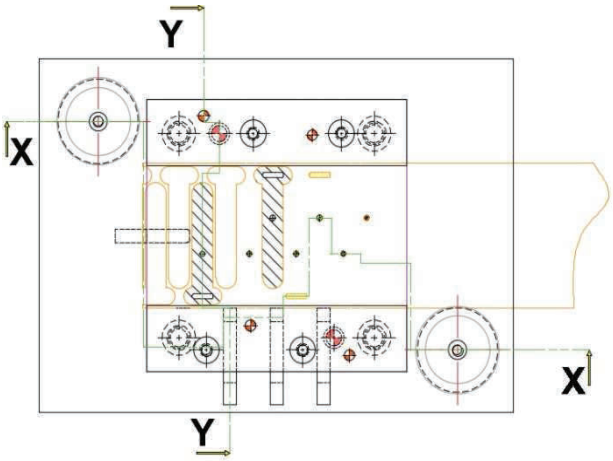

Figure 24. Bottom assembly of the progressive tool

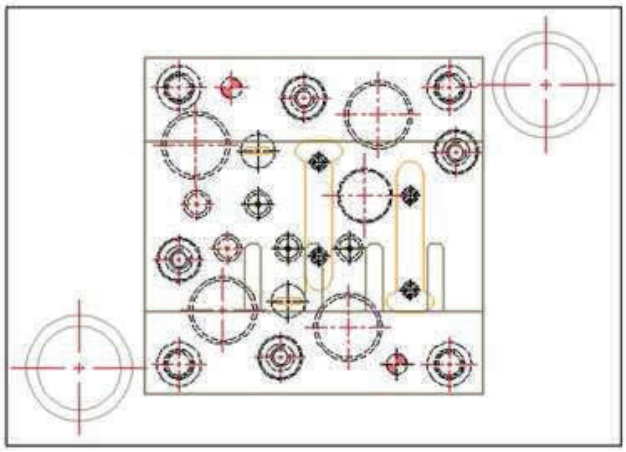

Figure 25. Top half assembly (inverted view) of the progressive tool

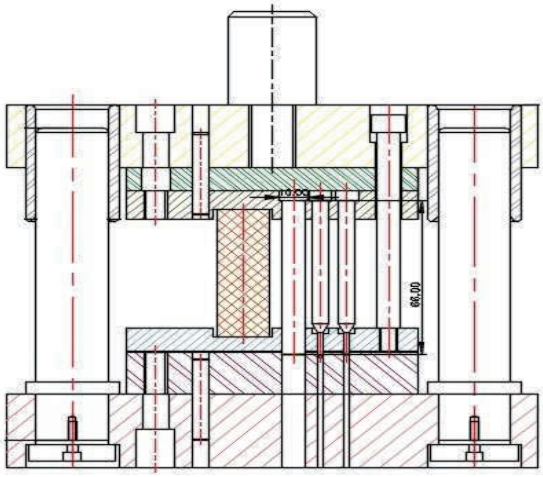

Figure 26. XX-Sectional view of the progressive tool

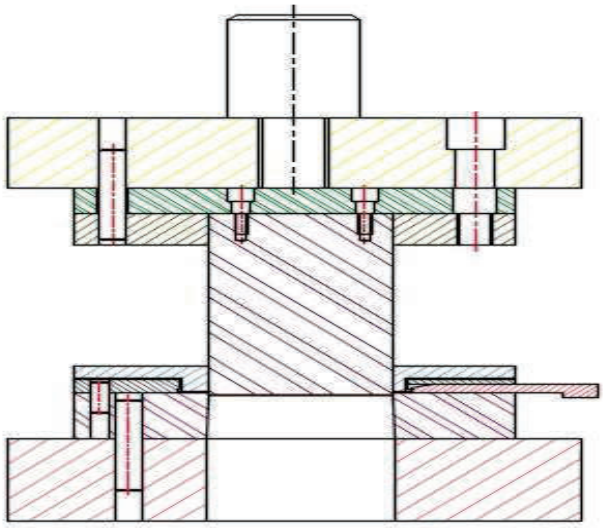

Figure 27. YY-sectional view of the progressive tool

IX. Conclusions

In this paper, a four stage progressive tool wire clip is designed, modeled, analyzed and drafted. Modeling has done in Creo2.0. Analysis has done in ANSYS 15.0 and Drafted in AutoCAD 2016. Strip layout for maximum stock strip utilization is developed. Stock strip utilization achieved is approximately 77 %. Further, finite element analysis for maximum Von-Mises stress and deformation is carried out on the punches using ANSYS 17.2 for validating the design. The results obtained are well within the limit. The press capacity obtained is of 10 T. The moment generation due to cutting force during cutting stroke will be negligible as location of centre of pressure locate the shank, which will fixed onto the ram of press machine in same axis.

Currently, the wire clip component is purchased from commercial stores in the market. By studying the component profile and its method of manufacturing, it is understood that the component is produced by simple single stage tool due which the concentricity in the profile of the component is missing out. To overcome it, progressive tool for its manufacturing is designed so that good profile concentricity can be maintained and finally the cost of component per piece can be reduced as compared from the previous method of manufacturing.

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Design and Crash Analysis of a Passenger Car using ANSYS Workbench

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Abstract: **In this paper, an automobile (car body structure) was designed and analyzed which can be used for travelling of the passengers and goods. The car body structure is made of aluminum and the crash analysis is performed on the car body structure to know how the car body structure deforms in a crash accident. Crash analysis is performed on car body designs for ensuring safety of passengers in accidents. A detail car body deformation analysis has been performed in ANSYS based on 3D LS-DYNA. A frontal impact crash of a car is performed. A Finite Element model of a car structure was used in a crash simulation to assess the safety and to know crashworthiness of the car.**

Index Terms**: Crash analysis, Crashworthiness, ANSYS, LS-DYNA.**

I. Introduction

A car is a wheeled, self-powered motor vehicle and a product of the automotive industry which is mainly used as transportation. Cars are constructed primarily for transportation of people rather than goods, which generally have seating for one to eight people. Cars are mainly designed to run on roads, which typically have four wheels with tyres. Automobiles can be classified by size or weight. Size classification of an automobile is based on wheelbase and weight classification of an automobile is based on curb weight.

Andrew Hickey et al. [1] has performed a quasi-static simulation, to simulate the car crash by using finite element method (FEM). Safety of passengers is one of the most important design considerations in the automobile community. Therefore, a crash test is a crucial step to validate the car design. Experimental crash tests results in higher cost, and acquired data might not be correct. Therefore, a numerical modelling and the simulations are used for studying a car crash than to perform experimental testing. Hence, a powerful numerical tool, FEM plays a crucial role in crash test simulations.

C. Sadhasivam et al. [2] has performed a detail car body mode analysis and stress analysis based on 3D LS-DYNA in ANSYS. Modal analysis has been performed to know the natural frequencies and mode shapes of a car body structure. Vibration and crash analysis of the car body is performed, which includes dynamic, static and crash analysis. Most of the automobile manufacturers generally prefer lightweight materials to reduce weight and these include composites, aluminium, magnesium or new types of high strength steels. These materials have a limited strength or ductility, in case of rupture which is a most common seen phenomenon during a crash accident. Material joining failure is also one of the consequences on the vehicle crashworthiness. In a car crash, front-part of the automobile structure absorbs a lot of impact and undergoes plastic deformation. Most of the vehicles are designed to increase the absorption efficiency, to enhance the safety of passengers and reliability of the vehicle. Crashworthiness of different parts of a vehicle needs to be evaluated at the initial stage of the vehicle design only. The dynamic behaviour of a structural member is always different from the static behaviour, therefore crashworthiness of the vehicle can be known by impact analysis. Hence, it is necessary to check the crash ability of car structure for both safety and fuel economy. The two ways of ensuring safety are by performing a crash test of a car or by simulating the crash analysis of the modelled car structure in analysis software.

Byeong Sam Kim et al. [3] has performed a crash analysis of sub frame and upper body for neighborhood electric vehicle (NEV). NEV's front platform assembly behaviour was simulated in LS-DYNA and results were observed when it is subjected to a frontal car crash. The safety of passengers at low cost reduction has been researched. When a vehicle crashes, the passengers inside the vehicle must be free from injury and the vehicle must be able to withstand impact loads. In crash accidents, capability of the vehicle structure to absorb the energy can be defined as crashworthiness. The vehicle structure should be designed to withstand higher speed and the passengers should not experience a net deceleration.

Lin et al. [4] had performed the computer simulation of a car crash analysis. They have analysed two crash situations: a higher speed car crashing into a wall and a high velocity car crashing into a static car. The objective of the research was to know the sources which can harm the driver and the passengers when car accidents occur and to create a model of a bumper for knowing its potentiality to withstand impact loads on it. The Simulations on bumper are performed to assure that the bumper design meets the safety requirements.

Tejasagar et al. [5] has studied different car crash simulations by using computer softwares because to reduce automobile developing time and to reduce the cost of manufacturing. A frontal impact crash analysis of a car was

researched, which made an impact on car crashworthiness. Crash test is one of the destructive tests performed on the car for ensuring safer design in crashworthiness and to know the crash compatibility of automobiles. The vehicle manufacturers perform different crash tests to ensure safety of the cars under various conditions such as various types of crashes, from different sides, different angles and with different objects, including other vehicles.

Praveen et al. [6] has performed a car crash analysis in non-linear transient dynamics. In the crash test, frontal collision and sideways collision analysis is performed to know deformations of the car. Crashworthiness of the car simulations is performed in Finite Element Analysis (FEA). The chassis frame takes the loads of a heavy vehicle, its function is to carry the loads on the vehicle safely for each operating condition. The frame of chassis should be able to support different chassis components and vehicle structure. Chassis frame should withstand both static loads and dynamic loads without any distortion or deflection in the vehicle. The frontal collision and side collision conditions are tested on the generated model, the total deformations and stresses developed are determined.

Saeed Barbat et al. [7] has modelled a car to evaluate the effects of design variables on dummy responses for front-to-side vehicle crash analysis. The striking or hitting vehicle was selected to be a SUV while the struck vehicle was a small size passenger car which consists of four seats. A deterministic approach that allowed analytical prediction equations for dummy responses was generated. A baseline front crash vehicle to the side crash was modelled in FE and correlated to a physical front crash to the side crash.

Ravinder Reddy et al. [8] has performed a crash analysis on the passenger car frontal bumper beam by using Hypermesh and RADIOSS software. A bumper is used for passenger's protection from both front and rear collisions. Bumpers are used for absorbing impact energy. Design of a bumper is based on the degree of absorbing impact loads. The analysis is performed on the bumper beam model with different materials and different designs of the bumper. The analysis was done against a fixed wall with different materials of bumper. Behaviour of the bumper in crash simulations is observed and modifications are done in the design of bumper. The materials of bumper used for crash test analysis are carbon fibre composite, E-Glass epoxy and aluminium 6063-T6.

Xinping Song et al. [9] has performed a car crash analysis in FEM. The front collision of crash test was simulated in the LS-DYNA software and car model is designed in Hypermesh software. The longitudinal front beam is used for absorbing the kinetic energy during crash test of the vehicle. The longitudinal front beam can efficiently absorb the kinetic energy and avoid high acceleration of the car. The acceleration time history curves and the deformations of the car during the crash test were analysed. From the results, anti-impact capacity of the car is observed. These simulation results show that optimization of the car structure can improve the results in the car crashworthiness, but further improvements are necessary in the car structure for the safety of passengers. Selecting the correct material of the car in the vehicle collision experiment, will influence the results.

A. Types of Car Body Structures

The car body structures vary from country to country. The different car names are given to different car models based on the technology used, utility, customization and design. General car body styles used in India are given below:

1. Convertible
2. Hatchback
3. Wagon
4. Sedan
5. Jeep
6. MUV/SUV
7. Van
8. Coupe

A hatchback model of the car is modelled in CAD software and crash analysis is performed on the car model in ANSYS software.

B. Material Used For Car and Wall

Aluminium material is widely used for car body structures because it is corrosion resistant, ductile, has a high electrical conductivity and is a soft material compared to other available engineering materials. It is one of the lightest engineering metals available in nature, which has a superior strength to weight ratio when compared with steel. Therefore, aluminium is suited as the material for car body, and concrete is taken as the wall material. The properties of aluminium and concrete material are shown in Table 1.

TABLE I.
PROPERTIES OF ALUMINIUM

S. No	Properties	Aluminium	Concrete
1.	Density (g/cm^3)	2.70	2.35
2.	Young's Modulus (GPa)	70	33
3.	Poisson ratio	0.35	0.2
4.	Shear modulus (GPa)	26	16
5.	Bulk modulus (GPa)	76	18
6.	Thermal Conductivity (w/mK)	205	0.8

II. MODELLING AND ANALYSIS

A. Assembled Model

A car body outer part is modelled by using different commands in SOLIDWORKS software. After creating the car model, another car model is placed exactly opposite to the first car structure at a distance of 10 m as shown in Fig. 1.

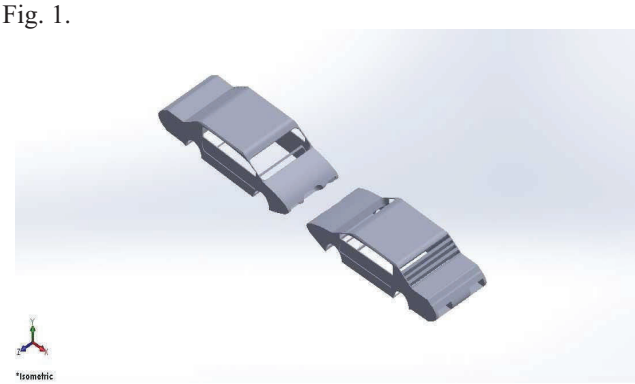

Figure 1. Assembling of the car structures.

The outer part of a car body and the wall are modelled in SOLIDWORKS software and are placed exactly opposite to each other at a distance of 10 m as shown in Fig. 2.

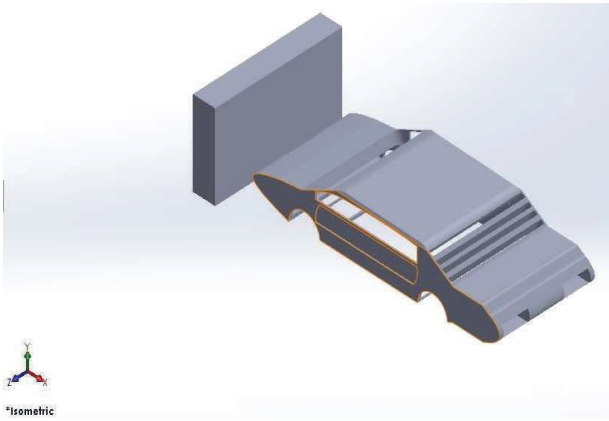

Figure 2. Assembling of the car and wall.

B. Element Type

The element type used is SOLID 186. SOLID 186 is a higher order 3-D with 20-node having three degrees of freedom per node, solid element that exhibits quadratic displacement behaviour. This element supports large deflection, plasticity, large strain capabilities, hyper elasticity, stress stiffening, and creep.

C. Meshing

After assigning the element type of the car structure, the solid model is converted into the IGES format and imported into ANSYS Workbench. Meshing is an important process of an analysis and it should be performed on the car structure. Meshing is the process of dividing the created model in number of divisions or elements which consists of nodes. By applying meshing process, we can determine the efficiency and effectiveness of any analysis. An automated mesh generation is as shown in Fig. 3.

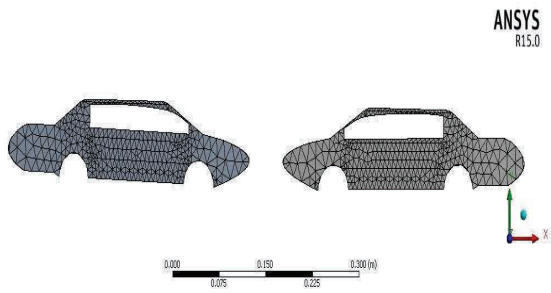

Figure 3. Applying mesh on the car structures.

Meshing is applied by using automatic mesh. Under mesh sizing, mesh was set to fine mesh to achieve accurate and precise results. Rather than using a fine mesh all over the components, coarse mesh was used on large area and fine mesh was used at the area of stress concentration as shown in Fig. 4.

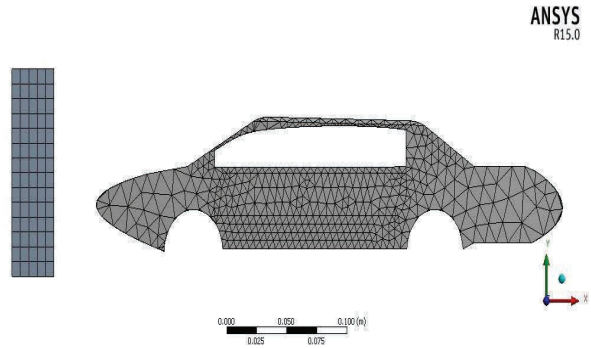

Figure 4. Applying mesh on the car and wall.

D. Applying Loads

In the analysis setting, a velocity of 1000 m/s is assigned to the car structure in X-direction and the end time is 0.001 seconds as shown in Fig.5

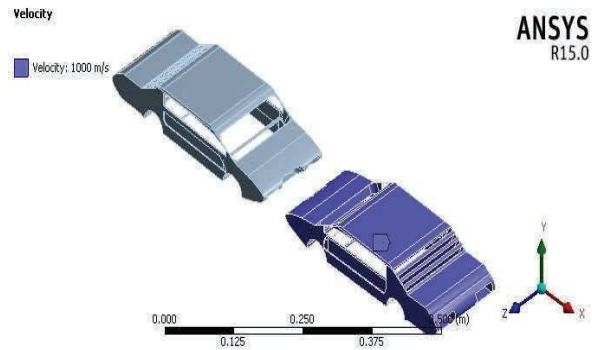

Figure 5. Assigning velocity of 1000 m/s to the car structure.

In the analysis setting, a velocity of 1000 m/s is assigned to another car structure in X-direction such that car to car collision would take place and the end time is 0.001 seconds as shown in Fig.6.

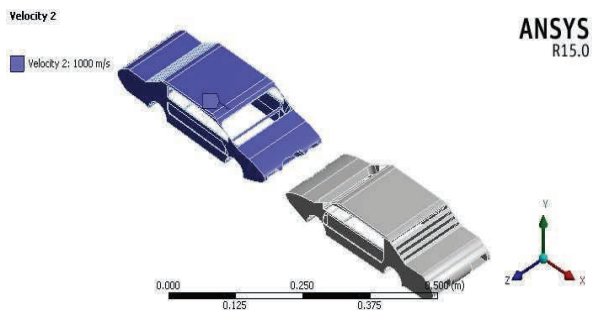

Figure 6. Assigning velocity of 1000 m/s to another car structure.

In the analysis setting, fixed support is applied to the concrete wall, so that the wall is constrained in all degrees of freedom and it would withstand different types of loads as shown in Fig.7.

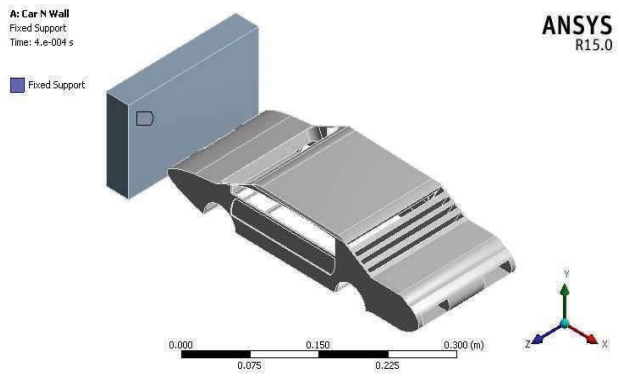

Figure 7. Fixing the wall.

In the analysis setting, a velocity of 1500 m/s is assigned to the car structure in the X-direction so that the car would hit the wall as shown in Fig.8.

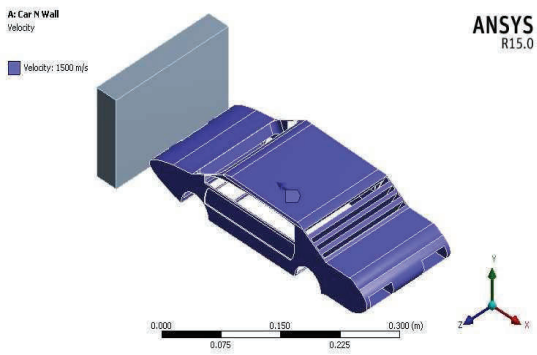

Figure 8. Assigning velocity of 1500m/s to the car structure.

III. Results And Disscussions

After assigning velocity to car structures and fixing the wall, crash analysis is performed in ANSYS workbench and the following results were observed in crash analysis.

A. Total Deformation of Car to Car

After performing crash analysis of one car hitting another car with a velocity of 1000 m/s, a maximum total deformation of 0.09 m and minimum total deformation of 0.03 m is observed from the Fig.9.

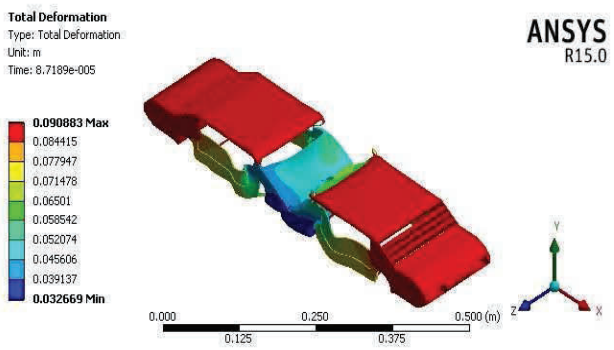

Figure 9. Total deformation of the car to car.

B. Total Deformation of a Car to Wall

After performing crash analysis of the car hitting the wall with a velocity of 1500 m/s, maximum total deformation of 0.33 m and minimum total deformation of 0.03 m is observed in the car from the Fig.10.

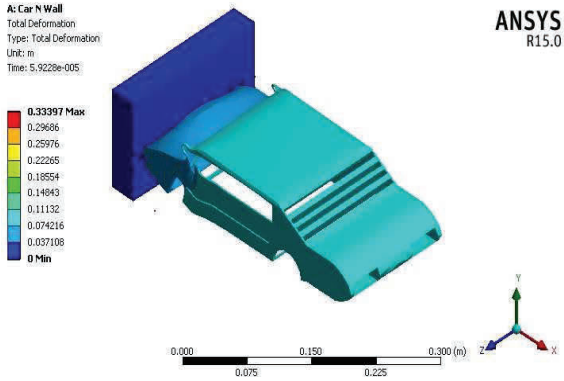

Figure 10. Total Deformation of the car hitting the wall.

IV. Conclusions

In this paper, a car structure is modelled in SOLIDWORKS, a crash analysis of one car to another car with the initial velocity of 1000 m/s and car to wall with the initial velocity of 1500 m/s is performed in ANSYS software. The total deformation of the car structure is analyzed. From the results, it is observed that the maximum deformations in car structures crashing a car and wall are within the limits. Therefore, the modelled car structure is safe for the passengers to travel in view of car accidents.

In the future scope, different car body structures can be modelled and different car body materials can be taken by assigning different velocities for crash analysis.

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Experimental Analysis on Nano-based Phase Change Material for Cooling Applications in Tropical Buildings

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Abstract: **The main aim of the investigation is to develop new nano-based PCM (phase change materials) establishing thermal energy storage for catering cooling needs in tropical buildings. PCM's lag with their thermal properties like thermal conductivity, latent heat of capacity etc. To enhance its properties generally, nanoparticles are dispersed in PCMs. The present work deals with the synthesis of TiO_2 nanoparticles using sol-gel chemical method and characterizing particle size, shape and its morphology. The as-prepared TiO_2 nanoparticles were dispersed with different wt. % in Rubitherm 21 type PCM. Then, nano based PCM's were tested for its melting, freezing, latent heat characteristics and concluding for compact ability with building applications to cater cooling needs.**

Index Terms: **Phase Change Materials, Nano particles, Thermal Energy Storage, Buildings.**

I. Introduction

The increasing concerns about climate change and environmental emissions have led to conserve energy in buildings through the development of several energy-efficient technologies. From early 1970's to till this point in time, huge importance has been given to the net energy being consumed in buildings.

In the recent years, increased demand in the construction sector has paved way for the development of huge and elegant building structures worldwide. Albeit, the required purpose of these structures is being continuously met, factually, buildings would consume almost one-third to one-quarter of the total energy being produced, globally.

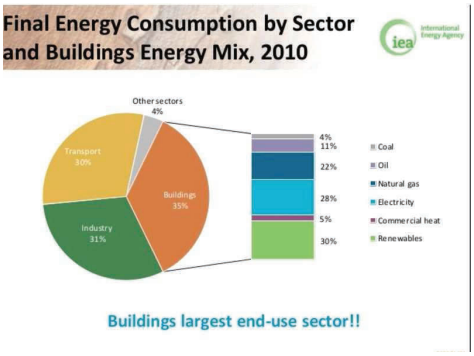

Figure 1. Energy consumption break-up by sector wise [1]

According to the statistical report of international energy agencies [1], the building sector in developed nations is accounting for about 35% of energy consumption. Further buildings consume energy from different sources; among them, it consumes approximately 30% in the form of renewable energy and 28 % in the form of electricity. Hence, there is an immense need to go for energy-efficient technologies in order to bridge the gap between the energy supply and end-use energy demand (Fig. 1).

There are wide varieties of energy storage technologies available, each type has its own advantages and limitations. Thermal energy storage is an important technique used widely for storing energy. Thermal energy storage is further classified as shown in Fig. 2. Latent Thermal Energy Storage (LTES) is widely used for storing energy to cater to cooling needs for building applications. PCM plays an important role in the performance of latent thermal energy storage system which stores energy during off-peak demand and redistributes the energy during on-peak demand.

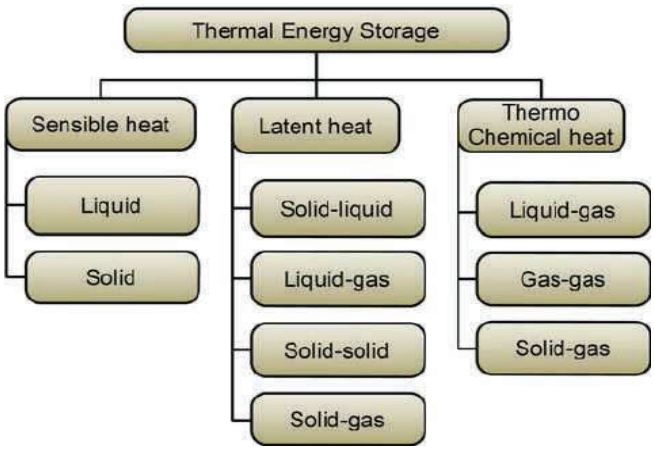

Figure 2. Classification of Thermal Energy Storage [16].

The PCMs were classified as inorganic PCMs (eg. Salt hydrates), organic PCMs (eg. paraffin's, fatty acids and fatty acid esters) and eutectic PCMs (eutectic salts and solutions) as shown in fig. 3. Among three, organic type PCMs are mostly preferred for cooling applications in buildings due to their excellent thermo-physical properties.

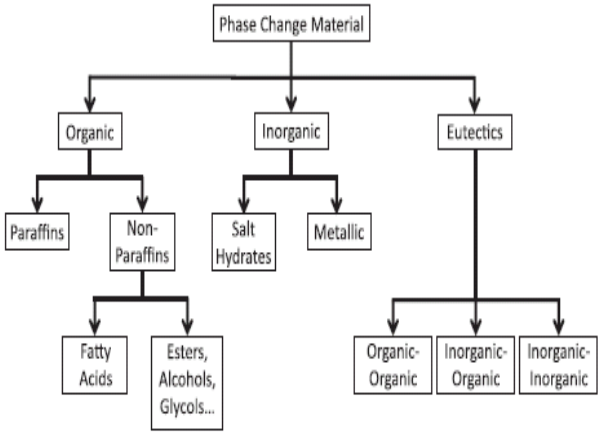

Figure 3. Classifications of Phase Change Materials [8]

Fig. 4 & 5 depict the working principle of PCM. PCMs during charging absorb cool energy thereby phase transforms from liquid to solid and during discharging they redistribute absorbed cool energy, thus maintaining human comfort temperatures for some time period.

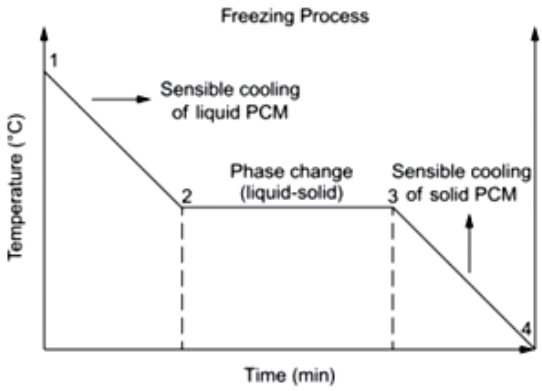

Figure 4. Schematic representation of freezing process for PCMs [15]

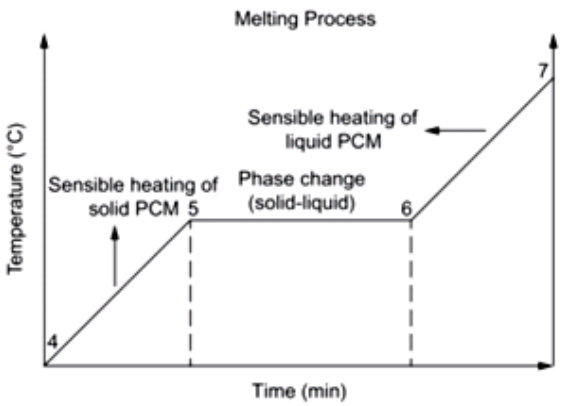

Figure 5. Schematic representation of melting process for PCMs [15]

II. Literature Survey

Pisello et al. [3] investigated for morphology, optical features, thermal characteristics, electrical properties and strain-sensing capability of cement-based composites doped with different carbon nano-inclusions, namely MWCNTs (multi walled carbon nano tubes), CNFs (carbon nano films), CB and GNPs (graphene nano platelet). The author also reported that all carbon nano-inclusions are seen to reduce solar reflectance capability, while they produce negligible variations in thermal emittance. Thermal conductivity and diffusivity were increased with Graphene nano platelet and better distribution of thermal wave. Consistently, the same graphene samples produce the largest electrical conductivity and capacitance.

Tang et al [4] prepared myristic-stearic acids (MA-SA) binary eutectics with appropriate phase change temperature. The melting temperature of the MA-SA eutectics and the mass fraction of the MA in the eutectic mixtures are 42.70°C and 54%. Then, a series of the MA-SA/CNTs with different mass fractions of the Carbon Nano Tubes (3%, 6%, 9%, 12% and 15%) were synthesized in order to investigate the thermal properties of the CPCM (composite phase change materials). The test results showed that, compared to the thermal conductivities of the MA-SA eutectics, the thermal conductivities of the CPCM's increase by 23.2%, 49.4% and 63.7% in the solid state, and 15.6%, 32.0% and 39.7% in the liquid state as the mass fractions of the CNTs are 9%, 12% and 15%.

Khodadadi and Babaei [5] performed a research study on the PCM incorporated with the copper nanoparticles, wherein the copper nanoparticles added to the PCM in molar concentrations of 0.1 and 0.2 have yielded the reduction in the overall freezing time of the PCM. This, in turn, facilitates for consuming less energy per unit mass of freezing the PCM.

Wu et al [9] investigated on melting/freezing characteristics of paraffin by adding Cu nanoparticles. Thermal stability of Cu/paraffin is good after 100 thermal cycles. With the increase in mass concentration of Cu nanoparticles, there was a nonlinear increase in thermal conductivity of Cu/Paraffin composites. With 2 wt % Cu/paraffin the maximum thermal conductivity enhanced up to 14.2% in solid state and 18.1% in the liquid state. The melting and freezing times for 1 wt % Cu/paraffin can be saved as about 33.3 and 31.6 %.

Lotfi et al [10] performed thermodynamic simulation using TRNSYS 17 software by incorporating PCM 204 in the walls of concrete ceiling and hollow bricks. The results revealed that there was 4 °C increased temperature in winter and reduced temperature of 7 °C in summer. There was energy saving of 25% in heating and cooling with the implementation of 30% PCM in gypsum panels used as interior plaster in buildings.

The study conducted by Li et al. [11] revealed the importance of incorporating the expanded graphite/paraffin PCM into the cement mortar, wherein the composite material developed, showed good temperature regulation with reduced maximum indoor centre temperature difference by 2.2 K and 1.5 K during heat storage and release processes, respectively. The test board fabricated using this composite material exhibited 1.74 higher heat storage coefficient than an ordinary cement mortarboard.

III. SYNTHESIS AND CHARACTERIZATION

For a synthesis of nanoparticles, sol-gel method was used. 25 ml of titanium tetrachloride ($TiCl_4$) is kept in ice cool bath which liberates heat because of an exothermic reaction. The solution having a very low temperature is slowly made to room temperature with a stirring process done on the magnetic stirrer at 350 rpm as shown in Fig. 6. Later the bath temperature should be increased slowly to 100 ºC until solutions get converted to thick as shown in Fig. 7. The contaminants present in the solution need to be removed, which can be done by incremental heating in a furnace to 250, 350 and to 550 ºC, Later it is milled using ball milling at 550 RPM. Finally, TiO_2 nanoparticles are prepared. The nanoparticles are then characterized for its size and morphology. It was revealed from TEM studies that the size is approximately 50nm as shown in Fig. 9. The as-prepared nanoparticles are then dispersed with varying increments of 0.5, 1, 2, 5 % in Rubitherm 21 type PCM.

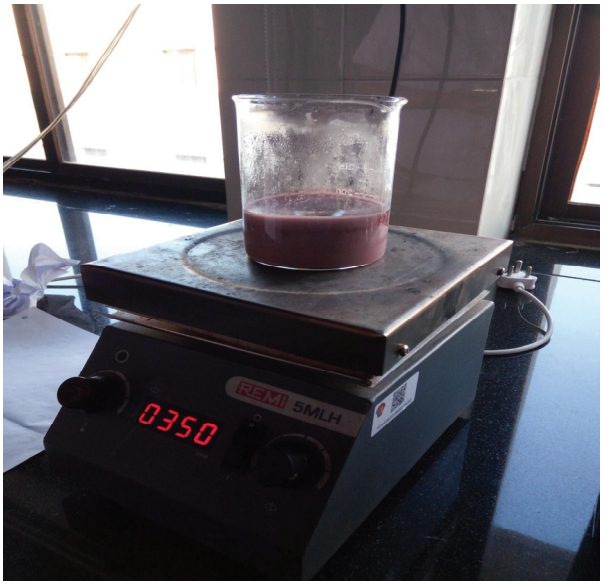

Figure 6. Solution stirred on magnetic stirrer

Figure 7. Thick solution of TiO_2

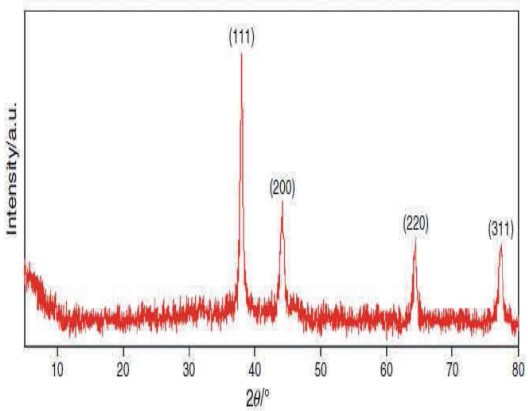

Figure 8. XRD pattern of Titania nanoparticles.

The nanoparticles were examined by X-Ray diffraction. The graph as shown in Fig. 8 reveals that nanoparticles prepared were highly crystalline. The XRD peaks for Titania nanoparticles obtained at 38.11º, 43.26º, 65.38º, and 76.39º of 2θº. Debye–Scherrer method [12] was used for average crystallite size which is 61 nm.

The as-prepared nanoparticles are characterized by shape, size using transmission electron microscope. The SEM results reveal that the nanoparticles are spherical in shape and size ranging from 50 nm to 100 nm.

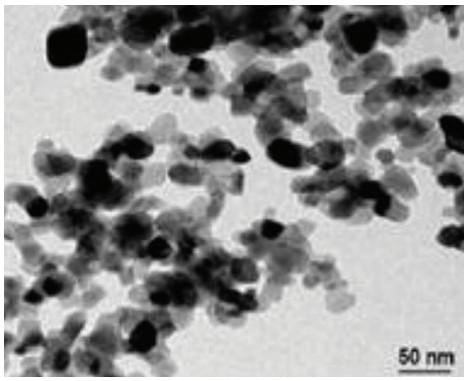

Figure 9. TiO_2 nanoparticles.

IV. PREPARATION OF NPCM

Ultrasonication process to avoid agglomeration and uniform mixing of titania nanoparticles in Rubitherm 21 type PCM.

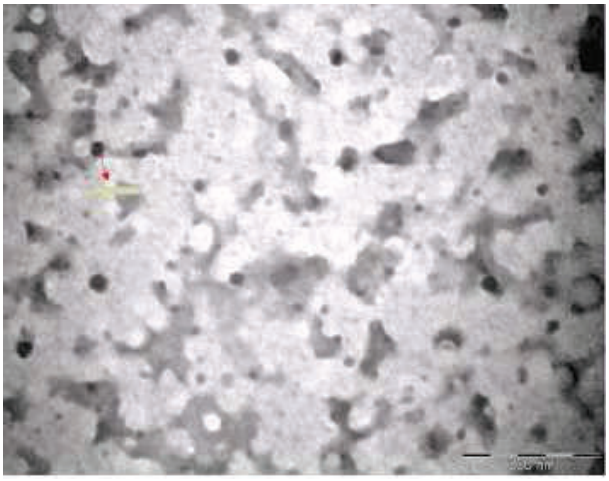

Figure 10. PCM dispersed with 0.5 % TiO_2 nanoparticles

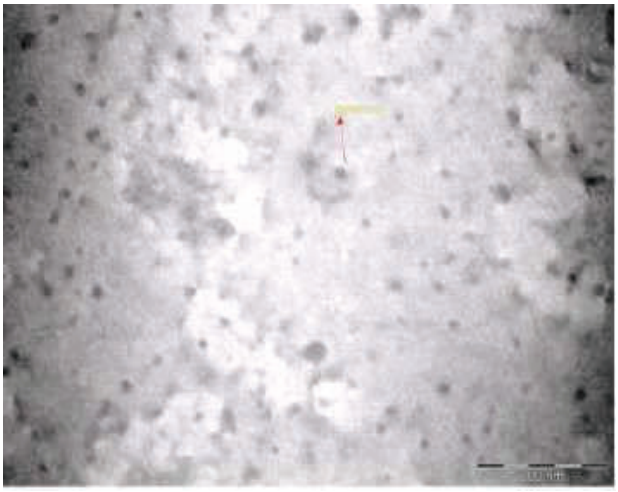

Figure 11. PCM dispersed with 1 % TiO_2 nanoparticles

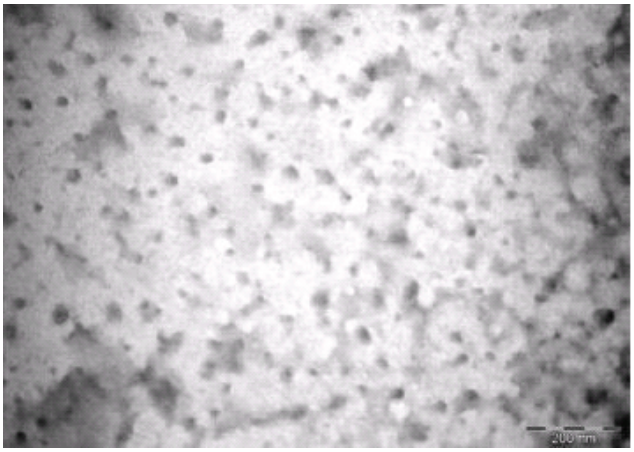

Figure 12. PCM dispersed with 2 % TiO_2 nanoparticles.

Figure 13. Nano based PCMs samples

Figure 14. Thermal Energy Storage Set up

V. EXPERIMENTATION

Thermal energy storage system was used for melting and freezing temperatures of different samples as shown in Fig. 14. System equipped with heating and refrigeration circuits controlled automatically for increasing and decreasing temperatures of the water bath. The setup has a capacity to perform experiments in the range of 2 ºC to 90 ºC. Thermocouples were used for sensing temperature of the water and samples. The Stirrer is provided in the water bath for stirring by making a uniform water temperature.

The thermal conductivity of pure PCM is 0.2 W/ m k. With the TiO_2 nanoparticles dispersion in PCM, thermal conductivity enhances, it varies from 0.279 to 0.749 W/ m k.

For freezing and melting characteristics of NPCM, bottles filled with NPCM having a room temperature are immersed in a cool water bath. Solidification process takes place in three stages. Firstly, PCM gives out sensible heat to the cool fluid, thereby PCM temperature decreases gradually. In the second stage, it dissipates latent heat at isothermal conditions. The solidification starts from outer

most and ends at the center with uniform conditions. In the third stage after complete solidification, further decrease in temperature takes place. The results revealed that solidification takes place at the fastest rate and latent heat capacity increases due to a dispersion of TiO_2 nanoparticles.

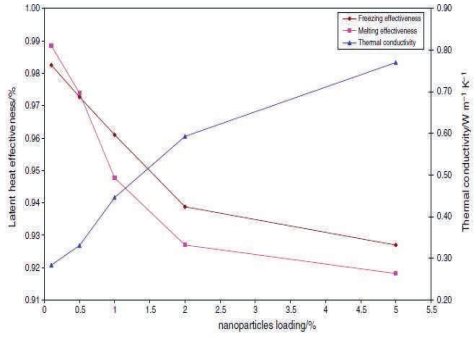

Figure 15. Effect on latent heat effectiveness and thermal conductivity with varying % nanoparticles

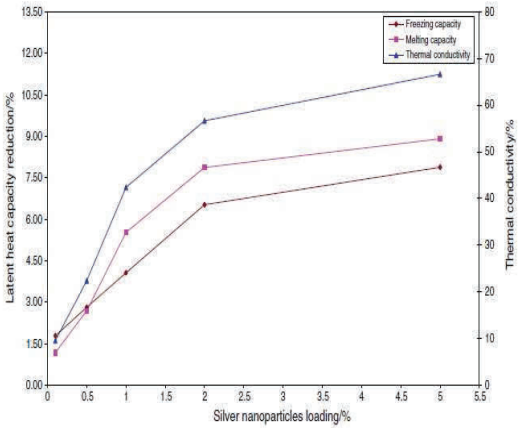

Figure 16. Effect on latent heat reduction and thermal conductivity with varying % nanoparticles

VI. RESULTS AND DISCUSSION

TABLE I
Summary of latent heat and degree of super cooling for different nano particles loading in pcm.

TiO_2 % loading	Latent heat kJ/kg		Degree of super cooling
	Freezing	Melting	
0	148	155	1.76
0.5	147	152.78	1.65
1	147.45	151.01	1.52
2	144.44	150.98	1.51
5	143.20	150.2	1.30

The Titania nanoparticles prepared were uniformly dispersed leading to enhanced thermal properties compared with pure PCM. During charging, it was noticed that there was a faster rate of cold energy transfer from HTF (heat transfer fluid) to PCM, because of the nanoparticles. Due to a faster rate of heat transfer, the time taken for charging (Off-peak demand) and discharging time (On-peak demand) were reduced. The Titania nanoparticles, when dispersed in PCM were chemically stable.

The experimental results suggest that NPCM can be beneficial and practically implemented for cooling needs in buildings, cold storage, etc.

VII. CONCLUSIONS

From the experimental work following points were concluded.

1. With the sol-gel process and controlled process parameters like volume percentage of solute, solvent and treating temperatures, TiO_2 particles prepared were in nano range.
2. The prepared TiO_2 nanoparticles are spherical in shape and average size distribution is 61 nm.
3. When the nanoparticles are dispersed in PCM the mixture is stable with no chemical reaction between PCM and nanoparticles.
4. From the experimentation, it is concluded that with the increased mass percentage of nanoparticles thermal conductivity increases enhancing the faster rate of nucleation making solidification faster.
5. Latent heat storage capacity has increased compared to pure PCM and exhibits slight differences during melting and freezing cycles.
6. It is also noticed that with the increased percentage of nanoparticles, degree of super cooling has decreased.

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A Study on Investment Behavioural Patterns of Women Investors

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Abstract: **The socio-economic status of women is changing. With increase in the number of working women, there has been an increase in the number of women investors. Their financial influence is becoming stronger as they feel responsible for household expenditures and savings. So women structure their expenditures and savings for specific purposes. Thus, this study examines the investment behaviour of women investors in different investment avenues.**

Index Terms: **women investors, investment behaviour**

I. Introduction

Financial markets help in accelerating investment activities in the country. Investments can have a major impact on an investor's well-being. There are a large number of women investors who have the ability to make investments in insurance, gold, real estate, bank deposits, share market, provident funds, chit funds and post office. Each of these investments has common features like potential returns and risks. A great number of women are being employed and their attitude towards investment avenues is also changing. Instead of keeping their savings idle, women are showing keen interest in investing their money saved in various investment avenues to get returns and to meet present and future expenditures. With more autonomy in decision making, women are playing a pivotal role in socio-economic growth of the country. Women are playing more active economic role due to diverse reasons such as recent global financial crises and more men are losing jobs due to recession in the economy and automation of jobs.

II. Literature Review

Individual investment choices are influenced by lifestyle and demographic attributes (Rajarajan, 2000). Though investors are in cognitive illusions, they consider multiple factors and try to create self-awareness before taking an investment decision (Shinde C.M., et.al., 2014). Women are more comprehensive information processors than men and therefore can deal with more complex financial products more accurately (Monica Sharma, et.al., 2013). But confidence in investment decisions is strongly affected by gender. Women are less confident than men in making investments (Powell and Ansic, 1997). As confidence level is low, women are more risk averse than men in making financial investments (Patti J.Fisher, 2010). There are differences between active and passive women investors based on demographic factors, psychographic factors and investment characteristics. Irrespective of age, educational qualifications and occupation, women think that saving for the future is desirable (J.Klaymanet, 1999). Women investors are more likely to enter into stock market trading, if their parents have been into stock market trading during the past few years (P.Paramashivaiah, et.al, 2014). Women investors are financially knowledgeable but need better financial planning skills (C.Gnana Desigan, et.al, 2006). Working women are more aware of the various investment avenues and take better investment decisions when compared to non-working women. Very few women investors have a good understanding of investment risks. In unprecedented financial markets volatility, women become more cautious and thoughtful with regard to financial investments (R.Suyam Praba, 2016). There is an impact of intuitive thinking of women investors on investment preference. Emotions act as a barrier to rationality and logic thinking of women investors and affect their prospects of generating additional income through investments (Manish Mittal, et.al, 2009).

III. Objectives of The Study

1. To understand the investment objectives of women investors
2. To analyze the sources of information on investments
3. To identify the investment avenues of women investors
4. To study the variables influencing the investment decisions taken by women investors

IV. Research Methodology

This study is based on survey conducted in Hyderabad during January to June 2017. The primary data was collected through questionnaire method, using Judgment (Purposive) sampling. The respondents were selected on the basis of judgment to include all demographic segments. Questionnaire was distributed to 105 women investors, out of which 80 responded. The questionnaire consisted of 26 questions related to the Investment Decision variables. The theoretical foundation of the study is based on various secondary sources such as textbooks, articles, quality magazines, article features and published papers.

TABLE I.
DATA ANALYSIS

Demographic Variables	Total No. Of Respondents	Percentage
Age		
Below 25 years	12	15
25-35 years	45	56.25
35-45 years	14	17.5
Above 45 years	9	11.25
Total	80	100
Educational Qualification	Total No. Of Respondents	Percentage
Std 10th	11	13.75
Graduate	34	42.5
Post Graduate	16	20
Professional Degree	19	23.75
Total	80	100
Marital Status	Total No. Of Respondents	Percentage
Single	21	26.25
Married	59	73.75
Total	80	100
Occupation	Total No. Of Respondents	Percentage
Government Employee	11	13.75
Private Employee	32	40
Self Employee	22	27.5
Housewife	15	18.75
Total	80	100
Annual Income	Total No. Of Respondents	Percentage
Less than 150000	8	10
150000-300000	30	37.5
300000-600000	26	32.5
600000-900000	10	12.5
More than 900000	6	7.5
Total	80	100

The above table shows that out of 80 respondents, 56.25% were in the age group of 25-35 years, 42.5% were graduates, 73.75% were married, 40% were private employees and 37.5% were having annual income of Rs. 150000 to Rs. 300000.

TABLE II.
INVESTMENT OBJECTIVES

Investment Objectives	Ranking					Total Score
	Rank 1	Rank 2	Rank 3	Rank 4	Rank 5	
Regular Income	31	11	16	13	6	77
Childrens' Education	13	30	6	16	9	74
Wealth Creation	10	20	19	11	24	78
Provision for Retirement	8	4	18	15	25	70
Meeting Medical Expenses	11	15	20	10	24	80
Tax Benefit	8	16	19	20	10	73
Meeting Contingencies	2	11	15	13	31	72

The above table shows that the investment objective of meeting medical expenses has got the highest score of 80 followed by wealth creation with the total score of 78. The investment objective of provision for retirement has got the least total score of 70. This means that women investors are more concerned about medical expenses and are investing with the main objective of meeting medical expenses.

TABLE III.
SOURCES OF INFORMATION

Sources of Information	No. of Respondents	Percentage
Self Awareness	21	26.25
Financial Advisor	15	18.75
Internet	4	5
Family/Friends/Relatives	32	40
Media	8	10
Total	80	100

The above table shows that the main source of information is from family, friends and relatives. 32 out of 80 women investors (40%) are relying on family, friends and relatives for information on investments. There has been an increase in the self awareness of the women investors on investments, with 21 out of 80 women investors (26.25%) relying on the information, procured on their own through various sources. Only 4 out of 80 women investors (5%) made investments based on the information that they got through internet.

TABLE IV.
INVESTMENT AVENUES

Investment Avenues	No. of Respondents	Percentage
Government Securities	5	6.25
Bank Deposits	22	27.5
Provident Fund	4	5
Insurance Scheme	11	12.5
Mutual Funds	6	7.5
Shares/Debentures	2	2.5
Bonds	2	2.5
Real Estates	3	3.75
Gold	17	22.5
Chit Funds	8	10
Total	80	100

The above table shows that bank deposits are the most preferred investment avenue with 22 out of 80 women investors (27.5%) opting for bank deposits. This is followed by investments made in gold with 17 out of 80 women investors (22.5%) opting for purchase of gold as an investment. The least preferred investment avenues are shares/ debentures and bonds with only 2 out of 80 (2.5%) respectively, opting for it.

TABLE V.
INVESTMENT DECISION

Investment Decision	No. of. Respondents	Percentage
Independent	28	35
Dependent	52	65
Total	80	100

The above table shows that 28 out of 80 women investors (35%) have taken investment decisions independently and 52 out of 80 (65%) have been dependent on others for taking investment decisions. It depicts that they are still mostly dependent on their family members, friends and relatives for investment related information and for taking investment decisions.

TABLE VI.
DURATION OF INVESTMENT

Period of Investment	No. of Respondents	Percentage
Less than 1 year	10	12.5
1 to 3 years	36	45
3 to 5 years	17	21.25
5 to 10 years	9	11.25
More than 10 years	8	10
Total	80	100

The above table shows that most of the women investors prefer making investments for duration of 1 to 3 years. 36 out of 80 women investors (45%) have made investments for a period of 1 to 3 years. 17 out of 80 women investors (21.25%) have made investments for a period of 3 to 5 years. Very few have shown interest in making long term investments with only 8 out of 80 (10%) having made investments for more than 10 years.

TABLE VII.
FORMATION OF FINANCIAL PLAN

Formulation of Financial Plan	No. of Respondents	Percentage
Yes	23	28.75
No	57	71.25
Total	80	100

The above table shows that 57 out 80 respondents (71.25%) have not made any financial plans regarding various financial goals. This shows that a majority of women did not plan for their investment avenues and have invested as and when opportunities came. Thus, without a proper financial plan they may lack focus on financial requirements.

TABLE VIII.
USE OF FUNDS IN THE PORTFOLIO

Use of funds in the Portfolio	No. of Respondents	Percentage
Above 10 years	16	20
6 to 10 years	43	53.75
0 to 5 years	21	26.25
Total	80	100

The above table shows that most of the women investors (53.75%) use the investment funds within 6 to 10 years and very few women investors use their funds in their portfolio for more than 10 years. It depicts that most of the women investors do not have very long term use of their funds.

TABLE IX.
PERCENTAGE OF INCOME INVESTED

Percentage of Income invested	No. of Respondents	Percentage
Less than 10%	23	28.75
10% to 20%	29	36.25
20% to 30%	17	21.25
More than 30%	11	13.75
Total	80	100

The above table shows that 29 out of 80 respondents (36.25%) have invested 10% to 20% of their income and 17 of them invested 20% to 30% of their income in various investment avenues. Only 13.75% of the respondents have invested more than 30% of their income in various investment avenues because many women investors do not have a thorough knowledge of all the prospective investment avenues and dislike taking risks.

TABLE X.
FREQUENCY OF INVESTMENT

Frequency of investment	No. of Respondents	Percentage
Weekly	10	12.50
Monthly	20	25
Quarterly	26	32.5
Half yearly	11	13.75
Yearly	13	16.25
Total	80	100

The above table shows that 26 out of the 80 respondents (32.5%) make investments on quarterly basis. This is followed by those who make monthly investments. Very few women investors invest on weekly or yearly basis.

TABLE XI.
REACTIONS WITH DECREASE IN PORTFOLIO VALUE

Reactions with decrease in portfolio value	No. of Respondents	Percentage
Transfer of money immediately	37	46.25
Concerned but wait for improvement	28	35
Withdraw the investments	11	13.75
Invest more funds	4	5
Total	80	100

The above table shows that 37 out of 80 respondents (46.25%) transfer their money immediately with the fall in the portfolio value. Most of the women investors hesitate to take risk and feel that it is better to transfer the money immediately in other portfolios rather than wait for improvement in the current portfolio value. Very few of them continue to invest in the funds with decrease in the value of the portfolio.

TABLE XII.
PERCEIVED INVESTMENT CONTROL VARIABLES

Perceived investment control variables	Mean	Standard Deviation
Confidence in ability to invest	3.59	0.644
Regular review and comparison of investment performance with market benchmarks	3.20	0.850
Consistent investment strategy	3.96	0.735
Knowledgeable about investing	3.17	0.617
Satisfaction with current investment mix	3.02	0.798

The above table shows that the variable of consistent investment strategy is considered as the highest perceived investment control variable with a mean of 3.96 (SD 0.735) followed by the variable of confidence in ability to invest with a mean of 3.59 (SD 0.6444). The variable of satisfaction with current investment mix is considered as the least perceived investment control variable with a mean of 3.02 (SD 0.798).

TABLE XIII.
MEAN AND STANDARD DEVIATION FOR INVESTMENT DECISION VARIABLES

Investment Decision Variables	Mean	Standard Deviation (SD)
Safety	4.6	0.912
Liquidity	4.0	0.750
Tax Benefit	3.5	0.808
Returns	3.9	0.891
Capital Appreciation	3.8	0.956
Risk Coverage	4.2	0.863
Personal Ability to Invest	2.8	0.654
Access to Information on Investments	3.6	0.867
Advice or recommendation from Family/ friends/ stock holder/ broker	3.7	0.789
Easy availability of funds whenever required	4.4	0.704

The above table shows that the variable of safety has the highest impact on investment decision making of women investors with mean value of 4.6 (SD 0.912) followed by the variable of easy availability of funds whenever required, with mean value of 4.4 (SD 0.704). The variable of personal ability to invest has the least impact on the investment decision making of the women investors with mean value of 2.8 (SD 0.654).

V. CONCLUSIONS

This research showcases that women are more concerned about meeting their immediate expenses like medical expenses. Therefore women investors prefer short term investments rather than making provisions for long term benefits. Though there has been an increase in the number of educated working women, they are still mostly dependent on their family members, friends and relatives for investment related information and for taking investment decisions. Women do not want to take much risk while making financial investments and therefore opt for safer investments like bank deposits and gold rather than investing in shares and bonds. As women investors want to create more wealth to meet short term expenses, they want funds to be easily available whenever required. The government must strive to promote financial literacy through its public policies so that women can have better financial planning skills.

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In the next issue (Vol 14, June, 2018)

Template for the Preparation of Papers for Publication in CVR Journal of Science and Technology

First A. Author[1] and Second B. Author[2]
[1]Designation, Name of Institution/Department, City, Country
Email: first.author@hostname1.org
[2]Designation, Name of Institution/Department, City, Country
Email: second.author@hostname2.org

Abstract: **These instructions give you basic guidelines for preparing camera-ready papers for CVR College journal Publications. Your cooperation in this matter will help in producing a high quality journal.**

Index Terms: **first term, second term, third term, fourth term, fifth term, sixth term**

I. Introduction

Your goal is to simulate the usual appearance of papers in a Journal Publication of the CVR College. We are requesting that you follow these guidelines as closely as possible. It should be original work. Format must be done as per the template specified. Diagrams with good clarity with relevant reference within the text are to be given. References are to be cited within the body of the paper. Number of pages must not be less than five, but not more than eight.

A. Full-Sized Camera-Ready (CR) Copy

Prepare your CR paper in full-size format, on A4 paper (210 x 297 mm, 8.27 x 11.69 in). No header or footer, no page number.

Type sizes and typefaces: Follow the type sizes specified in Table I. As an aid in gauging type size, 1 point is about 0.35 mm. The size of the lowercase letter "j" will give the point size. Times New Roman has to be the font for main text. Paper should be single spaced.

Margins: top = 24.9mm (0.98 in), bottom, left and right = 16 mm (0.63 in). The column width is 86mm (3.39 in). The space between the two columns is 6mm (0.24 in). Paragraph indentation is 3.7 mm (0.15 in).

Left- and right-justify your columns. Use tables and figures to adjust column length. On the last page of your paper, adjust the lengths of the columns so that they are equal. Use automatic hyphenation and check spelling. Digitize or paste down figures.

For the Title use 24-point Times New Roman font, an initial capital letter for each word. Its paragraph description should be set so that the line spacing is single with 6-point spacing before and 6-point spacing after. Use two additional line spacings of 10 points before the beginning of the double column section, as shown above.

Each major section begins with a Heading in 10 point Times New Roman font centered within the column and numbered using Roman numerals (except for ACKNOWLEDGEMENT and REFERENCES), followed by a period, two spaces, and the title using an initial capital letter for each word. The remaining letters are in SMALL CAPITALS (8 point). The paragraph description of the section heading line should be set for 12 points before and 6 points after.

TABLE I.
TYPE SIZES FOR CAMERA-READY PAPERS

Type size (pts.)	Appearance		
	Regular	Bold	Italic
6	Table caption, table superscripts		
8	Tables, table names, first letters in table captions, figure captions, footnotes, text subscripts, and superscripts		
9	References, authors' biographies	Abstract	
10	Section titles ,Authors' affiliations, main text, equations, first letters in section titles		Subheading
11	Authors' names		
24	Paper title		

Subheadings should be 10 point, italic, left justified, and numbered with letters (A, B, …), followed by a period, two spaces, and the title using an initial capital letter for each word. The paragraph description of the subheading line should be set for 6 points before and 3 points after.

For main text, paragraph spacing should be single spaced, no space between paragraphs. Paragraph indentation should be 3.7mm/0.21in, but no indentation for abstract & index terms.

II. Helpful Hints

A. Figures and Tables

Position figures and tables at the tops and bottoms of columns. Avoid placing them in the middle of columns. Large figures and tables may span across both columns. Leave sufficient room between the figures/tables and the main text. Figure captions should be centered below the figures; table captions should be centered above. Avoid placing figures and tables before their first mention in the text. Use the abbreviation "Fig. 1," even at the beginning of a sentence.

To figure axis labels, use words rather than symbols. Do not label axes only with units. Do not label axes with a ratio

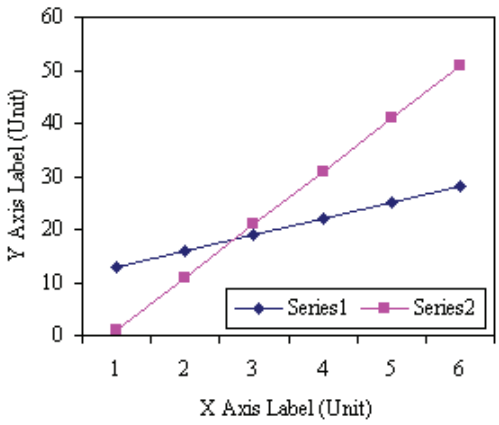

Figure 2. Note how the caption is centered in the column.

of quantities and units. Figure labels should be legible, about 9-point type.

Color figures will be appearing only in online publication. All figures will be black and white graphs in print publication.

B. References

Number citations consecutively in square brackets [1]. Punctuation follows the bracket [2]. Use "Ref. [3]" or "Reference [3]" at the beginning of a sentence:

Give all authors' names; use "et al." if there are six authors or more. Papers that have not been published, even if they have been submitted for publication, should be cited as "unpublished" [4]. Papers that have been accepted for publication should be cited as "in press" [5]. In a paper title, capitalize the first word and all other words except for conjunctions, prepositions less than seven letters, and prepositional phrases. Good number of references must be given.

C. Footnotes

Number footnotes separately in superscripts [1, 2, ⋯]. Place the actual footnote at the bottom of the column in which it was cited, as in this column. See first page footnote as an example.

D. Abbreviations and Acronyms

Define abbreviations and acronyms the first time they are used in the text, even after they have been defined in the abstract. Do not use abbreviations in the title unless they are unavoidable.

E. Equations

Equations should be left justified in the column. The paragraph description of the line containing the equation should be set for 6 points before and 6 points after. Number equations consecutively with equation numbers in parentheses flush with the right margin, as in (1). Italicize Roman symbols for quantities and variables, but not Greek symbols. Punctuate equations with commas or periods when they are part of a sentence, as in

$$a + b = c \,. \tag{1}$$

Symbols in your equation should be defined before the equation appears or immediately following. Use "(1)," not "Eq. (1)" or "equation (1)," except at the beginning of a sentence: "Equation (1) is ..."

F. Other Recommendations

Use either SI (MKS) or CGS as primary units. (SI units are encouraged.) If your native language is not English, try to get a native English-speaking colleague to proofread your paper. Do not add page numbers.

III. Conclusions

The authors can conclude on the topic discussed and proposed, future enhancement of research work can also be briefed here.

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ABOUT THE COLLEGE

CVR College of Engineering (A UGC Autonomous Institution) was established in the year 2001, and its Thirteenth batch of students graduated from the College. This college is on a roll with the recent NIRF ranking within the top 4 colleges in the state of Telangana, followed by record placements and now with the setting up of a new Apple lab. The new lab consists of state of the art iMacs that enables students to develop new applications on the Apple devices. With the Make in India initiative and the expected manufacturing and increased sales of Apple devices in the country, new applications need to be developed for our needs and this lab will transform students into developers.

The College was the first college in Telangana that was promoted by NRI technology professionals resident in the US. The NRI promoters are associated with cutting-edge technologies of the computer and electronics industry. They also have strong associations with other leading NRI professionals working for world-renowned companies like IBM, Intel, Cisco, Motorola, AT&T, Lucent and Nortel who have agreed to associate with the College with a vision and passion to make the College a state-of-the-art engineering institution.

The college has many accomplishments and to name a few, it obtained NBA Tier 1 accreditation for four UG programs, NAAC 'A' grade, UGC autonomous status, National Employability Award for sixth year in a row and got a very high rating by several ranking agencies including the most recent Education World ranking of third best college in Telangana and Outlook magazine, rating CVR CE, one among the top 100 colleges in the country.

Placements at the college continue to create a record year after year with average salary going up to a record Rs. 3.90 Lakhs and a record 20 students getting offers of above Rs. 10Lakhs and another 160+ students above Rs. 4 Lakhs with a total of about 610 job offers. 10 students have offers of Rs. 16Lakhs, which is the highest. CVR has made huge progress in a short span of time and is preferred by the students and parents, among the top 4 colleges in the state, during the EAMCET counseling this year.

In keeping with the current global emphasis on green and eco-friendly energy generation, 360kW Solar PV plant has been installed in the campus to meet the power requirements of the college to a significant extent.

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CVR JOURNAL OF SCIENCE & TECHNOLOGY

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http://cvr.ac.in

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