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CVR COLLEGE OF ENGINEERING

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CVR COLLEGE OF ENGINEERING

(UGC Autonomous - Affiliated to JNTU Hyderabad)
Mangalpalli (V), Ibrahimpatnam (M),
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EDITORIAL

It is with delight that we bring out Volume-12 of the Biannual Journal of our college, CVR Journal of Science and Technology. This Volume is brought out in colour similar to the previous one. We thank the Management for the same. The figures and graphs in colour will enable the researchers and readers to have more clarity.

We are very happy to share with our readers that our CVR College of Engineering is ranked **among the TOP 5 institutions**, **in the State of Telangana**, as per the **NIRF MHRD rankings**. It is ranked in the **101-150 band** of rankings by the **NIRF**. For a college which is about 16 years old, it is a remarkable achievement. This made the management of the college to launch Mission 100, to be among the top 100 institutions in the country. Research activity plays an important role in this aspect. Hope the Journal and the contributors will help in improving the ranking of the institution. We are also happy to share with the readers that the college is **Accredited by NAAC with 'A' grade.** Affiliation for all courses and all seats in all branches for UG programmes is also obtained from JNTUH for the academic year 2017-18. It is expected that the contributors will further enhance the reputation of the college through this Journal.

We have received good number of research papers for review, from our own faculty and from outside our institution also. A rigorous filtration process is done, anti plagiarism check by software, and review by experts are done. Finally research papers were selected for publication in the present volume.

For convenience of the readers, the research articles are grouped branch wise and the name of the branch is indicated in the contents page.

The breakup of the papers among various branches is:

Civil – 4, EEE – 2, Mech – 3, ECE – 5, CSE – 3, IT – 2, EIE – 1, H & S- 1.

The management is supporting the research and Ph.D Programmes by liberally sanctioning study leave for the faculty of this college. Faculty members working for Ph.D and on research projects are expected to contribute for the journal. Management is also encouraging the authors of research papers with incentives, based on merit. Some of the research articles accepted for publication in the forth coming Volume 13 are listed in Page No.127.

I am thankful to all the members of the Editorial Board for their help in reviewing and short listing the research papers for inclusion in the current Volume of the journal. I wish to thank **Dr.S.Venkateshwarlu, HOD EEE and Associate Editor**, for the effort he has made in bring out this Volume. Thanks are due to **HOD, H & S, Dr. E. Narasimhacharyulu** and the staff of English Department for reviewing the papers to see that grammatical and typographical errors are corrected. I am also thankful to **Smt. A. Sreedevi**, DTP Operator in the Office of Dean Research for the effort put in the preparation of the papers in Camera Ready form.

For further clarity on waveforms, graphs, circuit diagrams and figures, readers are requested to browse the soft copy of the journal, available on the college website **www.cvr.ac.in**, wherein a link is provided and is available in color.

Prof. K. Lal Kishore
Editor

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Flexural Behaviour of Reinforced Concrete Beams using ANSYS

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***Abstract*—In the present paper,the flexural behavior of reinforced concrete beams with minimum flexural tension reinforcement and the beams with the design reinforcement was studied by varying the concrete grades(M20,M25 and M30), grades of steel (Fe250,Fe415 and Fe500) and different beam width-to-depth ratios(0.5,0.6 and 0.7) under three point bending using ANSYS 12.1 version through load-deflection diagrams. The variation of deflection, strain energy and stress intensity factor was studied for different beam width-to-depth ratios and different grades of concrete and steel. Twenty seven reinforced concrete beams with minimum flexural reinforcement and twenty seven reinforced concrete beams with design reinforcement have been modelled and analysed in ANSYS. Total beams modelled and analysed were fifty four.**

***Index Terms*—Strain energy, Stress Intensity factor, Peak load, Finite element analysis, ANSYS.**

I. Introduction

Concrete structural components exist in buildings and bridges in different forms. Reinforced concrete (RC) has become one of the most important building materials and is widely used in many types of engineering structures. The economy, the efficiency, the strength and the stiffness of reinforced concrete make it an attractive material for a wide range of structural applications. Understanding the response of structural components during loading is crucial to the development of an overall efficient and safe structure. Different methods have been utilized to study the response of structural components. Experimental based testing has been widely used as a means to analyze individual elements and the effects of concrete strength under loading. This method of testing produces real life response but it is time consuming and the use of materials can be quite costly. Hence, in recent years, the use of finite element analysis has increased due to the progressing knowledge and capabilities of computer software and hardware. It has now become the choice method to analyze concrete structural components [2][4][5][6]. The use of computer software to model these elements is much faster and extremely cost-effective. The use of finite element analysis has been the preferred method to study the behavior of concrete for economic reasons [7][9][10][11].The evaluation of adequate margin of safety of concrete structures against failure is assured by the accurate prediction of ultimate load and the complete load-deformation behaviour or moment-curvature response[1][3][8]. A typical three point bend setup is presented in Figure 1.

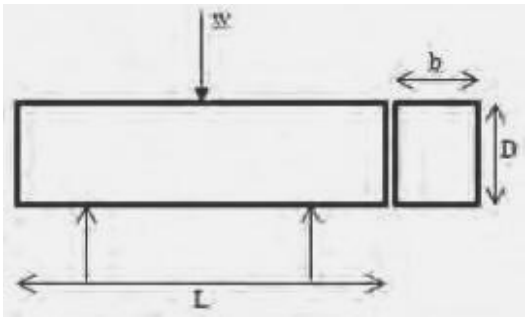

Figure 1. Typical three point bending test set up

II. Sample Load Calculation

Design of reinforced concrete beam [13]

CASE – 1(Fe 250)

b/D=0.5 & M20

Grade of steel:	Fe250
Grade of concrete:	M20
Length of beam:	2500mm
Width/Total depth of beam:	0.5
Load:	190KN/m

For simply supported beams, if the uniformly distributed load is acting than maximum bending moment at mid span is $M = \frac{wl^2}{8} = \frac{190 \times 2.5 \times 2.5}{8} = 148.437$ KN/m

Factored bending moment = 1.5 × M = 1.5 × 148.437 = 222.65 KN/m

For Fe250, $\frac{x_{umax}}{d} = 0.53$

$M_{ulim} = 0.36 \left(\frac{x_{umax}}{d}\right) (1\text{-}0.42\frac{x_{umax}}{d})\, bd^2 f_{ck}$

$222.65 = 0.36 \times 0.53\ (1\text{-}(0.42\times0.53))\ b \times (2b)^2 \times 20$

b = 266mm

D = 532mm

d = 492mm

clear cover = 25mm

Calculation of tension reinforcement:

$M_u = 0.87 \times f_y \times A_{st} \times d\ (1\text{-}\frac{A_{st} \times f_y}{f_{ck} \times b \times d})$

$222.65 = 0.87 \times 250 \times A_{st} \times 492\ (1\text{-}\frac{A_{st} \times 250}{20 \times 266 \times 492})$

$A_{st} = 2865mm^2$

Provide 25mm diameter bars

Number of bars $= \frac{2865}{\frac{\pi}{4} \times 25^2} = 6$

Minimum $A_{st}= \frac{0.85}{f_y} bd = \frac{0.85}{250} \times 266 \times 492 = 445\ mm^2$

$A_{st\ min}= 445\ mm^2$

Calculation of shear reinforcement :

Dead load = 0.266 × 0.532 × 1 × 25 = 3.537 KN/m

Live load = 190 KN/m

Factored load = 190 + 3.537 = 193.537 KN/m

$$V_u = \frac{wl}{2} = \frac{193.537 \times 2.5}{2} = 242\ KN$$

$\tau_c\ for\ M_{20}$from IS456-2000

$100 \times \frac{A_{st}}{b \times d} = 100 \times \frac{2865}{266 \times 532} = 2.189$

$\tau_c = 0.8\ N/mm^2$

$\tau_{cmax} = 2.8\ N/mm^2$ for M20

$\tau_v = \frac{V_u}{bd} = \frac{242}{266 \times 532} = 1.848\ N/mm^2$

$\tau_v > \tau_c$

Design shear

$V_u = V_{us} + V_{uc}$

$V_{uc} = \tau_c \times bd = 0.8 \times 266 \times 492 = 104697.6$ N

$V_{us} = V_u - V_{uc} = 242000 - 104697.6 = 137224$ KN

Use 8mm diameter, 2-legged stirrups

$A_{sv} = 2 \times \frac{\pi}{4} \times 8^2 = 100.5\ mm^2$

$S_v = \frac{0.87 \times f_y \times A_{sv} \times d}{V_{us}} = \frac{0.87 \times 250 \times 100.5 \times 492}{137224} = 75$ mm

Calculation of development length :

$L_d = \frac{\phi \sigma_s}{4 \times \tau_{bd}} = \frac{25 \times 0.87 \times 250}{4 \times 1.2 \times 1.6} = 708$ mm

$L_d \leq (\frac{M_1}{V} + L_0)$

$= (\frac{222.65 \times 10^6}{242000} + (x_0 + 8\phi))$

$= \frac{222.65 \times 10^6}{242000} + (125 + (8 \times 25))$

$= 1245.04$ mm

Therefore development length L_d= 708mm

Similarly for different grades of steel (Fe250, Fe415 and Fe500), different grades of concrete (M20, M25 and M30) and beam width to total depth ratios (0.5,0.6 and 0.7) are designed and presented in Table I, Table II and Table III respectively.

TABLE I
DESIGN DETAILS OF REINFORCED CONCRETE BEAM WITH DESIGN REINFORCEMENT (Fe250)

Grade of steel	b/D	Grade of concrete	Width b (mm)	Total depth D (mm)	Design steel A_{st} (mm^2)	Minimum steel $A_{st\ min}$ (mm^2)
Fe250	0.5	M20	266	532	2865	445
		M25	247	494	3127	381
		M30	233	466	3340	337
	0.6	M20	301	502	3060	473
		M25	279	465	3362	403
		M30	263	439	3603	357
	0.7	M20	333	476	3272	494
		M25	309	442	3589	422
		M30	291	416	3861	372

TABLE II
DESIGN DETAILS OF REINFORCED CONCRETE BEAM WITH DESIGN REINFORCEMENT (Fe415)

Grade of steel	b/D	Grade of concrete	Width b(mm)	Total depth D(mm)	Design steel A_{st} (mm^2)	Minimum steel $A_{st\ min}$ (mm^2)
Fe415	0.5	M20	273	546	1607	283
		M25	253	506	1760	241
		M30	238	476	1892	213
	0.6	M20	308	514	1728	299
		M25	286	477	1885	256
		M30	269	449	2029	225
	0.7	M20	341	488	1840	313
		M25	317	453	2003	268
		M30	298	426	2161	236

TABLIII
DESIGN DETAILS OF REINFORCED CONCRETE BEAM WITH DESIGN REINFORCEMENT (Fe500)

Grade of steel	b/D	Grade of concrete	Width b (mm)	Total depth D (mm)	Design steel A_{st} (mm^2)	Minimum steel $A_{st\ min}$ (mm^2)
Fe500	0.5	M20	276	552	1298	240
		M25	256	512	1417	205
		M30	241	482	1520	181
	0.6	M20	311	519	1399	253
		M25	289	482	1522	217
		M30	272	454	1635	191
	0.7	M20	345	493	1482	266
		M25	320	458	1621	227
		M30	301	430	1745	200

III. FINITE ELEMENT MODELLING

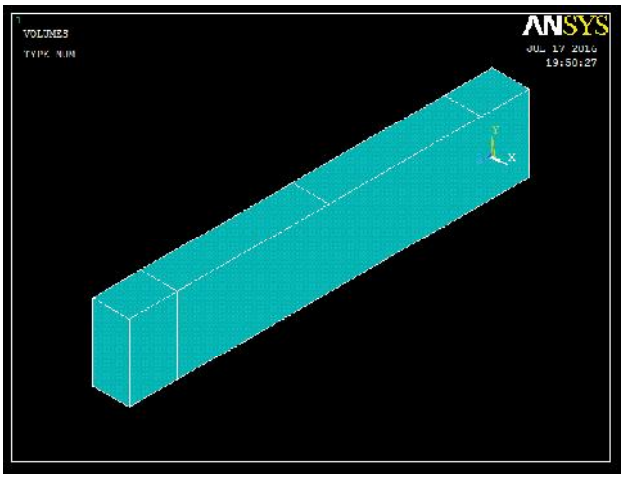

Figure 2. 3D Modeling of concrete beam

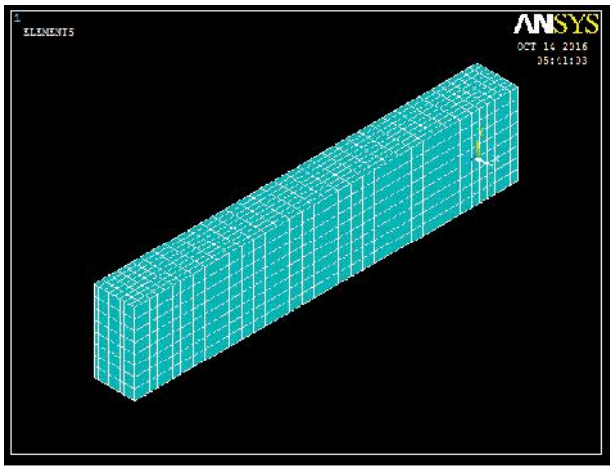

Figure 3. Elements of concrete beam

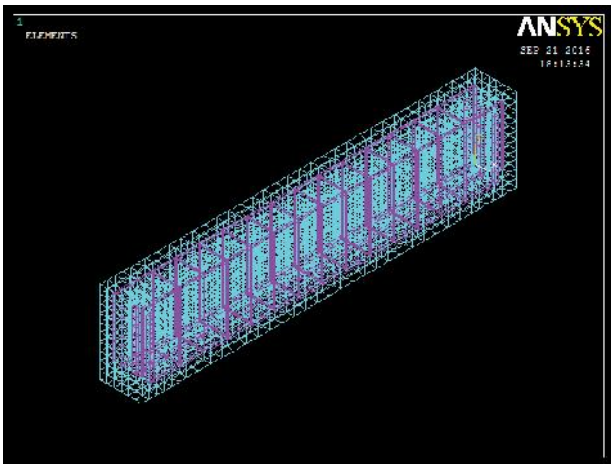

Figure 4. 3D Modeling of reinforced concrete beam

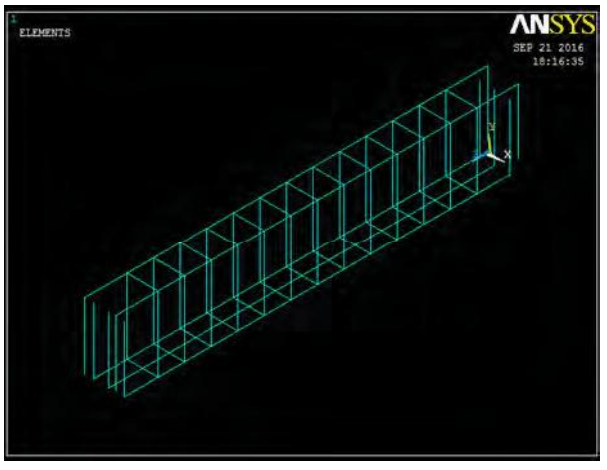

Figure 5. Reinforcement of beam

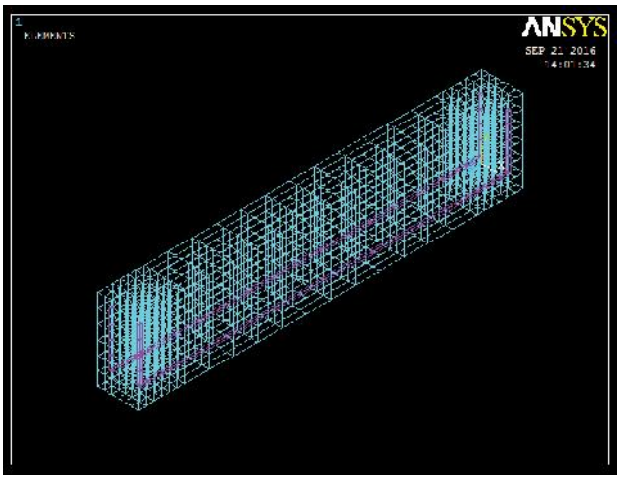

Figure 6. 3D Modeling of nominal tension reinforced concrete beam

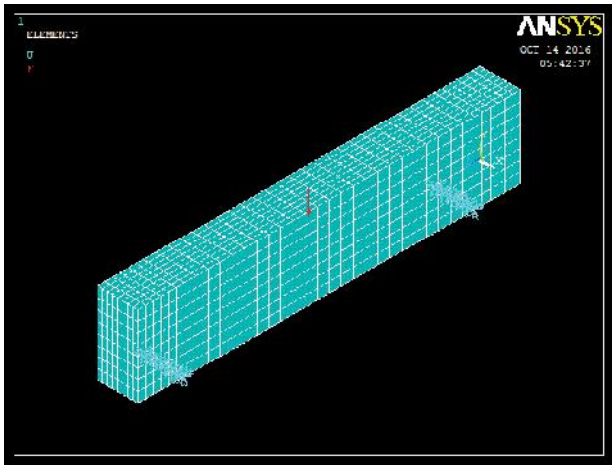

Figure 7. Application of load on reinforced concrete beam

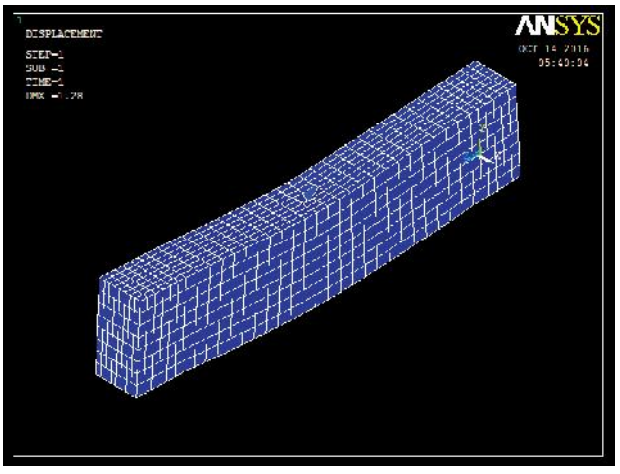

Figure 8. Deformed shape of reinforced concrete beam

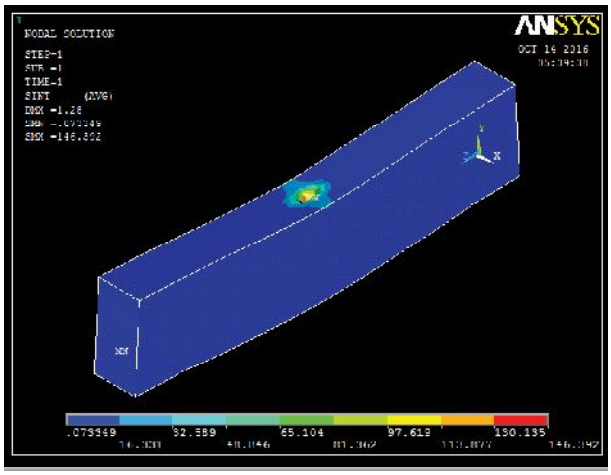

Figure 9. Stress intensity of reinforced concrete beam

IV. Analysis Of Reinforced Concrete Beams

In the present paper, the flexural behavior of reinforced concrete beams with minimum flexural tension reinforcement and the beams with the design reinforcement was studied by varying the concrete grades (M20,M25 and M30), grades of steel (Fe250,Fe415 and Fe500) and different beam width-to-depth ratios (0.5,0.6 and 0.7) under three point bending using ANSYS 12.1 version[12] through load-deflection diagrams. The variation of deflection, strain energy and stress intensity factor was studied for different beam width-to-depth ratios and different grades of concrete and steel and presented in Table IV to Table IX. Twenty seven reinforced concrete beams with minimum flexural reinforcement and twenty seven reinforced concrete beams with design reinforcement have been modeled and analysed in ANSYS and presented in Figure 2 to Figure 9. Total beams modeled and analysed were fifty four. The variation in the flexural behaviour of RC beams is studied with minimum Tension reinforcement and Design Tension reinforcement for different grades of steel and presented in Table X to Table XV and Figure 10 to Figure 21 respectively. Similarly the variation in the flexural behavior of RC beams is also studied using minimum Tension reinforcement and Design Tension reinforcement for different $\left(\frac{b}{D}\right)$ ratios and presented in Table XVI to Table XXI and Figure 22 to Figure 33 respectively.

TABLE IV
REINFORCED CONCRETE BEAM WITH MINIMUM TENSION REINFORCEMENT (Fe250)

Grade of steel	b/D	Grade of concrete	Peak load P_{max}	Max deflection Δ_{max}	Strain Energy N-mm	Stress intensity factor N/mm^2
Fe250	0.5	M20	483840	1.01	244339	54.564
		M25	482620	1.069	257960	58.645
		M30	481780	1.126	271242	62.064
	0.6	M20	484430	1.003	242942	54.021
		M25	483100	1.073	259183	58.152
		M30	482200	1.133	273166	61.497
	0.7	M20	485000	1.009	244682	53.484
		M25	483500	1.079	260848	57.436
		M30	482500	1.151	277679	60.849

TABLE V
REINFORCED CONCRETE BEAM WITH MINIMUM TENSION REINFORCEMENT (Fe415)

Grade of steel	b/D	Grade of concrete	Peak load P_{max}	Max deflection Δ_{max}	Strain Energy N-mm	Stress intensity factor N/mm^2
Fe415	0.5	M20	484300	0.957	231738	53.196
		M25	483000	1.013	244639.5	57.292
		M30	482000	1.07	257870	60.788
	0.6	M20	485000	0.956	231830	52.823
		M25	483500	1.012	244651	56.753
		M30	482500	1.073	258861	60.174
	0.7	M20	485380	0.957	232254	52.226
		M25	484000	1.017	246114	56.08
		M30	483000	1.085	262027.5	59.497

TABLE VI
REINFORCED CONCRETE BEAM WITH MINIMUM TENSION REINFORCEMENT (Fe500)

Grade of steel	b/D	Grade of concrete	Peak load P_{max}	Max deflection Δ_{max}	Strain Energy N-mm	Stress intensity factor N/mm^2
Fe500	0.5	M20	484500	0.937	226988	52.631
		M25	483000	0.986	238119	56.616
		M30	482000	1.037	249917	60.031
	0.6	M20	485000	0.936	226980	52.309
		M25	483700	0.988	238948	56.186
		M30	483000	1.044	252126	59.577
	0.7	M20	485600	0.935	227018	51.681
		M25	484140	0.993	240375	55.522
		M30	483000	1.058	255507	58.932

TABLE VII
REINFORCED CONCRETE BEAM WITH DESIGN TENSION REINFORCEMENT (Fe250)

Grade of steel	b/D	Grade of concrete	Peak load P_{max}	Max deflection Δ_{max}	Strain Energy N-mm	Stress intensity factor N/mm^2
Fe250	0.5	M20	483840	1.28	309657	146.392
		M25	482620	1.314	317081	156.926
		M30	481780	1.347	324478	167.464
	0.6	M20	484430	1.289	312215	149.408
		M25	483100	1.323	319570	159.068
		M30	482200	1.356	326931	168.69
	0.7	M20	485000	1.298	314765	149.392
		M25	483500	1.332	322011	159.378
		M30	482500	1.365	329306	169.916

TABLE VIII
REINFORCED CONCRETE BEAM WITH DESIGN TENSION REINFORCEMENT (Fe415)

Grade of steel	b/D	Grade of concrete	Peak load P_{max}	Maximum deflection Δ_{max}	Strain Energy N-mm	Stress intensity factor N/mm^2
Fe415	0.5	M20	484300	1.043	252562	87.65
		M25	483000	1.123	271204	106.892
		M30	482000	1.203	289923	126.134
	0.6	M20	485000	1.143	277177	92.675
		M25	483500	1.157	279704	111.917
		M30	482500	1.237	298426	130.152
	0.7	M20	485380	1.242	301421	97.421
		M25	484000	1.256	303952	115.654
		M30	483000	1.27	306705	133.887

TABLE IX
REINFORCED CONCRETE BEAM WITH DESIGN TENSION REINFORCEMENT (Fe500)

Grade of steel	b/D	Grade of concrete	Peak load P_{max}	Maximum deflection Δ_{max}	Strain Energy N-mm	Stress intensity factor N/mm^2
Fe500	0.5	M20	484500	0.948	229653	64.532
		M25	483000	1.031	248986	79.958
		M30	482000	1.113	268233	95.384
	0.6	M20	485000	0.964	233770	67.417
		M25	483700	1.047	253217	82.843
		M30	483000	1.133	273619	101.863
	0.7	M20	485600	0.982	238429	70.303
		M25	484140	1.067	258288	89.322
		M30	483000	1.153	278449	108.342

TABLE X
REINFORCED CONCRETE BEAM WITH MINIMUM TENSION REINFORCEMENT (Fe250)

Grade of steel	Grade of concrete	b/D	Peak load P_{max}	Maximum deflection Δ_{max}	Strain Energy N-mm	Stress intensity factor N/mm^2
Fe250	M20	0.5	483840	1.01	244339	54.564
		0.6	484430	1.003	242942	54.021
		0.7	485000	1.009	244682	53.484
	M25	0.5	482620	1.069	257960	58.645
		0.6	483100	1.073	259183	58.152
		0.7	483500	1.079	260848	57.436
	M30	0.5	481780	1.126	271242	62.064
		0.6	482200	1.133	273166	61.497
		0.7	482500	1.151	277679	60.849

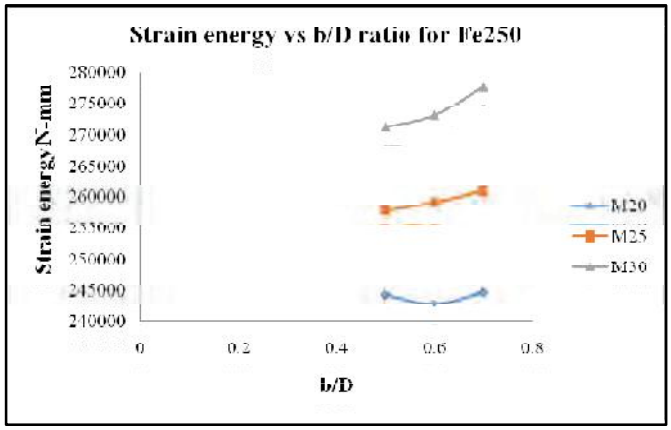

Figure10. Strain energy vs b/D ratio for Fe250

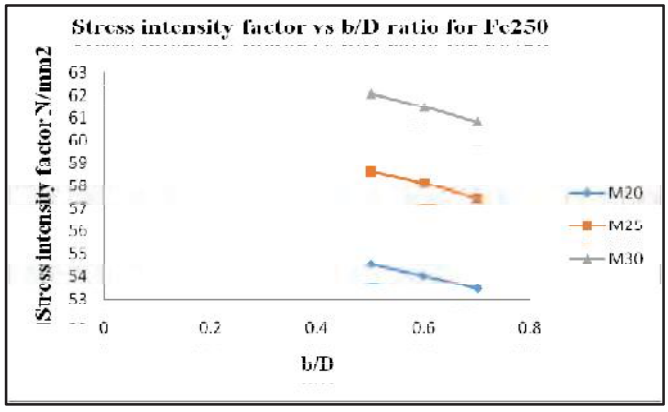

Figure11. Stress intensity factor vs b/D ratio for Fe250

TABLE XI
REINFORCED CONCRETE BEAM WITH MINIMUM TENSION REINFORCEMENT (Fe415)

Grade of steel	Grade of concrete	b/D	Peak load P_{max}	Maximum deflection Δ_{max}	Strain Energy N-mm	Stress intensity factor N/mm^2
Fe415	M20	0.5	484300	0.957	231738	53.196
		0.6	485000	0.956	231830	52.823
		0.7	485380	0.957	232254	52.226
	M25	0.5	483000	1.013	244639	57.292
		0.6	483500	1.012	244651	56.753
		0.7	484000	1.017	246114	56.08
	M30	0.5	482000	1.07	257870	60.788
		0.6	482500	1.073	258861	60.174
		0.7	483000	1.085	262027	59.497

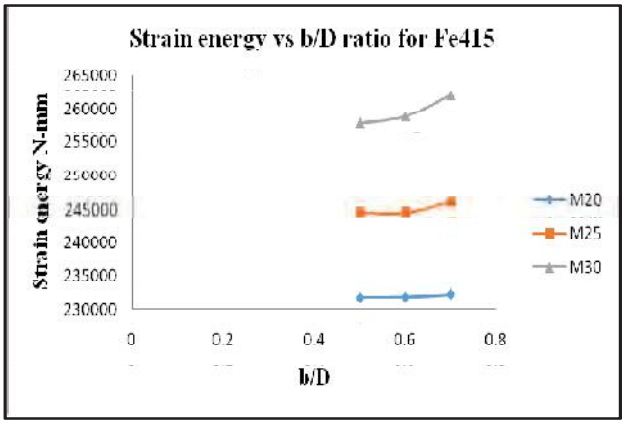

Figure12. Strain energy vs b/D ratio for Fe415

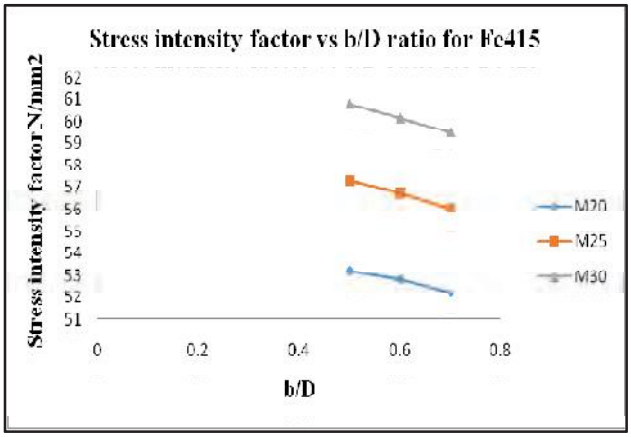

Figure13. Stress intensity factor vs b/D ratio for Fe415

TABLE XII
REINFORCED CONCRETE BEAM WITH MINIMUM TENSION REINFORCEMENT (Fe500)

Grade of steel	Grade of concrete	b/D	Peak load P_{max}	Maximum deflection Δ_{max}	Strain Energy N-mm	Stress intensity factor N/mm^2
Fe500	M20	0.5	484500	0.937	226988	52.631
		0.6	485000	0.936	226980	52.309
		0.7	485600	0.935	227018	51.681
	M25	0.5	483000	0.986	238119	56.616
		0.6	483700	0.988	238948	56.186
		0.7	484140	0.993	240375	55.522
	M30	0.5	482000	1.037	249917	60.031
		0.6	483000	1.044	252126	59.577
		0.7	483000	1.058	255507	58.932

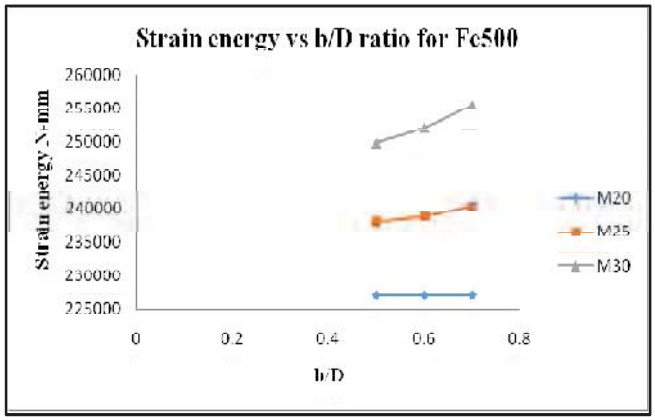

Figure14. Strain energy vs b/D ratio for Fe500

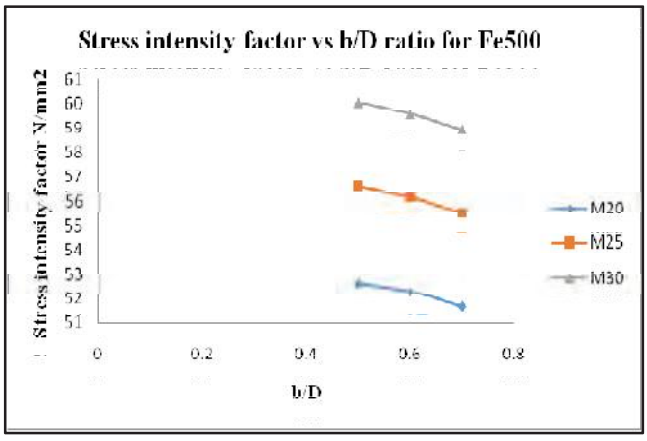

Figure15. Stress intensity factor vs b/D ratio for Fe500

TABLE XIII
REINFORCED CONCRETE BEAM WITH DESIGN TENSION REINFORCEMENT (Fe250)

Grade of steel	Grade of concrete	b/D	Peak load P_{max}	Maximum deflection Δ_{max}	Strain Energy N-mm	Stress intensity factor N/mm^2
Fe250	M20	0.5	483840	1.28	309657	146.392
		0.6	484430	1.289	312215	149.408
		0.7	485000	1.298	314765	149.392
	M25	0.5	482620	1.314	317081	156.926
		0.6	483100	1.323	319570	159.068
		0.7	483500	1.332	322011	159.378
	M30	0.5	481780	1.347	324478	167.464
		0.6	482200	1.356	326931	168.69
		0.7	482500	1.365	329306	169.916

TABLE XIV
REINFORCED CONCRETE BEAM WITH DESIGN TENSION REINFORCEMENT (Fe415)

Grade of steel	Grade of concrete	b/D	Peak load P_{max}	Maximum deflection Δ_{max}	Strain Energy N-mm	Stress intensity factor N/mm^2
Fe415	M20	0.5	484300	1.043	252562	87.65
		0.6	485000	1.143	277177	92.675
		0.7	485380	1.242	301421	97.421
	M25	0.5	483000	1.123	271204	106.892
		0.6	483500	1.157	279704	111.917
		0.7	484000	1.256	303952	115.654
	M30	0.5	482000	1.203	289923	126.134
		0.6	482500	1.237	298426	130.152
		0.7	483000	1.27	306705	133.887

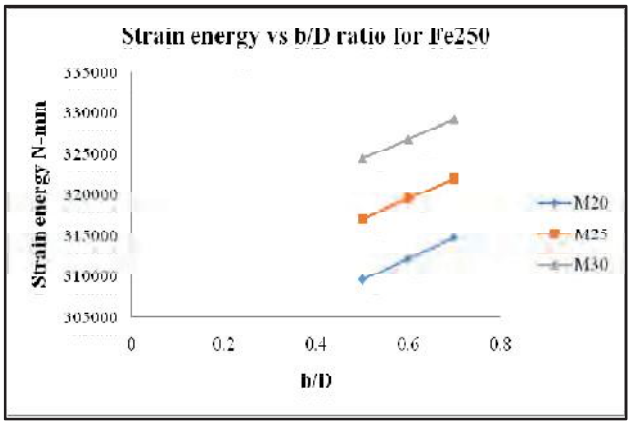

Figure16. Strain energy vs b/D ratio for Fe250

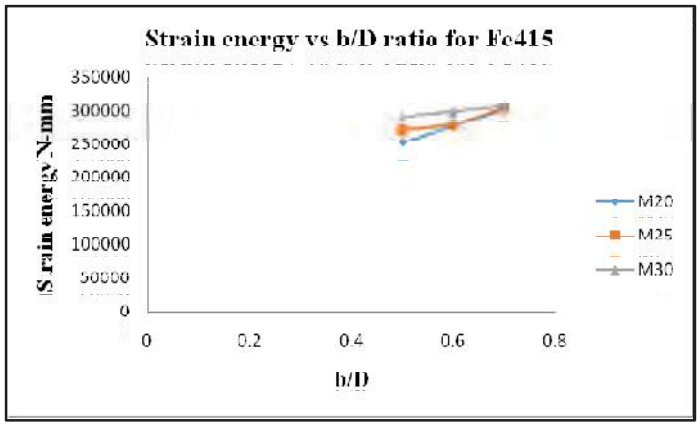

Figure18. Strain energy vs b/D ratio for Fe415

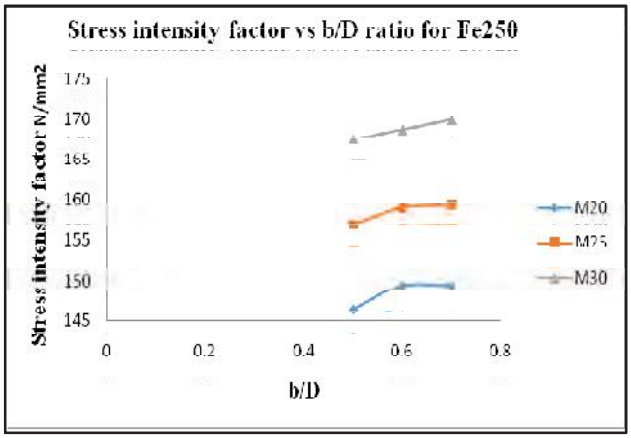

Figure17. Stress intensity factor vs b/D ratio for Fe250

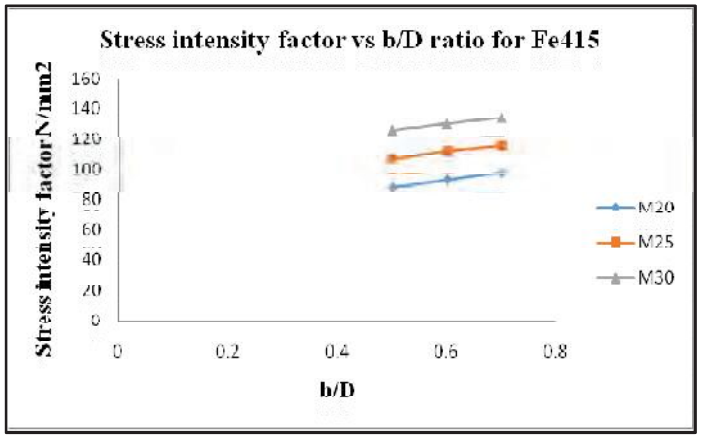

Figure19. Stress intensity factor vs b/D ratio for Fe415

TABLE XV
REINFORCED CONCRETE BEAM WITH DESIGN TENSION REINFORCEMENT (Fe500)

Grade of steel	Grade of concrete	b/D	Peak load P_{max}	Maximum deflection Δ_{max}	Strain Energy N-mm	Stress intensity factor N/mm^2
Fe500	M20	0.5	484500	0.948	229653	64.53
		0.6	485000	0.964	233770	67.41
		0.7	485600	0.982	238429	70.30
	M25	0.5	483000	1.031	248986	79.95
		0.6	483700	1.047	253217	82.84
		0.7	484140	1.067	258288	89.32
	M30	0.5	482000	1.113	268233	95.38
		0.6	483000	1.133	273619	101.86
		0.7	483000	1.153	278449	108.34

TABLE XVI
REINFORCED CONCRETE BEAM WITH MINIMUM TENSION REINFORCEMENT (b/D=0.5)

b/D	Grade of concrete	Grade of steel	Peak load P_{max}	Maximum deflection Δ_{max}	Strain Energy N-mm	Stress intensity factor N/mm^2
0.5	M20	Fe250	483840	1.01	244339	54.564
		Fe415	484300	0.957	231738	53.196
		Fe500	484500	0.937	226988	52.631
	M25	Fe250	482620	1.069	257960	58.645
		Fe415	483000	1.013	244639	57.292
		Fe500	483000	0.986	238119	56.616
	M30	Fe250	481780	1.126	271242	62.064
		Fe415	482000	1.07	257870	60.788
		Fe500	482000	1.037	249917	60.031

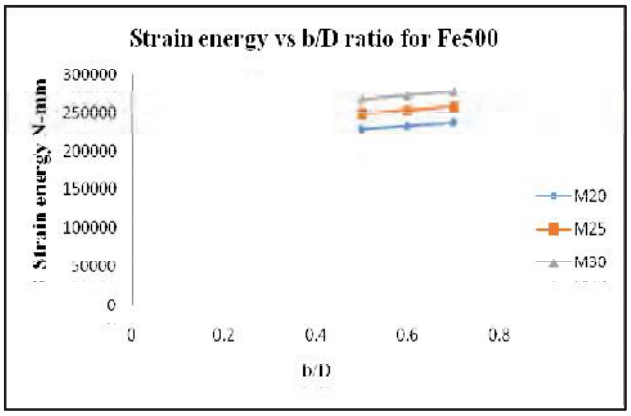

Figure20. Strain energy vs b/D ratio for Fe500

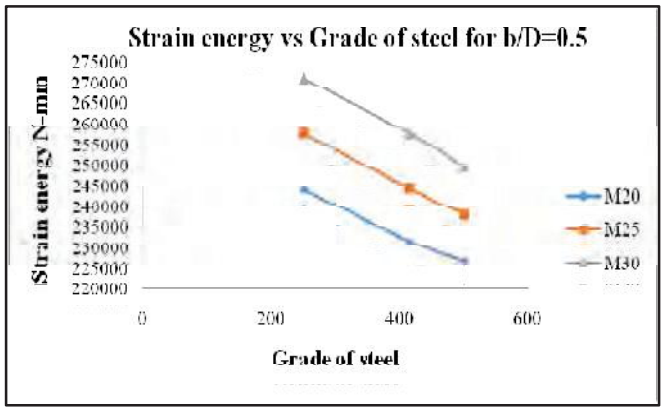

Figure22. Strain energy vs grade of steel for b/D=0.5

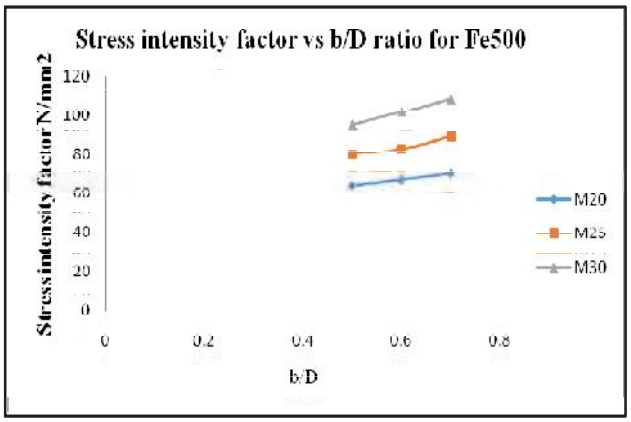

Figure21. Stress intensity factor vs b/D ratio for Fe500

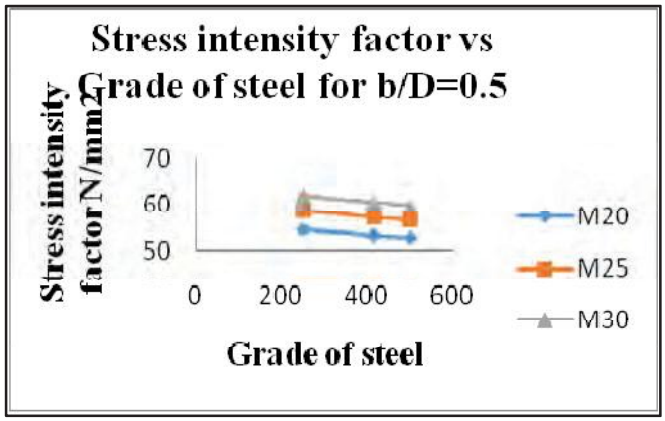

Figure23. Stress intensity factor vs grade of steel for b/D=0.5

TABLE XVII
REINFORCED CONCRETE BEAM WITH MINIMUM TENSION REINFORCEMENT (b/D=0.6)

b/D	Grade of concrete	Grade of steel	Peak load P_{max}	Maximum deflection Δ_{max}	Strain Energy N-mm	Stress intensity factor N/mm^2
0.6	M20	Fe250	484430	1.003	242942	54.021
		Fe415	485000	0.956	231830	52.823
		Fe500	485000	0.936	226980	52.309
	M25	Fe250	483100	1.073	259183	58.152
		Fe415	483500	1.012	244651	56.753
		Fe500	483700	0.988	238948	56.186
	M30	Fe250	482200	1.133	273166	61.497
		Fe415	482500	1.073	258861	60.174
		Fe500	483000	1.044	252126	59.577

TABLE XVIII
REINFORCED CONCRETE BEAM WITH MINIMUM TENSION REINFORCEMENT (b/D=0.7)

b/D	Grade of concrete	Grade of steel	Peak load P_{max}	Maximum deflection Δ_{max}	Strain Energy N-mm	Stress intensity factor N/mm^2
0.7	M20	Fe250	485000	1.009	244682	53.484
		Fe415	485380	0.957	232254	52.226
		Fe500	485600	0.935	227018	51.681
	M25	Fe250	483500	1.079	260848	57.436
		Fe415	484000	1.017	246114	56.08
		Fe500	484140	0.993	240375	55.522
	M30	Fe250	482500	1.151	277679	60.849
		Fe415	483000	1.085	262027	59.497
		Fe500	483000	1.058	255507	58.932

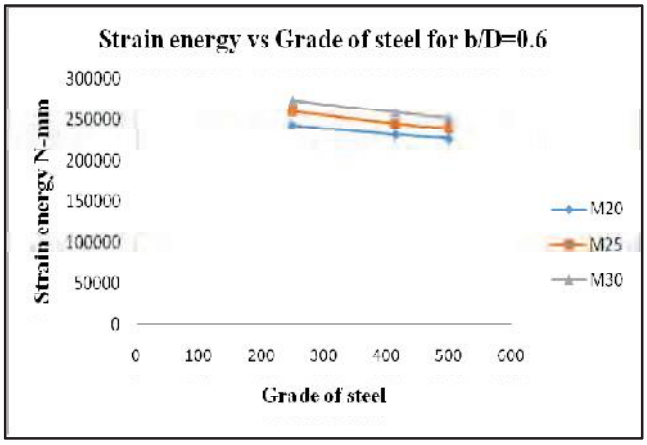

Figure24. Strain energy vs grade of steel for b/D=0.6

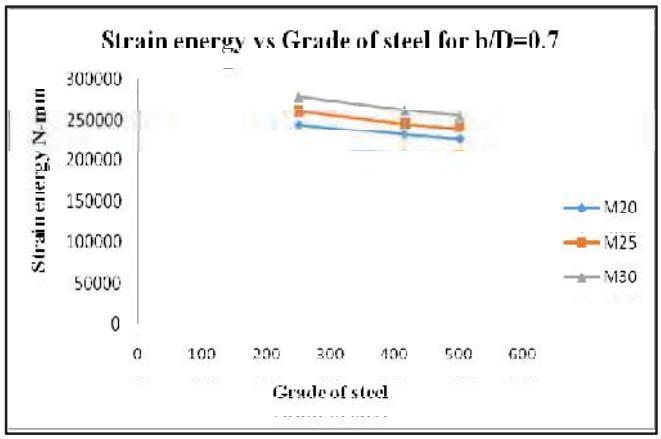

Figure26. Strain energy vs grade of steel for b/D=0.7

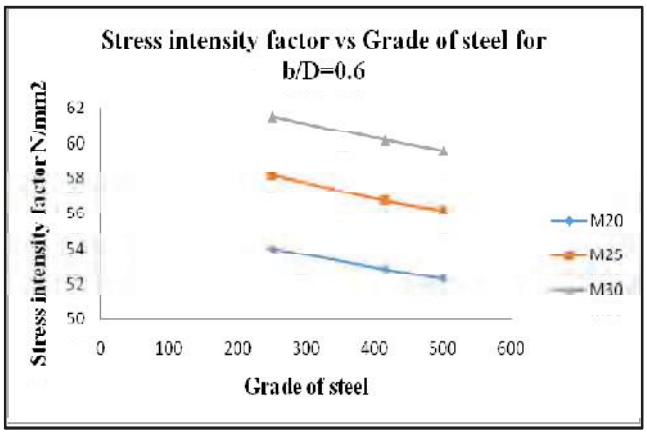

Figure25. Stress intensity factor vs grade of steel for b/D=0.6

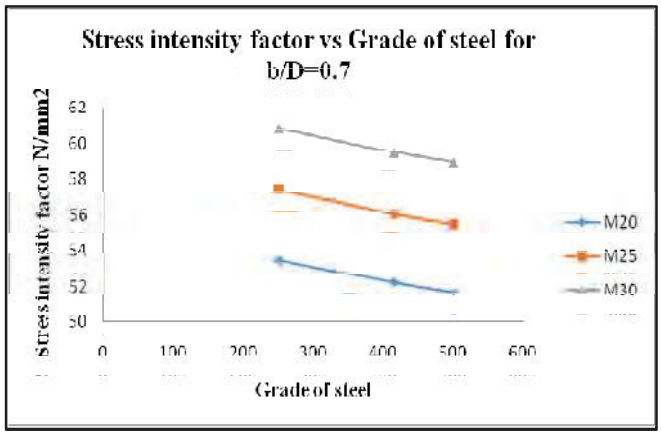

Figure27. Stress intensity factor vs grade of steel for b/D=0.7

TABLE XIX
REINFORCED CONCRETE BEAM WITH DESIGN TENSION REINFORCEMENT (b/D=0.5)

b/D	Grade of concrete	Grade of steel	Peak load P_{max}	Maximum deflection Δ_{max}	Strain Energy N-mm	Stress intensity factor N/mm^2
0.5	M20	Fe250	483840	1.28	309657	146.392
		Fe415	484300	1.043	252562	87.65
		Fe500	484500	0.948	229653	64.532
	M25	Fe250	482620	1.314	317081	156.926
		Fe415	483000	1.123	271204	106.892
		Fe500	483000	1.031	24898	79.958
	M30	Fe250	481780	1.347	324478	167.464
		Fe415	482000	1.203	289923	126.134
		Fe500	482000	1.113	268233	95.384

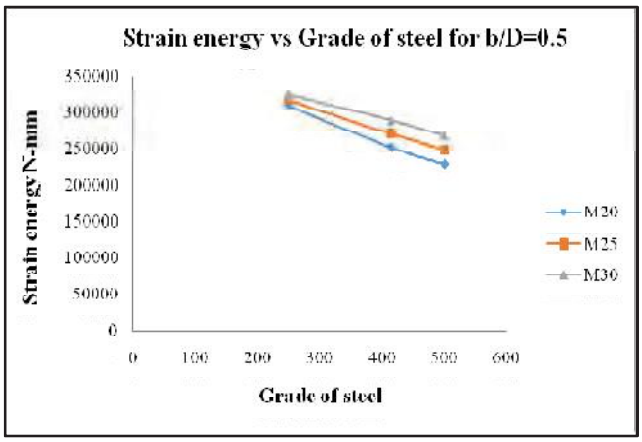

Figure28. Strain energy vs grade of steel for b/D=0.5

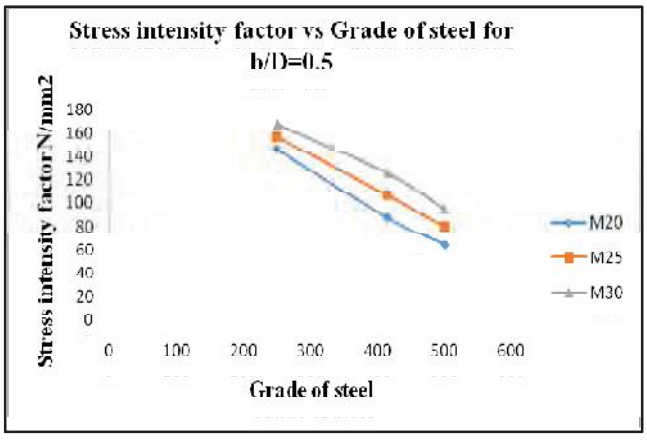

Figure29. Stress intensity factor vs grade of steel for b/D=0.5

TABLE XX
REINFORCED CONCRETE BEAM WITH DESIGN TENSION REINFORCEMENT (b/D=0.6)

b/D	Grade of concrete	Grade of steel	Peak load P_{max}	Maximum deflection Δ_{max}	Strain Energy N-mm	Stress intensity factor N/mm^2
0.6	M20	Fe250	484430	1.289	312215	149.408
		Fe415	485000	1.143	277177	92.675
		Fe500	485000	0.964	233770	67.417
	M25	Fe250	483100	1.323	319570	159.068
		Fe415	483500	1.157	279704	111.917
		Fe500	483700	1.047	253217	82.843
	M30	Fe250	482200	1.356	326931	168.69
		Fe415	482500	1.237	298426	130.152
		Fe500	483000	1.133	273619	101.863

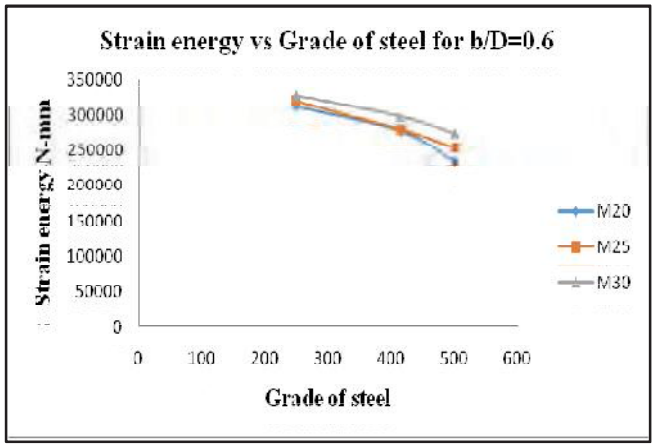

Figure30. Strain energy vs grade of steel for b/D=0.6

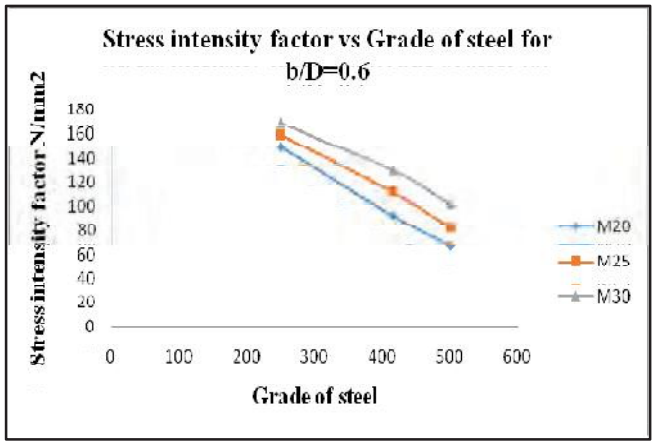

Figure31. Stress intensity factor vs grade of steel for b/D=0.6

TABLE XXI
REINFORCED CONCRETE BEAM WITH DESIGN TENSION REINFORCEMENT (b/D=0.7)

b/D	Grade of concrete	Grade of steel	Peak load P_{max}	Max deflection Δ_{max}	Strain Energy N-mm	Stress intensity factor N/mm^2
	M20	Fe250	485000	1.298	314765	149.392
		Fe415	485380	1.242	301421	97.421
		Fe500	485600	0.982	238429	70.303
	M25	Fe250	483500	1.332	322011	159.378
		Fe415	484000	1.256	303952	115.654
		Fe500	484140	1.067	258288	89.322
	M30	Fe250	482500	1.365	329306	169.916
		Fe415	483000	1.27	306705	133.887
		Fe500	483000	1.153	278449	108.342

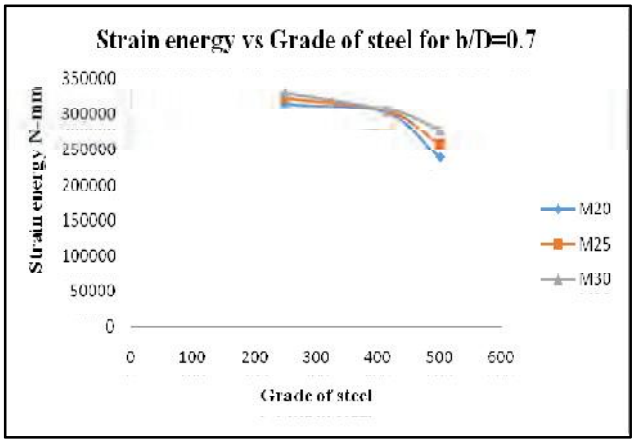

Figure32. Strain energy vs grade of steel for b/D=0.7

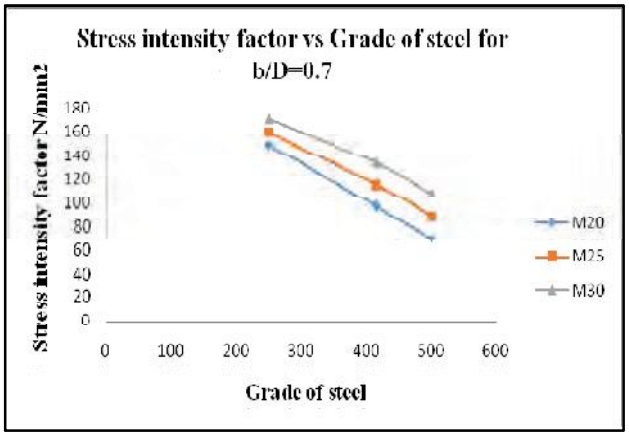

Figure33. Stress intensity factor vs grade of steel for b/D=0.7

V. CONCLUSIONS

The flexural behavior of the reinforcedconcrete beams of different grades of steel (Fe250, Fe415 and Fe500), different grades of concrete (M20, M25 and M30) and width to total depth ratios (0.5, 0.6 and 0.7) has been analyzed based on the modelling of beams in ANSYS and the variation of strain energy and stress intensity factor has been studied and presented below.

Reinforced concrete beams with minimum flexural reinforcement:

1. In case of Reinforced concrete beams with minimum flexural reinforcement, for a particular grade of steel and b/D ratio, the strain energy and stress intensity factor was observed to be increasing with the increasing grade of concrete.
2. Similarly, for a particular grade of steel and grade of concrete, the Reinforced concrete beams with minimum flexural reinforcement have shown that the strain energy as increasing with the increasing b/D ratio.
3. For a particular grade of steel and grade of concrete, Reinforced concrete beams with minimum flexural reinforcement have shown that the stress intensity factor was decreasing with the increase in b/D ratio.
4. Similarly, for a particular b/D ratio and grade of concrete, Reinforced concrete beams with minimum flexural reinforcement have shown that the strain energy and stress intensity factor as decreasing with the increasing grade of steel.

Reinforced concrete beams with designed reinforcement:

1. In case of Reinforced concrete beams with designed reinforcement, for a particular grade of steel and b/D ratio, the strain energy and stress intensity factor was observed to be increasing with the increasing grade of concrete.
2. Similarly, for a particular grade of steel and grade of concrete, Reinforced concrete beams with designed reinforcement have shown that the strain energy and stress intensity factor as increasing with the increasing b/D ratio.
3. For a particular b/D ratio and grade of concrete, the Reinforced concrete beams with designed reinforcement have shown that the strain energy and stress intensity factor as decreasing with the increasing grade of steel.

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[12] AnsysTutorials, release 12.1

[13] IS 456-2000 clause 26.2.1, clause 40.4, ANNEX G clause 38.1.

A Case Study on Effect of Lead Effluent from Batteries on Soil Properties.

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Abstract— **Recent method of construction requires not only basic study of the foundation materials, but also a well developed knowledge of the reasons responsible to the modifications in the course of the life of the structures resisted by it. The major source of surface and subsurface contamination are land disposal of industrial, mining, agricultural wastes and accidental spillage of chemicals during the course of industrial operations. . The unintended modification of soil properties due to interactions with contaminants can lead to various geotechnical problems. Lead–acid batteries also know as storage batteries are used primarily in automobiles, trains and other motor vehicles. As the name implies, lead acid batteries contain predominantly lead and sulphuric acid. In the present investigation, Battery effluent obtained from an industry situated near the pilgrim town of Tirupati has been added as contaminated to the Local soil collected from the CRS area near Tirupati. Soil properties has changed like Atterberg limits increases, Swell index increases, Unit weight of soil decreases, Unconfined Compressive Strength decreases, CBR value decreases with increase in Lead content. cohesion of soil decreases and Angle of internal friction increases with increase in Lead**

Index terms— Effect of battery effluents, Atterberg limits, swell index, pH, CBR, UCS, Shear parameters.

I. INTRODUCTION

The Bulk wastes from industrial, commercial, mining, agricultural and domestic activities cause soil and ground water contamination. The leachate can move down under gravity and contaminate the ground water resources. The polluted water will attack foundation structures such as footings, caissons, piles, and sheet piles. If the polluted water is used for mixing concrete, it will affect the workability and durability of the concrete. In embankment construction, the moisture-unit weight relationship of soil also will be affected. Hence, providing engineering solutions to minimize surface and subsurface contamination has become the dominant concern of governmental regulatory agencies and of geotechnical engineers. The lead battery contains of 17 percent metallic lead, 50 percent of lead oxide/sulfate, 24 percent of electrolyte, 5 percent of plastics and 4 percent of inert residuals. A mixture of 10% percent lead monoxide and 30% metallic lead, are used to manufacture lead acid batteries. Lead monoxide is the most key component of lead, based on volume. Waste battery paste has been analyzed by standard methods (APHA 1997). The composition consists of lead monoxide: 27.77%, lead sulfate: 63.08%, free lead: 7.44%, total lead: 75.42% (LOA technical notes, 1992).

TABLE I.
PROPERTIES OF LEAD

Atomic Number	82
Atomic Weight	207.21
Density , g/cc	11.34g/cc
Tensile Strength , Ultimate	18MPa
Modules of Elasticity	14GPa
Poisson's Ratio	0.42
Melting Point 0c	327 Deg
Boiling Point 0c	175 Deg

A. properties considered in this investigation:

1. Plasticity Characteristics
   (i)Liquid Limit
   (ii)Plastic Limit
   (iii)Plasticity Index
2. Hydrogen ion concentration (pH)
3. Swelling Characteristics
   (i)Differential Free Swell Index (DFSI)
   (ii)Swelling Pressure
4. Compaction Characteristics
   (i)Maximum Dry Unit Weight (MDU)
   (i)Optimum Pore Fluid Content (OPC)
5. California Bearing Ratio (CBR) Values
6. Strength characteristics
   (a)Unconfined Compression Strength
      (i)Effect of curing period
      (ii) Effect of pore fluid content
   (b)Triaxial Compression Strengt

II. LITERATURE REVIEW

Karen D bradhamand Elizabeth a Dayton (2006) have investigated Effect of soil properties on lead bioavailability and toxicity. **F. Gil Stores and C. Traser–cepeda (2004)** established different approaches to evaluating soil quality using biochemical properties. **W. J. Bond (1998)** have studied Effluent irrigation—an environmental challenge for soil science. **Zhen-Guo Shen, Xiang-Dong Li et.al (2001)** have investigated Lead Phytoextraction from Contaminated Soil with High Biomass Plant Species. **Dr.jevan singh and Ajay.s. kalamdhad (2011)** have investigated the effect of Heavy metals on soil, Human, health and Aquatic life..

III. MATERIALS USED

SOIL: The crystalized and powdered material passing through I.S.4.75 mm sieve is taken for the examination. The

soil is classified as 'SC' as per I.S. Classification (IS 1498:1978) indicating that it is clayey sand. The properties of the soil are given in below Table. It is highly expansive in nature as the (DFSI) Differential Free Swell Index is about percent.

TABLE II.
PROPERTIES OF THE UNCONTAMINATED SOIL

SI.No.	Property	Value
1.	Grain size distribution	
	(a)Gravel (%)	2
	(b)Sand (%)	67
	(c)Silt and Clay (%)	31
2.	Atterberg Limits	
	(a) Liquid Limit (%)	77
	(b)Plastic Limit (%)	30
	(c) Plasticity Index (%)	47
3.	Differential free swelling Index (%)	254.54
4.	Swelling pressure (kN/m^2)	246
5.	Specific gravity	2.76
6.	pH value	8.45
7.	Compaction characteristics	
	(a) Maximum dry unit weight (kN/m^3)	18.49
	(b)Optimum moisture content (%)	12.8
8.	California Bearing Ratio Value (%)	
	(a) at 2.5 mm penetration	10.236
	(b) at 5.0mm penetration	8.990
9.	Unconfined Compression Strength (kN/m^2)	217
10.	Triaxial Compression Test Results	
	(a)Angle of Internal Friction (degrees)	3.4
	(b)Cohesion (kN/m^2)	66.3

BATTERY EFFLUENT

Battery effluent is a colorless liquid and soluble in water

TABLE III.
CHEMICAL COMPOSITION OF BATTERY EFFLUENT

SI.No.	Parameter	Value
1.	Color	White
2.	pH	8.45
3.	Sulphates	250 mg/l
4.	Chlorides	30 mg/l
5.	Lead Monoxide	27.77%
6.	Lead Sulfate	63.08%
7.	Free Lead	7.44%
8.	Total Lead	75.42%
9.	BOD	110 mg/l
10.	COD	320 mg/l

TABLE IV.
PLASTICITY CHARACTERISTICS OF CONTAMINATED SOIL

Battery Effluent (%)	Plastic Limit (%)	Liquid Limit (%)	Plasticity Index (%)
0	30	77	47
20	30.5	79	48.5
40	31	80.5	49.5
60	31.5	82	50.5
80	32	83	51
100	32.5	84	51.5

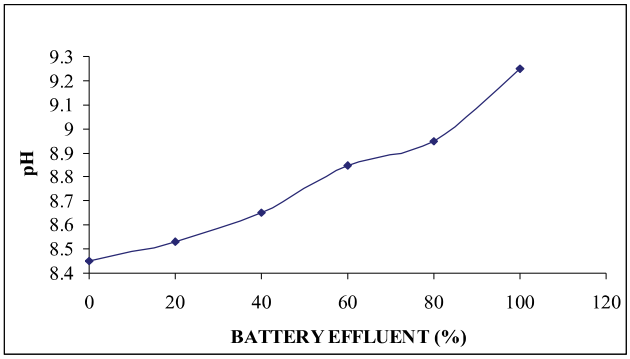

Figure 1. Varitation of pH with percentage of battery effluent

The pH value of uncontaminated soil is 8.45.From the above fig. it is observed that, the pH value of contaminated soil increases with per cent increase in Battery effluent.

TABLE V.
DIFFERENTIAL FREE SWELL INDEX OF CONTAMINATED SOIL

Battery Effluent (%)	DFSI(%)	Percent increase in DFSI
0	254.54	-----
20	255.45	0.36
40	256.36	0.71
60	259.1	1.79
80	261.82	2.86
100	272.73	7.15

The variation of Differential Free Swell Index with per cent Battery effluent is shown in Table V. It is observed that the Differential Free Swell Index rices a little with per cent rise in Battery effluent. The per cent increase in the Differential Free Swell Index is about 7% at 100% of Battery effluent

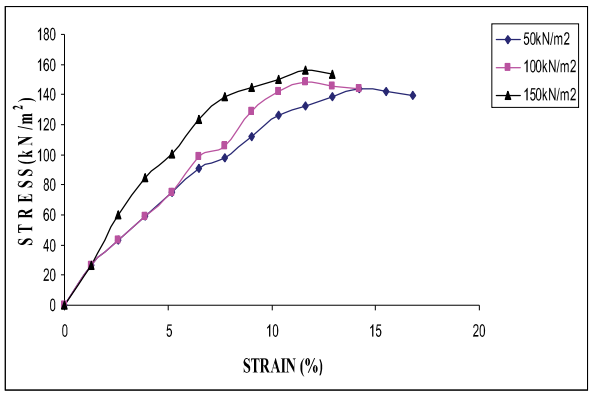

Figure 2. Deviator stress versus strain for soil contaminated with 0% battery effluent

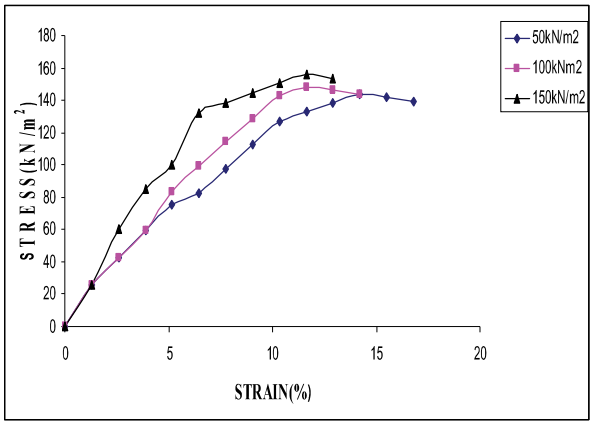

Figure 3. Deviator stress versus strain for soil contaminated with 20% battery effluent

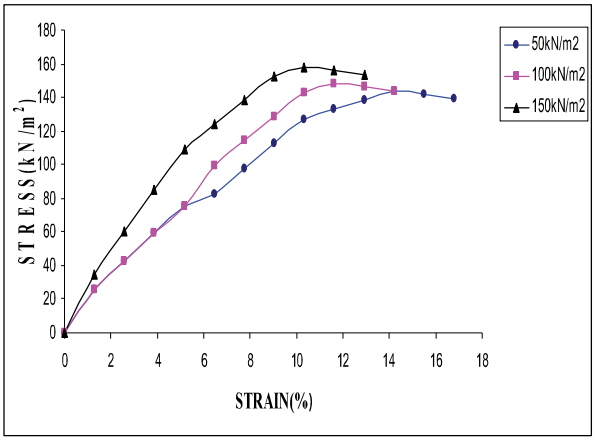

Figure 4. Deviator stress versus strain for soil contaminated with 40% battery effluent

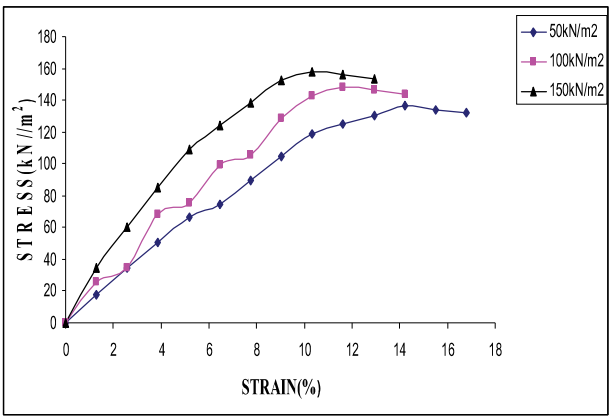

Figure 5. Deviator stress versus strain for soil contaminated with 60% battery effluent

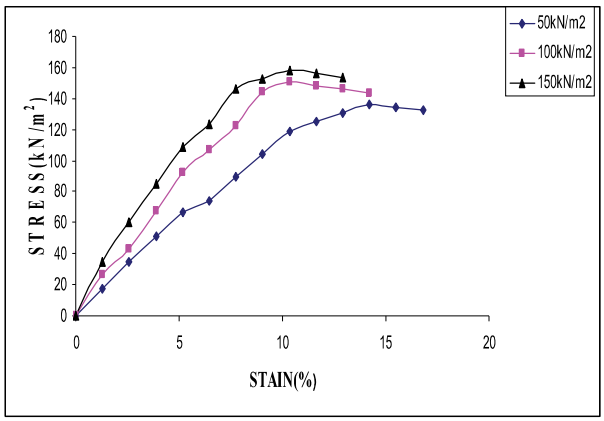

Figure 6. Deviator stress versus strain for soil contaminated with 80% battery effluent

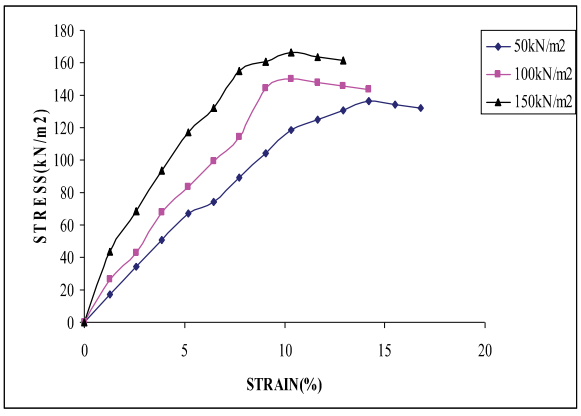

Figure 7. Deviator stress versus strain for soil Contaminated with 100% battery effluent

TABLE VI. ANGLE OF INTERNAL FRICTION AND COHESION OF SOIL CONTAMINATED WITH BATTERY EFFLUENT

Battery Effluent (%)	Cohesion (C)	Angle of Internal Friction (Φ)	Percentage Decrease in Cohsion(C)	Percentage Increase in Angle of Internal Friction(Φ)
0	65.04	3.4	---	----
20	61.214	4.3	5.88	26.47
40	58.762	5.4	19.652	58.82
60	55.721	6.3	14.33	85.29
80	53.857	7.25	17.2	113.23
100	51.60	8.03	20.664	136.18

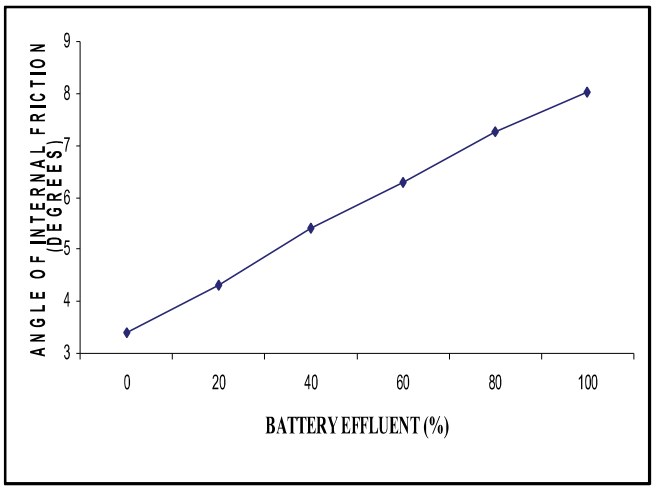

Figure 8. Angle of internal friction versus percentage of battery effluent

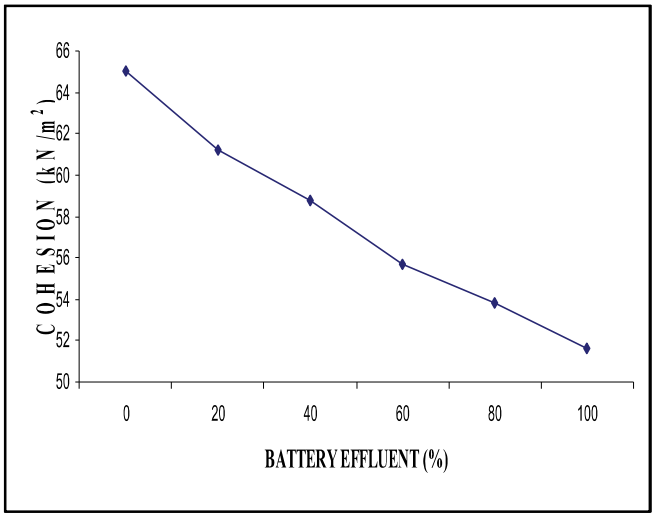

Figure 9. Cohesion versus percentage of battery effluent

V. CONCLUSIONS

1. With successive increase of 20% battery effluent Liquid limit varies 2% up to 60 and later varies in 1%. Plastic limit values of the contaminated soil varies 0.5%with increase of 20% Battery effluent.
2. The Plasticity index values of the contaminated soil also increases at a rate of 0.5% with increase of 20% Battery effluent.
3. pH of the soil increases at a rate of 1.5 with increase of 20% battery effluent
4. Differential Free Swelling index increases at rate of 1% up to 60% effluent, for 80% it increases 2.86% and for 100% it increases 7.15% and Swelling pressure increase slightly with increase in per cent Battery effluent.
5. The contaminated soil is susceptible to heaving and shrinkage at 100% Battery effluent.
6. There is a small increment (1 percent) in optimum pore fluid content as % increase in 20% of effluent from Battery.
7. The maximum dry unit weight of contaminated soil decreases slightly (1 percent) with increase in 20 percentage of effluent from Battery.
8. The California Bearing Ratio (CBR) values of the soil at 2.5 mm and 5.0 mm penetrations contaminated with Battery effluent decrease at a rate of 5 per cent increase in 20% of Battery effluent.
9. The Unconfined compressive strength of the contaminated soil decreases at a rate of 3 %with increase in curing period irrespective of per cent Battery effluent.
10. The Unconfined compressive strength of contaminated soil decreases at a rate of 2 % with increase in 20 percentage of Battery effluent irrespective of curing period.
11. The angle of internal friction of soil contaminated with Battery effluent increases at a rate of 1% with increase in 20 per cent Battery effluent.
12. The cohesion values of the soil contaminated with Battery effluent decreases at a rate of 2% with increase in 20 percentage of Battery effluent.
13. The stability of a soil mass is deteriorated due to contamination by Battery effluent.

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Response of Reinforced Concrete Structural Components Subjected to the Blast Loading

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Abstract— **A explosion within or nearby a structure causes disastrous damage to internal and external structural system. These explosions cause masonry walls to collapse, blowing out large stretches of windows and closing all critical life-safety systems. Casualty occur due to direct contact with blast, structure failure, buried under debris, fire or smoke. Major catastrophes from gas-chemical explosions are cause for rise in large dynamic loads greater than the actual design loads. Efforts have been made to develop design and analysis methods to reduce the threats from extreme loading conditions. Study carried out on response of concrete under impact loads, enhance the understanding the role of structural design play in affecting the behaviour. Analysis and design of buildings under blast loads requires detailed study of dynamic response of structure. In this paper, the response of RC frame subjected to internal blast loads is studied. The RC frame was modelled in a finite element software (Abaqus). For the response evaluation, an internal explosion was first created inside a room and the equilibrium state was determined.**

Index Terms— **explosion, impact, Abaqus, impact, structural response, air blast, simulation.**

I. Introduction

Due to terrorist events in the past, design of structures against blast loading got importance. The conventional structures are not analysed for blast load. When blast loads are considered in design, the cost of design and execution becomes uneconomical. Recent incidents in the country forced the designers finding answers for protecting the occupants and building from blast loading [11]. Special courtesy is given for blast loads on ground breaking structures, such as sky scrapers in urban cities. The explosions inside and around the structure can affect the structural integrity of the building. Such damage to internal and external building frames can collapse entire system. The performance of high-rise buildings under influence of blast is of great importance to provide buildings which reduce damage to structure and property in the event of explosion. The analysis and design of blast resistant structures involves detail study on blast phenomenon, blast effects and the nature of explosives.

Objective

To accurately model flexural steel reinforcement as well as vertical shear reinforcement, study of interaction between flexural and shear reinforcement is a significant task. Broad assessment of the reliability of non-linear analysis for understanding reinforced building components subjected to impact loading react has been addressed.

Significant objectives addressed by this thesis are as to examine the effect of different non-linear material models which are accessible in the ABAQUS/Explicit material archive on the dynamic response of reinforced structural components, evaluate the effect of modelling different types of reinforcement in reinforced structural components subjected to impact loading and to simulate the distribution of crack and determine critical regions of elements.

Scope

To achieve the above objectives, tasks involving computations were carried. RC frame with openings has been subjected to dynamic loadings and the effect of blast pressure on structural components is evaluated.

II. Background

A. Explosion and Blast Phenomena

A Blast or explosion is outcome of an instant discharge of enormous energy confined to a limited space. Explosions are divided based on their nature as chemical, physical and nuclear events [12].

i) In Chemical Explosion: In chemical explosion**,** quick oxidation of fuel components (carbon and hydrogen atoms) is the prime source of energy.
ii) In Physical Explosion: In physical explosion, energy is unconstrained from the disastrous failure of cylinder containing compressed gas, volcanic eruption or mixing liquids at different temperature.
iii) In Nuclear Explosion: In nuclear explosion, energy is released from the construction of different atomic nuclei. It is caused by redistribution of the protons and neutrons within the inner acting nuclei.

The catastrophic action of a nuclear weapon due to blast or shock is much more severe than that of a conventional weapon. In a typical air burst at an altitude below 1,00,000 ft., an approximate distribution of energy would consist of 50% blast or shock, 35% thermal radiation, 10% residual nuclear radiation and 5% initial nuclear radiation [12].

A shock wave is a rapid release of energy which triggers a pressure wave in the surrounding atmosphere. As the wave travels far away from the point of explosion, the interior part that was previously compressed travels through the region

and gets heated by the foremost part of the wave. As the pressure waves travels with the velocity of sound, the temperature reaches 3000°C-4000°C [12] and the pressure is around 300 kb of the air cause this velocity to surge. The inner part of the wave starts to move faster and overtakes the leading part of the wave. After a short duration, the pressure wave front becomes rapid thus forming a shock. The maximum pressure forms at the shock front and is known as the peak overpressure. Behind the shock front, the overpressure falls very rapidly to about one-half the peak overpressure and remains constant in the core part of the explosion.

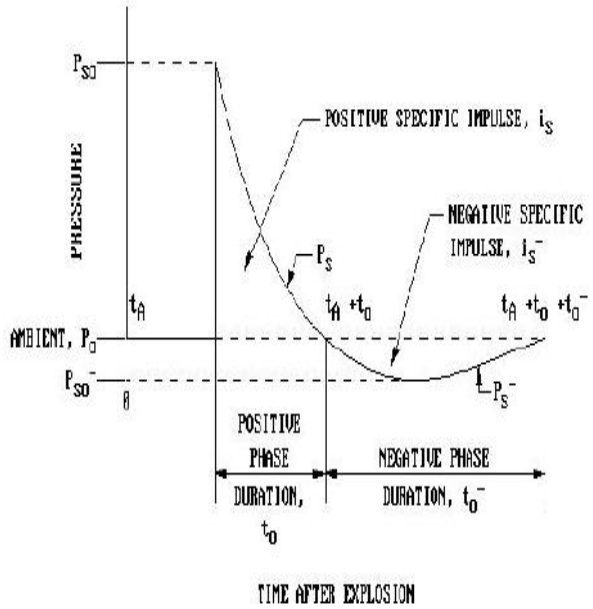

Figure1. variation of overpressure with distance at a given time from centre of explosion [8].

The pressure behind the front falls off in a standard manner without being constant. After the session, at a certain distance from the centre of explosion, the pressure behind the shock front decreases than that of the surrounding atmosphere and is called Negative Phase.

B. Difference between Blast Loads and Seismic Loads

Blast loadings are applied over a considerably short duration of time than seismic loads. Thus, the material strain rate effects become dangerous and are included to evaluate performance of short period loadings such as blast loads. Blast loads usually are applied non-uniformly onto a structure. There is difference in load amplitude across the surface of the building and radically reduces on the sides and end of the structure. The effects of blast loads are largely local, leading to severe damage or failure. Seismic loads are ground motions applied unvaryingly across the base of the building. All building components are subjected to "shaking" in association with this motion [11].

The difference between seismic excitations and blast-resistant design is the need for distribution of ductility over the entire building. Strong ground motions disturb entire lateral resisting system. The resistance to blast loading is more concentrated near the point where explosion occurred. The plastic hinges in the beams spread throughout the structure, as the Moment resisting frames provide high ductility and energy absorption.

The beam-column connections will develop flexural hinge in the beam. The distribution of deformation is inelastic throughout the structure. The elements are proportioned to prevent plastic story mechanisms which limit the inelastic energy absorbed in the isolated regions of the frame. This is achieved by "strong-column, weak-beam" (SCWB) methodology for blast and seismic resistant design. Since blast loading is more localized than seismic excitations, the resulting plastic hinge is more limited to a small area, with more severe rotations than those from strong ground movements. Structural systems such as concentrically and eccentrically braced frames can efficiently resist the lateral forces due to seismic activities. Such kind of systems can be considered on a case by case basis for use in blast-resistant design.

C. Influence of Blast Loads on Structures

The reflection of shock front influences the stress and duration of impulse. The ground under the explosion reflects the waves on to the surface of building. The pressures are magnified as a function of proximity, material characteristics of impacted object post reflection. Stronger the object, greater is the reflected energy because a lesser amount of energy is dissipated by the response of the surface. These variations are often neglected in conservative design [11].

Facades are designed to reflect the shock waves perfectly. Designers assume that the facade components remain static for duration of the impact shock front, causing peak pressures and impulses sufficient to reverse their direction. There is displacement of the facade during the blast loading. The displacement of façade reduces the efficiency of the reflector. Designing the facade to resist the blast load makes the structure become a support for blast loads. Depending on performance conditions, designers validate resistance of the framing system against applied loads. The building shall remain standing with an acceptable level of damage.

III. FINITE ELEMENT MODELLING

Due to restrictions in computing technology in the past, many structural analyses were led based on the basic SDOF model. Although the SDOF method can provide engineers with a sensible estimation of structural response, it cannot provide detailed analysis on the localized structural failure under extreme blast loading. The finite element method is more commonly used for structural analysis and in specific it has become an essential tool to model and simulate reinforced concrete system.

Analysis in Abaqus is done in three discrete steps: preprocessing, simulation, and post-processing. In preprocessing stage, geometry of building is defined and an Abaqus input file is created. The simulation generally runs in background is the step in which Abaqus solves the numerical problem defined in the step one. In post-processing,

after simulation, the evaluation of the results is done and the stresses, displacements and other required variables are calculated.

The following steps are performed and graphs for stresses and displacements are plotted.

1. Defining and creating parts
2. Generating material properties and assigning section properties
3. Model Assembly
4. Creating steps for analysis
5. Assigning boundary conditions and loads on the model
6. Meshing the Domain
7. Submitting the job
8. Results Review

Fig.2 to Fig.8 represents the modeling of the structure in order as mentioned above.

Simulation of a G+1 RC Building Subjected to Blast Loading:

The span, length and width of the building are 5.0m c/c, 10.0 and 10.0m respectively. The height of storey is 4.5m. The building height is 9m. Width of Wall has been taken as 0.15m with floor thickness as 0.125m. The building is standing free and is only fixed at the bottom. The density, Young's Modulus and Poisson's Ratio of the concrete are 2.5E-005 N/mm^3, 2.5e4 N/mm^2 and 0.2 respectively. The density, Young's Modulus and Poisson's Ratio of the steel has been taken as 7.335E-005 N/mm^3, 2e5N/mm^2 and 0.3 respectively. The density, Young's Modulus and Poisson's Ratio of the wall has been assumed as 1.9E-005 N/mm^3, 4.22e3 N/mm^2 and 0.3 respectively. A Blast caused in a room on the 1st floor for period of 0.01 seconds. A uniform distributed blast pressure loading was applied. Amplitude at time zero seconds is 167550 which are forced onto the structure for period of 0.01 seconds.

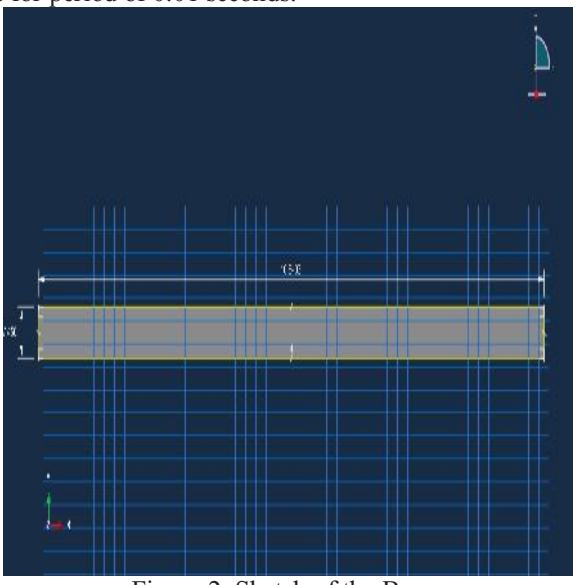

Figure 2. Sketch of the Beam

Figure 3. Isometric View of the Beam after Extrusion

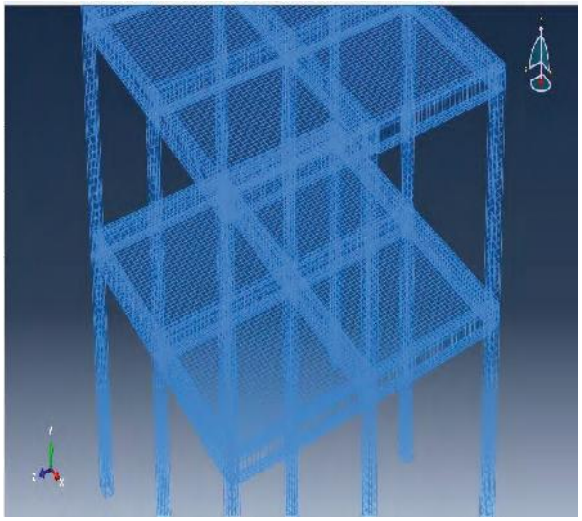

Figure 4. Reinforcement Assembly

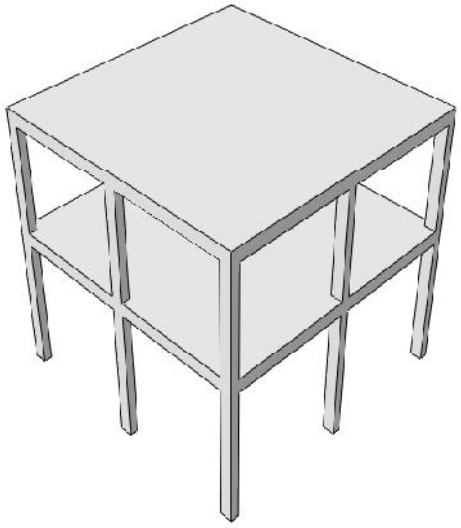

Figure 5. Frame Assembly

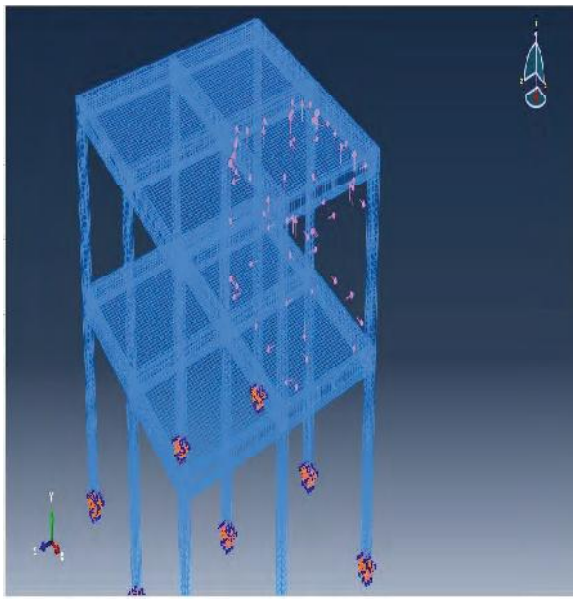

Figure 6. Blast loading in the room and Boundary Conditions (Fixed)

The meshing is done in two stages. In the first stage, the part instances are seeded. In the second stage, meshing the part instance is done. The number of seeds is based on the element size or the number of elements along an edge. Abaqus arranges the nodes of mesh at the seeds wherever possible. This process of seeding will generate tetrahedral elements. The type of tetrahedral element is C3D10M, Second Order Tetrahedral Element having 10 Nodes.

After meshing, the last step is to create a Job step which is submitted for analysis. After completion of Job submitted, results for blast loading analysis can be observed from visualization tab. Node wise displacements and stresses can be obtained using monitor option in the job tab.

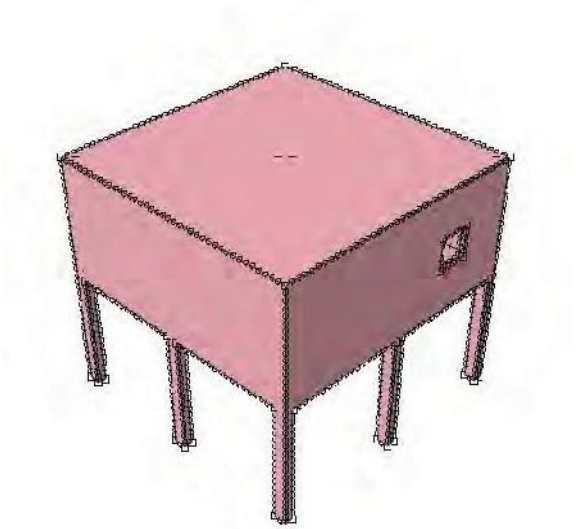

Figure 7. Seeding of Instance before Meshing

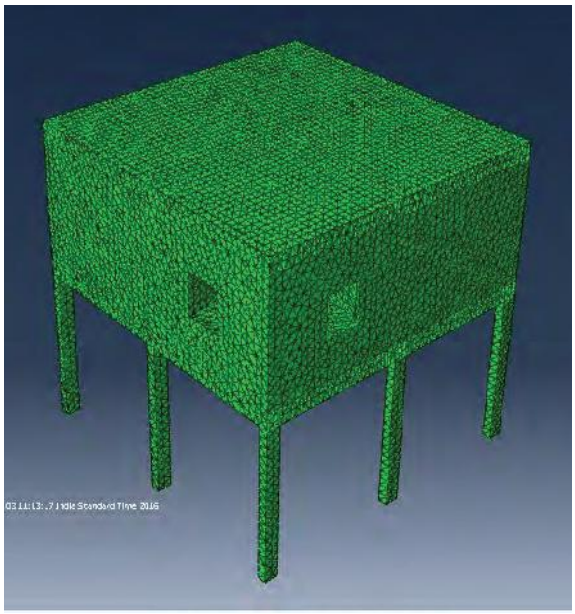

Figure 8. Second Order Tetrahedral Element having 10 Nodes for each Element

IV. Results

This chapter provides results and discussion on determining the variation of stresses and displacements under the blast impact caused by the explosion. In this case the entire room section on the first floor of the building, up to 4.5 m above ground level, failed under blast loading.

Sudden pressure is applied to the inner walls, ceiling and on floor of the room. All elastic models were constructed using Abaqus/CAE. Isometric views along with different sectional elevation and plans are illustrated below to examine the variation of stresses in the structure.

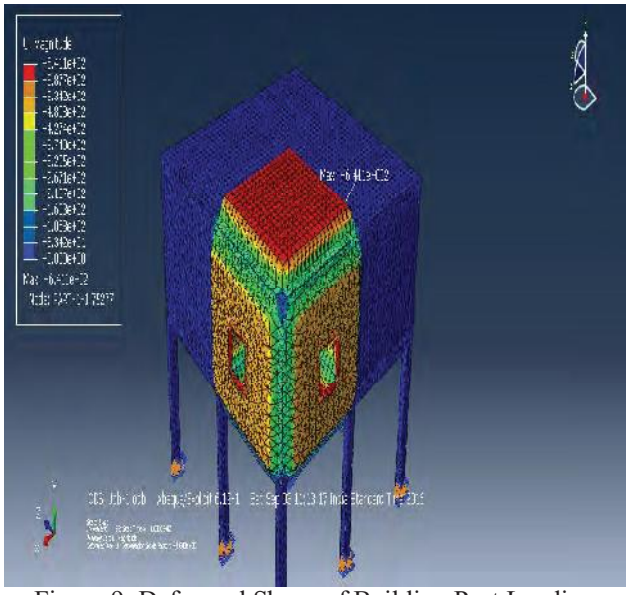

Figure 9: Deformed Shape of Building Post Loading

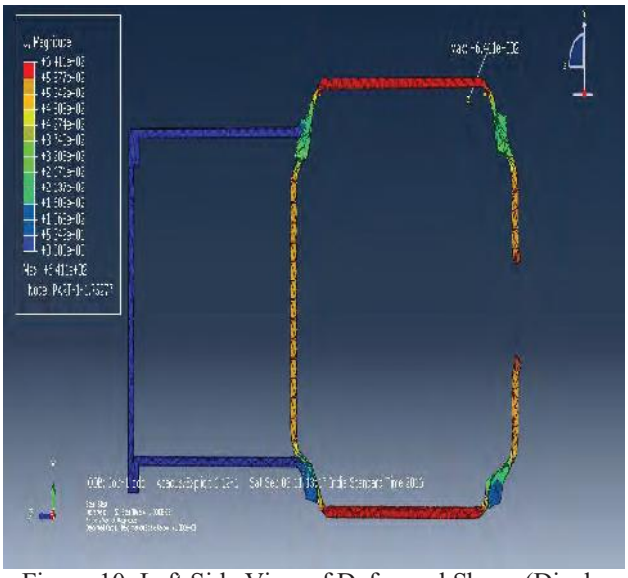

Figure 10: Left Side View of Deformed Shape (Displacement)

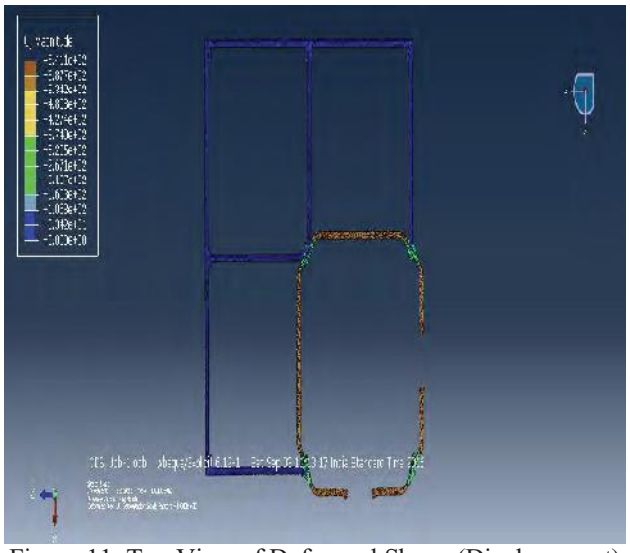

Figure 11: Top View of Deformed Shape (Displacement)

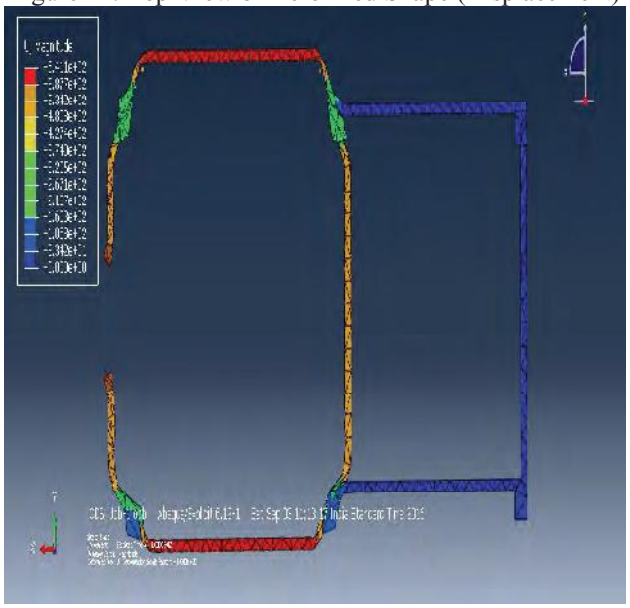

Figure 12: Right Side View of Deformed Shape (Displacement)

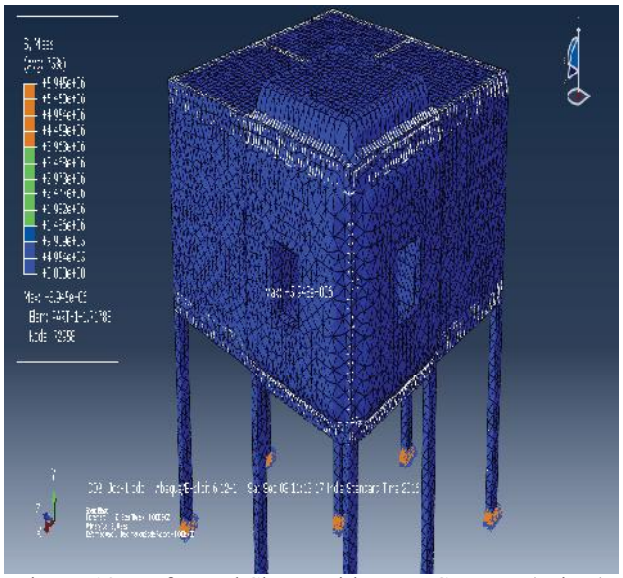

Figure 13: Deformed Shape with Max. Stresses (Mises)

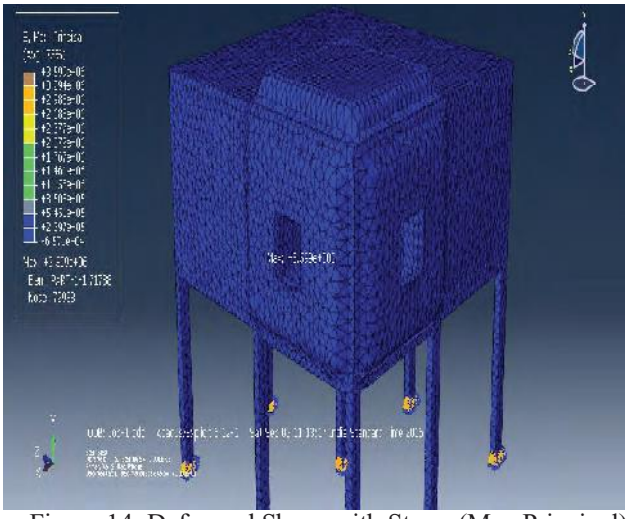

Figure 14: Deformed Shape with Stress (Max Principal)

Key Points of Analysis for the Maximum Principle Stress from the Blast Load were the explosion of the room encompassed around the openings. Stress inside the room propagate in a circular fashion making their way to the corners as shown in fig. 14. The walls of the building give a bouncing back or 'recoil' effect leading to high concentration of stress. The Maximum Principal stress value has been simulated to be 3.599E+06 N/mm^2 as in fig. 17. Rebounding of the building occur causing high localised displacement.

Key Points of Analysis for the Maximum Displacement from the blast load were explosion in the room caused maximum displacements at the openings, centre of slab and at joins as in fig. 9 and fig. 15. The largest displacement value has been simulated to be 6.411E+02 mm. Further increase in load caused distortion of structure. From the graph (fig. 16) the displacements were maximum at the centre and gradually reduce towards the joints. The deformed shapes at various sections have been shown in fig. 10 to fig. 12.

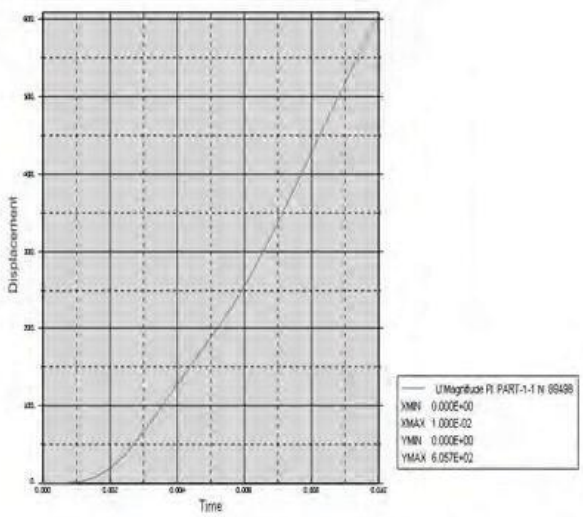

Figure 15: Time vs Displacement at Node Located at Max Deformation

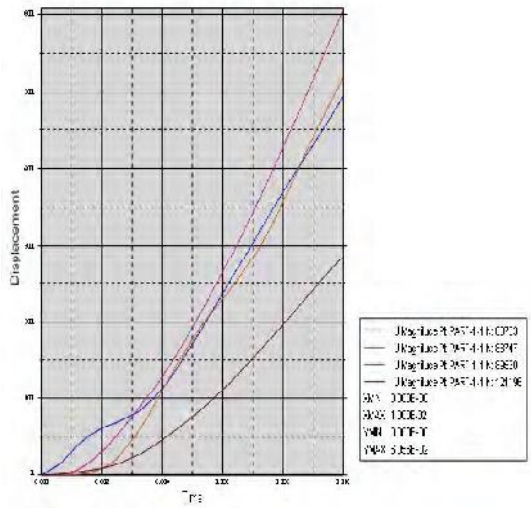

Figure 16: Time vs Displacement at Node Located at various Deformations

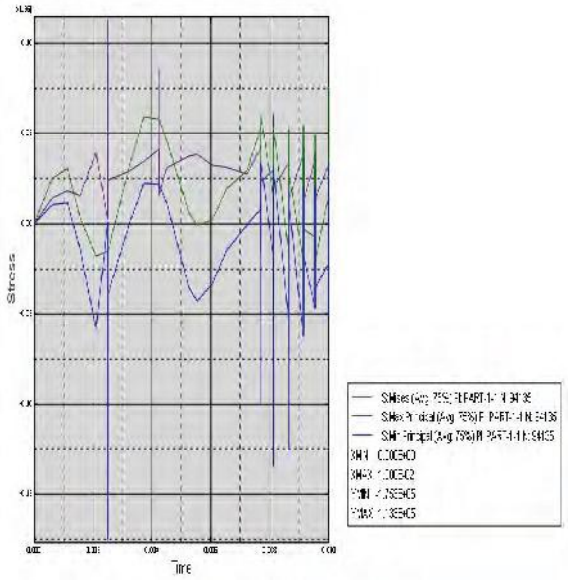

Figure 17: Time vs Stress (Mises), Max. & min. Principal Stresses

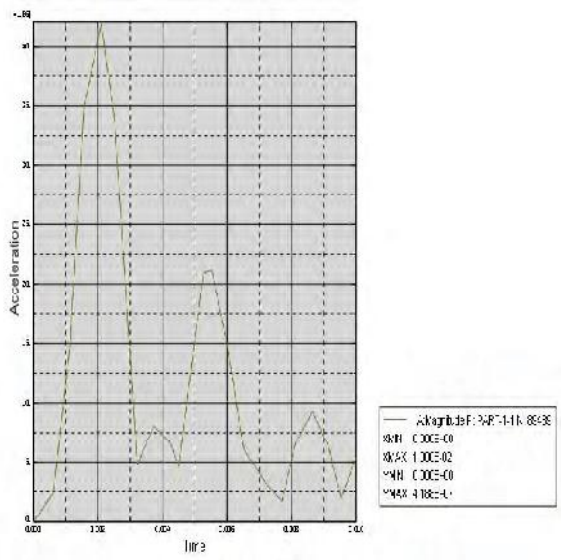

Figure 18: Time vs Acceleration

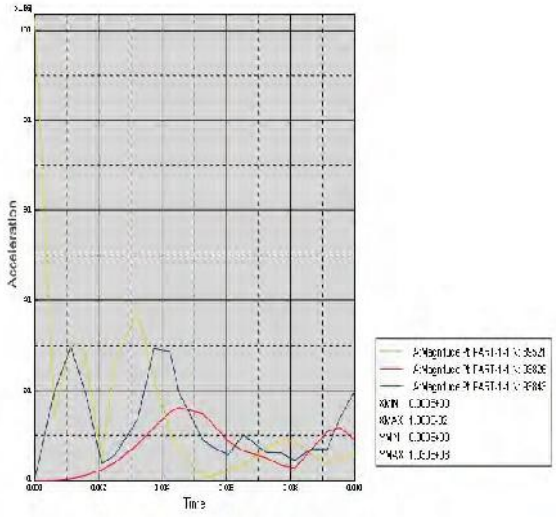

Figure 19: Time vs Acceleration at three nodes located at various deformations

Fig. 18 shows the variation of acceleration of elements with respect to time at node having maximum deformation or displacement. The difference in acceleration is shown with respect to time in fig. 19 at three different nodes in decreasing order of their displacements.

From research paper [13], it is seen that maximum stress from an 8-storey masonry building was 90,000N/mm^2. For 2-storey reinforced building with same dimensions, the maximum stress was 1, 67,550 N/mm^2. This shows that the reinforced structure offers more resistance to such blast loadings. Further, the resistance can be improved by additionally providing bracings or shear walls at surfaces fully exposed to blast loads.

V. Conclusions

A simple overview of the different types of loads is discussed here. When the blast load hits the structure, the blast pressure leads to an increase in the kinetic energy of the structural system. The increase in velocity results in a large displacement of the elements.

A two-bay two floors reinforced concrete structures have been modelled in Abaqus. The blast loading [13] is applied on the structure. The entire domain is discretized using ten node tetrahedron elements. The finite element analysis has been performed for different conditions of blast load. The maximum stress for an RC building is found to be 1.86 times the maximum stress for an 8-storey masonry building [13].

The finite element analysis revealed that, there exists a critical blast impulse for reinforced buildings. Blast impulse applied above the critical value will result in the collapse of building before the allowable deflection criterion is reached. The column and beam response to blast loads has shown to be significantly influenced by higher deformations.

The surfaces of the structure exposed to direct blast pressures cannot be protected. They are designed to resist the blast pressures by increasing the stand-off distance or designing the component against blast loading. High risk facilities such as public and commercial tall buildings the design considerations against extreme events (bomb explosion, high velocity impact) are very important.

The guidelines on abnormal load cases and provisions for progressive collapse prevention should be included in the current Building Regulations and Design Standards. Study on ductility requirement helps in improving the building performance under extreme load conditions.

Based on the results, some recommendations are made for future work concerning structures exposed to blast loads. All components constructed in this research are not pre-stressed. Therefore, it is necessary to develop a user defined material so that the pre-stressed concrete material model can be incorporated into the finite element model.

Multiple blast explosions are very likely to take place in terrorist attacks, especially for important structures. Hence, it is necessary to examine the structural response when subjected to such attacks. Based on the presented results, it appears that the employment of hollow section components in a structure can give a better blast resistance than filled section components under the blast load. Further investigation on this issue is necessary so that it can be incorporated into future blast resistant design. This research was only performed on a specific reinforced concrete building. As mentioned early in the study, different concrete structures exhibit disparities in structural integrity. Therefore, further research on various building types such as RC frame with stiffeners, bracings, shear walls, etc., are essential to determine their performance against blast load.

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Behaviour of Magnetised Water Concrete under Different Curing Conditions

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***Abstract*—Concrete is the most widely used man made building material. The reaction of OPC with water results in hydration, which glue the reacting cement together to form a hardened cement paste. When cement and water are mixed with fine and coarse aggregate the resulting product is called concrete. Till now potable (Normal) water is used for mixing different ingredients of concrete. It is expected that in the near future, the civil engineering community will have to produce structures in harmony with the concept of sustainable development through the use of high-performance materials with low environmental effects that are produced at a reasonable cost. Magnetic water concrete, synthesized from the normal materials used in manufacturing of concrete, provides one route towards this objective.**
This paper presents the effect of addition of magnetised water on behaviour of concrete under different curing conditions.
Total number of specimen casted are 12 cubes and 6 cylinders of normal water concrete normal curing, 12 cubes and 6 cylinders of magnetised water concrete normal curing, 3 cubes and 6 cylinders of normal water concrete accelerated curing, 3 cubes and 6 cylinders of magnetised water concrete accelerated curing each of M20 and M25 grade of concrete determining compressive strength and splitting tensile strength.

***Index Terms*—Magnetised water concrete, Normal water concrete, Magnetised water, Normal water, Normal curing, Accelerated curing.**

I. Introduction

Cement mortar and concrete are most widely used construction materials. Concrete is made by using Portland cement, fine aggregates, coarse aggregates and water. The hydration products act as binder to hold all the aggregates together to form concrete. The hydration is an exothermic reaction which liberates considerable quantity of heat and this is to be dissipated for continuing hydration process. Curing is generally done by immesion, spraying, ponding water on concrete surface. It is very difficult to choose another construction material which is as versatile as concrete.

II. Materials

A. Cement

Locally available 53 grade ordinary Portland cement has been used in the present investigation work for all concrete mixes.

TABLE I
PHYSICAL PROPERTIES OF ORDINARY PORTLAND CEMENT

Name of the test	Result	I.S Recommended values	I.S code
Finess of cement	3.5%	<10%	IS269-1976
Standard consistency	32%	From bottom 5 to 7mm	IS4031-1968
Specific gravity	3.02	3.15	IS2720 Part3
Soundness of cement	3mm	<10mm	IS269-1989
Compressive strength of cement (28 days)	53.5N/mm^2	>=53N/mm^2	IS269-1976

B. Magnets

In the present investigation, magnets were obtained from a scientific store. The shape of the magnets are rounded. The average magnetic strength of magnets is 985 gauss.

Figure 1. Magnets

C. Fine aggregates

In the present investigation, river sand available in the local market was used as fine aggregate. The physical properties of fine aggergates were tested in accordance with IS 2386.

TABLE II
PHYSICAL PROPERTIES OF FINE AGGREGATE

Properties	Result
Fineness	2.88
Specific gravity	2.74
Bulk density in loose state	1550 kg/m^3

Fine aggregate conform to zone-II in accordance with IS: 383-1970.

D. Coarse aggregate

In the present investigation, crushed coarse aggregate of 10mm size obtained from local crushing plants is used. The physical properties of coarse aggregate were tested in accordance with IS 2386.

TABLE III
PHYSICAL PROPERTIES OF COARSE AGGREGATES

Properties	Result
Finess Modulus	5.314
Specific Gravity	2.77
Bulk Density	1332 kg/m^3

E. Magnetised water

Magnetised water is obtained by placing 1liter beakers filled with water over the magnets for a period of 24 hours. During this time magnetic field is going to penetrate through the glass into the water, which absorbs the magnetism and this magnetised water is used for preparing concrete.

Figure 2. One liter beakers placeg over magnets

III. MIX DESIGN

In the present investigation, M20 and M25 grade concrete mix trials were done on procured material. The indian standard mix design procedure is adopted (i.e., IS: 10262-2009).

TABLE IV
M20 GRADE CONCRETE PROPORTION QUANTITIES PER CUBIC METER

Target strength f_{ck}	26.6N/mm^2
Volume of concrete	1m^3
Weightofwater	220.48kg
Weight of cement	400.48kg
Weight of fine aggregate	957.03kg
Weight of coarse aggregate	824.17kg
W/C ratio	0.55
Mix proportion	1:2.38:2.05

TABLE V
M25 GRADE CONCRETE PROPORTION QUANTITIES PER CUBIC METER

Target strength f_{ck}	31.6N/mm^2
Volume of concrete	1m^3
Weightofwater	220.48kg
Weight of cement	440.96kg
Weight of fine aggregate	937.35kg
Weight of coarse aggregate	807.233kg
W/C ratio	0.5
Mix proportion	1:2.125:1.83

IV. RESULTS AND DISCUSSIONS

Effect of magnetised water on workability of concrete mixes.Workability tests are conducted for different concrete mixes with normal water and magnetised water.

TABLE VI
WORKABILITY TESTS ON M20 GRADE CONCRETE

Workability tests	Normal water	Magnetised water
Slump cone test (mm)	35	55
Compaction factor	0.936	0.94
Vee-bee consistometer (sec)	6.2	5.13

TABLE VII
WORKABILITY TESTS ON M25 GRADE CONCRETE

Workability tests	Normal water	Magnetised water
Slump cone test (mm)	35	55
Compaction factor	0.936	0.94
Vee-bee consistometer (sec)	6.2	5.13

Compressive strength of Normal Water Concrete (NWC) and Magnetised Water Concrete (MWC) of M20 grade concrete cubes. (Normal Curing)

TABLE VIII
COMPRESSIVE STRENGTH OF M20 GRADE NWC AND MWC.

Days	Compressive strength of NWC	Compressive strength of MWC
7	18.48	27.16
28	25.43	31.4
60	30.05	34.76
90	35.01	39.82

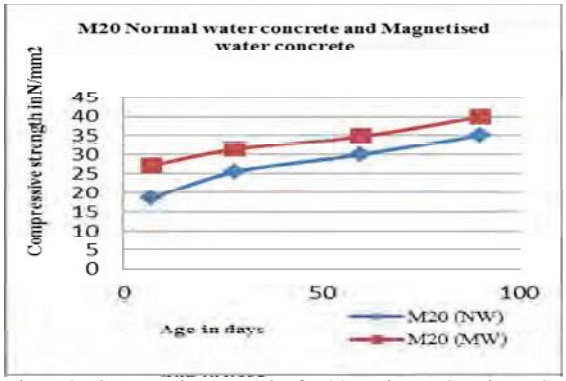

Figure 3. Compressive strength of M20 grade NWC and MWC.

Compressive strength of Normal Water Concrete (NWC) and Magnetised Water Concrete (MWC) of M25 grade concrete cubes. (Normal Curing)

TABLE IX
COMPRESSIVE STRENGTH OF M25 GRADE NWC AND MWC

Days	**Compressive strength of NWC**	**Compressive strength of MWC**
7	21.56	30.43
28	30.22	35.1
60	34.64	39.3
90	38.66	42.76

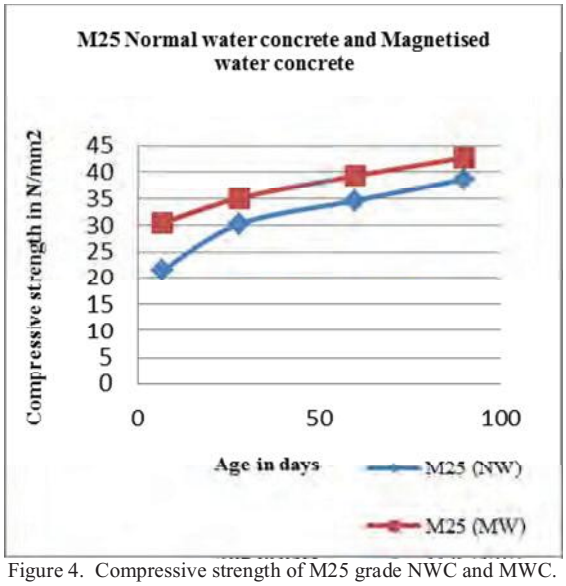

Figure 4. Compressive strength of M25 grade NWC and MWC.

Compressive strength of Normal Water Concrete (NWC) and Magnetised Water Concrete (MWC) of M20 grade concrete cubes. (Accelerated Curing)

TABLE X
COMPRESSIVE STRENGTH OF M20 GRADE NWC AND MWC

Compressive strength of NWC	Compressive strength of MWC
11.3	14.3
R28(strength at 28days)=8.09+1.64(Ra)	
26.62	32.36

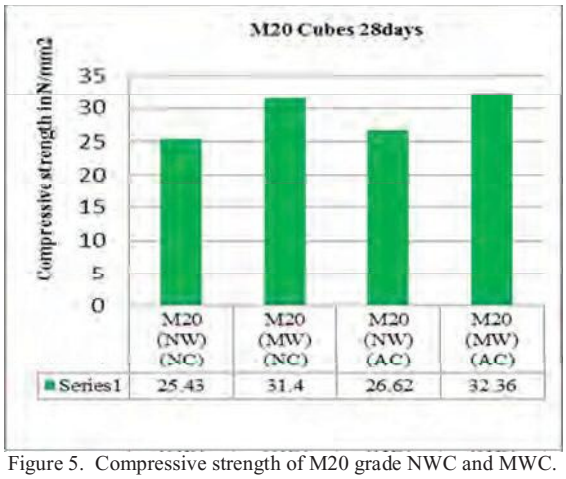

Figure 5. Compressive strength of M20 grade NWC and MWC.

Compressive strength of Normal Water Concrete (NWC) and Magnetised Water Concrete (MWC) of M25 grade concrete cubes. (Accelerated Curing)

TABLE XI
COMPRESSIVE STRENGTH OF M25 GRADE NWC AND MWC

Compressive strength of NWC	Compressive strength of MWC
13.7	16.8
R28(strength at 28days)=8.09+1.64(Ra)	
30.55	35.65

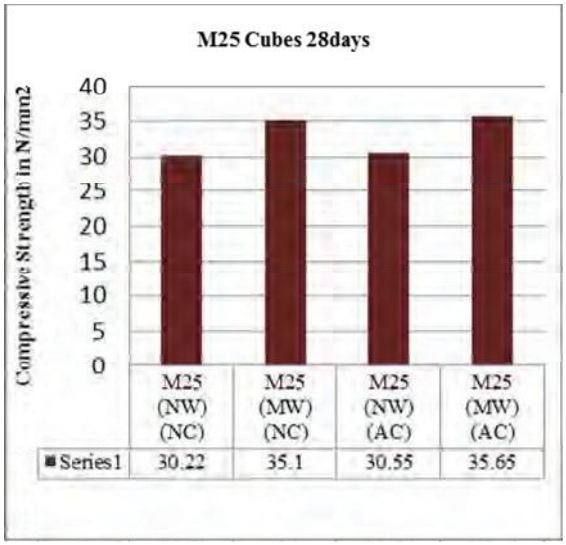

Figure 6. Compressive strength of M25 grade NWC and MWC.

Compressive strength of Normal Water Concrete (NWC) and Magnetised Water Concrete (MWC) of M20 and M25 grade concrete cylinders 28days. (Normal Curing)

TABLE XII
COMPRESSIVE STRENGTH OF NWC AND MWC CYLINDERS

Grade	Days	Compressive strength of NWC	Compressive strength of MWC
M20	28	18.6	21.4
M25	28	20.8	23.6

Compressive strength of Normal Water Concrete (NWC) and Magnetised Water Concrete (MWC) of M20 and M25 grade concrete cylinders. (Accelerated Curing)

TABLE XIII
COMPRESSIVE STRENGTH OF NWC AND MWC CYLINDERS

Grade	Compressive strength of NWC	Compressive strength of MWC
M20	8.1	10.4
M25	9.8	12.2
R28(strength at 28 days)=8.09+1.64(Ra)		
M20	21.37	25.14
M25	24.16	28.09

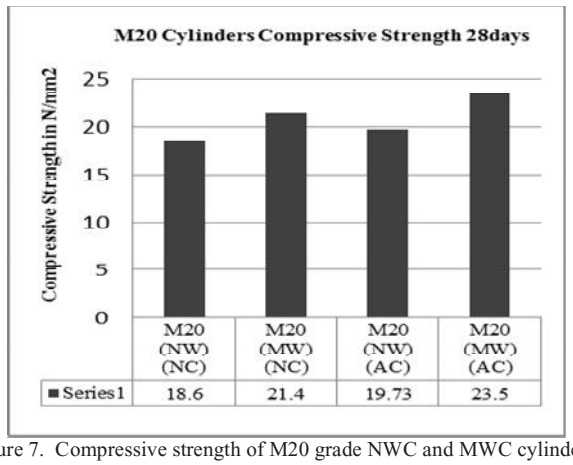

Figure 7. Compressive strength of M20 grade NWC and MWC cylinders.

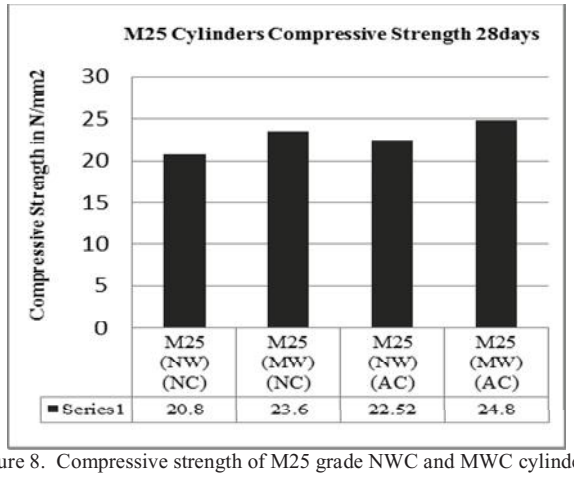

Figure 8. Compressive strength of M25 grade NWC and MWC cylinders.

Split tensile strength of Normal Water Concrete (NWC) and Magnetised Water Concrete (MWC) of M20 and M25 grade concrete cylinders 28days.

TABLE XIV
SPLIT TENSILE STRENGTH

Grade	Split tensile strength of NWC (NC)	Split tensile strength of MWC (NC)	Split tensile strength of NWC (AC)	Split tensile strength of MWC (AC)
M20	2.64	3.36	2.3	3.18
M25	2.9	3.62	2.57	3.4

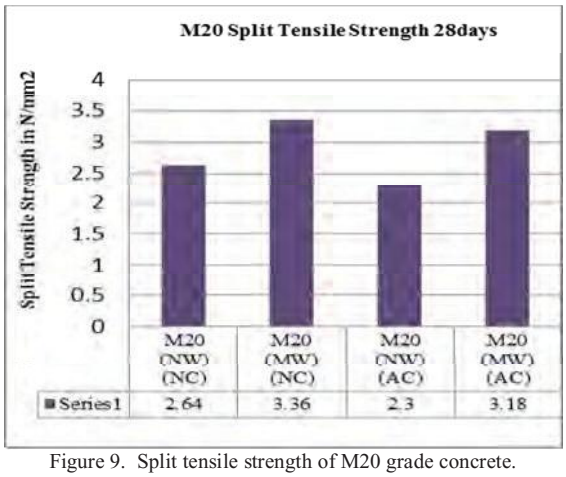

Figure 9. Split tensile strength of M20 grade concrete.

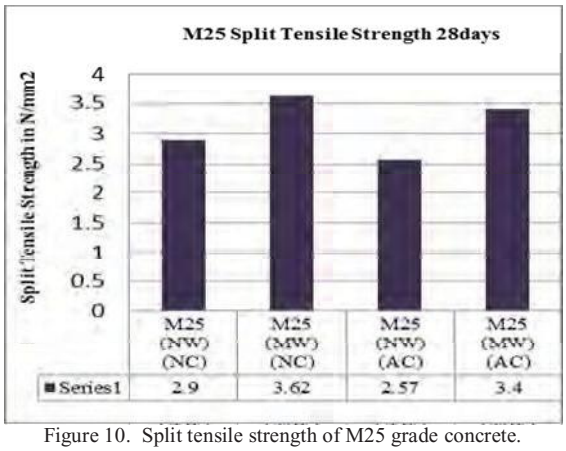

Figure 10. Split tensile strength of M25 grade concrete.

V. CONCLUSIONS

In this investigation, the behaviour of magnetised water concrete on compressive strength and splittensile strength are studied.

1. The workability of magnetised water concrete is slightly more than that of normal water concrete.
2. The compressive strength of concrete with two types of water in the mix, Normal water (Normal Curing and Accelerated Curing) is less than Magnetised water (Normal Curing and Accelerated Curing).
3. The split tensile strength of concrete with two types of water in the mix, Normal water (Normal Curing and Accelerated Curing) is less than Magnetised water (Normal Curing and Accelerated Curing).
4. Accelerated curing gives high early ge strength which enables the removal of the formwork within 24hours, thereby reducing the cycle time, resulting in cost-saving benfits.
5. The increase of strengths of concrete when MW is used as mixing water in concrete is due to filling up of the voids(pores) in concrete with more products of hydration.
6. The strength studies show that MWC also behaves like a NWC in strength development i.e., developing very high strengths at early ages and less strength at later ages.

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PLL Implementation and Reactive Power Compensation

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Abstract: **Phase locked loop (PLL) plays significant role in connecting a power electronic converter to the grid. A PLL can be implemented with software or hardware. In this paper, PLL is developed in MATLAB/SIMULINK using harmonic oscillator. The PLL can extract exact supply frequency information under balanced grid voltages. Static Synchronous Compensator (STATCOM) is a shunt connected Flexible AC Transmission Systems (FACTS) device which can able to absorb or generate reactive power. STATCOM is used in power transmission systems for reactive power compensation, load balancing etc. Secondly, a two level voltage source inverter based STATCOM is presented for reactive power compensation. A control strategy is developed for DC link voltage balance and instantaneous reactive power compensation. To validate the effectiveness of the control scheme, simulation study is done in MATLAB/SIMULINK for different load conditions.**

***Index Terms*— Phase locked loop (PLL), two level inverter, reactive power compensation, STATCOM.**

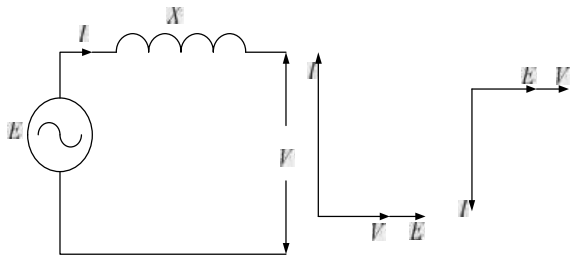
I. INTRODUCTION

The application of power electronic converters in power system is increasing because of improved power quality and providing reliable supply [1]. Power electronic converters are used in, Flexible AC Transmission Systems (FACTS), Grid connected solar PV system, High Voltage Direct Current (HVDC) Transmission and micro grid and so on [2]. For all such major applications, information of grid frequency is essential. Grid frequency is subjected to variations of loads, faults, disturbances in the system [3]. In detecting accurate value of grid frequency, Phase Locked Loop (PLL) plays significant role. Various PLL techniques are used for Synchronization between power electronic converter and grid [10]. An ideal PLL should provide the very fast and accurate value of frequency [4].

Static Synchronous Compensator (STATCOM) is a shunt connected Flexible AC Transmission Systems (FACTS) device which can able to absorb or generate reactive power whose output can be controlled so as to sustain definite parameters of the electric power system [5]. The STATCOM was initially named as advanced SVC (Static VAr Compensator) and then called STATCON (STATic CONdenser) and now a days, it is commonly known as STATic COMpensator (STATCOM).

The STATCOM gives working characteristics like a rotating synchronous compensator without the mechanical inertia. This is due to the STATCOM employs solid state power switching devices [6]. STATCOM also provides voltage support in distribution and transmission network by modulating bus voltages during disturbances [7].

The operation principle of STATCOM is as below. The Voltage Source inverter (VSI) produces a convenient AC voltage source (*E*). This voltage is compares the grid voltage *(V)* of the system; when the AC grid voltage amplitude is greater than that of the VSI voltage amplitude, the AC grid looks the STATCOM as an inductance connected to its terminals. Otherwise, if AC grid voltage amplitude is less than that of the VSI voltage amplitude, the AC grid looks the STATCOM as a capacitance connected to its terminals. If the voltage amplitudes are same, then the reactive power sharing between the grid and VSI is zero [3].



If the STATCOM has a DC source on its DC side, it can able to supply real power to the power system. This can be done by varying the phase angle of the STATCOM output and the phase angle of the AC power system. When the phase angle of the VSI lags grid phase angle, then STATCOM supplies real power to the AC system; if the phase angle of the VSC leads the grid phase angle, the STATCOM absorbs real power from the AC system [8]. If STATCOM supplies only reactive power, a capacitor is sufficient at the input of voltage source inverter, and DC link voltage can be maintained by drawing small active power from the grid.

Voltage source fed inverters are recently becoming very popular for FACTS devices due to improved voltage quality, very low voltage drop across the semiconductor device and low switching frequency of the semiconductor device compared to the conventional converters [2].

In this paper, a static VAr compensation system is developed using a two-level inverter as shown in fig.1. For the synchronization of grid to the inverter Synchronous reference frame PLL (SRF-PLL) is used.

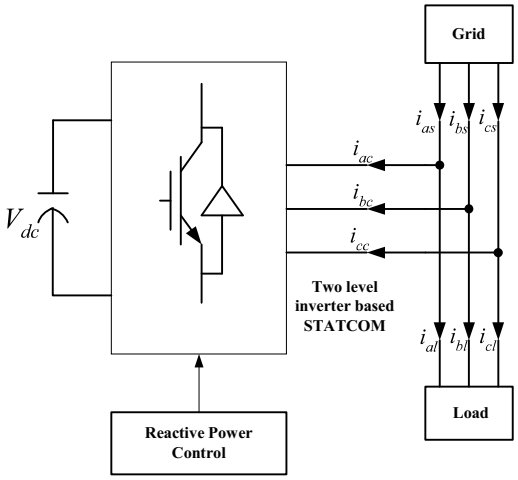


Figure 1. STATCOM with two level Inverter

II. PHASE LOCKED LOOP (PLL)

The emergent use of power electronic converters in both single and three phase applications requires a accurate and fast technique for phase angle evaluation. This is a major parameter in any application where reactive/active power flow control is required [8].

Synchronous Reference Frame (SRF) based PLL is developed in this paper and it estimates the phase angle exactly. The principle of SRF-PLL is estimates both the grid frequency and voltage phase angle for reference signal generation for the control of power electronic converters. The block diagram of three-phase SRF-PLL is illustrated in Fig.2 [9].

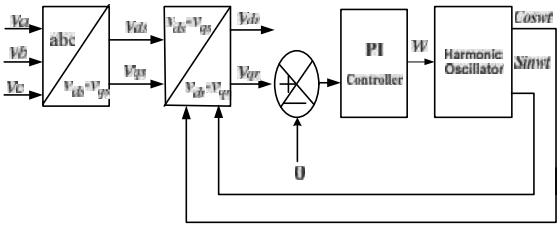


Figure 2. Three phase PLL basic structure

To obtain the phase information, the three phase (V_a, V_b and V_c) AC voltages are transformed into two phases (V_{ds} and V_{qs}) by using equation (1) and these two phases are transfer into direct and qudarature voltages (v_{dr},v_{qr}) axis by using Equation (2). The phase angle θ is estimated by synchronously rotating voltage vector along d or q axis by using PI controller [10-12].

$$\begin{pmatrix} v_{ds} \\ v_{qs} \\ v_0 \end{pmatrix} = \frac{2}{3}\begin{pmatrix} 1 & -\frac{1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{pmatrix}\begin{pmatrix} va \\ vb \\ vc \end{pmatrix} \quad (1)$$

$$\begin{pmatrix} v_{dr} \\ v_{qr} \end{pmatrix} = \begin{pmatrix} cos\theta & sin\theta \\ -sin\theta & cos\theta \end{pmatrix}\begin{pmatrix} v_{ds} \\ v_{qs} \\ v_0 \end{pmatrix} \quad (2)$$

The phase angle θ is expected with θ^* which is integral of the estimated frequency ω^*. The expected frequency is the sum of the PI controller output and feed forward frequency ω [13]. The gain of the PI controller is calculated that, v_q coincide the reference value $v_q^* = 0$. If $v_q = 0$ the space vector voltage is synchronized along the q-axis and expected frequency ω^* locked on the system frequency ω. So that the expected phase angle θ^* is equals to the phase angle θ.

The harmonic oscillator is designed based on the equation (3) and (4).

$$X_{n+1} = X_n + \omega y \Delta t \quad (3)$$

$$Y_{n+1} = Y_n - \omega x \Delta t \quad (4)$$

The simulation results for the direct and quadrature axes voltages are shown in Fig. 3. From the result quadrature axes voltage is zero. Fig. 4 shows the PLL generated sin and cos unit signals of same grid frequency. Fig.5 shows the grid frequency in rad/sec. The PLL generated two phase voltages are transferred to three phase by using inverse transformation to know the phase sequence. Fig.6 shows the grid voltage and PLL generated voltages both are in phase.

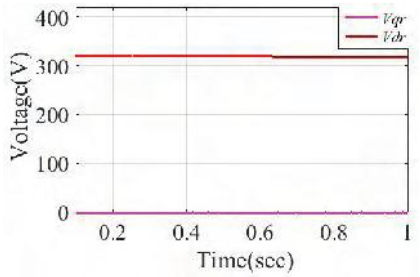


Figure 3. Direct and quadrature axes voltages (v_{dr} and v_{qr})

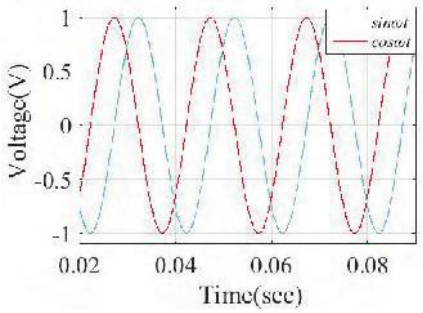


Figure 4. Unit voltage vectors

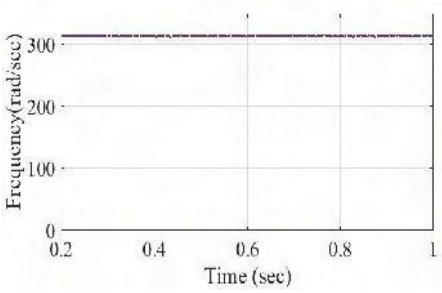


Figure 5. Frequency of grid voltages in rad/sec

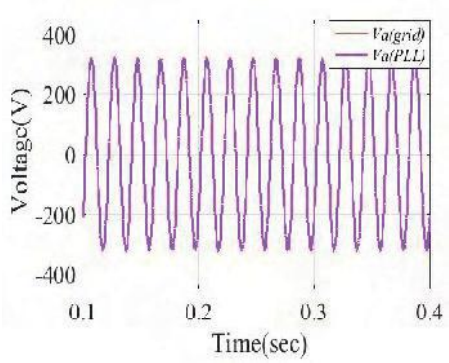


Figure 6. Grid and outupt voltages of pll

III. Reactive Power Compensation

Fig.7 shows two level inverter which is connected to the grid, through coupling inductor. The DC link voltage at the input of inverter is maintained by a capacitor. This is achieved by maintain certain phase angle between the grid and inverter voltages.

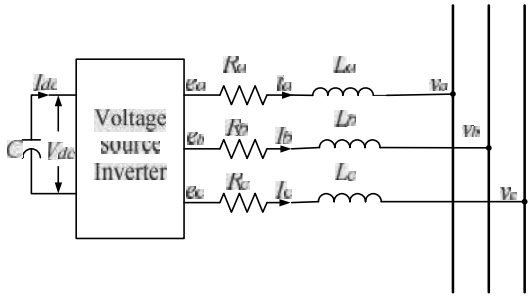


Figure 7. Equivalent circuit of two level inverter based STATCOM

In the Figure v_a, v_b *and* v_c are grid voltages, R_a, R_b *and* R_c are the resistances which represent the power losses in the coupling inductor and L_a, L_b *and* L_c are inductances of coupling inductors, e_a, e_b and e_c are the inverter output voltages. Assuming $R_a = R_b = R_c = R$ and $L_a = L_b = L_c = L$ and the dynamic model can be derived by writing KVL on AC side as follows [14]

$$\begin{bmatrix} \frac{di_a}{dt} \\ \frac{di_b}{dt} \\ \frac{di_c}{dt} \end{bmatrix} = \begin{pmatrix} -\frac{R}{L} & 0 & 0 \\ 0 & -\frac{R}{L} & 0 \\ 0 & 0 & -\frac{R}{L} \end{pmatrix} \begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} + \frac{1}{L} \begin{pmatrix} v_a - e_a \\ v_b - e_b \\ v_c - e_c \end{pmatrix} \quad (3)$$

Equation (3) is transformed to the synchronously rotating reference frame. The reference voltages of the inverter e_d^* and e_q^* are controlled in synchronously rotating reference frame as follows:

$$e_d^* = x_1 - \omega L i_q + v_d \quad (4)$$

$$e_q^* = x_2 + \omega L i_d \quad (5)$$

The parameters x_1 and x_2 are regulated as follows

$$x_1 = (K_{p1} + \frac{K_{i1}}{s})(i_d^* - i_d) \quad (6)$$

$$x_2 = (K_{p2} + \frac{K_{i2}}{s})(i_q^* - i_q) \quad (7)$$

Where, i_d^* is reference *d*-axis current and i_q^* is *q*-axis reference current. i_d^* is obtained from the DC link voltage requirement as

$$i_d^* = (K_{p3} + \frac{K_{i3}}{s})(V_{dc}^* - V_{dc}) \quad (8)$$

Where, V_{dc}^* and V_{dc} are the reference and actual DC link voltages across the capacitor.

The reference *q*-axis current, i_q^* is obtained by transforming the stationary load current into synchronous rotating frame, using equations (1) and (2). The control circuit is shown in Fig. 8. The reference *d-q* axes voltages of the inverter, e_d^* and e_q^* are inverse transformed to stationary reference frame voltages e_a^*, e_b^* and e_c^* using equations (1) and (2) [15]. Using this voltages e_a^*, e_b^* and e_c^* as reference signals, high frequency triangular wave as carrier signal and comparing carrier and reference signals gate pulses for the inverter are generated [2].

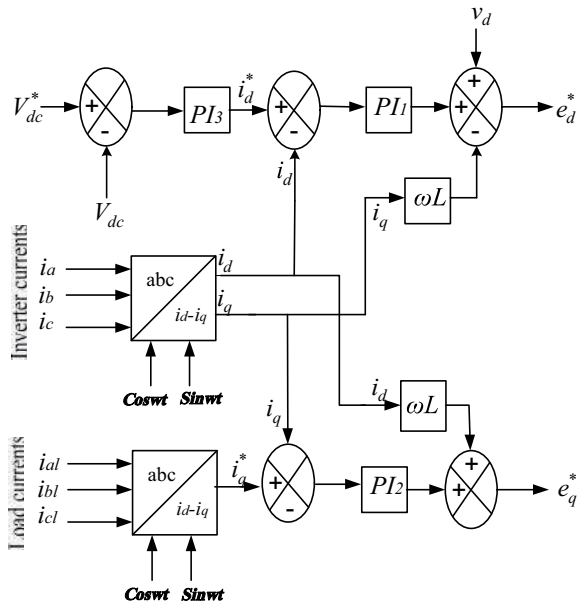


Figure 8. Control circuit

IV. Simulation Results

The block diagram shown in Fig.1 is considered for analyzing the system consisting of two level inverter based STATCOM using MATLAB/SIMULINK.

TABLE I
SIMULATION PARAMETERS

STATCOM Rating	70 KVA
Grid Voltage	415 (L-L)
Grid Frequency, *f*	50 Hz
DC Link Voltage, V_{dc}	1000 V
Switching Frequency	10 KHz
DC Link Capacitance, *C*	1200 μF

A. Capacitive Mode

Initially, the load impedance is set at (3.4 + j3.4) Ω, hence load draws a current of (50 - j50) A. To supply a reactive current of -j50A by the inverter, from (4) and (5), e_d^* and e_q^* are calculated to 375V and 49V respectively. The inverter output voltage $e_i = \sqrt{e_d^2 + e_q^2}$ is 378V. At *t* = 2 sec, load impedance is changed to (1.7 + j1.57) Ω, then load draws a current of (100 - j100) A.

For load variations, source always supplies active component of current, STATCOM supplies reactive component of current and source always operates at unity power factor as shown in Fig.9 (a). Fig.9 (b) shows variation of STATCOM current when the load reactive component is increased to –j100 A in synchronous rotating reference frame. From the figure, it can be seen that actual current approaches the reference current. Fig.9(c) shows the DC link voltage of the inverter. It can be seen that DC link voltage is maintained at the reference value even after load change. Fig.9 (d) shows inverter output voltage of Phase-A.

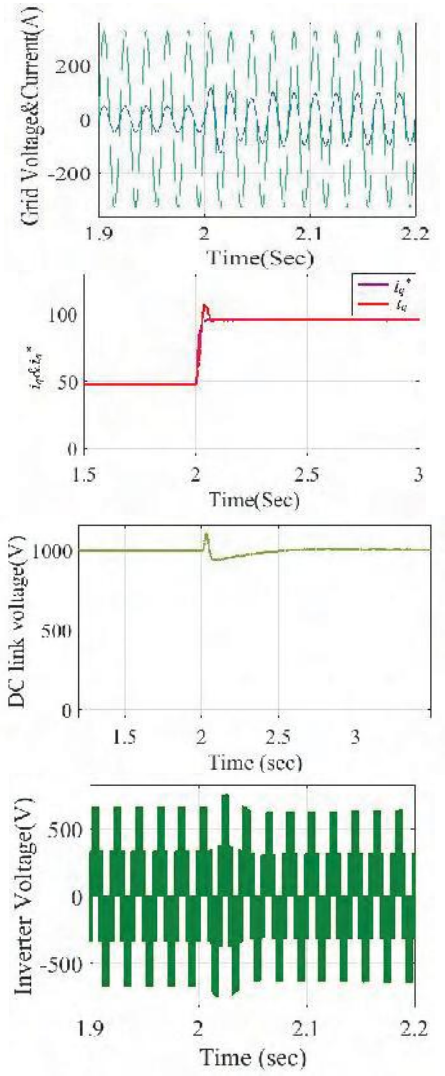


Figure 9. a) Grid current and voltage of phase-A b) Actual and reference reactive component of current c) Dc link voltage d) Inverter voltage

Fig.10 shows the total harmonic distortion of voltage. From the figure it can be seen that fundamental component of inverter voltage is 382.1V. Further, it can be seen that harmonics appear around multiples of switching frequency which is equal to 10 kHz. As discussed in section I the inverter output voltage is greater than the source voltage in capacitive mode of operation.

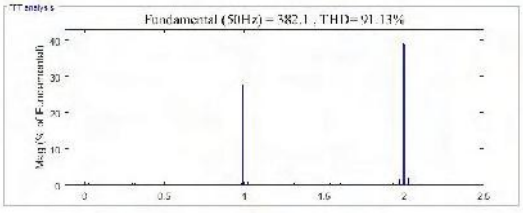


Figure 10. Harmonic spectrum of Inverter voltage

B. Inductive Mode

In the inductive mode, the load impedance is set at (3.4 + j6.78) Ω and load draws a current of (20 - j40) A. At *t* = 2

sec, load impedance is changed to (3.4 - j7.36) Ω, then load draws a current of (18 + j38) A. To supply a reactive current of +j38A by the inverter, from (4) and (5), e_d^* and e_q^* are calculated to be 260V and 65V respectively. Output voltage of the inverter is $e_i = \sqrt{e_d^2 + e_q^2}$ is 268V.

For inductive mode also, STATCOM supplies reactive component of current, grid supplies only active component of current and source always operates at unity power factor as shown in Fig.11 (a). Fig.11 (b) shows distinction of STATCOM current when the load reactive component is increased to +j38 A in synchronous rotating reference frame. From the figure, it can be seen that actual load current approaches the reference current. Fig.11(c) shows the DC link voltage of the inverter. It can be seen that DC link voltage is maintained at 1000 V after load change. Fig.11 (d) shows Inverter voltage of Phase-A.

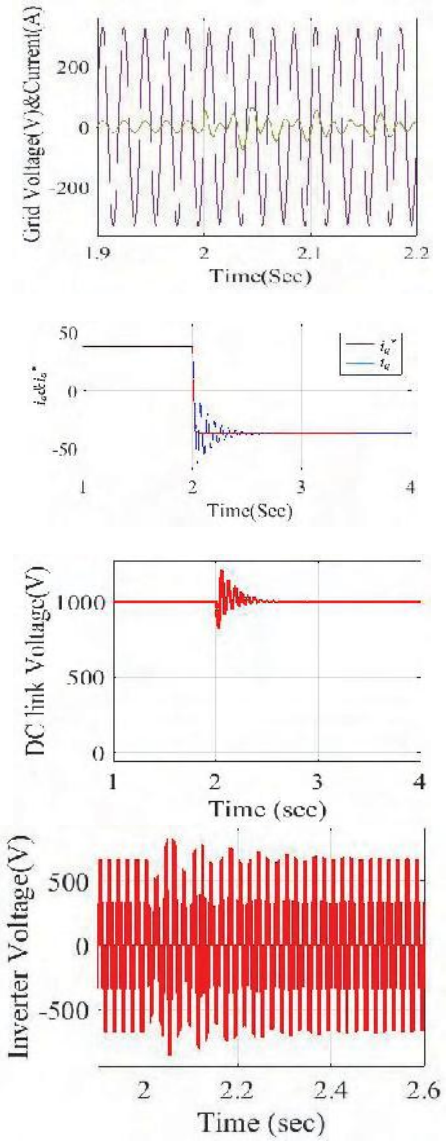


Figure 11. a) Actual and reference reactive component of current b) Dc link voltage c) Grid voltage and currents of phase-A d) Inverter current e)Inverter voltage

Fig.12 shows the total harmonic distortion of voltage. From the figure it can be seen that fundamental component of inverter voltage is 269.4V. Further, it can be seen that harmonics appear around multiples of switching frequency which is equal to 10 kHz. As discussed in section I the inverter output voltage is less than the source voltage in inductive mode of operation.

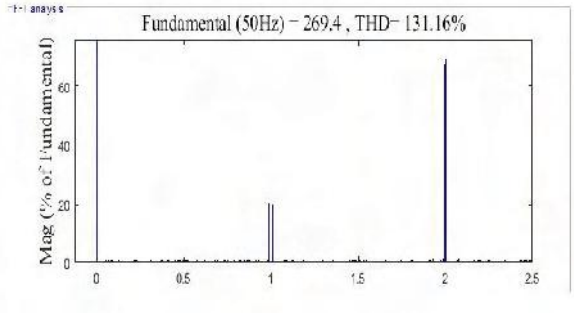


Figure 12. Harmonic spectrum of Inverter voltage

V. CONCLUSIONS

Phase locked loop plays a significant role in connecting a power electronic converter to the grid. In the first part of the paper, PLL is implemented in a grid connected system. The three phase voltages are converted into two phase voltages. The two phase voltages are transformed to synchronous rotating frame. The q-component of source voltage, v_q is made zero using PI controller, which ensures exact frequency information of source at any time.

In second part of the paper, static reactive power compensation is achieved using a two level inverter. Dynamic model of the two level STATCOM is developed. Based on the model the controller was developed. The controller generates reference voltages for the inverter. The effectiveness of the controller is analyzed by doing rigorous simulation studies. From the simulation study, it is concluded that the STATCOM ensures that the source always operates at unity power factor for different load conditions.

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Analysis and Simulation of STATCOM based SSR controller on the First Zone operation of Digital Distance Relay with Remedy

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***Abstract*—The adoption of compensation in series may cause to some problems in power system transmission lines like SSR (Subsynchronous Resonance). The damping of SSR is achieved by the injection of shunt current into the transmission line with static synchronous compensator (STATCOM) based on the information of Subsynchronous component (SSC) of current extracted from the study system. The use of STATCOM based SSR controller at centre of transmission line badly affects the operation of Distance relay. This research article addresses the prime issues that are concerns the problems of distance protection due to mid-point connected STATCOM based SSR controller in the transmission line. A novel algorithm is proposed to solve the associate problems with distance protection using the synchrophasors measurement. The power system is modelled as Bergeron model of transmission line using PSCAD software. The obtained simulation results show that the proposed adaptive setting scheme is more reliable and robust in comparison with existing distance protection schemes.**

***Index Terms*—Adaptive distance relay, Current control, Distance protection, STATCOM, SSR**

I. Introduction

The adoption of series capacitor compensation in transmission line is used to enhance the capability of power transfer capability HV and EHV lines, sharing of load among parallel lines and improves the system stability. Moreover, the placing of compensation in series to the line may results to new problems like SSR and oscillations shaft. Series capacitors may produce oscillations due to SSR with any small disturbance or fault when the system natural frequency coincides with complement of torsional modes of turbine-generator shaft [1- 4].

The rapid growth in power electronics leads to the advancement of FACTs devices like SSSC, TCSC and STATCOM. With reference to recent literature, many solutions and methods have been proposed by the so-called authors to mitigate the issue of SSR with the reference to FACTS controllers [5-9]. Regardless of the solution, the major difficulty is that how quick and precise assessment of components (subsynchronous) from the study system.

The addition of FACTS devices in power system leads to new problems in the protection of transmission line. These devices are the most frequently adopted in power systems due to its fast response time, line impedance, load currents and system power angle are also changed rapidly. Therefore, it is highly recommended for a protection engineers to investigate these changes in power system. The Distance relays are the most frequently utilized for protection of power system lines because of its simple operation and capacity to work independently under adverse situations. Due to the insertion of FACTS, distance relay might not work satisfactorily and is not able to protect transmission line. The unacceptable operation of relay causes to false tripping and also reduces the reliability of system, further initiates the cascade trippings and blackouts [11, 12].

The false operation of distance relay with STATCOM is addressed in Ref [10-12]. The above cited reference completely explains the consequences of STATCOM on distance relay. Due to the existence of STATCOM at midway of line, the mho distance relay may over-reaches or under-reaches to locate the fault point in the first zone of protection [11]. The STATCOM will not be responsible in fault loop if the fault occurs prior to the mid-point and its contribution in the fault current is zero. The foremost problem arises if the fault occurs after the midpoint only. For this the STATCOM compulsory comes in the fault loop and also contributes towards fault current.

The prime idea of this research article is to mitigate the problems of SSR with STATCOM and its effect on distance protections of transmission line without losing its security. To improve the performance of distance protection, first the behaviour of distance relay is analysed through the help of sequence components with STATCOM placed at midway of transmission line. The impedance due to STATCOM compensated the calculated impedance due to fault at relay point. The error produced by the calculated compensated impedance in the measurement of actual impedance can be nullified at relay point using proposed algorithm with the support of synchronized measurement.

This research article is framed as follows: Section II introduced the study system model i.e., Study system model with STATCOM based SSR controller. In Section III, the subsynchronous component controller is given for assessing the subsynchronous component of current and voltage. Section IV gives the mathematical analysis of distance protection scheme with STATCOM based SSR controller at centre of transmission line. Moreover Section V explains the

complete idea of synchronized measurement based adaptive mho relay setting. In section VI, simulation results of SSR mitigation and transmission line distance protection scheme with adaptive mho relay setting in presence of STATCOM are described. Section VII concludes the paper.

II. Study System with STATCOM based SSR Controller

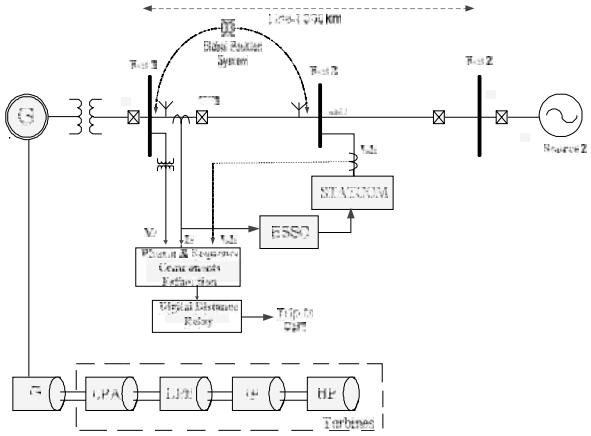


Figure 1. Study system model with STATCOM.

The study system model for this research work consists of two generators connected through single transmission line with different types of faults, location of fault and for different loading conditions [12]. Figure 1 shows the one line diagram of system under consideration and is modelled in PSCAD as a Bergeron model using the transmission line structural data. Appendix A determines the tower configuration of transmission line, parameters of conductor and source data. Figure1 illustrates the location of relay which is at bus A. The STATCOM is placed at midway of the transmission line-1to mitigate the SSR. An assumption is made that a GPS based synchronized measurement is existing on STATCOM bus and relaying bus. The data transmission is obtained with the help of an optical fiber. Therefore, the compensated current data of instantaneous time stamped is accessible at relaying bus with no delay. The generated voltage and grid current are denoted by v_s and i respectively. The injected current by STATCOM is denoted by I_{sh} [7, 8].

III. Sub-Synchronous Component Controller

The analytical procedure for seperating the components (voltage and current) of subsynchronous frequency from the measured signals explained as follows:

When the rotor of generator oscillates around its rated speed, the terminal voltage in synchronous dq rotating reference frame is given by

$$v_s^{dq}(t) = v_{s,sub}^{(dq)}(t) + v_{s,f}^{dq}(t) + v_{s,sup}^{(dq)}(t) \quad (1)$$

The subscripts "f", "sup" and "sub" denote the fundamental, super and sub-synchronous frequency components of voltage. For frequencies above the fundamental, the network offers a little positive damping, and hence the component of this frequency is not considered in the proposed work. If the rotor of generator oscillates with angular frequencyω_m the base frequency is denoted byω_0. The dq_mrepresents another set of co-ordinate systems which rotates with synchronous voltage vector, equation (1) can be written as

$$v_s^{dq}(t) = v_{s,f}^{dq}(t) + v_{s,sub}^{(dq_m)}(t)e^{-j\omega_m t} \quad (2)$$

The rearrangement of equation (2) results the extraction of sub-synchronous component of voltage, so that $v_{s,f}^{dq}$ and $v_{s,sub}^{(dq_m)}$components are decoupled and are given to a low-pass filter, the expression of subsynchronous component (ESSC) controller is given as

$$v_{s,f}^{dq}(t) = H_f(p)[v_s^{dq}(t) - v_{s,sub}^{(dq_m)}(t)e^{-j(\omega_m t)}] \quad (3)$$

$$i_f^{dq}(t) = H_f(p)\left[i^{dq}(t) - i_{sub}^{(dq_m)}(t)e^{-j(\omega_m t)}\right] \quad (4)$$

$$v_{s,sub}^{dq_m}(t) = H_{sub}(p)[v_s^{dq}(t)e^{j(\omega_m t)} - v_{s,f}^{dq}(t)e^{j(\omega_m t)}] \quad (5)$$

$$i_{sub}^{dq_m}(t) = H_{sub}(p)[i^{dq}(t)e^{j(\omega_m t)} - i_f^{dq}(t)e^{j(\omega_m t)}] \quad (6)$$

Where$H_{sub}(p)$and $H_f(p)$ represents the low pass filter (LPF) transfer function for subsynchronous and fundamental component, respectively. By writing the equation (3) in synchronous dq-frame as

$$v_{s,sub}^{dq}(t) = H_{sub}(p + j\omega_m)\left[v_s^{dq}(t) - v_{s,f}^{dq}(t)\right] \quad (7)$$

In same way the current can be written as

$$i_{s,sub}^{dq}(t) = H_{sub}(p + j\omega_m)\left[i_s^{dq}(t) - i_{s,f}^{dq}(t)\right] \quad (8)$$

Solving equation (3) and (7) results the fundamental and the subsynchronous components of voltage. Similarly, by solving equations (4) and (8) results the subsynchronous and the fundamental components from the measured current.

To assure the subsynchronous current component to zero, the subsynchronous voltage component of bus is injected by SSSC in the proposed control strategy. The Laplace domain of SSCC (sub-synchronous component controller) can be written as

$$V_{SSSC}{}_{sub}^{(dq_m)*}(s) = v_{s,sub}^{dq_m}(s) + (R + j(\omega_0 - \omega_m)(L_T + L^{\cdot\cdot}))i_{sub}^{(dq_m)}(s) + (K_p + \frac{K_i}{s})[i_{sub}^{(dq_m)}(s) - i_{sub}^{(dq_m)*}(s)] \quad (9)$$

$$I_{STAT}{}_{sub}^{(dq_m)*}(s) = i_{sub}^{dq_m}(s) + \frac{v_{s,sub}^{(dq_m)}(s)}{\left(R + j(\omega_0 - \omega_m)(L_T + L^{\cdot\cdot})\right)} + [(v_{s,sub}^{(dq_m)}(s) - v_{s,sub}^{(dq_m)*}(s)) \Big/ (K_p + \frac{K_i}{s})] \quad (10)$$

Figure2 illustrates the block diagram of SSCC. First three-phase currents and voltages which are measured from the line are converted in to αβ plane and then to dq-cordinate system with the help of θ_f(angle of transformation) obtained from PLL (phase locked loop). The resultant of the estimation block is the fundamental and

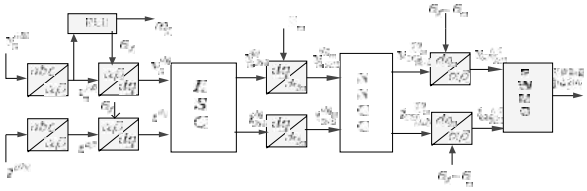


Figure2. Complete control diagram of SSCC

subsynchronous component of current and voltage in dq-frame of reference. The component of subsynchronous quantity is further transformed into dq_m-frame of systems using θ_m (transform angle), obtained by integrating oscillating frequencyω_m. The resultant quantities are then given to the SSCC. The output quantities of SSCC are again transformed into αβ-plane in and then to abc in natural reference frame and further given to the PWM pulse generator for switching the three phase 48 pulse voltage source converter.

IV. Realization of Apparent Impedance with Mid-Point STATCOM based SSR controller

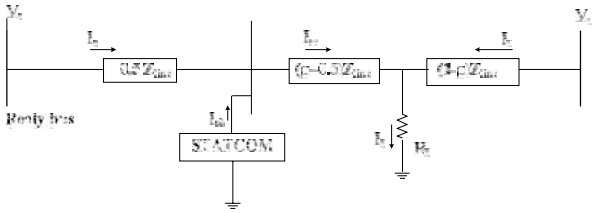


Figure 3. Simplified circuit of study with STATCOM during fault.

The apparent impedance expression is realized with STATCOM based SSR controller at centre of transmission line is realized, which is the basic step for calculating the adaptive distance relay setting. The digital distance relay is placed at bus A usually extracts the current and voltage samples and further the current and voltage in symmetrical components are utilized for calculating the apparent impedance. Generally Fast Fourier Transform (FFT) is used to calculate phasors (fundamental only) from voltage and current samples [15]. Fig.3 shows the simplified circuit of study system for line-1.

A. Apparent Impedance seen for Line to Ground Fault

With mid-point STATCOM and fault occur after the STATCOM in the line, the sequence voltage at relaying bus is expressed as follows:

$$V_{s1} = I_{m1}(\rho - 0.5)Z_{line1} + 0.5I_{s1}Z_{line1} + R_fI_{f1} \quad (11)$$

$$V_{s2} = I_{m2}(\rho - 0.5)Z_{line2} + 0.5I_{s2}Z_{line1} + R_fI_{f2} \quad (12)$$

$$[\text{Since } Z_{line2} = Z_{line1}]$$

$$V_{s0} = 0.5I_{s0}Z_{line0} + I_{m1}(\rho - 0.5)Z_{line0} + R_fI_{f0} \quad (13)$$

$$I_{m1} = I_{sh1} + I_{s1} \quad (14)$$

$$I_{m2} = I_{sh2} + I_{s2} \quad (15)$$

$$I_{m0} = I_{sh0} + I_{s0} \quad (16)$$

Where suffix,1, 0 and 2 represents positive, zero and negative sequence components. ρ is per unit distance of fault from relying bus.

V_{sa} can be obtained from sequence components as:

$$V_{sa} = V_{s1} + V_{s2} + V_{s0} \quad (17)$$

Substituting equation (11) to (16) in equation (17)

$$V_{sa} = \rho I_{sh1}Z_{line1} + \rho I_{s1}Z_{line1} - 0.5Z_{line1}I_{sh1} + R_fI_{f1}$$
$$\rho I_{s2}Z_{line1} + \rho I_{sh2}Z_{line1} - 0.5Z_{line1}I_{sh2} + R_fI_{f2}$$
$$\rho I_{s0}Z_{line1} + \rho I_{sh0}Z_{line1} - 0.5Z_{line1}I_{sh0} + R_fI_{f0} \quad (18)$$

Equation (18), represents the phase-a voltage at relying bus. Normalization of this equation will give the voltage (V_{sa}) in terms of line current (I_{fa}). For that, add and subtract ($\rho\, I_{s0}Z_{line1}$), ($\rho\, I_{sh0}Z_{line1}$), ($0.5\, I_{s0}Z_{line1}$) in equation (18) and after solving,

$$V_{sa} = \rho I_{sa}Z_{line1} + [(\rho - 0.5)(Z_{line0} - Z_{line1})(I_{sha} + I_{sho}) + \rho I_{s0}(Z_{line0} - Z_{line1})] + R_fI_{fa} \quad (19)$$

Considering R_f=0, the last term of equation (19) can be removed and zero sequence current of the STATCOM (I_{sh0}) as shown in (19) can be removed.

$$V_{sa} = \rho I_{sa}Z_{line1} + [(\rho - 0.5)(Z_{line0} - Z_{line1})I_{sha} + \rho I_{s0}(Z_{line0} - Z_{line1}) \quad (20)$$

$$Z_{app} = \frac{V_{sa}}{I_{sa} + mI_{s0}} \quad (21)$$

where, compensation factor i.e. $m = \frac{Z_{line0} - Z_{line1}}{Z_{line1}}$

Substituting the value of V_{sa} in (21) and after simplification we get,

$$Z_{app} = \rho Z_{line1} + \frac{(\rho - 0.5)I_{sha}Z_{line1}}{I_{sa} + mI_{s0}} \quad (22)$$

From equation (22), it is seen that in absence of STATCOM on the line (I_{sha}=0), calculated apparent impedance by the distance relay is only the function of Z_{line1} and the per unit distance (ρ) of fault point from relaying bus.

B. Apparent Impedance seen for LLL fault

the apparent impedance seen by the distance relay for LLL fault with R_f =0 can also be calculated in the same way

$$Z_{app} = \rho Z_{line1} + \frac{(\rho - 0.5)I_{sh}Z_{line1}}{I_s} \quad (23)$$

V. Adaptive Digital Distance Protection with Mid-Point STATCOM

Adaptive Protection scheme allows adjustments to various functionalities of protection in order to make them more recognizable to existing power system conditions [16-18]. To take prompt decision of trip or no trip for fault in the first zone of protection, compare obtained apparent impedance with distance relay first zone setting (Z_{set}) of relay. By considering the apparent impedance calculated in (22) to be equal to distance relay setting (80% of line)

$$Z_{app} = Z_{set} = 0.8Z_{line1} \quad (24)$$

Comparing equation (22) and (24), we get

$$0.8Z_{line1} = \rho Z_{line1} + \frac{(\rho-0.5)I_{sh}Z_{line1}}{I_s+mI_{s0}} \quad (25)$$

$$0.8 = \rho + (\rho - 0.5)\frac{I_{sh}}{I_s+mI_{s0}} \quad (26)$$

Let $\rho = (\mu + 0.5)$, substituting in (26)

$$0.8 = (\mu + 0.5) + \mu\frac{I_{sh}}{I_s+mI_{s0}} \quad (27)$$

$$\mu\left(1 + \frac{I_{sh}}{I_s+mI_{s0}}\right) = 0.3 \quad (28)$$

$$\mu = \frac{0.3}{\left(1+\frac{I_{sh}}{I_s+mI_{s0}}\right)} \quad (29)$$

Putting $\mu = (\mu + 0.5)$ in (29) we get,

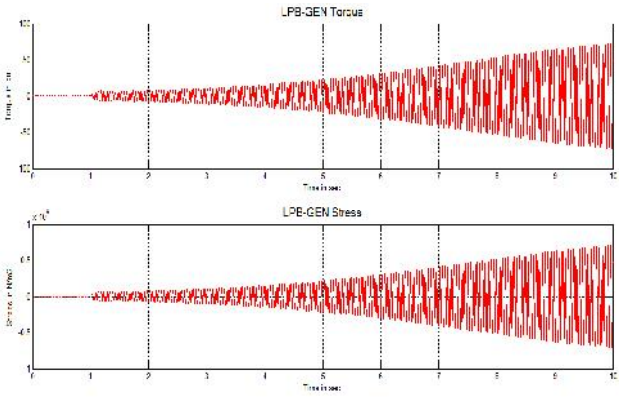


Figure 5. Simulated Turbine-Generator shaft Torque, Stress between LPB-GEN of Study system model without SSC based STATCOM.

$$\rho = 0.5 + \frac{0.3}{\left(1+\frac{I_{sh}}{I_s+mI_{s0}}\right)} \quad (30)$$

Hence to get the new setting, multiply equation (30) with Z_{line1}.

$$Z_{setnew} = \rho\, Z_{line1} \quad (31)$$

Multiplying equation (30) with (Z_{line1}) and substituting in (31), we get

$$Z_{setnew} = \left(0.5 + \frac{0.3}{\left(1+\frac{I_{sh}}{I_s+mI_{s0}}\right)}\right)Z_{line1} \quad (32)$$

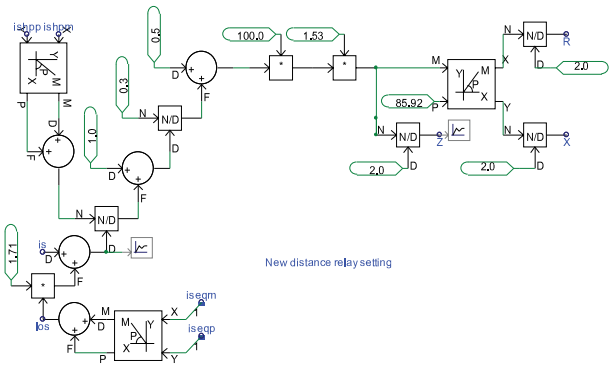


Figure 4. Simplified circuit of study system with STATCOM during fault.

From mentioning above equation, some important information is remarked as:

(i) If the injected current of STATCOM is capacitive, that is I_{sh} is positive and there is an increase in adaptive zone where as for inductive (I_{sh}) is negative and there is decrease in adaptive zone.

(ii) Depending on the compensation level the proposed adaptive distance protection setting will automatically adjusts the first zone reach.

(iii) With the nature of injected voltage the adaptive distance protection primary zone setting formula adjusted adaptively.

(iv) Injected current of STATCOM will also affect the calculation of apparent impedance with fault after STATCOM.

The location of STSATCOM also affects the calculation of apparent impedance. Modelling of Adaptive distance protection is shown in Figure 4.

VI. Simulation Results and Discussions

To test the efficiency of the suggested controller to diminish SSR, the study system model with SATCOM is simulated in Mat lab-Simulink environment. With 55% compensation, a symmetrical (LLL) fault is initiated at 1sec for duration of 0.05 sec to the grid. Due to the SSR, the oscillations are increased between the various sections of the turbine-generator shaft after the clearance of fault. Figure 5 illustrates LPB - Generator torque and stress. Even though the fault is clear the mechanical stress and torque of LPB-Generator are amplifies with a faster rate because of SSR which is avoidable.

The STATCOM injects the shunt current into the line in accordance with the triggering pulse produced by the PWM generator. The control of firing angle for STATCOM is designed based on the knowledge of Subsynchronous component controller. Figure6 illustrates the SSR mitigation with shunt injected current supplied by STATCOM. The magnitude of current injected in to the line with STATCOM is shown in Figure 7.

To investigate the effectiveness of the suggested adaptive distance protection scheme with STATCOM shown in Figure 1 is simulated in PSCAD software. If the STATCOM takes reactive power (inductive), the mid-point voltage decreases as compared to nominal operating voltage in absence of STATCOM. This leads to relay bus voltage to reduce and further there is a decrease in seen impedance (apparent) by distance relay causes to over-reach. The ρ (setting factor) for adaptive distance relay with STATCOM taking reactive power of 100 MVAR (inductive) for forward power flow is shown in Figure 8.

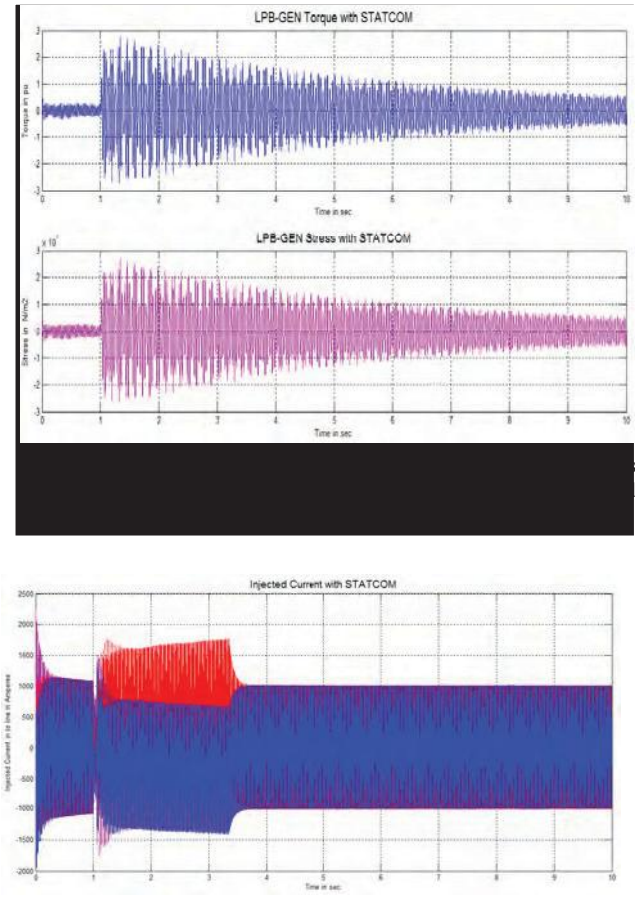


Figure 7. Injected Current in to the line to mitigate SSR oscillations with SSC based STATCOM

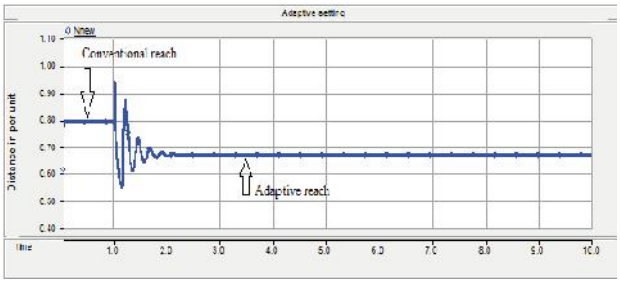


Figure 8. Adaptive Distance Protection Setting factor ρ with reactive power of 100 MVAR (inductive) of STATCOM.

If the STATCOM enters into the system at 1.05 sec and taking reactive power of 100 MVAR (inductive) for this the setting factor ρ is is reduced adaptively to 0.7671 per unit distance and it takes 40 milliseconds to acquire new adaptive setting which is shown in Figure 9.

With capacitive reactive power injected by STATCOM, there is an increase in the mid-point voltage in comparison with usual operating voltage in absence of STATCOM. Further increase in voltage of relay bus also cause an increase in seen impedance (apparent) by distance relay leading to under-reach. The calculated adaptive relay setting factor for STATCOM supplying 100 MVAR (capacitive reactive power) into the system for forward power flow is shown in Figure 10. It is observed that the setting factor is 0.8 in absence of STATCOM. With the insertion of STATCOM at 1.1 seconds the setting factor is adaptively increased and settled to 0.8425 per unit in 25 milliseconds.

Figure 11 clearly shows the conventional mho relay and

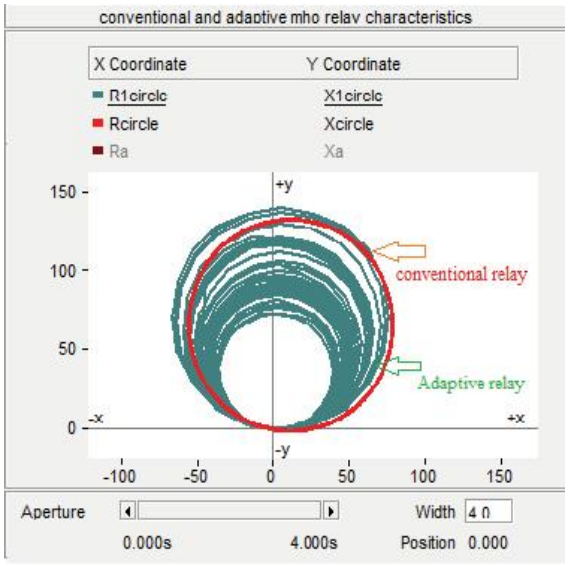


Figure 9. Characteristics of Adaptive Mho relay Distance Protection with STATCOM supplying reactive power of 100 MVAR (inductive)

adaptive mho distance relay with different colours. With the injection of capacitive reactive power, there is an increase in adaptive mho relay reach as compared with conventional mho relay reach.

The variation of adaptive setting factors obtained by varing the STATCOM reference reactive power injection

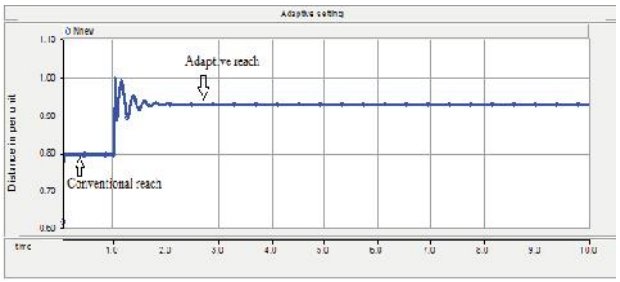


Figure 10. Adaptive Distance Protection Setting factor ρ with STATCOM supplying reactive power of 100 MVAR (capacitive).

(Q_{ref}) in step of 10 MVAR. The positive value represents the reactive power injection of capacitive and the negative value represents the reactive power of inductive. When STATCOM is in inactive mode the system neither injects nor absorbs any reactive power and the corresponding setting factor is 0.7998. For power flow A to B, the setting factor (adaptive) is 0.7671, 0.7998 and 0.8425 per unit distance for 100 MVAR inductive compensation level, 0 MVAR and 100MVAR capacitive respectively. Adaptive setting factor is 0.8575, 0.7998 and 0.7071 for compensation level of 100 MVAR capacitive, 0 MVAR and 100 MVAR inductive respectively for power flow B to A.

VII. Conclusions

In this research article a robust subsynchronous component based STATCOM controller with adaptive setting scheme is proposed to mitigate the SSR and its effect on distance protection of transmission line. By injecting the current (shunt) into the line using STATCOM, the adverse effect of SSR on turbine-generator is reduced to a great extent. In order to diminish the effect of STATCOM at midway of transmission line on distance protection an adaptive setting scheme is proposed. For various compensation levels, the reported adaptive distance protection setting algorithm (first zone) gives required data for modifying the zone reach of mho distance relay. For lower level of compensation, the Adaptive distance protection setting factor is reduced and is increased for higher level of compensation. By comparing the conventional technique with proposed adaptive scheme, there is a noteworthy enlarges in the enclosed area by distance relay and the false operation of distance relay with SSSC has been overcome. Finally, the simulation result illustrates the robustness of the suggested distance relay setting, the zone is increased adaptively and gives very accurate relay trip decision.

Appendix

The study system parameter of IEEE first bench mark model, SSSC parameter and Bergeron model are given in Tables I-III [1, 3, 4, 15, 16].

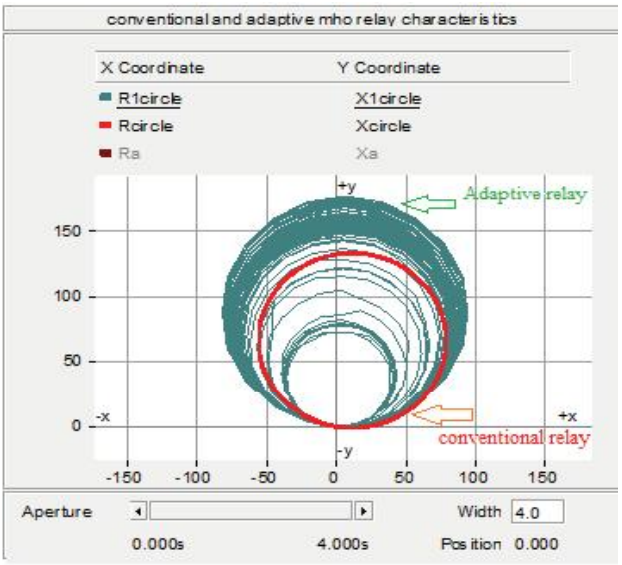


Figure 11. Characteristics of Adaptive Mho relay Distance Protection with STATCOM supplying reactive power of 100 MVAR (capacitive).

TABLE I
STUDY SYSTEM NETWORK PARAMETERS

Network resistance	R_L	0.0113 pu
Transformer reactance	X_T	0.142
Transformation ratio		22/539KV
Line reactance	X_L	0.50pu
Transmission line reactance	X_{sys}	0.08pu

TABLE II
SYNCHRONOUS MACHINE PARAMETERS

Reactance	Value [pu]	Time constant	Value [sec]
X_a	0.130	T'_{d0}	4.3
X_d	1.79	T''_{d0}	0.032
X'_d	0.169	T'_{q0}	0.85
X''_d	0135	T''_{q0}	0.05
X_q	1.71		
X'_q	0.228		
X''_q	0.200		

TABLE III
STUDY SYSTEM DATA OF FIG.1.

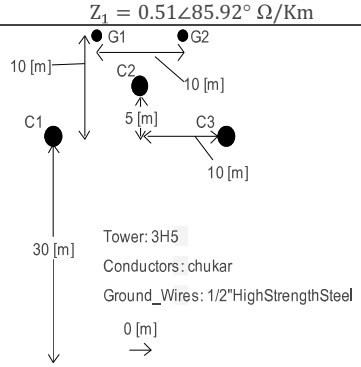
Study System Elements	Quantity
Equivalent Source (1-6)	Frequency of System = 60Hz Voltage of System = 230 KU $Z_1 = 25.9\angle 80° \Omega$ $Z_0 = 25.9\angle 80° \Omega$
Connecting Transformer = (Y/y/d) 3 winding	Impedance of Transformer = 0.1 p.u. Transformer ratio =230/11/11KV Rating of Transformer = 200 MVA
STATCOM rating	+/- 100 (inductive & capacitive)
Transmission Line (I-V)	Line length = 300 Km $Z_0 = 1.385\angle 74.68° \Omega$/Km $Z_1 = 0.51\angle 85.92° \Omega$/Km
Fig A.1 shows the physical structure of the Bergeron model.	

Fig.A.1. Transmission Line in Bergeron model

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An Experimental Investigation to Predict the Influence of Number of Peltier Modules and Input Voltage during Non-Conventional Cooling

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***Abstract*—Requirement of low temperature (air conditioning and refrigeration) has many applications in the industry. However, excessive use of refrigerants for this purpose leads to ozone depletion and increase in global warming. Development of an alternative eco-friendly refrigeration system is in great demand. Non-conventional cooling using Seebeck and Peltier effect is gaining importance as an alternative. The data pertaining to the number of modules and input voltage required to obtain a specific temperature drop is not available in the literature. Hence, in the present work an equipment is developed and experimental investigation is carried out to find the effect of number of modules and the input voltage to obtain a temperature drop of water by 10 ^{O}C. The time taken for lower input voltages (2 V to 6 V) is 50 to 30 minutes. For input voltage of 10 V the time taken to reduce the temperature of water is only 10 min. The data obtained from the experimental investigation predicts the number of modules required to cool the water to 0 ^{o}C and also the heat transfer rate for every 1 ^{o}C change in temperature. The results will help to design thermo-electric coolers of different capacities with temperature control.**

***Index Terms*—Peltier Effect, Refrigeration, Non-conventional cooling**

I. Introduction

Global warming and Energy crisis have become the major concern for developing as well as developed countries. Conventional refrigeration systems, besides having many industrial /domestic / commercial applications significantly contribute to ozone layer depletion and energy consumption. Hence, the need for non-conventional and systems with energy conservation are gaining more and more importance. Thermo-electric refrigeration is one of the solutions and the present research work focuses on the non-conventional cooling using Peltier effect. The advantage of this technique is that there are no moving parts, lightweight, free of maintenance, silent during work, less electrical consumption, heating and cooling can be done with the same module, wide operating temperature range, highly precise temperature control (to within 0.1°C) and environment friendly.

S.B. Riffat et al.[1] applied thermo-electric system for refrigeration. Cold side was replaced with a heat pipe and phase change material. Without the use of heat sink fan, the temperature of the cold junction was reduced few degrees and then increased. However, by using a fan the cold junction temperature continued to decrease. Anutosh Chakraborty and Kim Choon Ng [2] formulated for the entropy flux and plotted T-S diagram for thermo-electric cooler. Current density, temperature gradient, Seebeck coefficient and local temperatures were considered as the parameters which effects the cooling. Chien-Yi Du and Chang-Da Wen [3], experimentally and numerically analyzed a one-stage thermo electric cooler. The thermo electric cooler was made of Thomson effect. An increase in temperature difference between hot and cold side was observed for higher current input. It was emphasized that a specific current is to be selected during the design of a thermo-electric cooler. Satheeshkumar Palaniappana and Balachander Palanisamy [4] analyzed and compared Pb-Te and Bi-Te combination for thermo-electric modules. At ambient temperature, Pb-Te module showed lower performance than Bi-Te module. Gang Tan and Dongliang Zhao [5] introduced a design procedure to integrate thermo-electric cooling with a phase change material. Wei et al.[6] reviewed the development of the thermoelectric cooler and generator. They suggested for a research of materials with high "figure of merit" and generator to be used for the electricity production in place of PV technology. ZhongBing Liu et al.[7] reviewed various thermoelectric cooling techniques used for zero energy buildings. Yazeed Alomair et al.[8] constructed a chiller using thermo-electric cooling. With increase in water bulk mean temperature, the heat removal rate was observed to increase. The capacity of the evaporator significantly affected heat removal rate.

Earlier researchers have used thermoelectric modules for cooling and heating but the data related to the number of modules required to obtain a heating/cooling rate is not available. Hence, an experimental setup is designed and developed to obtain time-temperature data with respect to the variation in input voltage and number of modules. The data will be used to propose the input voltage and number of modules required to obtain the temperature difference of 10 ^{o}C and the results can be extrapolated to obtain higher cooling rates.

A. Principle of Peltier Effect

If current is passed through a pair of dissimilar metals, there occurs heating at one junction and cooling at the other junction. The schematic of Peltier circuit is shown in Fig. 1. Two junctions are made with two dissimilar metals A and B. When voltage is applied, one junction shows low temperatures and the other junction shows high temperatures.

The amount of temperature difference depends upon the material combinations. Peltier varied the current and observed the heating and cooling rate for different sets of elements. He found that:

$$q \alpha I \quad (1)$$

where q is the cooling or heating rate and I is the current. The proportionality constant is called as Peltier coefficient, π i.e.,

$$q = \pi * I \quad (2)$$

where π is the coefficient for two different metals.

Hence Peltier effect can be used to replace the conventional refrigeration system. In the present work the Peltier Module made of Bismuth and Telluride is employed.

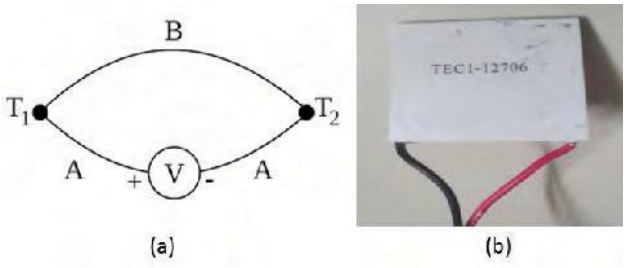

Figure 1. (a) Schematic of Peltier Circuit (b) Module

II. EXPERIMENTATION

Aim of the present work is to reduce the temperature of 500 ml of water by 10 ^{o}C and suggest input voltage, time taken and number of modules required to meet this objective. An equipment is designed and constructed to perform experimental investigation. The components required by the equipment are a) Thermo-electric module b) Tapping transformer c) Heat sinks d) Fans e) MCB unit f) Digital temperature indicator g) Thermo couple h) Energy meter i) Thermo coal container with copper plates attached to modules j) Five copper plates of 0.5 mm thick and 20 sq.cm area h) Thermal paste. The technical specifications of the thermo-electric module (Fig. 1(b)) used in the equipment are as given in table I below.

TABLE I
TECHNICAL SPECIFICATIONS OF THE PELTIER MODULE

1	Operational voltage	12 V DC
2	Current Max.	6 Amp
3	Power Nominal	60 Watts
4	Power Max.	92.4 Watts
5	Operating temperature	-30 ^{o}C to 70 ^{o}C
6	Couples	127

Figure 2. Transformer with five ouput voltages (2V, 4V, 6V, 8V, 10V)

Figure 3. Experimental Setup

A circuit consisting of transformers, five in number, is designed to convert the available AC power input to DC (Fig. 2). There are five output terminals each having a maximum capacity of 10 amps at 12-Volt DC current. In the experimentation, it is required to vary the input voltage to the module. As the maximum voltage input to the modules is 12 V, tapping transformer is specially designed to vary the voltage from 2 V to 10 V individually for each thermo electric module. For this purpose knobs are attached to each of the terminals to vary the voltage from 2 to 10 in steps of 2 Volts.

Fig. 3 shows the complete equipment designed for the experimentation. Cold side of five thermo-electric modules (Peltier modules) are attached to the copper plates, placed at the bottom of the container holding 500 ml water at atmospheric temperature. Each module is connected to the tapping transformer. The transformer 5 outputs are

connected to the main circuit and each output is controlled by a switch. The switches are used to on/off the supply of voltage to each module. Each module (hot side) is mounted on an aluminum heat sink and each heat sink is connected to a 12 V, DC cooling fan. Each cooling fan is connected to the main power supply using an on/off switch. As the input supply to the fans is to be DC, a converter for each fan is employed. A digital temperature indicator is connected to a thermo couple probe to measure the temperature of ambient air and water.

500 ml of water is taken in a container made of thermo coal. Thermo coal is selected as a container to prevent the heat loss from the walls to the atmosphere. Copper plates are placed in the grooves provided at the bottom of the container and the gap is sealed with water resistant gum. Water is in contact with the copper plates fixed on the cold side of the Peltier modules. Heat sink is attached directly on the hot side of each module. A small out let pipe is grooved at the bottom of the container to remove and replace the water for every experiment. The pipe is closed during the experiment with a clip. Initial and final temperature of water is recorded for every experiment.

In the first set of experiments, temperature of water is recorded (Table II) by changing the input voltage to 2 V, 4 V, 6 V, 8 V and 10 V. As the rated voltage is 12V, the maximum operating limit is taken as 10 Volts. Water is removed and replaced for every experiment. Atmospheric temperature is recorded as 35 ^{o}C.

TABLE II.
RECORD OF TEMPERATURE OF WATER VARYING VOLTAGE

Expt. No.	No. of Modules	Voltage of each module (V)	Initial temperature of water (^{o}C)	Final temperature of water (^{o}C)	Heat transfer rate Q (W)
1	4	2	33	32	2090
2	4	4	33	30	6270
3	4	6	33	28	10450
4	4	8	33	25	16720
5	4	10	33	22	22990

In the next set of experiments the temperature of water is recorded (Table III), keeping the input voltage as maximum i.e 10 V, varying number of modules as 1, 2, 3 and 4. The time given for each experiment is 10 minutes. As mentioned earlier water is removed and replaced for every experiment.

TABLE III.
RECORD OF TEMPERATURE OF WATER VARYING NUMBER OF MODULES.

Expt. No.	No. of Modules	Voltage of each module (V)	Initial temperature of water (^{o}C)	Final temperature of water (^{o}C)	Heat transfer rate Q (W)
6	1	10	33	32	2090
7	2	10	33	30	6270
8	3	10	33	27	12540
9	4	10	33	22	22990

Final experiment is performed with 5 modules, input voltage at 10 V, initial temperature of water and atmosphere at 33 (^{o}C) and 34 (^{o}C) respectively. Four modules are placed one at each corner and the fifth module is placed at the center of the container. The Time-Temperature history of water is recorded (Table IV) and tabulated.

TABLE IV.
TIME-TEMPERATURE HISTORY OF WATER

S.No	Temp. of Water (^{o}C)	Time (minutes)	Total heat transfer rate at a given instant of time Q(W)	Heat transfer rate for every 1 ^{o}C change in temperature Q (W)
1	33(Initial)	0	0	0
2	32	0.3	2090	2090
3	31	0.7	4180	2090
4	30	1.1	6270	2090
5	29	1.6	8360	2090
6	28	2.3	10450	2090
7	27	3.1	12540	2090
8	26	3.9	14630	2090
9	25	4.8	16720	2090
10	24	5.7	18810	2090
11	23	6.7	20900	2090
12	22	7.6	22990	2090
13	21	8.9	25080	2090
14	20	11.2	27170	2090

III RESULTS AND DISCUSSION

A. Effect of Input Voltage

Water at an initial temperature of 33 ^{o}C is cooled using 4 Peltier modules placed one at each corner of the container varying the input voltage 2 V, 4V, 6V, 8 V and 10 V. The temperature of water is reduced with increase in input voltage (Table II). The time taken for lower input voltages (2 V to 6 V) is about 50 to 30 minutes. The final temperature is recorded once the drop in temperature is steady. However for input voltage of 10 V the time taken to reduce the temperature of water is only 10 min. and the drop is unchanged later with time.

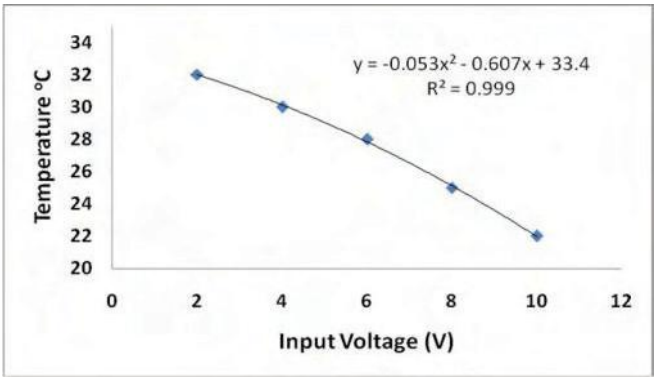

Figure 4 Variation of temperature with increase in input voltage

It can be inferred from this result that the cooling rate can be increased or decreased by increasing or decreasing the voltage input (Fig. 4). However, as the rated voltage of the module is 12 V, the maximum input voltage is fixed to 10 V. It is interesting to observe that for a specific input

voltage the temperature of water reaches a steady state. The investigation is continued to find the effect of number of modules on cooling rate.

B. Effect of number of Modules

Keeping initial temperature of water at 33 ^{o}C and input voltage at 10 V, experiments are performed by varying the number of modules. Input voltage is supplied for each module through each output of the transformer.

Table II gives the record of temperature of water for increase in number of modules. Fig. 5 gives the variation of temperature of water with increase in number of modules. Equations shown in the graphs are obtained by curve fitting the experimental data points. These equations can be used to interpolate or extrapolate to predict the values beyond the range of observed data.

With increase in number of modules the rate of cooling is increased. For an input voltage of 10 V using one module give a temperature drop of only 1 ^{o}C in 10 min. However using 4 modules the drop in temperature is increased to 11 ^{o}C. The result can be inferred that with increase in number of modules the drop in temperature or cooling rate can be increased. In the present experimentation, a temperature drop of 10 ^{o}C is achieved using 4 modules at 10 V, within 10 Minutes.

The last experiment is repeated to record the temperature-time history while cooling of 500 ml of water initially at 33 ^{o}C with 5 modules at 10 V (Table III). Fig. 6 gives the drop in temperature of water with time. It clearly shows that with increase in time the drop in temperature is increased. It has been observed with 4 modules that a temperature drop of 10 ^{o}C is achieved in 10 minutes and there is no further drop with time until an addition of one more module.

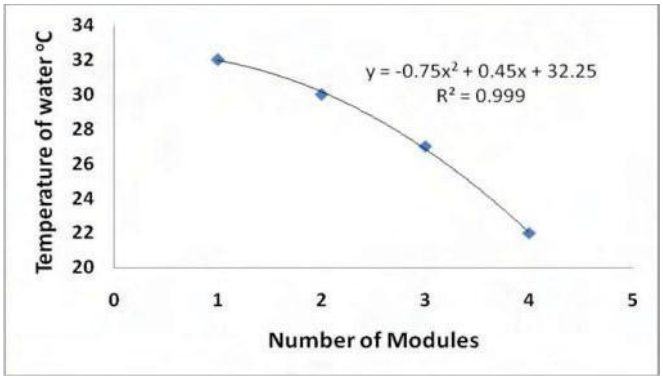

Figure 5. Variation of temperature with increase in number of modules

Fig. 7 shows the graph obtained from the extrapolated experimental data to predict the number of modules required to further reduce the temperature of water. It is interesting to observe that if the number of modules is increased to 7, the temperature of water can be reduced to 'zero' degree Celsius for the present quantity of water taken. The work can be extended further by varying the quantity of water and time required to cool to the required temperature.

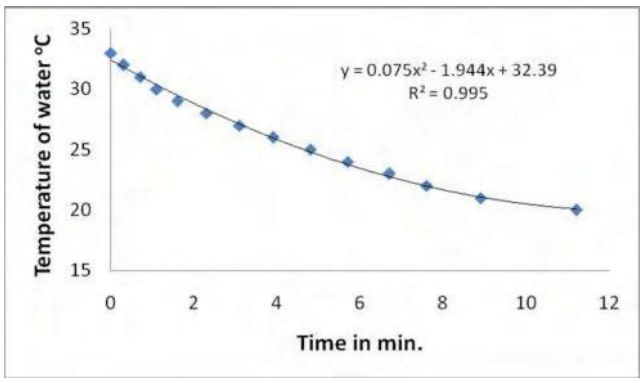

Figure 6. Fall in Temperature of water with time with 5 modules

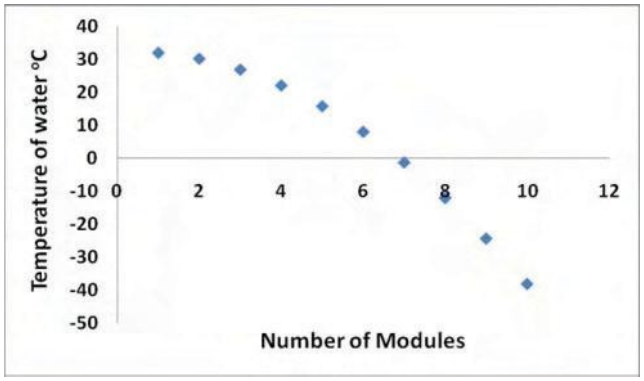

Figure 7. Extrapolated data for increase in number of modules

C. Heat Transfer rate

Heat transfer rate depends on the convective heat transfer coefficient 'h' between the copper plates and water. However, the value of 'h' for the present system is unavailable in the literature. Hence, the heat transfer rate is estimated using the heat lost by the water varying the input voltage and number of modules. The following heat energy equation is used for this purpose.

$$Q = m\, C_p\, \Delta T_w \qquad (3)$$

where m=mass of water

C_p = specific heat of water

ΔT_w= difference in initial and final temperature of water

Fig. 8 shows the change in heat transfer rate with increase in input voltage. Table II shows the heat transfer rate estimated for each experiment. The value of 'Q' is increased with increase in input voltage. This is because of the increase in heat absorption by the copper plates with voltage. As all the final temperature values are recorded after the steady state condition, the heat transfer shows direct proportionality with voltage.

$$Q \propto V \qquad (4)$$

Table III shows the change in the value of 'Q' with increase in number of modules. The value increased with increase in number of modules as the convective area increases. It is interesting to observe that the 'Q' value achieved in 10 min. at higher voltage (10 V) is same when 4 modules are used at lower voltages. i.e when 4 modules at 2 V and 4 V obtained a heat transfer rate of 2090 W and 6270 W respectively (Table II, Expt. No. 1 &2). Whereas, at 10 V (i.e highest voltage) the heat transfer rate is same when there are 1 module and 2 modules respectively (Table III, Expt. No 6 &7). For the first case the time taken is more (nearly

50 min). But the experimental results given in table III are taken at 10 min. for each experiment. Fig. 8 shows the change in heat transfer rate with change in input voltage.

Table IV shows the value of heat transfer rate for every 1 ^{o}C change in temperature. It is interesting to observe that the value of Q is 2090 W even with 5 modules operating at 10 V each which is same as Expt. No. 1 and 6. This is because of continuous cooling the difference in temperature of water is less. But, during the experiments 1 to 9 the ΔT of water is high. Total heat transfer rate with five modules is 27170 W. Table III and IV clearly show that, to obtain a required temperature drop, the time required with more number of modules is less.

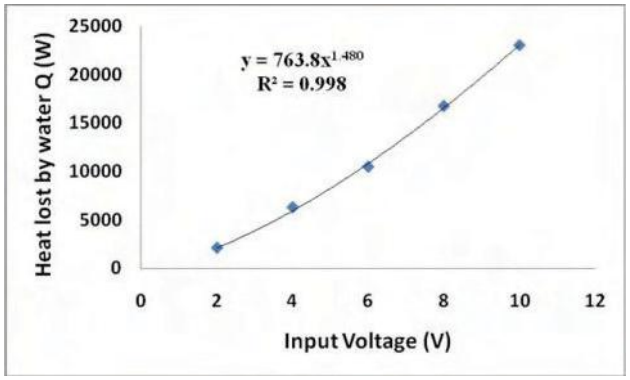

Figure 8. Heat lost by water with increase in input voltage

IV. Conclusions

An experimental investigation is carried out to obtain low temperatures using Peltier Modules and find the effect of increase in input voltage and number of modules on drop in temperature of 500 ml of water.

- Drop in temperature of water is increased with increase in input voltage. The difference of temperature increases between the hot and cold surfaces of the modules with increase in voltage input.
- Cooling rate increases with increase in number of Peltier modules as cooling area is increased.
- Increase in input voltage increases cooling rate. Time taken for cooling is lowest at the rated voltage.
- Extrapolated data shows sub-zero temperatures can also be attained with increase in number of modules.
- The data recorded can be used to design controlled cooling units using Peltier modules.

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Design and Analysis of Seven Stage Progressive Tool for Automobile Engine Starter Key

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Abstract: **Sheet metal operations are carried out in press machine. Mainly, the types of tools are simple tool, compound tool and progressive tool. Progressive tools have high productivity, maximum stock strip utilization and have low cost as well. Close tolerances can also be achieved in a progressive tool. This paper describes the design of a seven stage progressive tool for irregular-shaped sheet metal automobile engine starter key of brass alloy material. The software used for modeling and assembling is CATIA V5. Finite element analysis using ANSYS 14.0 is performed on the punches to ensure the working condition of the tool well within the limit.**

Index Terms: **Strip layout, progressive tool, press capacity**

I. Introduction

Metal stamping process is popular because of high productivity, ease in manufacturing, production of intricate shape and low cost [1].

Progressive die design is an important component of tool engineering. It consists of two or more dies and can perform multiple operations in single stroke of the press machine. The work is carried forward to next station at each press stroke. Products made by progressive tool can be found in almost all household or industrial appliances which are made by sheet metal [2]. Waller identified four factors which are quite essential to execute first class presswork which are good operation planning, excellent tool design, accurate tool making and knowledgeable press setting [3].

Design of right tool is the foremost aspect of tooling as it holds a considerable portion on overall cost of the manufactured component. It's important to keep the tooling cost low without compromising the longevity of the tool as well [4].

In most industries, progressive die design is an art rather than a science. The tooling, the design sequence is decided based on individual designer's skill and knowledge which are accumulated primarily through working experience [5].

In this paper, a seven stage progressive tool for automobile engine starter key is designed and finite element analysis is conducted over the punches. The 3D CAD model of the automobile engine starter key is shown in figure 1.

II. Component Details

The progressive die is to be designed for an automobile engine key starter of brass alloy. The details of the alloy and other properties such as thickness of the stock strip, shear strength, area of the component (obtained through CAD model), volume and weight of the component are tabulated in table 1.

TABLE I.
COMPONENT DETAILS

Material	ISO CuZn35Pb1 Brass
Thickness	2 mm
Shear strength (kg/mm2)	24 kg/mm2
Area of the component	525.735 mm2
Volume of the component	1051.47 mm3
Weight of component	8.8401047 g

Figure 1. 3D CAD model of the key

III. Strip Layout Development And Shear Force Calculation And Press Capacity

The first step of designing a progressive tool is development of the strip layout. It represents the sequence of operations to be carried out in each stages (or stations) [6].

A. Strip Layout

A = Back scrap = Front scrap = 2mm
B = Bridge scrap = 2mm
Width of the stock = 80mm
Pitch = B + L = 51.52 mm

Equation 1 shows the percentage utilization of the stock strip. The development of strip layout is shown in figure 2.

% Stock strip utilization (n)

$$n = \frac{Area\ of\ blanks\ from\ the\ strip}{Area\ of\ strip\ before\ blanking} \times 100 \quad (1)$$

= 74.1 %

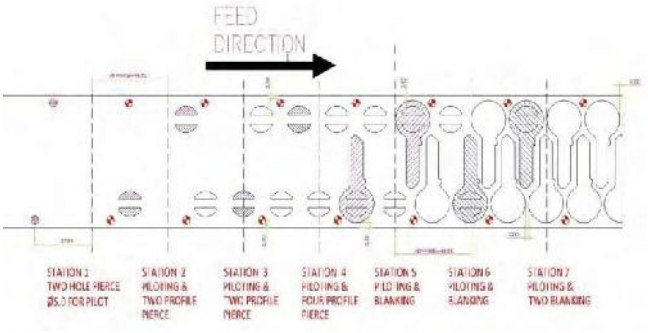

Figure 2. Development of the strip layout

As shown in figure 2, from the left hand side, at station 1 two holes for piloting are pierced. At stage 2 and 3 piloting on the sheet is done along with piercing two profile holes respectively.At station 4 four profile holes are pierced and at station 5 blanking of the outer profile of the key is performed. At station 6 and station 7, two blanking of two key profiles are performed in zigzag orientatation to have maximum stock utilization.

B. Shear Force calculation in Tons (T)

Equation 2 shows the shear force for cutting in tons (T) [7].

Stock Thickness, t = 2mm

Total cutting perimeter, L = 824 mm (Obtained from CAD model)

$$\text{Shear force, } F_{sh} = \frac{K \times L \times t \times S_{sh}}{1000}\ \text{T} \quad (2)$$

K= Factor of safety = 1.35

S_{sh}= Shear strength of the stock material = 24 kg/mm^2

Therefore, F_{sh} = 53.3952 ≈ 54 T

C. Ejection force (F_{ej}) & Press Capacity (P_c) in tons (T)

The sheet metal after shearing gets stuck in the land provided in the die hole. Therefore, it is required to push the slug out of the die hole by applying ejection force or push through force. Press capacity is the capacity of the press machine in which the progressive tool has to be installed. Equation 3 and equation 4 shows the calculation for ejection force and press capacity respectively [7].

$$\text{Ejection force, } F_{ej} = 0.1 \times F_{sh} \quad (3)$$

= 0.1 × 54 = 21.6 T

$$\text{Press Capacity, } P_c = 1.5 \times F_{sh} \quad (4)$$

= 1.5 × 54 = 81 T

IV. Development Of The Progressive Tool

A. Clearance (C)

Equation 5 shows the calculation for clearance to be given between die and the punch for shearing [7].

$$C = 0.005 \times t \times \sqrt{F_{sh}} \quad (5)$$

= 0.063 mm per side

B. Die Block Design

Equation 6 shows the thickness of the die which is also known as the female member of the tool [7].

a) Thickness of the die (T_D)in mm

$$T_D = \sqrt[3]{F_{sh}} \times 10 \quad (6)$$

= 37.7 ≈ 38 mm

b) Land and draft

If draft is not given, internal stress in the punch will cause crack in the die block. The standard value of land is 8 mm and draft angle is 1/2°.

c) Thickness of Bottom and Top Bolster

Equation 7 and equation 8 show the calculation for calculating the thickness of the bottom bolster and top bolster of the die set respectively [7].

$$\text{Thickness of bottom bolster} = 1.75 \times T_D \quad (7)$$

= 66.5 ≈ 67 mm

$$\text{Thickness of Top bolster} = 1.25 \times T_D \quad (8)$$

= 47.5 ≈ 48mm

d) Stripper plate design

During return stroke the scrap material adheres to the punch and causes interference. Stripper plate is used to strip the scrap material from the die block.

There are two types of stripper plate i.e fixed stripper plate and floating stripper plate. The later is used when the stock thickness is less than 1 mm, number of stations is more and various operations are present.

Equation 9 shows the calculation of the thickness of the stripper plate.

$$\text{Thickness of the stripper plate, } T_{ST} = 0.5 \times T_D \quad (9)$$

T_{ST} = 19mm

e) Spring Design

When floating stripper plate is used, it is essential to use spring followed by shouldered pin. Mostly, helical springs are used for the floating stripper.

The two important parameters of spring design are maximum force (F_{max}) exerted by the spring shown in equation 10 and total deflection (Y_{max}) [8].

Stroke length or travel of the stripper in mm = Y_{st}

Y_{st} = (t+2) = 4 mm

Deflection of the spring = Y_{1max}

Y_{1max} = 4 times Y_{st} = 16 mm

Considering resharpening allowance, s = 2mm

Y_{max}= Y_{1max} + s = 18 mm

Now,

$$F_{max} = \left(1 + \frac{s}{Y_{1max}}\right) \times F_2 \quad (10)$$

F_2= Force exerted by the spring in fully compressed position.

F_c= Cutting force

F_{st}= Stripping force

Equation 11 and equation 12 show the equation for force exerted by the spring in fully compressed position and stripping force respectively [8].

$$F_2 = \frac{1.5 \times F_{st}}{i} \quad (11)$$

$F_c = L \times t \times S_{sh}$
= 39552 kgf
i= Number of springs = 23

$$F_{st} = 8\% \text{ of } F_c \quad (12)$$

= 3164.16 kgf

Equation 13 and equation 14 show the calculation for wire diameter and deflection of one free coil respectively [8].

$F_2 = \frac{1.5 \times 3164.16}{23} = 206.35$ kgf
Therefore, F_{max} = 232.143 kgf

$$\text{Wire diameter, } d = \left[\frac{k \times 8 \times F_{max}}{\pi \times S} \times C\right]^{\frac{1}{2}} \quad (13)$$

Where, k = 1.36 (Wahl's factor which is calculated from graph between C and k)
S = Permissible shear strength of the spring material = 70 kg/mm^2

$C = \frac{D}{d}$ = spring index = 4
D = Coil diameter
Therefore, d = 6.75≈ 7 mm

$$\text{Deflection of one free coil, } Y_1 = \frac{8 \times F_{max}}{G} \times \frac{D^3}{d^4} \quad (14)$$

G = Modulus of rigidity of the spring = 8300 kg/mm^2
D= C × d = 4 × 7 = 28mm
Therefore, Y_1 = 2.04 mm

Equation 15, 16, 17 and 18 show the calculation for number of coils, compressed length of the spring, free length of the spring and pre-compressed length on assembly respectively [8].

$$\text{Number of coils, } n = \frac{Y_{max}}{Y_1} \quad (15)$$

= 8.82 ≈ 9 coils

$$\text{Compressed length, } L_{min} = (1.1 \times n \times d) + d \quad (16)$$

= 76.3 mm

$$\text{Free length of the spring, } L_0 = L_{min} + Y_{max} \quad (17)$$

= 94.3 mm
Pre-compressed length on assembly,

$$L_1 = L_{min} + Y_{st} + s \quad (18)$$

= 82.3 mm

V. Finite Element Analysis Of The Punches

A. Results for Piloting punch

The CAD models of the punches are imported to ANSYS 14.0 for validating the working of the tool. The type of element chosen is tetrahedron (10 nodes) shown in figure 3.

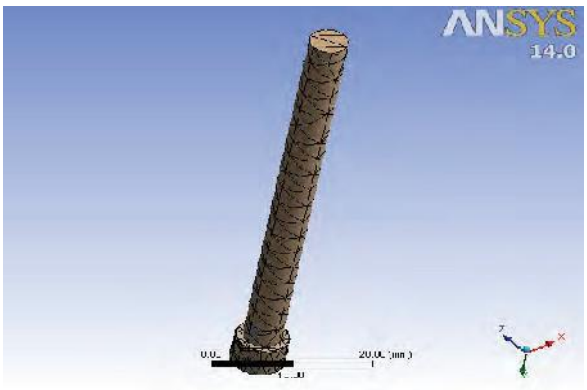

Figure 3. Meshing of the piloting punch (Tetrahedron 10-nodes)

Force required for piloting punch = $\frac{L_p \times t \times S_{sh1}}{1000}$ Tons
L_p= Length of cut by the piloting punch = πD_p
D_p= Diameter of the piloting punch = 5 mm
L_p= 15.71 mm
S_{sh1}= 24 kg/mm^2
Area of the piloting punch = $\frac{\pi}{4} \times D_p^2$ = 19.634 mm^2
Therefore, force required for piloting punch = 0.754 T or 7396.7 N

The results for maximum Von-Mises stress and total deformation after applying a load of 7396.7 N on the piloting punch are shown in figure 4 and figure 5.

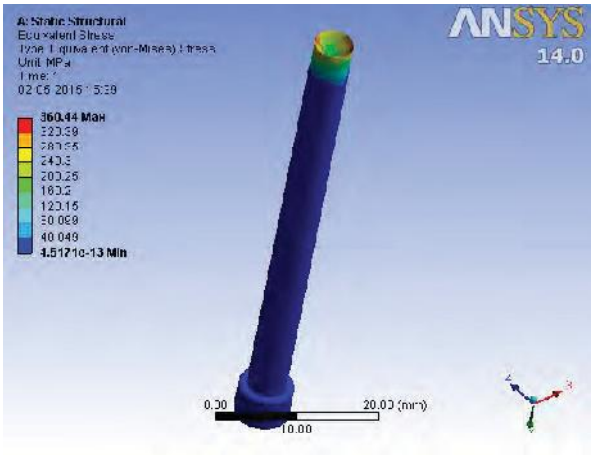

Figure 4. Von-Mises stress developed in the piloting punch

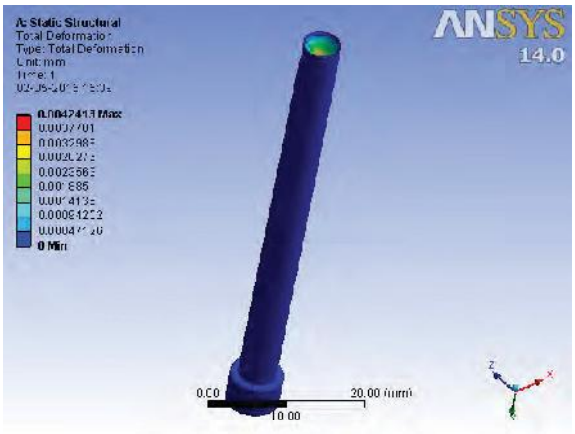

Figure 5. Total deformation occurred in the piloting punch

It is required to calculate the stress develop in the piloting punch analytically.

Stress developed (σ_1) in piloting punch in N/mm^2

$$\sigma_1 = \frac{Force\ required\ for\ piloting\ punch}{Area\ of\ the\ piloting\ punch} = 376.63\ \text{N/mm}^2$$

B. Results for piercing profile punch

Force required for piercing profile punch = $\frac{L_{p1} \times t \times S_{sh1}}{1000}$ Tons
L_{p1}= Length of cut by the piloting punch = 34.6 mm (Obtained by CAD model)
S_{sh1}= 24 kg/mm^2
Area of the profile punch = 37.79 mm^2
Therefore, force required the profile punch = 16294.4 N

The type of meshing for the profile punch is similar to the meshing for the piloting punch.

The results for maximum Von-Mises stress and total deformation after applying a load of 16294.4 N on the profile punch are shown in figure 6 and figure 7.

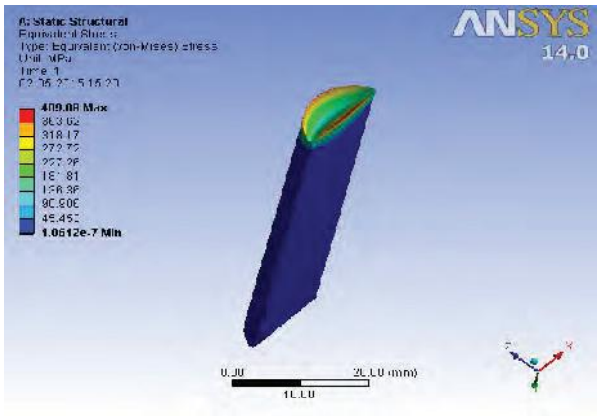

Figure 6. Von-Mises stress developed in the profile punch

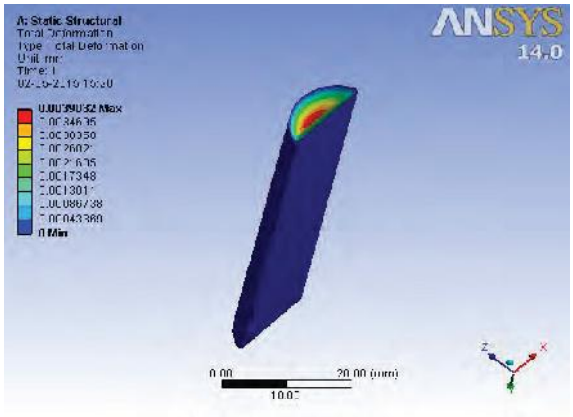

Figure 7. Total deformation occurred in the profile punch

It is required to calculate the stress develop in the profile punch analytically.

Stress developed (σ_2) in profile punch in N/mm^2

$$\sigma_2 = \frac{Force\ required\ for\ profile\ punch}{Area\ of\ the\ profile\ punch} = 431.11\ \text{N/mm}^2$$

C. Results for blanking punch

Force required for piercing profile punch = $\frac{L_{p2} \times t \times S_{sh1}}{1000}$ Tons
L_{p2}= Length of cut by the piloting punch = 128.8 mm (Obtained by CAD model)
S_{sh1}= 24 kg/mm^2
Area of the blanking punch = 161.05 mm^2

Therefore, force required the profile punch = 60822 N

The type of meshing for the blanking punch is similar to the meshing for the piloting punch.

The results for maximum Von-Mises stress and total deformation after applying a load of 60822 N on the blanking punch are shown in figure 8 and figure 9.

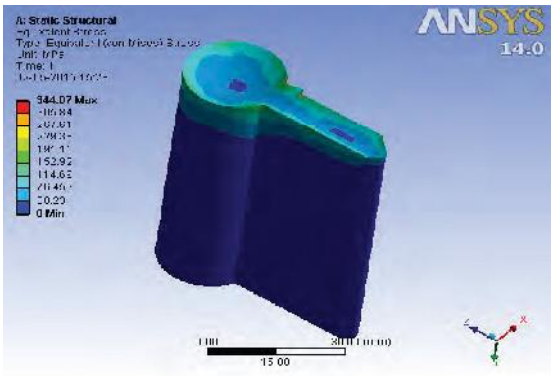

Figure 8. Von-Mises stress developed in the blanking punch

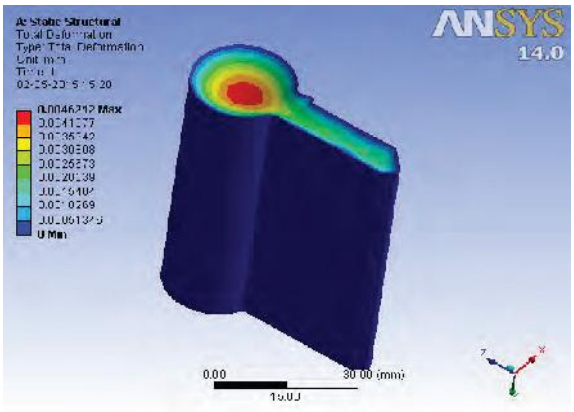

Figure 9. Total deformation occurred in the blanking punch.

It is required to calculate the stress develop in the blanking punch analytically.

Stress developed (σ_3) in blanking punch in N/mm^2

$$\sigma_3 = \frac{Force\ required\ for\ blanking\ punch}{Area\ of\ the\ blanking\ punch} = 377.64\ \text{N/mm}^2$$

VI. Results And Discussions

The results of obtained from finite element analysis and analytical method is tabulated in table II.

TABLE II.
RESULTS AND REMARKS

Serial number	Punches	Maximum Stress developed obtained through ANSYS	Stress developed analytically	Remarks
1.	Piloting Punch	360.44 MPa	376.63 MPa	Safe
2.	Profile Punch	409.08 MPa	431.11 MPa	Safe
3.	Blanking punch	344.07 MPa	377.64 MPa	Safe

The material of all the three punches is high carbon high chromium steel (D2 steel). Yield strength of D2 steel is 1476 N/mm^2 and the results obtained from both ANSYS and analytical method are less than the yield strength of the material. Hence, the material will not fail in the required working condition.

VII. FINAL ASSEMBLY

The final assembly consists of bottom bolster, stripper plate, punch plate and punches. The top assembly and bottom assembly are shown in figure 10 and figure 11 respectively.

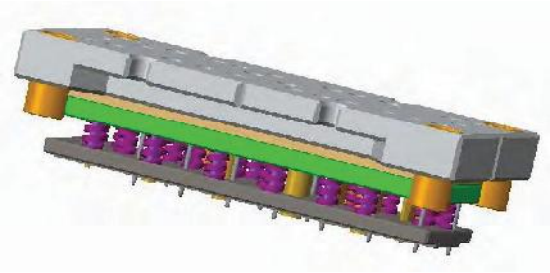

Figure 10. Top Assembly of the progressive tool

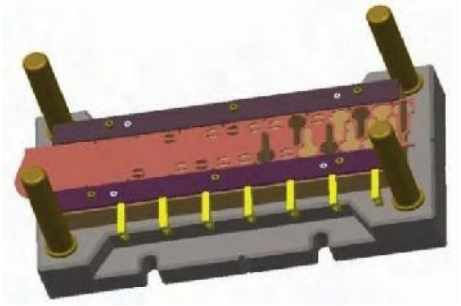

Figure 11. Bottom assembly of the progressive tool

VIII. CONCLUSIONS

In this paper, a seven stage progressive tool for automobile engine starter key is designed and modeled. Strip layout for maximum stock strip utilization is developed. Stock strip utilization achieved is 74.1 %. Three punches i.e. piloting punch, profile punch and blanking punch and the die elements are designed and assembled in CATIA V5. Further, finite element analysis for maximum Von-Mises stress and deformation is carried out on the punches using ANSYS 14.0 for validating the design. The results obtained are well within the limit. The press capacity obtained is of 81 T.

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A Study of Corrugated GFRP Composite subjected to Transverse loading

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Abstract— **Now a days, glass fiber reinforced polymer(GFRP) composites became the best alternative to replace the traditional materials due to its superlative properties such as high stiffness to weight ratio, strength to weight ratio & corrosion resistance etc., the present work focuses replacement ship container wall of corrugated structure with GFRP composites. These structures are tested for flexural and bending strength. General purpose (GP) polyester resin is used as matrix and glass fabrics of orientations 0&45 are used as reinforcement to make the two ply corrugated composite& hand lay-up technique is employed.**

Index Terms : GFRP composites, GP Resin, Corrugated Structure, Glass Fabric.

I. Introduction

Though wide variety of traditional metal materials and alloys are available for different applications, still composites are competing due to its outstanding properties strength to weight ratio, stiffness to weight ratio, corrosion resistance, low density, electrical resistance etc., glass fiber reinforced polymer composites have huge applications in electronics, structural, aviation, navy and automobile fields[1].in composites, reinforcement (fiber or fabric)is major load carriers and where as matrix holds the fibers together, protects from environment effects and transfers the load to the reinforcement. the present investigation is carried out on corrugated composites for structural applications.

Jin Zhang et al.,[2] studied for bending strength, stiffness and energy absorption of corrugated sandwich composite structure for energy absorption in transportation vehicles & they have considered the design parameters to be selection of fiber type, corrugation angle and core-sheet thickness, The results revealed that Increasing the corrugation angle and the core sheet thickness improved the specific bending strength of the sandwich structure, while increasing the bond length led to a reduction in the specific bending strength.

Ziad K et al.,[3] studied Optimum Design of Structural Fiber Composite Sandwich Panel for Flooring Applications based on cost. they have followed Finite Element (FE) and Genetic Algorithm (GA) method to analyze the composite sandwich panel for civil engineering applications. Not only the type of matrix and fabric but also fabric orientation is going to effect the performance of corrugated structures [4,5].

S. C. Mohanty [6] modeled multi-layered symmetric sandwich beam and analyzed using numerical methods and finally suggested that optimization can be done using finite element method for vibration analysis.

ES Kocaman et al.,[7] studied foam core sandwich composites failure modes with the help of Fiber Bragg Grating sensors. They have fabricated using vacuum infusion process and then, composites are subjected to a static and a cyclic loading under the three-point bending. They have found depending up on damage modes, different responses of the Fiber Bragg Grating sensor.

S. Heimbs et al.,[8] followed autoclave technique to fabricate the Folded Structures for the aero space application. They have tested the sandwich structure with a folded core made of carbon fiber-reinforced plastic for compressive strength, shear strength and impact strength based on numerical methods and experimentation. high stiffness and strength values leading to a very localized failure under impact loads and the delamination propagation in the face laminate is limited by the adjacent core cell connections are observed.

Bartolozzi, G et al.,[9] considered sandwich corrugated layers to be orthotropic homogeneous layers and carried out finite element analysis and found experimental and NM results are comparable.

Carlson, L.A et al.,[10] studied deformations and failure modes like global buckling, wrinkling local instabilities, and face/core debonding of sandwich panels subjected different types of loads and given analytical solutions to the corrugated structure. Guru Saiprasad et al.,[11] used simple hand lay-up technique to find the mechanical compressive strength of hybridized sandwich coupons with different combination of reinforcements namely glass fabric, jute fabric and Kevlar fabric by keeping the corrugated angle to constant 45^{0}.results revealed that hybridization can be successfully implemented for better mechanical performance and cost.

The present investigation is carried out to know whether the orientation of reinforcement is effective or not for the corrugated glass fiber reinforced polyester composite.

II. Materials And Methods

13mill glass fabric (400gsm) of orientations 0&45 and general purpose resin is purchased from Allied agencies, tarbund Hyderabad. mould is required for giving shape to the resin/ fiber combination. A Wooden mould is prepared by using wood router machine as shown in fig - 1. The plain shaped mould is used at the time of assembly i.e., joining of the flat composite with the corrugated composite using the matrix. Cut the E-glass fiber as per the mould dimension. The fiber is marked using scale and then it is cut with a scissor as shown in fig-2.

Fig-1. Wood Mould

Fig-2. Cutting of Glass Fabric

The matrix consists of resin (Polyester resin), catalyst and accelerator. The resin is mixed with the catalyst and accelerator in the ratio given in the table-1.

TABLE-I.
MIXING RATIO OF MATRIX

S. No	Material Name	Volume used	Percentage
1	GP Polyester resin	1 liter	96.153%
2	Catalyst	0.02 liter	1.923%
3	Accelerator	0.02 liter	0.923%

The simplest and oldest technique, used to fabricate the composite laminate is Hand lay-up. In this process successive layers of matrix and reinforcement are manually applied to an open mould for the fabrication of composite laminates. This process is used in making both corrugated and plain composite. The mould releasing agent (i.e. silicon spray) is applied on to the mould surface. Then after a few minutes the matrix over the mould is applied and place the fiber and press it with hands using gloves. Rollers are also used for avoiding air bubbles then again apply the matrix and follow the same. Leave the specimen for about 2 hours to dry up. Then, remove the specimen from the mould.

Assembly is the process of joining all component together in order to get the required laminates. Perfect assembly provides strong joining of corrugated shape and plain shaped composite sheets. In perfect assembly, there is no gap at any section of sheets where it is joined. Thus, making the assembly is very strong and reliable. The matrix is applied on the surface of flat shaped specimen and also corrugated shaped specimen. Then the corrugated shaped specimen is placed over the flat shaped specimen, where both the specimen has the same fiber. The complete procedure is shown in figures from 3-5.

Fig-3 Removing the bubbles with a roller

Fig-4 Plain Composite

Fig-5 Removing the Composite from mould

Heavy load is kept on the joined specimen to make the assembly very strong. Finally, load is removed at about 2 hrs and the required assembly is achieved.

TABLE: II
ORIENTATIONS AND NUMBER OF LAYERS

S. No	Fiber orientation (in degrees)	No. of layers of fiber	Thickness in mm
1	0,0	2	2
2	0,45	2	2
3	0,-45	2	2
4	45,45	2	2
5	45,-45	2	2

3-point bend test is carried out to find the flexural strength of the composite at Jyothi spectro analysis laboratories located in balanagar, Hyderabad with universal tensile testing machine. a ball drop impact test setup is made with

maximum ball bounce to be 160cm as shown in figures from 6-7, to know the impact strength of the corrugated composite.

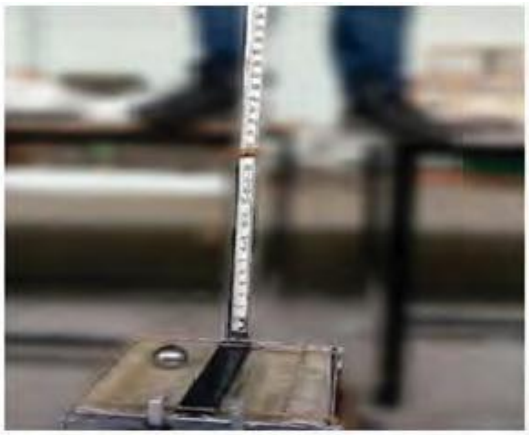

Fig -6 Impact load setup

Fig-7 Bend test setup

III. Results And Discussion

After preparing the specimens, they are tested to know the maximum amount of transverse load and amount of energy it is absorbed. the maximum gradual transverse load to deflection are shown in figures 8-12 for the GFRP composite corrugated beam. The load increases steadily with the displacement up to the highest peak load. There after the wall of core begins to buckle and the load has abruptly decreased. Global failure is observed during bend test before the delamination of layers

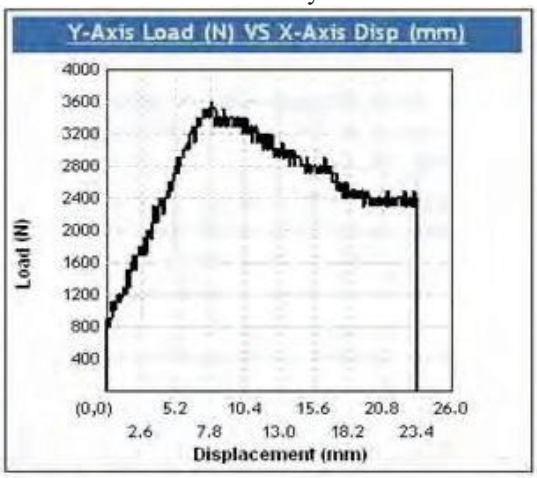

Fig-8 Load vs Defelction graph of (0, -45)

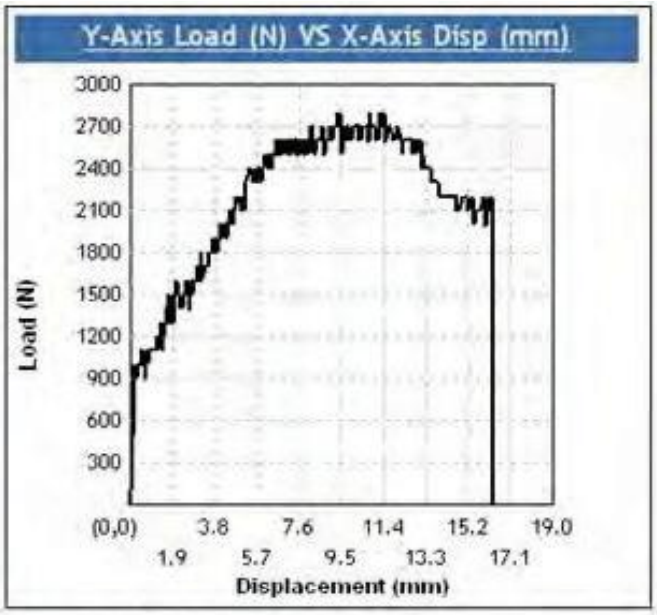

Fig-9 Load vs Defelction graph of (+45, +45)

Ball drop Impact test is conducted to calculate the following and results are tabulated in table III and comparison has made in figures 13-16:

Absorbed energy (AE)

Co-efficient of restitution (COR)

Brinell hardness (HB)

Thus the specimen that absorbs the highest amount of energy is the best among all the specimens.

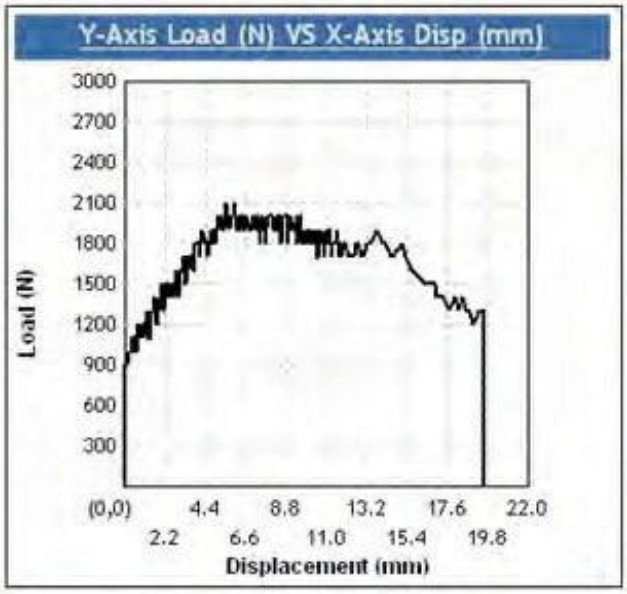

Fig-10 Load vs Defelction graph of (0, +45)

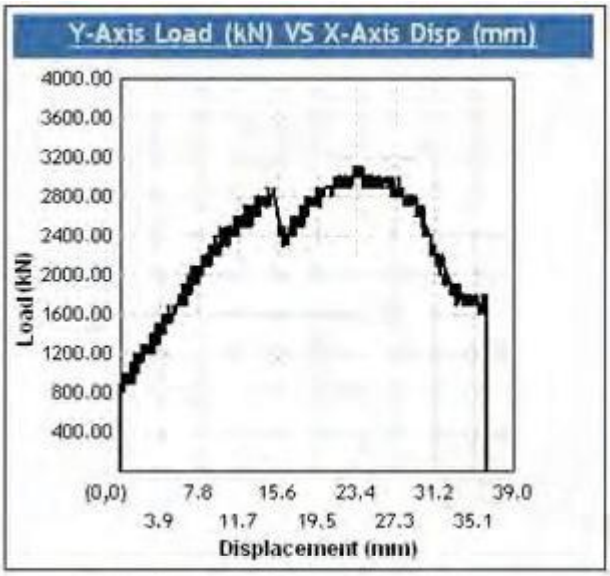

Fig-11 Load vs Defelction graph of (0, 0)

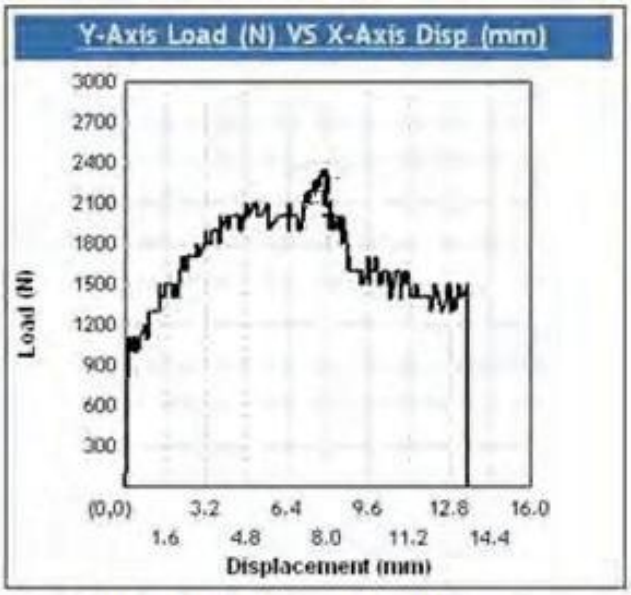

Fig-12 Load vs Defelction graph of (+45, -45)

Formula 1: Absorbed energy(AE) = Total energy–Potential energy

$$AE = \tfrac{1}{2}mv^2 \quad - \quad mgh$$

m= Mass of the ball in Kg.
v= velocity of specimen in m/s.
g=gravitational constant in m/s^2
h=height of the ball in mm.

Formula 2: Co-efficient of restitution(COR)

COR = coefficient of restitution $c = \sqrt{\frac{h}{H}}$
h = bounce height
H = drop height
D = Diameter of the ball
d = Diameter of the indentation.

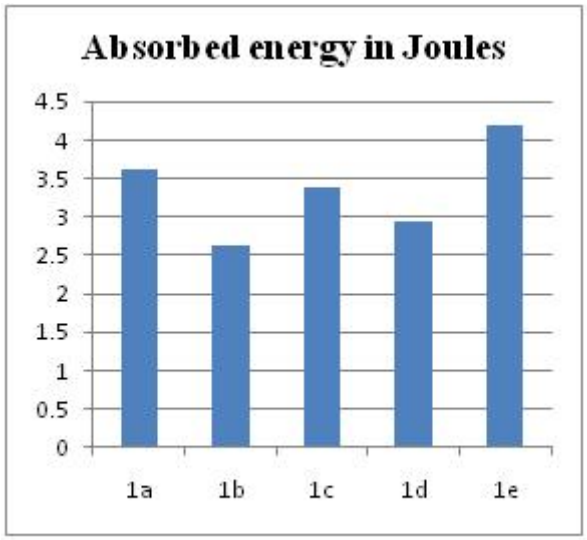

Fig-13 the amount of energy absorbed in joules

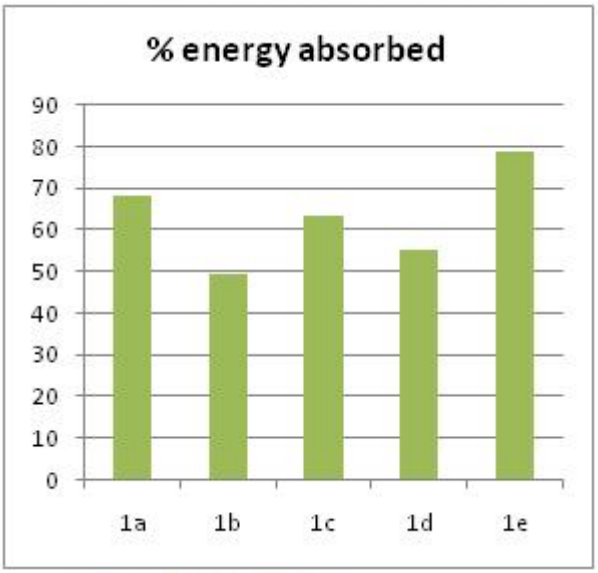

Fig-14 % Energy Absorbed

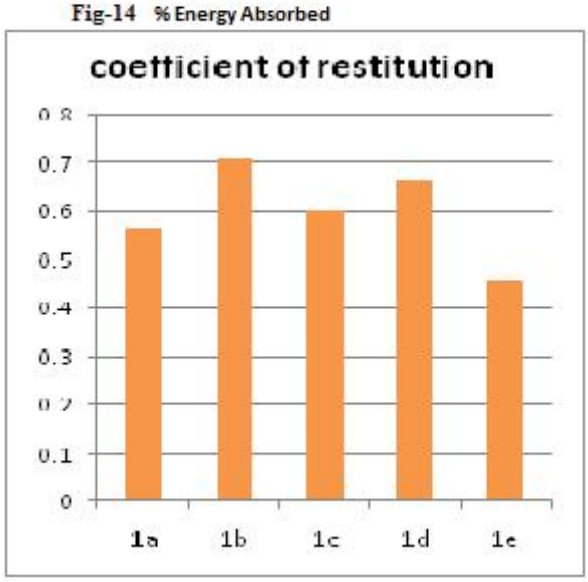

Fig- 15 Coefficient of Restitution

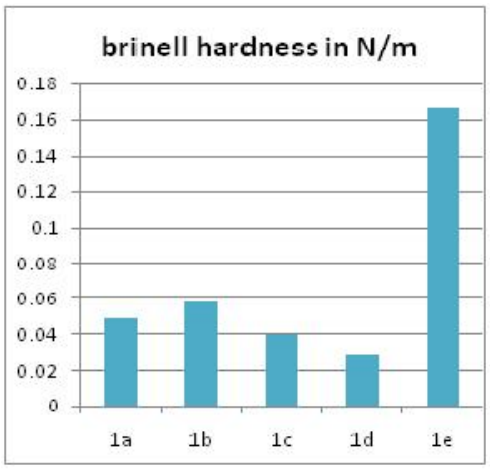

Fig- 16 Brinell Hardness in N/m

TABLE-III
HARDNESS AND ABSORBED ENERGY FOR SPECIMENS

S.No	Composite Sample	Fiber Orientation	A.E. in (kgm^2/s^2)	% A.E	COR	Brinell Hardness in N/m
1	1a	0, -45	3.616	68.149	0.565	0.049
2	1b	0, +45	2.637	49.69	0.709	0.058
3	1c	+45, +45	3.379	63.68	0.602	0.039
4	1d	0, 0	2.949	55.57	0.666	0.029
5	1e	+45, -45	4.181	78.79	0.46	0.167

IV. CONCLUSIONS

The GFRP composite corrugated beams fabricated using hand lay-up and compression moulding technique using different orientation of glass fabric. Later all the fabricated specimens are tested for 3 point bending test and impact test for finding the load resistance capacity of different orientations .The (0,-45) orientation has the best bending strength obtained during three point bending test The (+45,-45) oriented specimen has highest energy absorption capacity which is obtained during impact test. The specimen of orientation (0,+45) has highest coefficient of restitution and specimen of orientation (+45,-45) high brinell hardness value. The Results showed that fabric orientations can affect the performance of composite corrugated structures.

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Validation of Diagonal Power Routing Approach in Very Large Scale Integration Design for Better Prospects over Orthogonal Routing at Nanometre Era

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Abstract: This paper focuses on top metal layer routing in very large scale integration design in nanometre era, to show that the diagonal routing approach has improvised prospects than the existing orthogonal power routing approach. In this paper, the proposed diagonalised routing and orthogonal routing for an operational amplifier, and both routing techniques are incorporated with HVT swapping. In addition to this diagonal routing implementation, some parameters get affected, i.e., power, delay and length etc. This approach is meant for specific limitation of application areas in very large scale integration design.

Index terms: Diagonal routing, orthogonal routing, operational amplifier, high voltage threshold (HVT)

I. INTRODUCTION

The overall capacity of a chip depends on less glitch, IR drop reduction, compact Area and reduction in delay of the circuit. One approach to reduce the effect of these parameters is by using a top metal layer arrangement. In this approach, metal layer values and design aspects are optimum. Both Manhattan and non Manhattan interconnect routing architectures are implemented with the ACO algorithm [1]. When SSN is produced during the transmission of the signal from one node to other nodes and due to return path currents, led to malfunctioning and degraded performance of the the power distribution in VLSI circuits and it became a challenging issue due to the severe switching noise on the power distribution network. Hence, estimation of the worst case switching noise is essential to ensure the proper functionality of the VLSI circuits [3]. For the varying rise and fall times intended to reduce the performance at high frequency of operation [4, 5]. The IR drop power routing at physical layout is more important to simulate expected outputs in the sense of reducing dreadful conditions of the system. In many cases, researchers investigate to minimize the power dissipation / IR drop, propagation delay and switching activities, etc.. In this conflict, they have mentioned several techniques to identify and investigate the problems. By using several techniques to reduce the cost of fabrication of chip and prediction of several techniques and propose a new technique to implement, for reducing the dynamic IR drop and switching noise during the transmission of the signal [6,7]. In this paper the task to reduce the IR drop using a new technique i.e. diagonal power routing with HVT swapping method is implemented. It is well known that the performance of the chip is significantly affected by power routing technique.

The Maxwell equations relate to E and H fields, that are proportional to the antenna affect in transmission lines of circuit boards and metal layers. Switching activities also affect the various parameters of the device, which is also led to degrading the performance of the device. The inductive effect is more important at high frequency operation [8]. At high frequency of operation, power leakage is reduced by inserting dye caps for static power, whereas in dynamic power analysis the IR drop should vary with R, L & C affects. The present paper analyses the IR Drop with the diagonalized and an orthogonal power grid of dynamic analysis for op-amp. In this paper, mainly focussing the mathematical and simulation of diagonal routing and orthogonal routing top layer routing and comparison of them from obtaining the results to improve the IR drop reduction, reduce the effects of delay, noise and area. This work results will show that the proposed method of diagonal routing is improved in some aspects compared to the existing methods for certain limits, which is implemented to op-amp for validation.

The interconnection delay of the IC is increased and greater than the delay due to MOSFETS [13]. However, these design approaches has increased the speed of the MOSFET to increase the lifetime of the systems few technologies [14]. The increase in the speed of the MOSFET devices has primarily been enabled due to a reduction in their sizes. Metal area of the device reduced is proportional to cross sectional area of devices IC [15]. In scrolling down technology the complexity of the system density with decreases interconnect delay at high frequency of operation [16]. In this work the simulation is done by using diagonal power routing for various blocks and analysis is done over orthogonal routing for a typical 9-metal layer sub NM CMOS technology using Redhawk tools [26]. The methodology applied to validate this approach for all scaling

down technologies in VLSI. In this work it is mainly concentrated on various parameters affecting and the performance of the device with functionalities like antenna effect on metal interconnects [17,18] and the effect of the electromagnetic radiation from the onchipantennas on the MOSFET devices [19], Antenna gain decreases at low frequency range and increases at high and mid frequency ranges in metal interconnects due to the parallel orientation antenna. With the growing technology the devices are very compact and more sensitive to power and delay and area. This has led to many challenges to the designers for interconnection layers in the network.

II. Theoretical Formation

2.1 Orthogonal and diagonal power routing

The modern VLSI has multiple paths at different layers in horizontal and vertical layers. Wires on the same layer cannot cross each other based on the connection establishment. In multiple layers the distance between the components is very less, thus reducing the wire length. To reduce the wire length, cost and power consumption, the wires are routed on the upper layers in a 2D-plane.

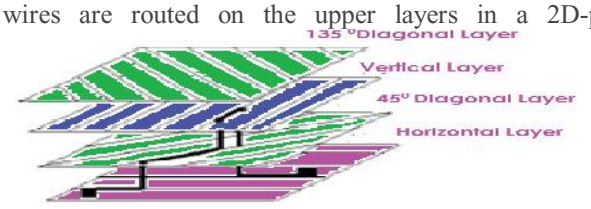


Figure 1. An example of HVHV- Horizontal Vertical Horizontal Vertical layer

In the figure1 shown above to provide connection between layers, horizontal layers allow only horizontal wire route and vertical layers allows only vertical wire route.

$$C = 2\,X\,10^{-6}(\text{wire} - \text{Length}) + 2.3\,X\,10^{-13}(\text{No. of Vias}) \quad \text{m} \qquad (1)$$

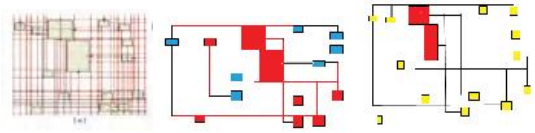


Figure 2.a Figure 2.b Figure 2.c

Figure 2. Three stage routing: (a) The orthogonal visibility graph, (b) The optimal connector routes, (c) The final routes after centering and nudging. Arrows indicate routing direction for connectors.

Right = { E→S,S→W,W→N N→E }-------(2)

Left = { E→N,S→E,W→S, N→W }----------(3)

Reverse= { E→W,S→N,W→E, N→S }-------(4)

in these equations, the distance between two points in orthogonal routing $||(R1, R2)||_1 = |p_1 - p_2| + |q_1 - q_2|$ has been applied to measure the shortest path between any two points R1 = (p1; q1) and R2 = (p2; q2). In this calculation take into the 4 cardinal directions: N, S, E, W. It is assumed that the functions right, left, and reverse defined by the mappings.

The directions of point R2 = (p2; q2) from R1 = (p1; q1) are defined as directions $(R_1, R_2) = \{N \mid q_2 > q_1\} \cup \{E \mid p_2 > p_1\} \cup \{S \mid q_2 < q_1\} \cup \{W \mid p_2 < p_1\}$ Note dirns(R1,R2) ={ D} means R2 is on the line in direction D drawn from R1.e in direction *D* drawn from R1.

2.2. Visibility graph of orthogonal routing

The orthogonal visibility graph is used to minimize the penalty function. Let me (p, q) be the set of intersecting points in the diagram i.e, the connecting points and corners of the bounding box of each object. Let P1 and Q1 be the set of p and q coordinates respectively in I. The orthogonal visibility graph VG= (R, G) is made up of nodes. R P, Q1 s.t. p, q∈ R. If q s.t (p, q1) ∈ I think there is no intervening object between (p, q) and (p, q1). There is an edge e∈ E between each nearest neighbourhoods on all the sides and faces without any intervening object in the original diagram.

Observations: This simply takes the route R and "shrink" each segment on the route onto a path in the visibility graph to give R'. By construction R' is no longer than R and has no additional bends.

The orthogonal visibility graph can be constructed using the following algorithm. It has three steps:

1. Generate the interesting horizontal segments

$$H_I = \left\{ \begin{array}{c} ((p,q),(p',q)) \mid (p,q) \in I \;\; s.t. \;\; p \;\; \leq p1 \\ \\ \text{and there is no intervening object} \\ \text{between } (p,q) \text{ and } (p',q) \end{array} \right\}$$

2. Generate the interesting vertical segemnts

$$V_I = \left\{ \begin{array}{c} ((p,q),(p,q1)) \mid (p,q),(p,q1) \in I \;\; s.t. \;\; q \leq q1 \\ \text{and there is no intervening object between} \\ (p,q \text{ and } (x,y')) \end{array} \right\}$$

3. Compute the orthogonal visibility graph by intersecting all pairs of segments from H_I and V_I. The orthogonal visibility graph can be constructed with n objects using the algorithm with time O (n^2). The interesting horizontal segments can be generated in O (n log n) time where n is the number of objects in the diagram by using a variant of the line- sweep algorithm [3,4]. This uses a vertical sweep through the objects, keeping a horizontal "scan line" list of open objects with each node having reference to its closest neighbors. Interesting, horizontal segments are generated, when an object is opened, closed 'or' connection point is reached. Where as vertical segments can generated in O (n log n) time using horizontalsweep. The last step takes O (n^2) time since O (n) horizontal and vertical segments.

***Final placement of orthogonal routing**:*

Finally the layout is to find the exact coordinate points of orthogonal connector segments. This nudges connector route and "alleys" to make shortest path in a given network. The horizontal pass works as explained here

and the vertical pass is symmetric, which provides the separate passes

1.Determine a desired horizontal position for all non-end segments in the connector. For the middle segment in an "S" or "Z" bend, this is the middle of the "alley" that the segment is in. For the middle segment in an "⊏" or "⊏"bend, this is the vertex of the object that the segment bends around.

2. Provide a set of horizontal separation constraints to ensure that segments maintain their current relative horizontal ordering with each other and with the other objects in the diagram. The constraints designed led to enforce non-overlap.

3. Project the desired values on to the separation constraints to find the horizontal position of the segments using the approximate projection algorithm satisfy VPSC from [24,25]. The constraints and desired positions can be generated algorithm [3] in O ((n+s) lag (n+s)) time where n is the number of diagram objects and so the total number of vertical connector segments. The approximate projection algorithm has O (⟦ (s + n) ⟧ ^2) worst-case complexity, but in practice O ((s + n) log (s + n)) complexity [5].

2.3. Diagonal routing

A diagonal routing is a technique that uses diagonal wiring which is partially applied to critical nets.To minimize the enhancements needed for the existing CAD system the usage of diagonal wires is limited (Fig.3).

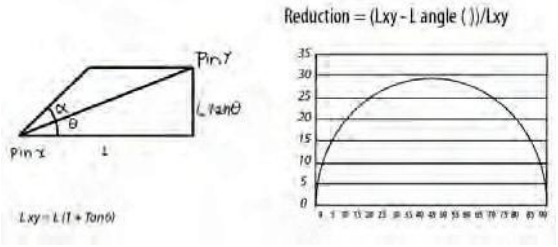


Figure 3. Theoretical Effect of length estimation

The figure 4 represents the theoretical estimation of a given block. In the actual design, the two lengths are compared for 6000 long distance nets. In diagonal routing the net length is reduced by about 12% on average.

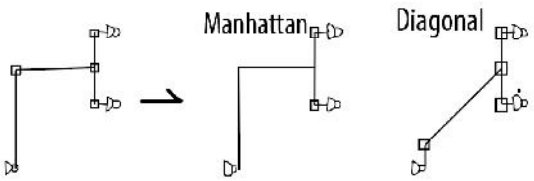


Figure 4. Effect estimation of actual

*The effect of delay estimation:*When a net length is about 1500, the improvement of delay is about 7 pico-seconds.When a diagonal routing is applied to a longer net,then the reduction of delay improved .

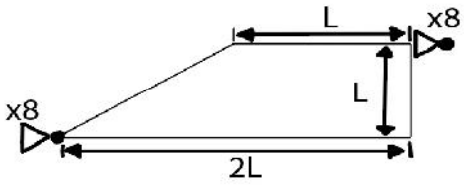


Figure 5. Effect estimation of delay

The diagonal routing can reduce the net length by about 20% in this case (fig. 6).In this paper we are using diagonal routing. The details of Manhattan routing are as follows.

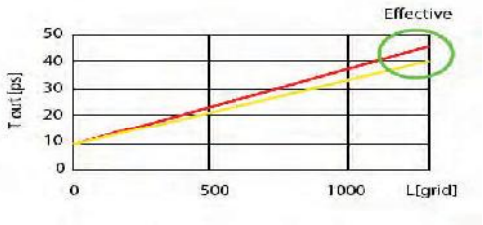


Figure 6 Graphical representations of the diagonal and Manhattan routing

Manhattan routing

The Manhattan routing is a special type of connection lines in graphical modeling tools on the other hand an algorithm for computing networks in VLSI design for integrated circuits. In graphical modeling tools are called with Manhattan routing the layout of connections in which only horizontal and vertical lines can be used with rectangular branches / turns and fixed distances from one another. It is usually not relevant whether crossing lines or may overlap or not. In general, a Manhattan Routing a grid or grid with fixed intervals based on the line extension. In Manhattan routing 45 and 135 degree layers are assigned to upper layers, having smaller wire resistance. With conventional Manhattan routing, the channels are left unused to route regular nets.

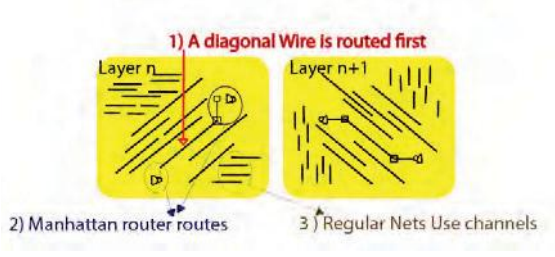


Figure 7: Layer representation of diagonal and Manhattan router Capacitance extraction of the Manhattan routing and diagonal routing

Additional capacitance table, Gapbetween Manhattan wires: 1 gird*N

Gap between Diagonal wires: 1/SQRT(2) grid*N

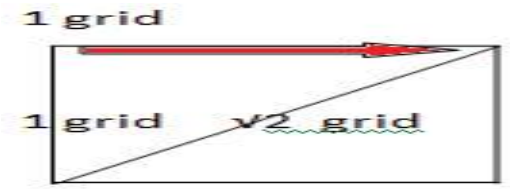
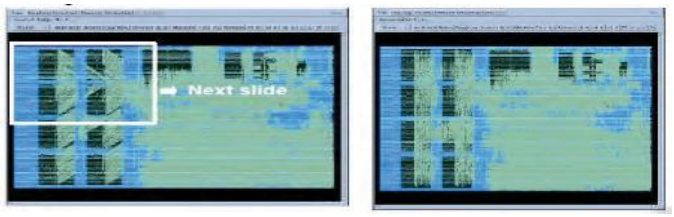


Figure 8. Capacitance table Diagonal wires:

Diagonal wiring directions in integrated circuits are simulated with wires deposed in purely Manhattan directions (e.g., horizontal and vertical directions). A metal layer of an integrated circuit contains at least two pairs of conductors to interconnect one or more points on the integrated circuit.



a. Diagonal b. Manhattan

Figure 9 (a) Diagonal routing and (b) Manhattan routing

III .APPLICATION

Op-amp design using orthogonal routing and Diagonal routing schemes in the nanometre era for validation purpose.

For the above points validation done for op amp using the orthogonal and Diagonal routing approaches, the schematic of op-amp using numberof **nmos** and **pmos** transistors combinations.

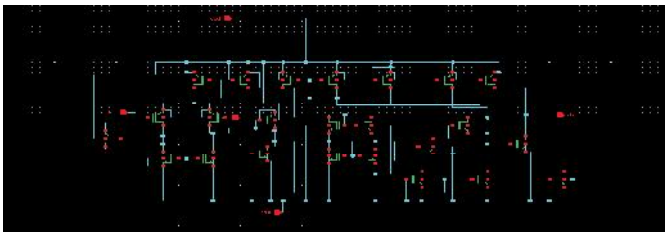


Figure 10. schematic diagram of op-amp

This is the op-amp schematic diagram. It has total 24 transistors(11 PMOS +13NMOS)

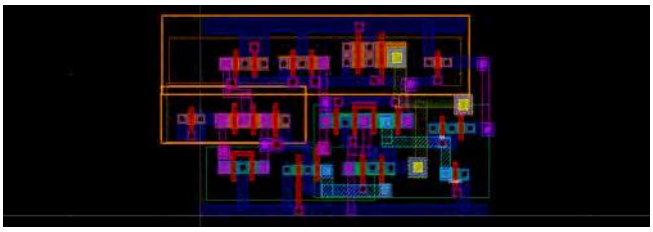


Figure 11. Schematic orthogonal Lay out of op-Amp

The complete orthogonal layout structure for the op-amp is given above. This layout is designed in the conventional orthogonal scheme in 180nm & 90 nm Technology.

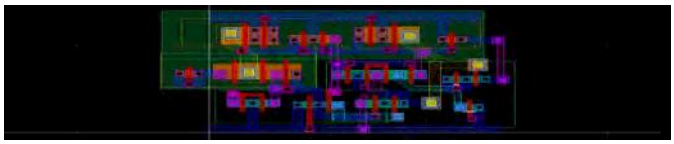


Figure 12. Schematic Diagonal Layout diagram of op-amp

The above image is for the diagonal layout scheme for the op-amp. We can observe some paths are routed in orthogonal manner.

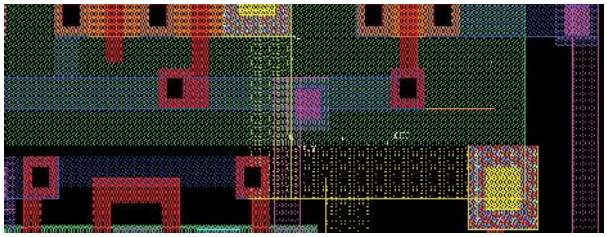


Figure 13.Path length of first path length of orthogonal routing

From above Figure, the path length of the first path is given. Orthogonal routing will take 0.9450+1.0350 = 1.980 micro meters

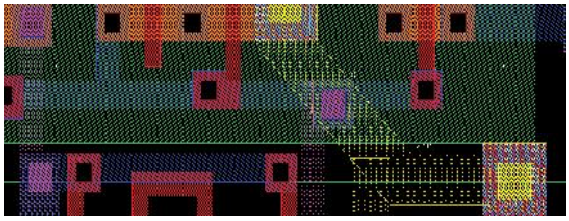


Figure 14.Path length of first path length of diagonal routing

If we observe the same path in the diagonal the length is given bellow. for path 1 - diagonal will take 1.46 micro meters. The difference between the lengths of the paths is 1.980 µm -1.46 µm = 0.52 µm. So from this we can observe that the path length is reduced to 0.52 µm lesser than actual path length when we are using the orthogonal routing.

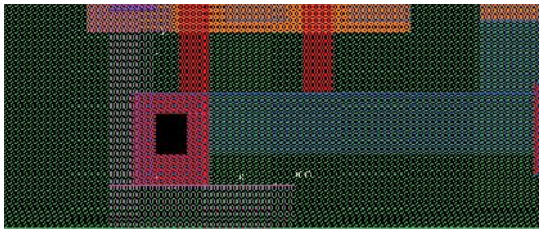


Figure 15.Path length of second path length of orthogonal routing

The second path is taken into consideration and length for orthogonal routing is 1.556 µm .

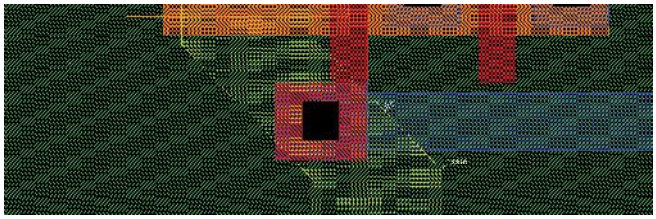


Figure 16.Path length of second path length of diagonal routing

For the diagonal routing the path length is 0.8810 micro meters, The difference between two paths is 1.556-0.88810 = 0.675 µm and this is reduced.

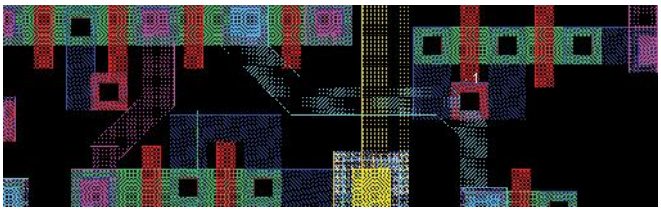


Figure 17.Path length of rest of path length of Diagonal routing for validation

The remaining paths used in diagonal outing. Pink colour path routing and the blue colour path routing.

Figure 18.Simulation output of diagonal routing power calculation

This is power calculation for the orthogonal routing extracted view of the layout. The power dissipation for this routing is 409.5E-3. By converting the floating point into power the power consumption is 409.5 micro watts(µw).

Figure 19 Simulation output of orthogonal routing power calculation

The power for diagonal routing is calculated for the extracted view of the layout. The power consumption is given as 406.3E-6 by converting it into watts we get 406 micro watts(µW). So from this we can observe that the power dissipation is reduced by 3 micro watts(µW). 409.5 – 406.0 = 3.5 µW .

The results describes that the power dissipation is reduced to 3.5 micro watts for a modelling of op-amp .which relates to validated proposal approach in the view of power dissipation reduction and it effects on the other parameters also .

This is the delay consumed by the orthogonal layout the delay value is 509E-9. so this indicates it is taking 5ns delay to produce output

Figure 20.Simulation output of orthogonal routing Delay calculation

The above table shows that the delay calculation for the diagonal is 419.0E-6. It gives the delay of 4.19ns. So from these two values we can get that the circuit is given less delay than orthogonal routing.

The delay is reduced by 1ns approximately. 5.2 – 4.19 = 1.01ns. From the above results describes that diagonal routing delay is low compared to the orthogonal routing for a proposed model of Op-Amp in a VLSI design.

Figure 21.Simulation output of Diagonal routing power calculation

IV.RESULTS & DISCUSSIONS

TABLE I.
VARIOUS PARAMETERS EFFECTED IN 180 NM TECHNOLOGY BY USING DIAGONAL AND ORTHOGONAL ROUTING TO CMOS BASED OP-AMP

Effecting Parameters	Orthogonal routing used in op-amp	Diagonal routing in op-amp	Difference B/w Diagonal & orthogonal	Remarks
Path Length	a)1.556 µM b)1.98 µM	0.8881 µM 1.46 µM	0.6679 µM 0.52 µM	Length reduced in diagonal routing
Delay	5.20 nS	4.19 ns	1.01 nS	Delay reduced
Power dissipation	409.5 µW	406.3 µW	3.2 µW	Power dissipation is better in diagonal

TABLE 2
.VARIOUS PARAMETERS AFFECTED IN 90 NM TECHNOLOGY BY USING DIAGONAL AND ORTHOGONAL ROUTING TO OP-AMP

Effecting Parameters	Orthogonal routing used in op-amp	Diagonal routing in op-amp	Difference B/w Diagonal & orthogonal	Remarks
Path Length	1.236 x10 -6µM	0.687 µM	0.549 µM	Length reduced in diagonal routing
Delay	4.50 x 10nS	3.63 ns	0.87 nS	Delay reduced in diagonal routing
Power dissipation	345.2 µW	337 µW	8.2 µW	Power dissipation is better in diagonal

From the above results obtained our approach is justified that to applicable for specific conditional applications for top layer routing in VLSI design Here, the proposed approach is justified that there is no cross over problems, because the approach is meant for only top layer in design so what so ever the routing in orthogonal approach crossover problems the same thing is replica in rest of metal layers ,but overall performance of the systems is better in some specific applications in VLSI design by this proposed approach, since the results confined that to validate with existing approaches.

*1.Effects in length:*In the diagonal routing, net length reduction reduces the net length by 42% on an average. This reduction exceeds the theoretical maximum value 32.4%. This is due to the total detour of the net with diagonal routing is smaller than orthogonal routing.

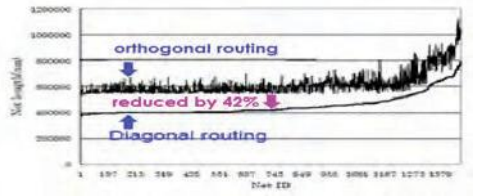


Figure 22: Effects of length

3. *Effects on delay:* Path delay reduction: The path delay is improved by up to about 1.01nano seconds per night on a path when diagonal routing applies to critical paths. This improvement is more than the delay of a gate with no load. The average improvement is about 1nano-second.

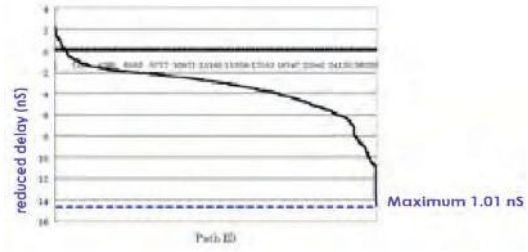


Figure 23: Effects on delay

c. Effects of noise

Noise reduction Coupling capacitance can cause crosstalk noise which is less when diagonal routing is applied. This is due to the associated reduction of net length. Finally, the overall crosstalk is reduced by about 18%.

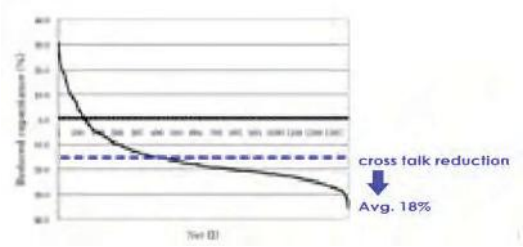


Figure 24: Effects of noise

A diagonal routing function is examined and able to reduce the net length by 42% per net on average, and path delay by up to 1.01nanoseconds.

D. Power dissipation reduction:

Power dissipation reduction is 3.5micro watts by using diagonal routing over orthogonal routing . Finally it is foud that reduction of power dissipation, is better than the orthogonal routing approach.

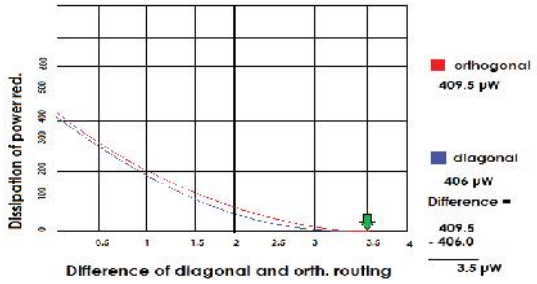


Fig 25.Power dissipation of diagonal and orthogonal approaches

This work is done by using the technology of 180nm and 90 nm in diagonalized and orthogonal routing approaches for design of op – amp uses voltage storm tools. These approaches are compatible with all scaling down technologies for specific application in VLSI design.

V. Conclusions

In this paper, it is presented as the diagonal power routing and orthogonal power routing applied in VLSI design and which has been validated for op-amp device. The results of the proposed approach shows better prospects when compared to the existing method of orthogonal routings. In this approach, there is no cross over problems, because diagonal routing is applied to the only top metal layer and the rest of lower metal layers are arranged same as existing approaches, from this methodology, this is allowing specific limits to be applied this technique in VLSI physical design. In future some fine tuning is needed for more reduction of power dissipation, area, delay for its applications in nanometer era and this approach is compatible with all scaling down technologies in VLSI design.

The authors wish to thank to Mr. Mastanaiah and Srikanth for their supporting to do this work.

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Testing and Validating of Water Quality Using Raspberry Pi2 Model B With the help of IOT.

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Abstract: **Water being hypothetical solvent, varies from region to region. Now a days water pollution becomes a universal concern for not acquiring green globalization, and also it should meet the Environmental Protection Agency (E.P.A) standards. The typical method of challenging fluoride, turbidity, and pH is done by collecting water samples manually, these samples are sent to the laboratory for quality check. It is time consuming process. The above method is unable to reach water quality testing standards. The run of the mill method comprises of fluoride sensor, turbidity sensor and pH sensor for water grade testing. The Raspberry Pi2 model B gets the data from these three sensors and it will be sent to the server through internet via the communication modules like GPRS/UMTS/CDMA. It can detect various testing parameters pertaining to the purity of water and it implements the required task. The existing system will be suitable for a particular area and it helps in avoiding health hazarding conditions. In the proposed method a simple system for testing and validating the water quality check is implemented using Raspberry Pi2 model B. It has been developed in order to cover more water storage areas with the help of IOT technique.**

Index Terms: **Raspberry Pi2 Model *B,* Fluoride sensor, Turbidity sensor, pH sensor, IOT and water quality.**

I. Introduction

Presently, contamination of water is a significant global problem, which requires continuous assessment and testing. It has been suggested that contamination of water is one of the leading world wide problems for causing deaths and diseases. About 80% of water in the cities of India is marked below the standard purity levels. Regular testing and validating of the water quality parameters are conductivity, pH, turbidity, fluoride,nitrate, nitrite,phosphate, various metal ions and so on. In the run-of-the-mill method most of the water samples are collected manually and sent to thelaboratory. It is a very tedious and time consuming process. Keeping in mind the end goal to wipe out such issues, another strategy for testing and approving of water quality check can be actualized by utilizing three sensors and Raspberry Pi2 model B.

II. Problem definition

As an example, Hyderabad is taken into consideration, where the environmental regulations require the testing and approving of Manjira and Musi river water quality.The current system from the Manjira and Musi water basin travels to 28 locations on to the states of Maharashtra, Karnataka and Telangana. At each location a manual sensor sample for conductivity, pH, turbidity, fluoride content and bacteria are recorded by hand. Manual Testing occurs once a week during the months from May to October. The process of travelling and collecting data takes more than two hours to complete. The water collected for sampling is sent to the laboratory. There is a lot of time delay between these cycles and there is a chance of recording data incorrectly. After completion, the manually recorded data is given to the master as an input to the system. As a result of the manual process, there is no sufficient time to investigate water quality.

Disadvantages of an existing system:

1.High cost.
2.More Man power

III. Proposed Methodology

This method explains the complete structure of the proposed system where it presents the detailed explanation of each and every block. The overall diagram is shown in figure1. The following Block diagram consists of three sensors such as turbidity, fluoride, and pH. The collected data from the sensors is given as input to the Raspberry Pi2 Model B circuit board by using Python Programming. The outputs obtained from the Raspberry Pi 2 are stored in the cloud data base and it can be sent to the server with the help of IOT. By this way, we can eliminate certain issues such as time delay, and inaccuracy etc.

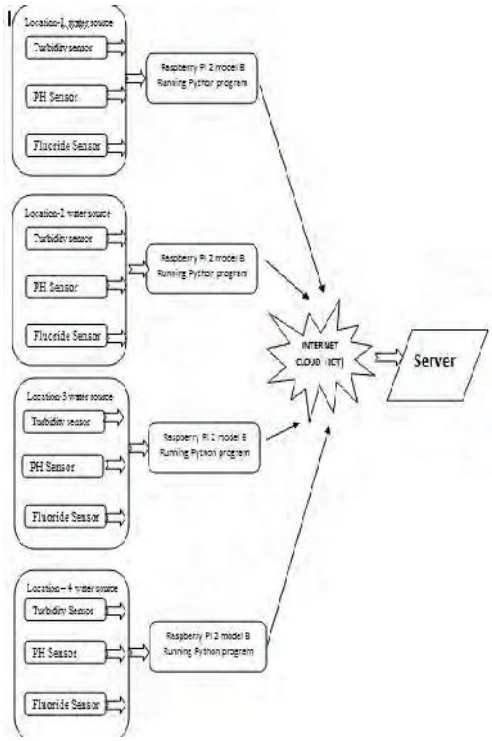

Figure.1. Block Diagram Of Water Quality Monitoring at Different locations

IV. HARDWARE DESCRIPTION

The following are the major components used in the proposed system. Brief explanation of each component is given as follows.

A.Raspberry Pi2 Model B:

Raspberry Pi2 Model B is shown in figure2. It is the second era Raspberry Pi. It has supplanted the first Raspberry Pi1 Model B+ and it has the accompanying progressed features such as 900MHz quad center ARM Cortex_A7 CPU and 1GB RAM. It supports Microsoft Windows10.

Figure.2. Raspberry pi 2 Model B

B.GPIO Pins:

One of the robust features of Raspberry Pi families is the row of GPIO pins which are located at the top brim of the board. These pins are programmed to interact Raspberry Pi2 to the external world. Inputs should be given from a sensor or a signal from another computer or device.

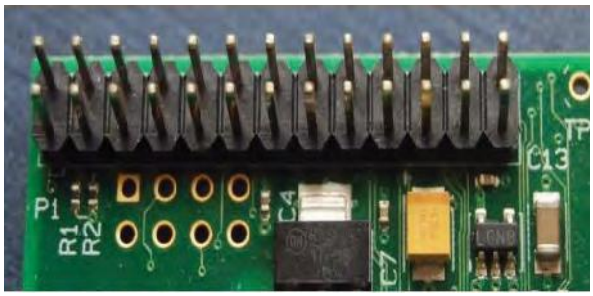

Figure.3. GPIO PINS

C. Turbidity Sensor:

The Turbidity Sensor measures the turbidity of crisp water or seawater in terms of NTU (Nephelometric Turbidity Units). The DTS-12 is a turbidity and temperature sensor which provides accurate measurement. Due to Nephelometry's, accuracy and appropriateness over a wide particle size and turbidity range, it's the favored technique for measuring turbidity by the EPA. The DTS-12 is easy to arrange and utilize. It offers a standard (Serial Digital Interface) SDI-12 output for communicating with data measuring instruments.

Figure.4. Turbidity Sensor

D. pH Sensor:

Being one of the water quality measures 'pH' indicates how much water is acidic or alkaline. It is controlled by the measure of free hydrogen and hydroxyl particles in the water. Water, that has free hydrogen ions is acidic, and alternately water that has more free hydroxyl ions is alkaline. Measuring pH is in the scope of 0 – 14: the scale is logarithmic. pH below 7 is acidic and pH above 7 is alkaline. It is essential to screen the pH of a water body since it influences aquatic animals. A modification in normal pH in a water body can be an indication of expanded contamination or other environmental pollution factors. This

is because of the way that pH can be influenced by chemicals in the water.

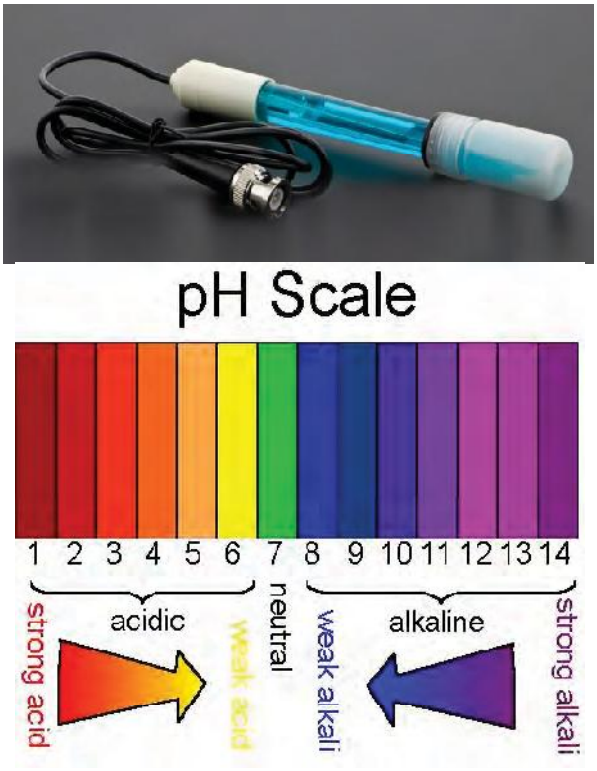

Figure.5. pH sensor

E. Fluoride Sensor:

The Fluoride Sensor is a potentiometric sensor, working with ion selective electrodes (ISE) and a reference electrode supplying the measurement signal (mV).The following are the main features of fluoride sensor:

- Measurement is instantaneous.
- Sensor provides stable measurement.
- For simple and quick installation, Fluoride sensors are available for quick operation and mounted on PE-boards, i.e. plug and play within adjustable segments.

Figure.6. Fluoride sensor

V. Software Description

1.GUI Platform:

GUI platform has been successfully developed by using html and java programming. Here, the real time values of fluoride, pH and water turbidity are displayed on the monitor. The user can get the real time status of every sensor on the web page.

2.Pycharm Software:

Pycharm software is used in this system. The source code for Raspberry Pi2 Model B is written in a language called *Python* programming. The program will be coded and dumped to the Raspberry pi2 model B processor so that the data is read from the sensor. It will be sent to the server with the help of IOT environment. Finally the result is viewed in the web server.

3.Internet Of Things:

The Internet of things (stylized as IOT) is comprised of sensors and actuators, the innovation turns into an occasion of broad class of digital physical frameworks. Web of Things is concerned with an idea in which, gadgets can gather and percept information from the world, share the information over the web which can be used and handled for different purposes. The idea of Internet of Things is especially useful to accomplish constant checking of sensor data.In proposed framework, Cloud computing procedure is utilized for storing and watching sensor outputs such as fluoride,turbidity and pH values on the web.Cloud computing unit processes in run time and it is less expensive to implement using IP.

VI. Results

The following are the results which are obtained from this work,

- Waste Level detection inside the water resources.
- Transmission of data to web.
- The data can be accessed on demand to assess the water quality .
- Data transmission and access will be in real time.

The Online Monitoring of Water Quality using Raspberry Pi2 Model B is very useful for water works department in smart cities. For example in cities such as Hyderabad ,there are different water sources located in the different areas and water gets polluted many times and the people do not get information about this. The system is designed to solve this issue and will provide pollution details of the water source located in the different areas throughout the city. The concerned authority can access the required information on demand. The following figures show the results obtained at fourdifferent locations.

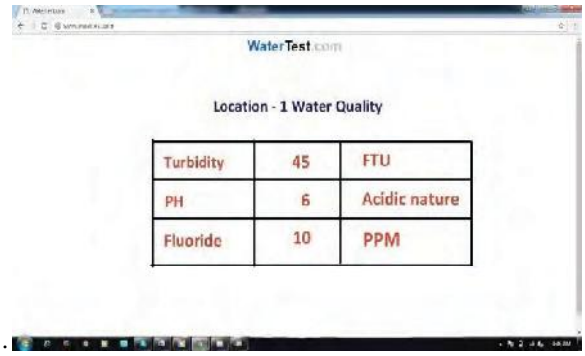

Figure.7. Location-1 Output

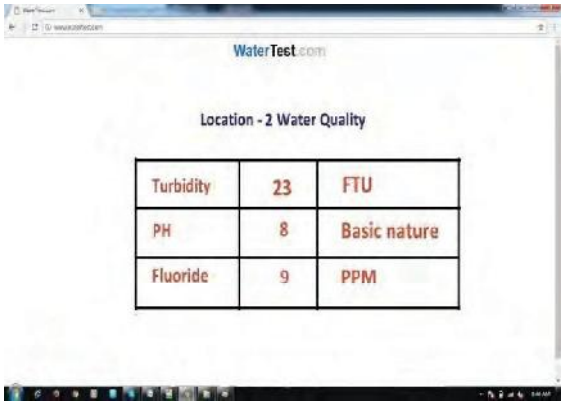

Figure.8. Location-2 Output

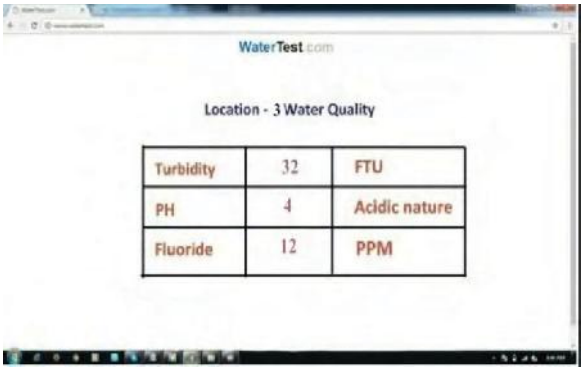

Figure.9. Location-3 Output

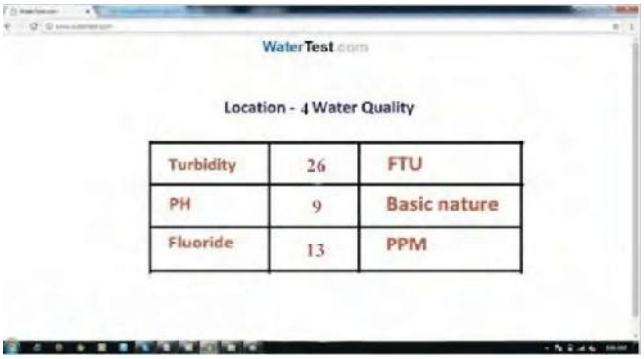

Figure.10. Location-4 Output

The proposed system, discussed in the paper provides data pertaining to water quality to the wide variety of users stationed at geographically different locations.By using more number of sensors, additional parameters such as temperature and conductivity can also be monitored. However skilled technicians are required to maintain the sophisticated electronic gadgets comprising Raspberry Pi board, sensors, and associated electronic circuitry. This drawback can be overcome by enhancing the reliability and simplicity of operation.

Applications:

- Water storage tanks before distribution.
- Health inspection agencies check and evaluates water quality at public gathering places like transport stations hotels etc.
- In health department for identifying the cause of water diseases.

VII. Conclusions

Testing of Turbidity, pH and fluoride of Water requires the use of corresponding sensors. The framework can screen water quality consequently, and it updates to servers website with minimal effort and does not require individuals on obligation. So the water quality testing must be more efficient, helpful and quick. The framework has great adaptability by supplanting the corresponding sensors and changing the applicable python programs. This framework can be utilized to screen other water quality parameters.

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SoC Implementation of Two Step Parallel ADC using Cadence Tools

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Abstract: **This paper presents the circuit of digital control logic for a 2 step parallel ADC. The goal behind in designing the control logic for parallel ADC (Analog to Digital Converter) circuits is used in many integrated circuits for detection of ionizing radiation. The converter employs a two step parallel technique employing a resistive DAC and is configured as a fully differential circuit. The results which are obtained from two step are further combined by using digital error correction algorithm to produce the final output. To design two step parallel ADC the following blocks are required i.e. comparator, resistive DAC, digital error correction block. All blocks are coded using Verilog HDL and compiled using Ncvlog Simulator, synthesized by using RTL Compiler and finally implemented on SoC Encounter.**

***Index Terms*— First Stage, Second Stage, Comparator, Resistive DAC, Digital error Correction Block, RTL Compiler, SoC Encounter.**

I. Introduction

Need of effective analog to digital converters with high resolution and high speed realization gave rise to the design of two step Parallel ADC architectures. This type of ADC's can be implemented without any high gain operational amplifiers having a large output swing. Compared with fully parallel designs, conversion rates are almost half in the case of half parallel design. These architectures provide low power decadence and small input capacitance. For an ADC to be suitable on different integrated chips, resolution should be of 10 bit/12-bit resolution and a few MSamples/ sec sampling rate [2]. In this design, resistive ADC replaces the traditional switched capacitance (SC) to DAC [11] which results in high performance. For the required 12-bit output to be produced, DCL is used to combine both estimates outputs which are produced in the above stated stages. There is a no necessity to correct out-of-range errors in the 1st-stage. The input of ADC ranges between -1.2 Volts to 1.2 Volts relative to AGND (analog signal ground which is of 2.4 Volts). Based on the above input ranges, the effective input of the ADC ranges from 1.2 to 3.6 Volts. The ADC is designed such that it produces 12-bit zeros for 1.2 Volts and 12-bit all ones for 1.8 Volts.

II. Blocks Of Adc Architecture

A. Two Step Algorithm

As shown in figure 1, V_{in} (input voltage) is applied to the first stage [11] of ADC resulting in the "coarse" output which is a 7-bit output in the form of digital samples. This 7-bit digital output is given as input to 7-bit DAC to produce an analog estimate of the coarse value which is again subtracted from the input voltage by using residue generator to produce "residue" output. This voltage is then passed as an analog input to second stage of the ADC. To produce the 12-bit digital output, the coarse output is passed through delay register, corrected using digital correction logic and combined with six-bit output of second stage.

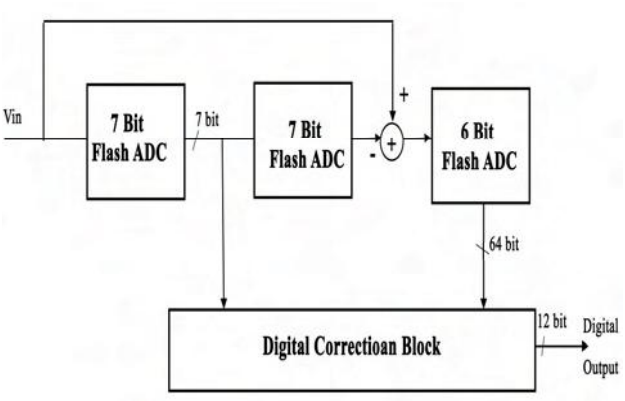

Figure 1. Parallel ADC Converter Architecture

B. First Stage

The first stage as shown in figure 2 comprises of a sequence of comparators, a resistive DAC [11,9], a residue generator and a TBC as shown in figure 2. In this ADC, 129 comparators are used. Out of these 129 comparators, 127 are used for normal digitization and the other two are used for checking the overflow and underflow conditions. If the applied tap voltage is greater than V_{in}, comparator [10] produces a 'one' else 'zero'. 127-bit thermometer code is produced as an output out of 127 first stage comparator array.

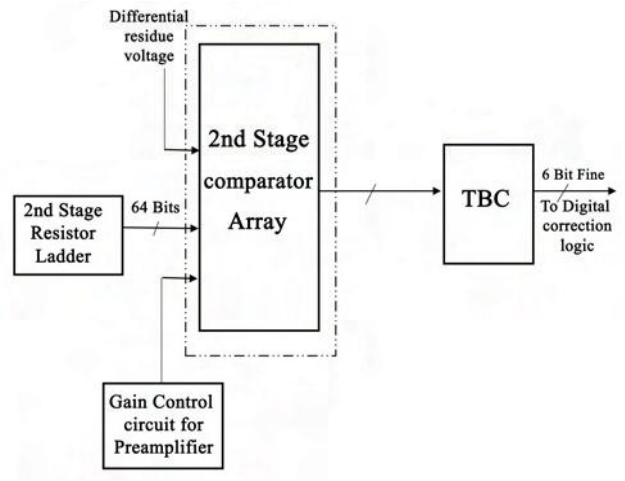

Figure 2. First Stage Flow Structure

C. *Second Stage*

The second stage [11] as shown in figure 3 comprises of a resistive ladder circuit, a sequence of 64 comparators, and a TBC as shown in figure 3. The main operation of the second stage is to digitize the differential output of residue generator in first stage to encode the "fine" bits of the ADC [7]. The comparators in this stage are set if the applied tap voltage is greater than residue voltage, else it produces a 'zero. A 64-bit thermometer code is generated out of array of comparators. This code is then encoded into binary and passed on to digital correction logic [1].

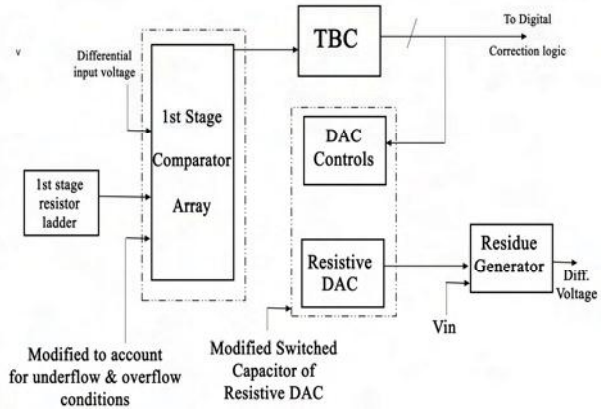

Figure 3. Second Stage Flow Diagram

D. *Digital Encoding*

Digital [2] is the process of converting the thermometer code into a binary code. 7-bit "coarse" output and 6-bit "fine" output are generated using this encoding process. The correction is done by sensing three adjacent levels in thermometer [8] code. A series of AND gates and an encoder forms the encoding logic. The binary outputs are corrected digitally to form 12-bit ADC output.

E. *Redundancy and Digital Correction Algorithm*

The first stage comparators are used for high speed and resolution. There exists one bit overlap between the stages to accommodate potential moderate errors. The overlap makes sure that residue of the first stage falls within the input range of second stage. The digital outputs of the ADC are added using digital correction logic whose algorithm is depicted as in figure 4. Firstly, checking of 7-bit output from the first stage is done. If it is zero, entire output of first stage is shifted to left by five places, and is added to 6-bit second stage output to get the final output. If the output of first stage is non-zero, we shift it to the left by five places and shift it down by 16 LSB's i.e., shifting the DAC [11] output by half of sampled step. Then the 12-bit final output is generated from the outputs of first and second stages. The Figure 4 gives the Flow chart of Digital error correction algorithm. [6]

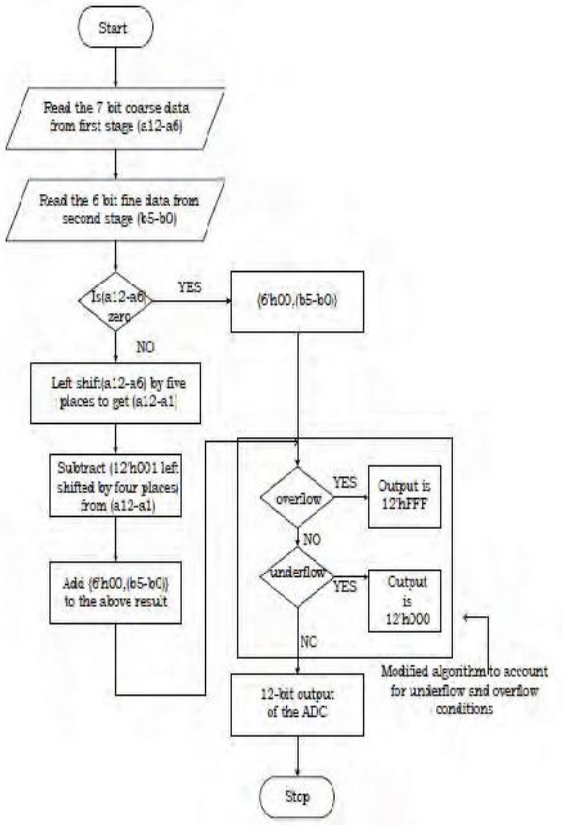

Figure 4. Structure of Digital Error Correction Algorithm

III. Implementation And Analysis Results

All the blocks are designed by using Verilog HDL and implemented using ASIC Cadence SoC Encounter tool with 45 nm technology libraries. Figure 5 shows RTL [3] [12] Schematic of Fine Technique, Figure 6 shows RTL Schematic Register network, Figure 7 shows RTL Schematic of DAC block, Figure 8 shows RTL Schematic of Digital error Correction Block.

Figure 9 shows net power usage of two step parallel ADC. Table 1 show Pre CTS and Post CTS analysis report, Table 2 shows the power analysis. Figure 11 shows the inner layout of parallel ADC and finally figure 12 shows the GDS II [4] layout structure of two step Parallel ADC.

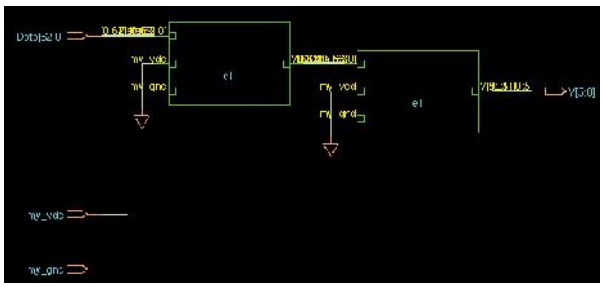

Figure 5. RTL Schematic of Fine Technique

Figure 6 gives the Register Transfer level of register ladder network which converts a parallel digital symbol or word into an analog voltage. This network consists of some unique and interesting properties i.e. easily scalable to any desired number of bits, uses only two values of resistors which make for easy and accurate fabrication and integration, output impedance is equal to R, regardless of the number of bits, simplifies filtering and further analog signal processing circuit design.

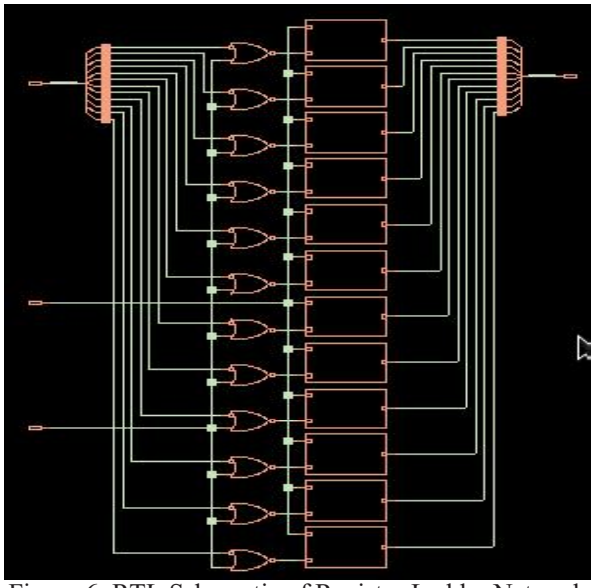

Figure 6. RTL Schematic of Register Ladder Network

Multiplying Digital to Analog Converter operates on discrete time signals and switched capacitor circuits. These circuits are used to perform highly accurate mathematical operations such as addition, subtraction and multiplication, due to the availability of capacitors with a high degree of relative matching. These circuits also facilitate multiple, simultaneous signal manipulations with relatively simple architectures. It is possible to combine the S/H, subtraction, DAC and gain into a single SC circuit, referred to as the Multiplying DAC.

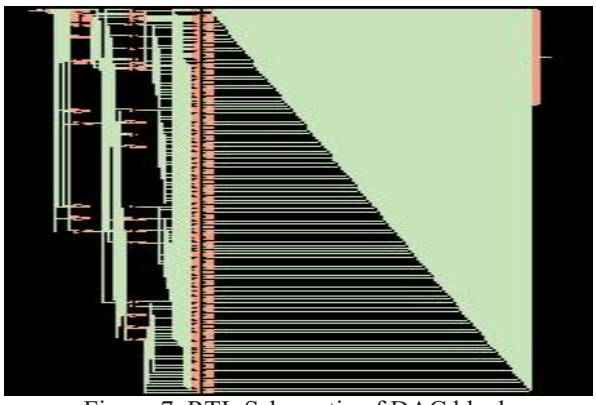

Figure 7. RTL Schematic of DAC block

Digital error correction block greatly reduce the accuracy requirement to the parallel ADCs. The 3-bit residue at the summation node output has a dynamic range of one eighth than that of the original stage 1 input VIN, yet the subsequent gain is only 4. Therefore, the input to stage 2 occupies only half the range of the 3-bit ADC in stage 2.

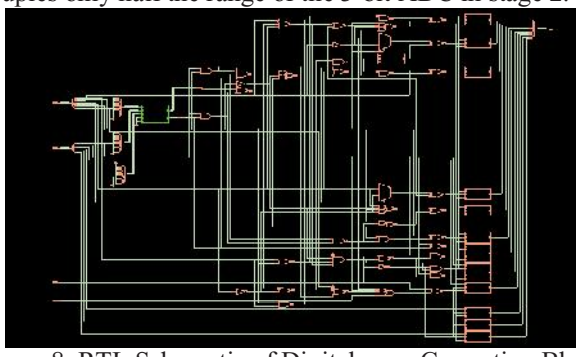

Figure 8. RTL Schematic of Digital error Correction Block

Net power usage gives the power distribution of all the blocks in two step parallel ADC i.e. coarse, fine technique blocks and register ladder network as shown in figure 9.

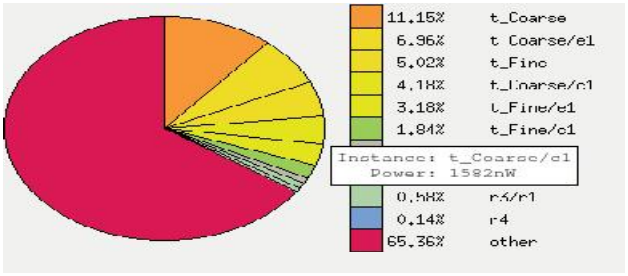

Figure 9. Net Power Usage of Two Step Parallel ADC

Pre CTS and Post CTS Analysis Report gives the details of clock tree synthesis in terms of nano seconds for all the paths. Register 2 register paths and 0 violating paths are there in two step parallel ADC before routing and after routing steps in the fabrication.

TABLE I.
PRE CTS AND POST CTS ANALYSIS REPORT

Setup mode	all	reg2reg	default
WNS (ns):	8.218	8.218	9.701
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	48	19	41

The circuit performance depends on the power consumption, i.e. when it consumes very less power the design will be more efficient and flexible in nature. Total internal power gives the entire power consumed through all the blocks, switching power gives the power consumed between the blocks and leakage power gives the power dissipated through the blocks. For an efficient design leakage power to be very minute as shown in Table 2. Entire power is calculated in terms of watts.

TABLE II.
POWER ANALYSIS REPORT

Total Power (Watts)		
Total Internal Power	0.2213742	59.2987%
Total switching Power	0.01515964	40.6076%
Total Leakage Power	0.0000348	0.0937%
Total Power	0.0373320	

The internal structure gives layout description of the blocks of two step parallel ADC i.e., Fine Technique Block, Coarse Technique Block, Multiplying Digital to Analog Converter block, Digital Error Correction Block and Register Ladder Network and it finally gives the memory occupancy on an IC as shown in figure 11.

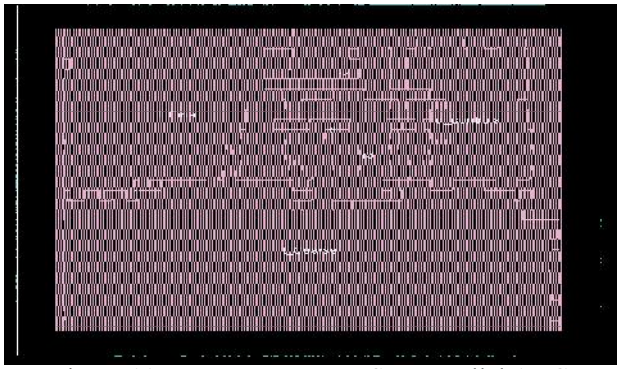

Figure 11. Inner Layout Two Step Parallel ADC

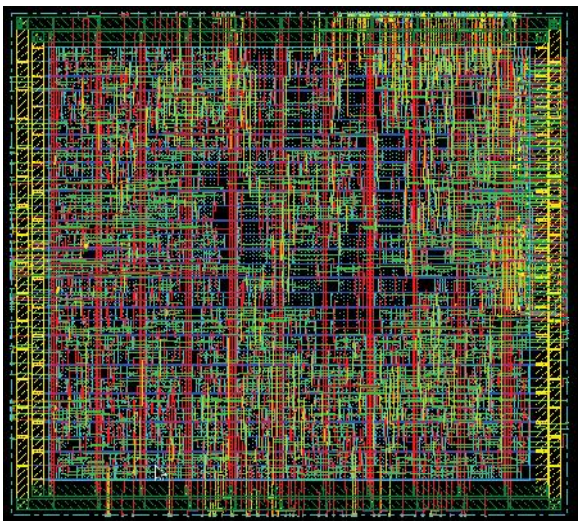

Figure 12. GDS II of Two Step Parallel ADC

GDS II is obtained by performing the following steps i.e., importing .netlist file, standard design constraints file, capatable file, power nets (VDD, GND) and technology libraries etc. floor planning, placement - placing standard cells, check placement, nano routing, pre timing analysis - clock tree synthesis, optimization, detailed routing, post timing analysis - Post CTS, Verify geometry, verifying connectivity, power planning and finally layout is obtained as shown in the figure 12.

IV. CONCLUSIONS

Parallel ADC is also known as Flash ADC or Direct Conversion ADC. It uses a linear ladder circuit which contains different voltage values with a comparator at each crosspiece (step) of the ladder to compare the input supply voltage to successive reference voltages. Instead of voltage ladder circuit it can be replaced with resistive network. The two step parallel technique with resistive or capacitive DAC is configured as a fully differential circuit. It performs coarse parallel conversion followed by fine parallel conversion and combined through a digital error correction block to produce the final digital output. All the blocks are simulated and synthesized by using Ncvlog and RTL Compiler. The netlist file of RTL Compiler is given to SoC Encounter to obtain final chip layout structure in terms of OAS/GDS II file.

Technology : GPDK 45nm, 90nm technology libraries
Simulation: Ncvlog Simulator
Synthesis Tool : RTL Compiler
(Area, Timing - Worst Path Analysis, Power Analysis)
Implementation (Back End Tool) : SoC Encounter

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Power Saving and Delay Analysis of Adder Circuit using Adiabatic Logic

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Abstract— In the implementation of all Integrated circuits (IC), the design parameter power consumption is considered as important parameter. It is considered as top design challenge among all the challenges in the international Integrated Circuit (IC) roadmap technology. The implementation of low power VLSI circuits has been emerged as they are very high in demand because of the rapid growth in technologies.

In the IC chips the transistor count is increasing rapidly and proportionally, as the semiconductor technology entered into nanotechnology scale. The portable and smart electronic gadgets requires more energy efficiency and compact in size. But this improvement increases the clock speed to satisfy the above specifications. Hence, the dynamic power dissipation of the circuits increased. The portable electronic gadgets that are always require high speed clock.

Due to this high speed of the clock the dynamic power dissipation is increased in the VLSI circuits. In the conventional Complementary Metal Oxide Semiconductor (CMOS) techniques, the power dissipation is minimized by supply voltage reduction, reducing the activity of the transistor switches and by considering the less load capacitance. These techniques will be useful to reduce some part of the power dissipation only and still power dissipation is taken place. The further power dissipation can be reduced using adiabatic logic technique.

This paper has presented all the gates (NAND, NOR etc.) implementation using adiabatic logic. The complex circuits such as, full adder and a Carry Look ahead Adder (CLA) circuits are implemented using adiabatic 2PASCL topology and also implemented in conventional CMOS technology. All these implementations are done in 180nm technology using VLSI full-custom cadence tools. The results of the above circuits are compared in terms of delay and power consumption. The comparison states that, the adiabatic logic circuits consume less power with little bit penalty of delay.

***Index Terms*—CMOS logic, adiabatic logic, 2PASCL, power.**

I. Introduction

The word adiabatic is derived from thermodynamics that logic is preferably used to reduce the energy consumption. This process do not use the exchange of heat with the external environment. The main principle of the adiabatic logic is energy reusing. Basically, the stored energy in the capacitor discharging through the ground. But, in this adiabatic logic, this energy is reused itself. The power wastage is taken place in the traditional concept. In adiabatic technology, due to the reusing power saving taken place and power dissipation reduces. This adiabatic logic increases the circuit complexity with advantage of low power [1].

Mainly, there two types of adiabatic structures are mostly used. Those are fully adiabatic logic structure and second is semi or partially adiabatic structures. The design of fully adiabatic logic circuits is very complex due to the complex clock tree design. The advantage of this logic is no losses are occurred. The counterpart, the non-adiabatic logic circuits provides many losses, but design of this style is easy. The trapping of charge at nodes only treated as losses in this structure [2][3].

In the recent years, many adiabatic logic methods are emerged to reduce the power dissipation. Some of them are, trapezoidal waveform at the power supply and QSERL is one of the adiabatic technique that uses two sinusoidal waves, which are 180^{o} phase shift to each other [4]. This technique may consist some limitations regarding to nodes with floating, depletion region of the node capacitor and fan in and fan-out. In some gate implementations, the diodes are needed. These diodes also degrade the output levels and provide power dissipation issues.

Practically, the power or energy consumption associated with charging or discharging of the capacitors in adiabatic components. Hence, the reduction of complete power dissipation may not possible. The adiabatic logic switching approach is conserves the complete energy. But, in the other logics the energy is converted into heat. Hence, these adiabatic type of approaches are used to reduce the power dissipation in digital circuits based on requirements and applications.

A. Conventional Switching

In CMOS circuits, the Dynamic and static power dissipations are mainly contribute for the total power dissipation. The magnitude of the dynamic power dissipation in any circuit is depends on the load capacitance charging and discharging. The static power never depends on the signal switching, which depends on the static current flowing between the power rails. Whenever short circuit is taken place based upon the logic states between VDD and GND, large static current flows and causes to produce more static power dissipation.

The static power dissipation mainly depends on the leakage currents. These leakage currents may be diode leakage, gate oxide leakage and sub-threshold leakage currents. In deep sub-micron technology, the leakage power is the dominant to produce static power dissipation. The expression for the leakage power is given by equation (1)

$$P_{lkg} = I_{lkg} \times V_{dd} \quad (1)$$

During charging of the capacitor the total energy supplied by the power supply CV_{dd}. The 50% of the power is dissipated in the PMOS transistor and its interconnect and remaining 50% power is dissipated or stored in the load capacitor C_L. The load capacitor stored energy is dissipated through the NMOS interconnect as represented in the Figure. 1. Due to the slowly varying of the input signal transitions, the short circuit power dissipation occurs. At that time large static current is flowing through the power rails. That means a short connection is taking place between VDD and GND. The Figure.1 shows the equivalent circuits for the

charging and discharging of the CMOS logic circuit. The overall power dissipation is determined by equation (2).

$$P_{total} = CV^2{}_{dd}f_{clk} + I_{sc} + I_{lkg}V_{dd} \quad (2)$$

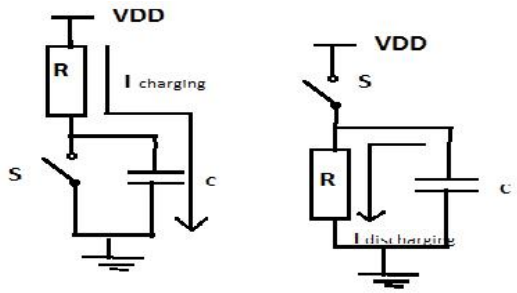

Figure. 1 Conventional CMOS switching.

II. Adiabatic Switching

In this section the adiabatic switching technique to minimize power consumption in VLSI circuits. The time constant RC of the adiabatic logic circuit is very much less than the ramp time period T. i.e., RC << T. Due to this condition, the voltage across the capacitor is nearly follows the VDD supply voltage. Then potential difference is almost zero across the resistor R. The voltage of the capacitor Vc is constant ramp with proportional with slope V/T. Here V means supply voltage and T is the Clock period of the power. The adiabatic circuit charging current and energy dissipated in the resistor are given by the following equations (3) & (4) respectively.

$$i_c = C\frac{dVc}{dt} = \frac{CV}{T} \quad (3)$$

$$E = i_c{}^2 RT = \frac{(CV)^2}{(T)^2}\ RT = \frac{RC}{T}CV^2 \quad (4)$$

The Figure. 2 represents the discharging equivalent circuit in the adiabatic switching technique. This is also same as the capacitor charging. But, the voltage in the power supply downs like ramp due to RC << T, and the equation is given by

$$E = \frac{RC}{T}CV^2 << \frac{1}{2}CV^2 \quad (5)$$

This explanation states that the energy of the capacitor is more than the resistor power consumption during the time of capacitor charging and discharging of the capacitor. While the capacitor discharging, the reusing of energy in the capacitor is taken place using returning of supply voltage concept [5][6].

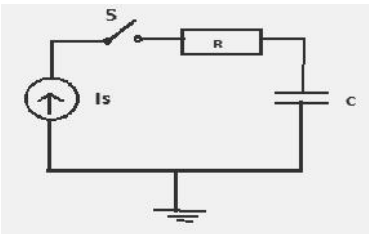

Figure.2 Adiabatic Switching

A. 2PASCL Circuit

The adiabatic logic family is a Two Phase clocked Adiabatic Static CMOS Logic (2PASCL). It contains extra two more transistors only comparatively normal adiabatic logic. In this logic, one transistor is placed in between the Power clock and output terminal. The other transistor is placed beside of the NMOS transistor or pull down logic, which is connected to the other power supply. In this technique, the supply voltage Vdd is replaced by PHI and ground terminal connection Vss is replaced by PHI_BAR respectively. In this method, two complimentary split level sinusoidal wave are used for power clock generation.

The adiabatic circuit operation is divided as two modes, One is evaluation mode and second is Hold phase [7][8]. In the evaluation phase, initially the Pmos logic is turned on. After that, the output becomes low and Load capacitor gets charged for VDD through Pmos transistor and output becomes high logic level. If Nmos transistor is on, the output node Y becomes low and no transition. Whenever, the output node is high the corresponding transistor i.e Pmos also turned on and there is no any transition. Finally, if output node is high, then the corresponding Nmos transistor turned on, discharging is taken place and diode D2 makes the output is low.

In the hold phase, if the output node Y is low, then the transistor NMOS switches to ON, that means no transition. Suppose, the node y is high then the PMOS becomes on then discharging taken place via the diode D1is shown in the Figure 3.

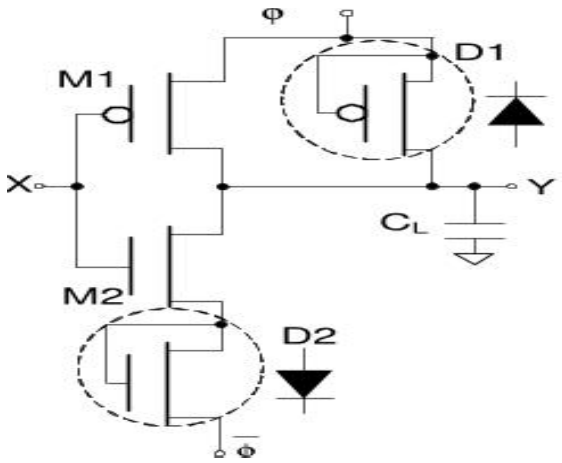

Figure.3 2PASCL Circuit.

III. Simulations and their results

The following Figures from Figure. 4 to Figure 39 are schematics, input and output waveforms, power and delay analysis of NOT, NAND, NOR, EXOR gates, full adder and a 4-bit Carry Look ahead Adder (CLA) circuits [9],[10],[11] using CMOS and adiabatic 2PASCL topology implemented using cadence virtuoso tool in 180nm technology.

Figure 4,5,6 are the schematic diagram, input, output waveforms, power analysis and delay analysis of CMOS inverter circuit.

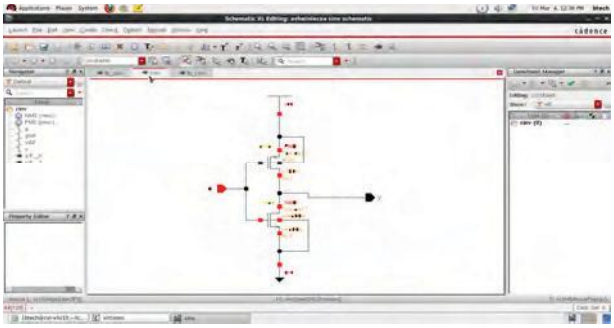

Figure.4 CMOS Inverter Schematic

Figure.5 CMOS Inverter Input ,Output waveforms and Power analysis

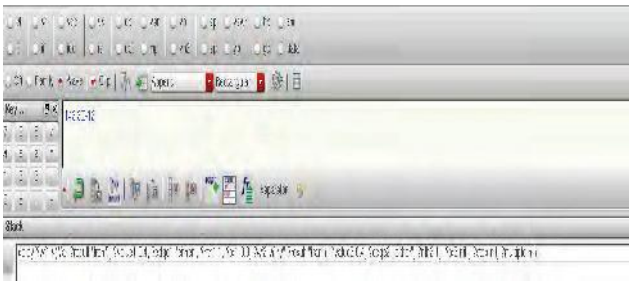

Figure.6 CMOS Inverter Delay analysis.

Figure 7, 8, 9 are the schematic diagram , input, output waveforms , power analysis and delay analysis of adiabatic inverter circuit.

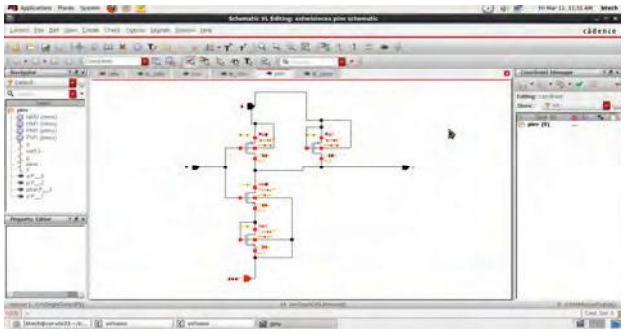

Figure.7 Adiabatic Inverter Schematic

Figure.8 Adiabatic Inverter Waveform & Power

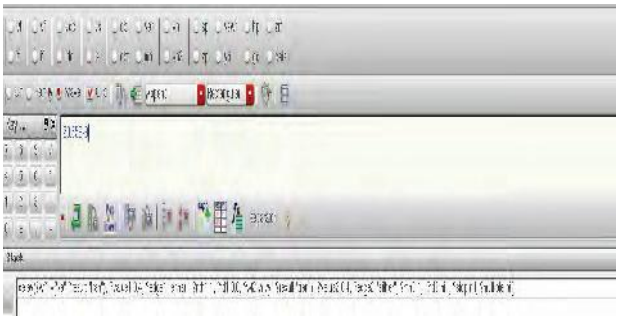

Figure.9 Adiabatic Inverter Delay

Figure 10,11, 12 are the schematic diagram , input, output waveforms , power analysis and delay analysis of CMOS NAND gate circuit.

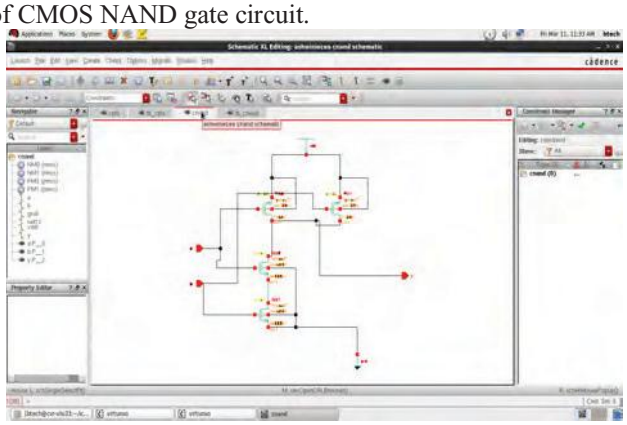

Figure.10 CMOS NAND Gate Schematic

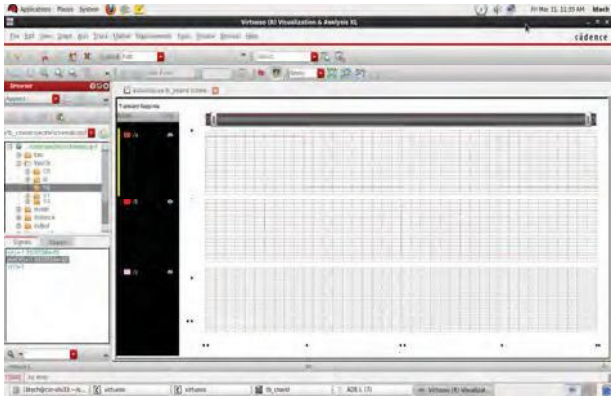

Figure.11 CMOS NAND Gate Input, Output Waveforms and Power

Figure.12 CMOS NAND Delay

Figure 13,14, 15 are the schematic diagram , input, output waveforms , power analysis and delay analysis of Adiabatic NAND gate circuit.

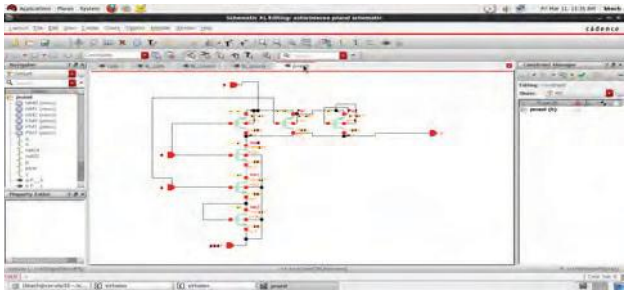

Figure.13 Adiabatic NAND Schematic

Figure14. Adiabatic NAND Waveforms and Power

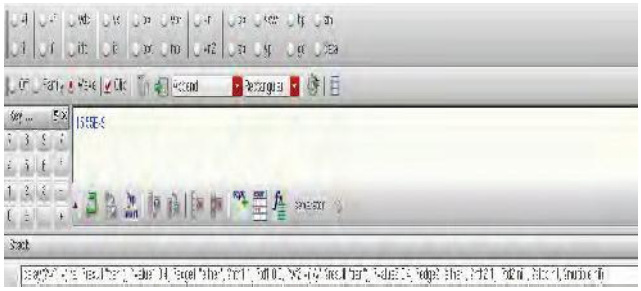

Figure.15 Adiabatic NAND Delay

Figure 16,17, 18 are the schematic diagram , input, output waveforms , power analysis and delay analysis of CMOS NOR gate circuit.

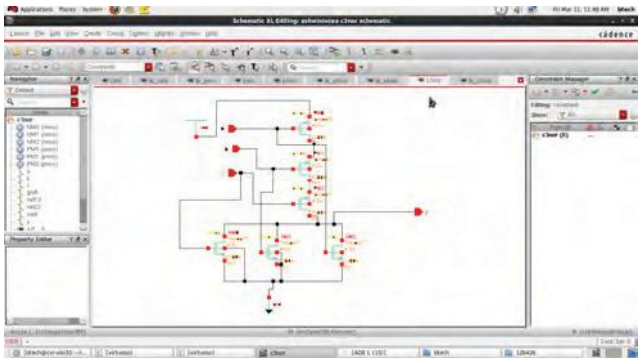

Figure.16 CMOS NOR Schematic

Figure.17 CMOS NOR Waveforms and Power

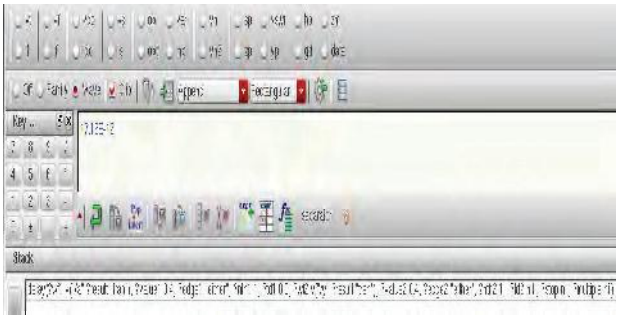

Figure.18 CMOS NOR Delay

Figure 19,20, 21 are the schematic diagram , input, output waveforms , power analysis and delay analysis of Adiabatic NOR gate circuit.

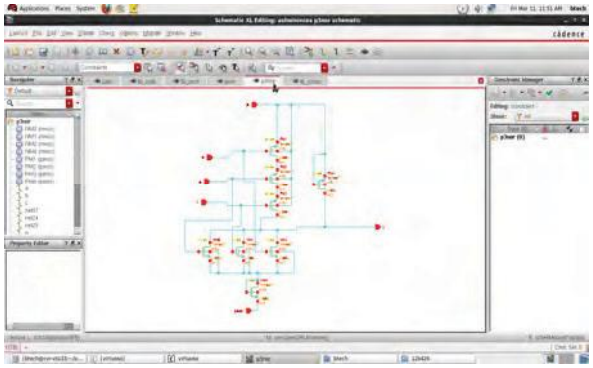

Figure.19. Adiabatic NOR Schematic

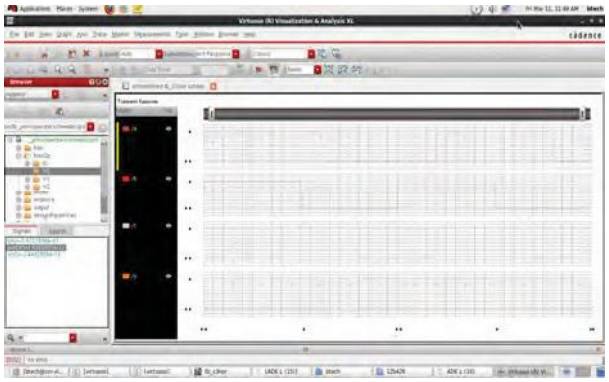

Figure.20 Adiabatic NOR Waveforms and Power

Figure.21 Adiabatic NOR Delay

Figure 22,23, 24 are the schematic diagram , input, output waveforms , power analysis and delay analysis of CMOS EXOR gate circuit.

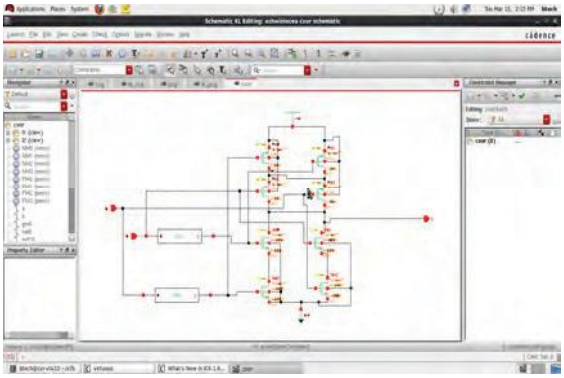

Figure.22 CMOS EXOR Schematic

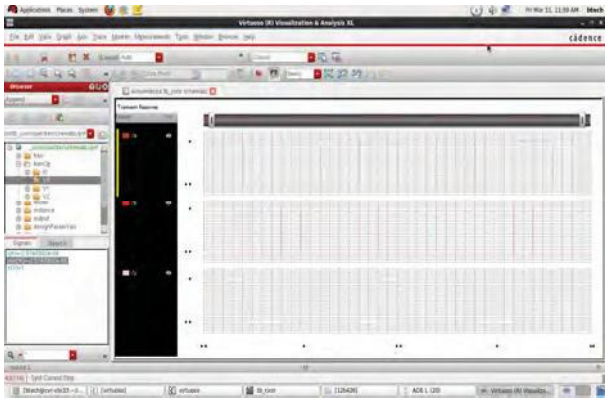

Figure.23 CMOS EXOR Waveforms and Power

Figure.24 CMOS EXOR Delay

Figure 25,26, 27 are the schematic diagram , input, output waveforms , power analysis and delay analysis of Adiabatic EXOR gate circuit.

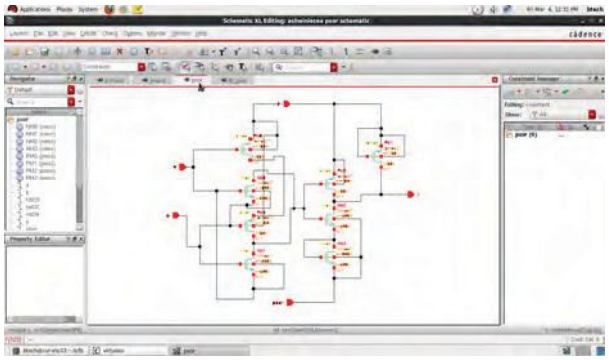

Figure.25 Adiabatic EXOR Schematic

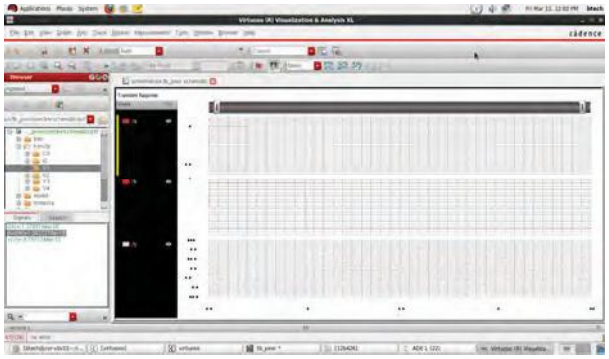

Figure.26 Adiabatic EXOR Waveforms and Power

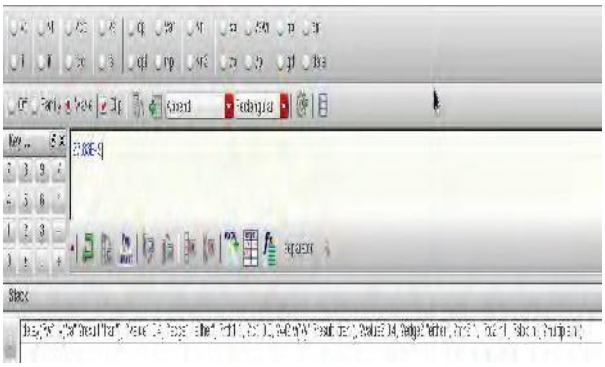

Figure.27 Adiabatic EXOR Delay

Figure 28,29, 30 are the schematic diagram , input, output waveforms , power analysis and delay analysis of CMOS Full Adder circuit.

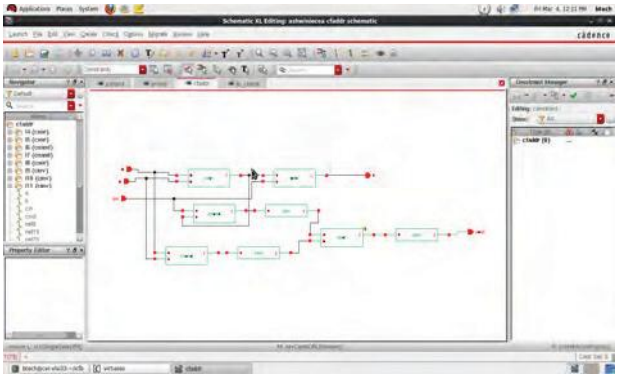

Figure.28 CMOS Full Adder Schematic

Figure.29 CMOS Full Adder Waveforms and Power

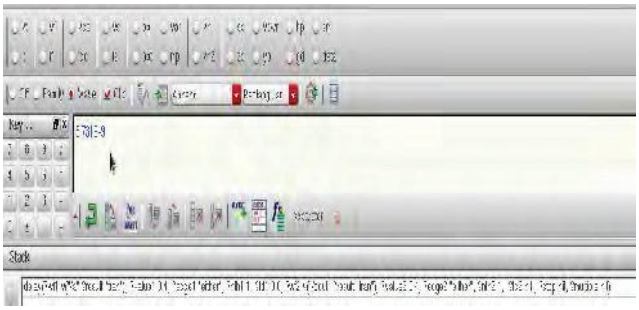

Figure.30 CMOS Full Adder Delay

Figure 31,32,33 are the schematic diagram , input, output waveforms , power analysis and delay analysis of Adiabatic Full Adder circuit.

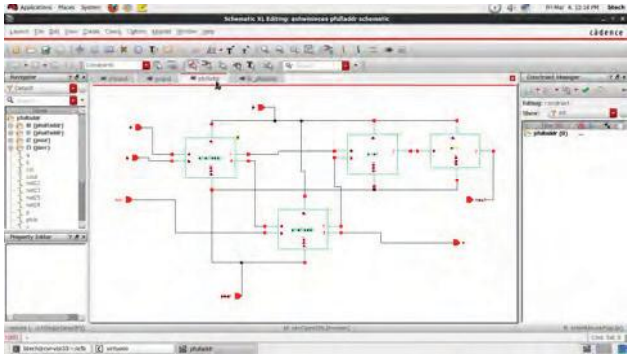

Figure.31 Adiabatic Full Adder Schematic

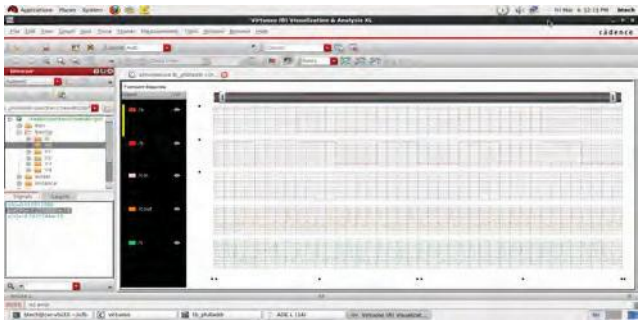

Figure.32 Adiabatic Full Adder Waveforms and Power

Figure.33 Adiabatic Full Adder Delay

Figure 34,35,36 are the schematic diagram , input, output waveforms , power analysis and delay analysis of CMOS CLA Adder circuit.

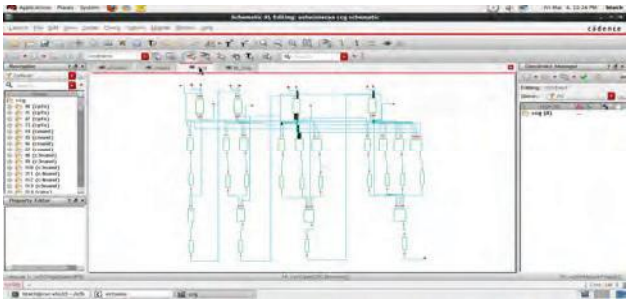

Figure.34 CMOS Carry look ahead adder Schematic

Figure.35 CMOS Carry look ahead adder Waveforms and Power

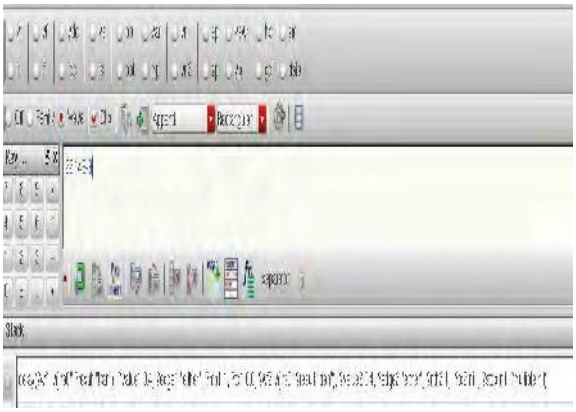

Figure.36 CMOS Carry look ahead adder Delay

Figure 37,38,39 are the schematic diagram , input, output waveforms , power analysis and delay analysis of Adiabatic CLA Adder circuit.

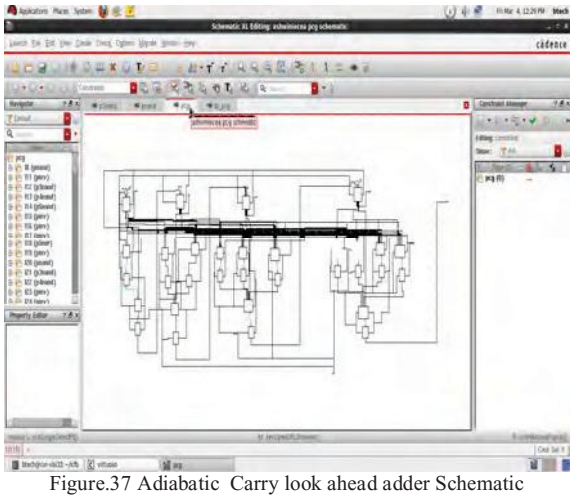

Figure.37 Adiabatic Carry look ahead adder Schematic

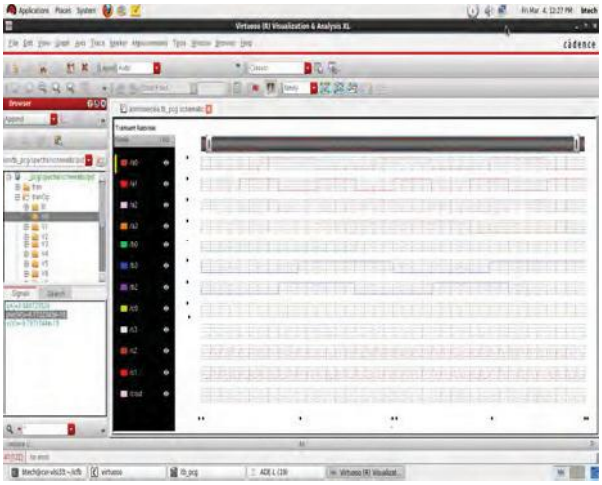

Figure.38 Adiabatic Carry look ahead adder Waveform and Power

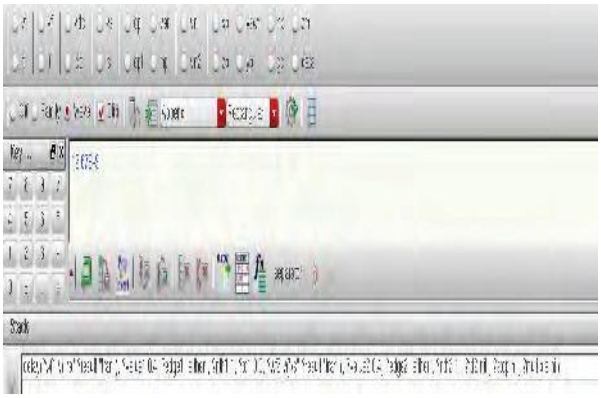

Figure.39 Adiabatic Carry look ahead adder Delay

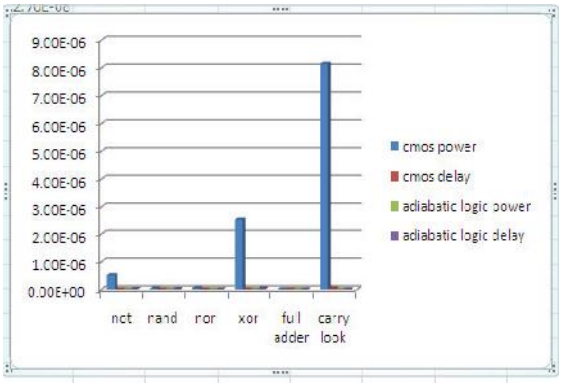

Figure. 40 Bar graph comparison of delay, power of CMOS and Adiabatic logic

TABLE I.
POWER AND DELAY OF CMOS AND ADIABATIC LOGIC

Circuit	Conventional CMOS		Adiabatic Logic	
	Power	Delay	Power	Delay
Inverter	5.44E-07	1.43E-10	6.02E-20	2.05E-08
Nand	3.16E-08	2.58E-10	3.59E-19	1.55E-08
Nor	4.19E-08	1.72E-11	4.60E-19	1.48E-11
Xor	2.57E-06	5.30E-09	1.37E-19	2.70E-08
Full Adder	1.39E-19	5.07E-10	1.38E-19	5.70E-09
Carry Look Ahead Adder	8.15E-06	2.21E-08	4.78E-16	2.68E-10

IV. CONCLUSIONS

In this paper, the logic gates are implemented by adiabatic logic techniques are fully compared with the traditional CMOS logic gates in terms of power and delay. The complex circuits such as, full adders and CLAs also implemented using adiabatic logics and compared with CMOS adders. The power dissipation of the adiabatic circuits are very much less comparatively the CMOS circuits as shown in table.1. The bar graph also shows the power dissipation of the adiabatic logic circuits on Figure 40. Results further affirm that with higher the load capacitance, the power dissipation in the 2PASCL circuits still remain low. From the above simulation results, the 2PASCL circuits consume less power comparatively static CMOS circuits. Finally, these adiabatic logic circuits are fit for the low power VLSI designs. However, in these circuits the delay is little bit increased.

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Analysis for the Implementation of Capacitive Couple Readout Circuit for Contact-less ECG and EEG

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Abstract—In modern medicine, the two most common and actively used techniques for measuring electrophysiological signal for human are Electrocardiography (ECG) and Electroencephalography (EEG) systems. These physiological signals are very weak in amplitude in terms of few millivolts down to 10's of millivolts. The major amount of power is located at very low frequencies from below 1Hz up to 40 Hz. The measurement of the above parameters is very tough job in electrical circuit designs. Generally, the measurement of these parameters is done by electrodes with direct skin contact by applying of some gels. For this, time consuming clinical set up is required. This paper introduces a method for the measuring the above type of signals using a capacitive coupled sensor. This sensor is completely non-contact type, but this method has to face some difficulties, such as: high input impedance and interfaces and some circuit nose problems. A capacitive coupled sensor is realized by the printed circuit board (PCB) bottom layer as a one capacitor plate and the signal source is considered as another plate. In this, PCB layer mask acting as an insulator. The high input impedance amplifier gives the gain for the sensed signals is 60 dB and filtering also taken place. Two measurements were made off using the same circuit for two different input impedances. The results of these measurements show that high input impedance is a crucial parameter for the functionality of the sensor circuit and the high input impedance circuit provides always good signal to noise ratio (SNR).

Index Terms—Sensors, ECG, EEG, Readout, PCB, Electrophysiological signals, Amplifier, Instrumentation amplifier, Low Noise, Low Frequency and SNR.

I. Introduction

In health monitoring and diagnostics, the measurement of Electrophysiological signals play a vital role. The real information of health state is given by the electrical activity of nerve and muscles. The mostly used measuring techniques for the above electrical signals are EEG and ECG. The EEG is used to measure the electrical signals originating from the brain and ECG is used to measure the electrical signals generated by heart muscle. The EEG can be used to develop prosthesis, which can be control the patient's thoughts. Another application is detection of drowsiness of vehicle drivers to avid the accidents [1, 2]. Generally, EEG and ECG generate very weak signals with an amplitude of millivolts and have the major amount of the power is mainly located at very low frequencies [3].The SNR and linearity of the interfacing circuitry, are affected by the above two characteristics and it is difficult to measurement. The most important challenge regarding EEG and ECG signal is the interfacing sensor circuit with high accuracy in the noise environment.

These days EEG and ECG signal are measured by direct contact with skin using conductive coupling. For this direct skin contact measurement the glue gels are used with the help of fixating electrodes. The electrodes are silver chloride or gold type electrodes. This combination setup working as an electrical transducer to convert skin surface-ionic current to electron current. This current is amplified by electrical read-out circuit with high precision and low noise.

A. Idea about Circui Designs

The authors Sullivan et.al[4] and Harland et.al [5] introduced electrical read-out circuit for bio-medical signals. This design considered PCB itself as a sensor and this sensor treated as a low noise read out sensor circuit. The PCB metal layer acts as one plate of the capacitor and it is charged by another plate is nothing but skin of the patient. This circuit is couple with the amplifying circuitry. The entire readout circuit is large in size, so it was split into two PCBs. These two PCBs are placed on top of each other to reduce the total size of the sensor. The area reduction means that within the same place more sensors can be occupied. One important aspect regarding to EEG measurement where it is beneficial to have a large number of sensors [6].The readout circuit is implemented using a bottom layer of the sensor board, which is filled with a metal. This acts as an antenna to receive the electromagnetic signals in the vicinity. This board is put in the form of flat, like a capacitor with its metal layer and the skin as two plates of the capacitor. The soldering mask or air is used as dielectric isolation between the plates. The overall interference in the circuit is reduced by a metal shield layer, which is placed between the sensor layer and the remaining circuitry This capacitor picks the signal, which is amplified by low noise, low input bias current and high input impedance instrumentation amplifier up to gain 50. Next, filtered by band pass filter and again amplified 20 times by another low noise operational amplifier. The total gain obtained as 1000 by amplifiers. From the input side of the instrumentation amplifier the capacitor cuts off the DC connection to ground effectively. Then the input bias current integrates onto the capacitor to increasing the offset voltage. This offset voltage slowly increasing and it would cross the common mode input voltage range. Finally, at particular stage the amplifier the operation becomes undefined and output gets distorted. To overcome this problem, a resistor is used to provide a return path for the input bias current. This resistor and sensor capacitor combination forms a high pass filter. Here,

the capacitor should be small and resistance will be high enough to pass the EEG and ECG signals. If this simple circuit is suitable for these applications then the complex design presented in the paper [6] can be ignored. By observing the possibilities and limitations this simple circuit can be used for the read out circuits.

II. System Overview

The complete Readout circuit system consists of four parts. The actual sensor, first amplification stage, notch filters and second amplification stage. The actual sensor is the capacitor plate. A high input impedance instrumentation amplifier used as first amplification stage and second amplification stage is for additional gain is combination of op-amp and band pass filter. For filtering the interfering signals two notch filters are used. The complete readout circuit shown in Figure.1.

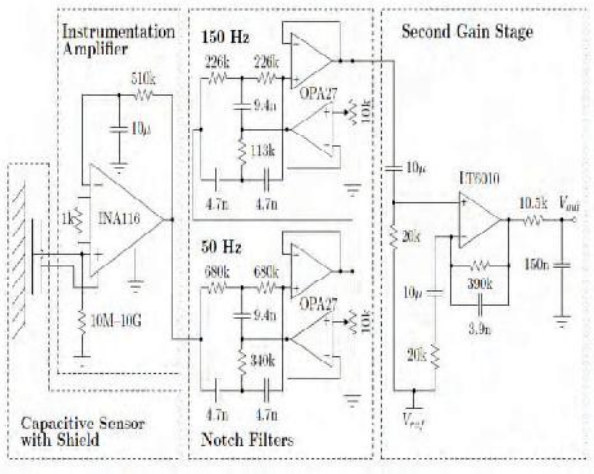

Figure 1. Circuit diagram of the complete system.

The sensor consists of two plates, such as PCB metal layer and skin of the subject to measure. The soldering mask or any material can be used as dielectric material. This sensor or capacitor is separated from the remaining circuit using a shielded layer and it is connected to the non-inverting terminal of the instrumentation amplifier. This instrumentation amplifier amplifies the signal by the gain of 50 and provides the feedback loop. In the feedback loop, the low pass filter makes the inverting terminal slowly follows the non-inverting terminal. The final circuit in the readout system is another amplifier, which gives the further gain of 20 and also provides the appropriate filtering by the band pass filter. Then the total gain in the system over the pass band is equal to the 1000 or 60 decibels theoretically.

A. The Capacitive Sensor

The capacitor sensor is implemented as a parallel plate capacitor. It means two metal plates are separated by a dielectric material. One plate is PCB metal layer and the second is skin of the patient. The figure 2. Shows the sensor setup. Here, the capacitor plates area is greater than the distance between the plates. Then the parallel plate capacitance is given by,

$$C = or\frac{A}{d}$$

Where, $\mathcal{E}o$and $\mathcal{E}r$ are the dielectric constant and relative dielectric constant, d is the distance between the plates and A is area of the platesrespectively.

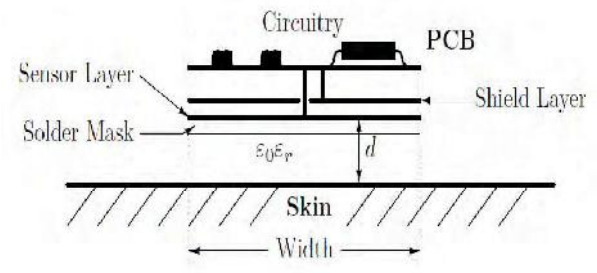

Figure 2. The cross sectional view of the PCB sensor.

The above figure represents the Capacitance equation variables and how those are physically determined. In this, the dielectric constant and distance'd' are varying with the position of the sensor. Due to this variation the determination of exact capacitance value is little bit difficult. The isolation dielectric constant value between the plates is defined by the air and solders mask material. The input resistance of the first stage amplifier and the sensor capacitance forms a high pass filter. For this low capacitance value is required. To lowering the capacitance, the sensor is moved away from the skin or source of the signal. It will change the cut-off frequency of the filter. Hence high input resistance is required to enable the low frequencies of the EEG and ECG. This high input resistance makes the less impact of the capacitance change to alter the cut-off frequency of the filter.

B. Instrumentation Amplifer

In this readout circuit, the INA116 used as instrumentation amplifier, which is provided by Texas instruments. It gives very low input bias currents and very high input impedance. It has low noise with respect to current and it is used for low noise applications. The buffer guard pins on output side to provide low output impedance [7]. These parameters are ideal to use for the reduction of the leakage currents in the sensor circuit

C. Notch Filters

The narrow band reject filter is used as a notch filter, which selects the specific frequency component from the input signal. Generally, these filters are used to reject the unwanted interfered signals and suppress the hum due to main power. From the input side of the instrumentation amplifier, at 150 Hz and50 Hz frequencies the sufficient large amplitudes are identified to saturate the last stage of the readout circuit. Two notch filters are used to suppress these interferences, which are inserted between two stages. Two operational amplifiers are require to implement the notch filters. In this design totally four OPA27 amplifiers are used from Texas Instruments. It is low noise and high precision amplifier.

D. Second Gain Stage and Band Pass Filtering

This stage is realized by one operational amplifier and the band pass filter. This stage provides the additional gain

and interested frequency selection. The LT6010 Op-Amp IC selected for this stage. It is operated for 3 volts supply voltage with high precision [9]. It is designed as a band pass filter with pass band gain of 20.5. This circuit is followed by another filter i.e. Low pass filter, is used for the limiting the upper band frequencies and aliasing problem is eliminated by this low pass filter. If any DC voltage is provided by instrumentation amplifier, is overcome by first stage high pass filter.

III. Circuit Analysis

In this section, the complete analysis of the system is presented. The Laplace transforms are used to obtain the frequency response of all the circuits.

The actual sensor circuit part is shown in the figure. 3. It is meant to create a capacitor between the circuit board and the human skin to pick up the weak signals that are generated by the human body. This capacitor and biasing resistance provides the very high input impedance to Dc voltages of instrumentation amplifier. It constitutes a filter with a high-pass characteristic. The overall capacitance of this sensor is determined using many parameters, such as area of the sensor, dielectric constant, and distance between the sensor and the skin etc.

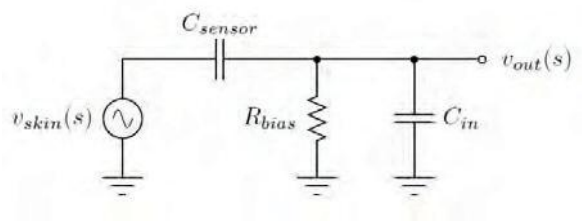

Figure 3. Small signal model of the capacitive sensor

The C_{in} is the input capacitance of the instrumentation amplifier. From this we can understand it is a simple high pass filter in nature. Here, the instrumentation amplifier input resistance is greater than the bias resistance, then the output is

$$V_{out}(s) = \frac{R\,bias \,||\frac{1}{sCin}}{\frac{1}{sCsensor}+(R\,bias\,||\frac{1}{sCin})}\quad V_{skin}(s)$$

After some algebra the transfer function H(s) is found as

$$H(s) = \frac{V\,out\,(s)}{V\,skin\,(s)} = \frac{C\,sensor}{C\,sensor+cin}\,\frac{s}{s+Wo}$$

$$W_o = \frac{1}{R\,bias\,(C\,sensor+C\,in)}$$

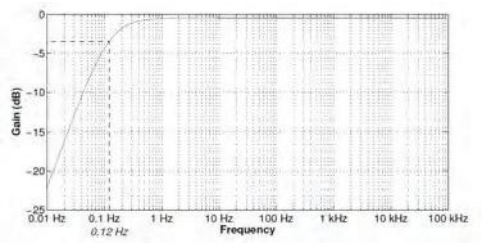

Figure 4. Transfer function of the filter at the input.

The cutoff frequency and high pass characteristics are given by the above equations. Another noticeable thing in the first equation is the constant loss of $\frac{C\,sensor}{C\,sensor+cin}$ in the pass band. The magnitude of the loss is depends on the capacitance value. If the capacitance drops to within one order of magnitude of the input capacitance, the loss will be more than 10 % of the amplitude.

The Figure 4 shows the frequency response of the filter with R_{bias} =10GΩ, C_{in} =7pF as per the amplifier datasheet [10] and C_{sensor} = 125 pF. In the above figure the -3 dB cutoff frequency is indicated with the dashed line and is 0.12 Hz.

A. Input Amplification Stage

The instrumentation amplifier (INA116) consists of three operational amplifiers as shown in Figure.5. The first two amplifiers provide gain to both the inputs. The gain is adjusted to suitable value by varying an external resistor R_G which is connected between the first two stages. The third operational amplifier acts as a difference amplifier, which amplifies the difference between these two amplified signals. A buffer is added for each input line of the instrumentation amplifier [7]. Those are considered for analysis, because they ideally will not alter the signals. The external feedback network is connected to the inverting terminal of the amplifier and input is applied for the non-inverting terminal of the amplifier. For the analysis of the instrumentation amplifier, the ideal op-amp characteristics are considered. Such as infinite gain, infinite input resistance and zero output resistance.

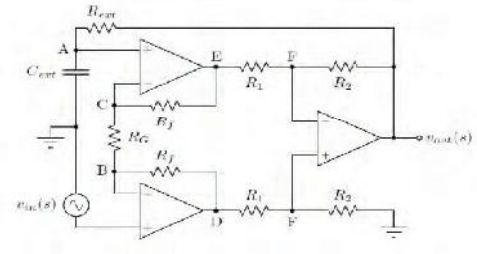

Figure 5. Small signal AC equivalent model of the instrumentation amplifier

The internal nodes A, B, C, D, E, FAND R1, R2, RF are marked out in the above equivalent circuit. The R_G and R_{ext}, C_{ext} are gain resistance and external feedback filter elements respectively as shown in the Figure. 5. The nodal equations with respect to above small signal model are:

At A node: $-V_a(s).sC_{ext} + \frac{V\,out\,(s)-V\,a\,(s)}{R\,ext} = 0,$

At B node: $\frac{V\,a\,(s)-V\,in\,(s)}{R\,G} + \frac{V\,d(s)-V\,in\,(s)}{R\,f} = 0,$

At C node: $\frac{V\,in\,(s)-Va\,(s)}{R\,G} + \frac{V\,e(s)-V\,a\,(s)}{R\,f} = 0,$

At F node: $\frac{V\,d(s)-V\,f\,(s)}{R\,1} - \frac{V\,f(s)-V\,in\,(s)}{R\,2} = 0,$

$$\frac{Ve\,(s)-V\,f\,(s)}{R\,1} + \frac{V\,out(s)-V\,f\,(s)}{R2} = 0,$$

The above equations can be rewritten as

$$V_a(s) = V_{out}(s).\frac{1}{1+s\,Rext\,Cext}$$

$$V_d(s) = \frac{Rf}{RG}(V_{in}(s) - V_a(s)) + V_{in}(s)$$

$$V_e(s) = -\frac{Rf}{RG}(V_{in}(s) - V_a(s)) + V_a(s)$$

$$V_{out}(s) = \frac{R2}{R1}(V_d(s) - V_e(s))$$

Figure. 6 represents the filter frequency response for the component values R= 20 k and C = 10 μF, the cutoff frequency is at 0.8 Hz.

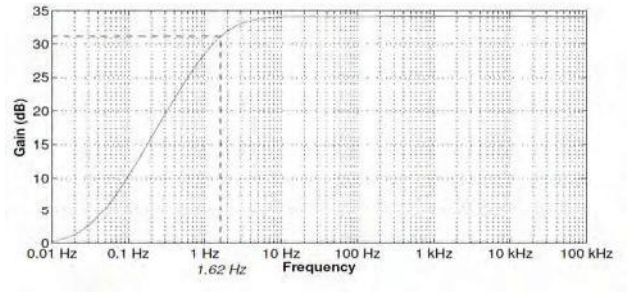

Figure 6. The frequency response of the input amplification stage.

B. Inter-stage Filter and Level Shifter

The inter stage filter is a simple passive HPF (high pass filter) but it working as a level shifter. The circuit shown in the figure 7 is used as level shifter circuit. This circuit brings the DC bias voltage to the middle of the Voltage rails VDD and GND of the second amplifier. That uses a single ended supply voltage.

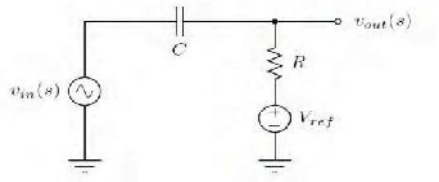

Figure 7. The AC equivalent mode of the inter stage high pass filter and level shifter.

In the DC analysis, the capacitors are open and nod V_{out} is floating. Then the output is equal to input DC voltage because no current in resistor. i.e. there isa level shift.

$$V_{out} = V_{ref}$$

For the AC equivalent model analysis, one of the condition with respect to DC voltage sources is short circuit. After shorting the Dc source the current in the circuit is given by

$$i_{out}(s) = \frac{Vin(s)}{R+\frac{1}{sc}}.$$

The o/p voltage then voltage drop in resistor due to i_{out} and is given by:

$$v_{out}(s) = \frac{sRC}{R+\frac{1}{sc}} . v_{in}(s)$$

The transfer function of the circuit is given as

$$H(s) = \frac{V\ out\ (s)}{V\ in\ (s)} = \frac{s}{s+Wo} \qquad \text{where} \quad w_o = \frac{1}{RC}$$

The above transfer function represents that the HPF with $w_o = \frac{1}{RC}$ as cut off frequency. The frequency response of this HPF is shown in the figure. 8. For this response the practical values are C=10µf and r=20KΩ and cut off frequency assumed as 0.8 Hz.

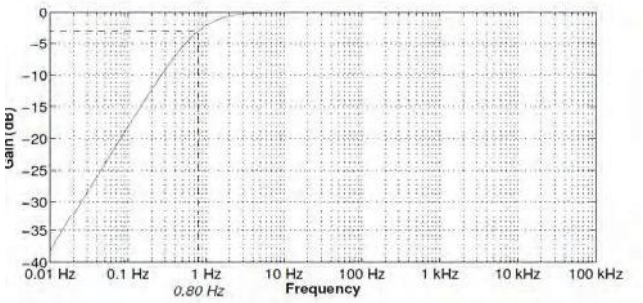

Figure 8. The frequency response of the inter stage HPF

C. Second Amplification Stage

The next stage is combination of amplification stage and band pass filter. This provides more gain and the selection of interesting frequency band using band pass filter. The filter is implemented using one active band pass filter and followed by passive low pass filter. The figure 9 represents filter circuit in the second stage of the read out circuit. The operational amplifier is considered as ideal amplifier with DC voltage as short circuit for the small signal AC analysis. Looking at Figure 9 we get the following nodal equations:

$$\text{Node A}: \frac{-V\ in(s)}{R+\frac{1}{sC1}} - \frac{V\ b(s) - V\ in\ (s)}{R\ 2 \| \frac{1}{sC2}} = 0,$$

$$\text{Node C}: \frac{V\ b(s) - V\ out\ (s)}{R\ 3} - v_{out}(s) .s\ C_3 = 0,$$

Solving the above equations for $v_b(s)$ and equating them gives the output voltage as

$$V\ out\ (s) = v\ in\ (s)\ (1 + \frac{R2 \| 1/sC2}{R1+1/sC1})\ . \frac{1}{1+sR3C3}$$

This results in the transfer function

$$H(s) = (1 + \frac{R2}{R1} . \frac{s}{s+w\ HP} . \frac{W\ LP1}{s+w\ LP1}) . \frac{W\ LP2}{s+w\ LP2}$$

Where

$$W_{HP} = \frac{1}{R1C1}\ , W_{LP1} = \frac{1}{R2C2}, W_{LP2} = \frac{1}{R2C2}$$

If $W_{LP1} \approx W_{LP2} >> W_{HP}$, this stage acts as a band-pass filter with a DC gain of 1 and a pass band gain of $1+\frac{R2}{R1}$.

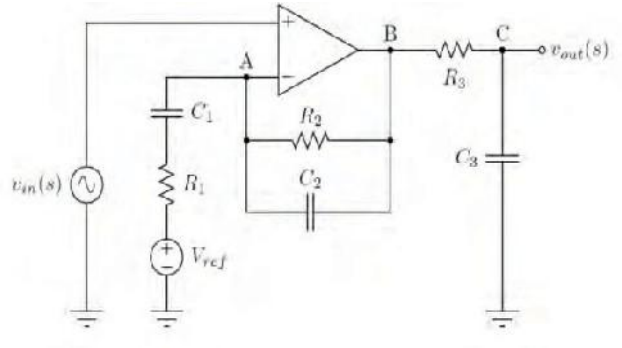

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Figure 9. Small signal model of the second amplification stage

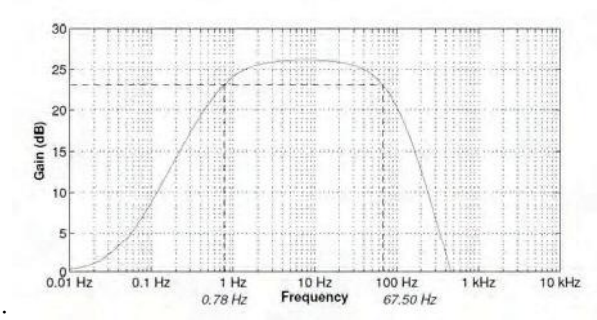

Figure 10. The second amplification stage frequency response.

The figure. 10 represents the frequency response of the second amplification stage with the following component values: $R1$ = 20 k $C1$ = 10 μF,$R2$ = 390 k $C2$ = 3.9 nF and $R3$ = 10.5 k $C3$ = 150 nF. The pass band of the filter in the figure is between 0.78 Hz and 67.5 Hz. The -3 dB cutoff frequencies are marked by the dashed lines and are 0.78 Hz and 67.50 Hz.

D. Notch Filter

The filter response and effectiveness depends on the quality factor Q value of the filter. The notch filter has to remove the selected sing frequency component. For this notch filter high Q value is required. The high quality factor filter working as is very narrow band notch filter.

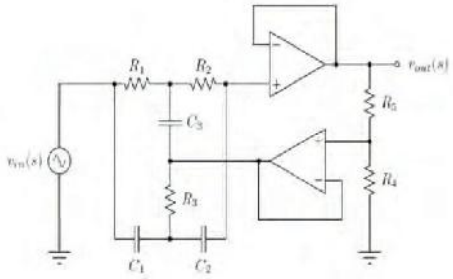

Figure 11. Circuit diagram of an active twin-T notch filter circuit.

The figure11 represents the notch filter circuit. It consists of an active filter with common passive twin-T notch filter. The Q value 14 is considered for original filter, the further Q value is much improved by active feedback. This type of circuit can be easily implemented by few elements and this circuit also makes Q quite sensitive for matching the components. The matching problem is eliminated by this notch filter.

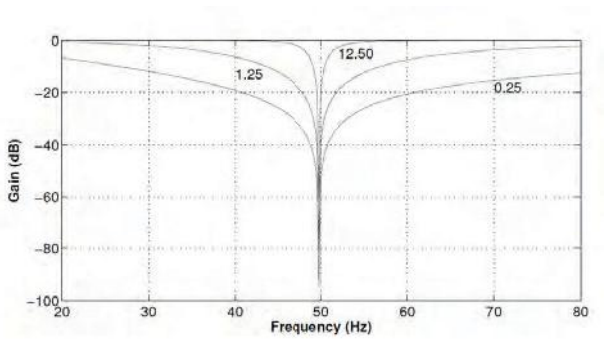

Figure 12. The notch filter Transfer function for different Q values.

IV. Results

The Figure 13 shows the complete frequency response of the system. This is achieved by combining or multiplying all the individual frequency responses of the sub blocks in the entire readout system. The another response also taken of all sub blocks are included to the total response except frequency response of the notch filter is presented in the Figure 14.

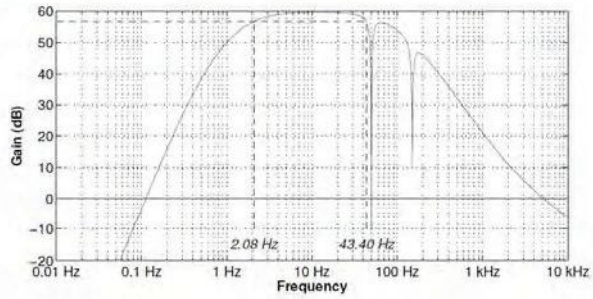

Figure 13.The complete Frequency response of the readout circuit including notch filters

The comparison between the figure 14 and figure 15 reveals that the without notch filters the frequency response is normal. The notch filter response limits the notch at 50 Hz and in the upper bound on the bandwidth. i.e 69.2 Hz to 43.4 Hz. This not considered as the big issue in the ECG and EEG measurements, because the most of the power is concentrated below the 40 Hz frequencies.

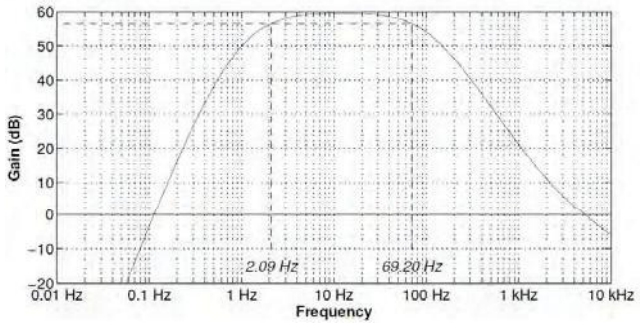

Figure 14. The Frequency response of the complete readout system without notch filters.

V. Conclusions

The low level, low frequency EEG and ECG signals are measured using a non-contact type readout circuit with simple PCB sensor. In this system implementation two major issues are, i) The high value of input resistor is required for the sensing low frequency signals; ii) the sensor amplifies the more noise generated from the main power lines.

The capacitive sensor is implemented using a PCB metal layer as one plate and the skin of the patient is considered as another plate for the capacitor. The air and solder masks are treated as isolation dielectric insulating material, which is placed between the capacitor plates. Due to the size complexity, the two PCBs are implemented and placed on one top to another. Then the overall size of the readout circuit is approximately 25 X25mm.

In the read-out circuit, the first stage is instrumentation amplifier which provided the gain of 50. The sensor input capacitance and the input bias resistance of instrumentation amplifier are very high to pass the low frequency signals sought to be measured. The second stage is a combination of amplifier with gain 20 and band-pass filter. To reduce the

unwanted interfering signal or noise one additional filter is required at some frequencies. This filter is inserted in the place between the two PCB circuits.

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Abstract: **In recent years, the amount of Semantic data on the Web has increased enormously. Since the initiation of the Linked Open Data project, the number of datasets added to the Web of Data has increased multifold. Although, the concept of Web of Data has been increasing in popularity, ease-to-use interfaces, to access and make sense of actual data are still far and few to accomplish the Semantic Web Vision to its full potential. Especially the non-experts in Semantic Web technologies are not benefitting from the value of Linked Data as promised by the Data providers. In this survey paper, we discuss the major prerequisites and challenges that need to be addressed by the modern Linked Data Visualization tools. In the pretext of these challenges, we present how the State-of-the-art Visualization tools from Web of Data literature, attempt to handle them. Finally, we survey and present the features of different systems developed by Semantic Web community in the context of Linked Open Data.**

***Index Terms*—Semantic Web, Linked Open Data, Visualization tools, Exploration, Visualization**

I. INTRODUCTION

"The term 'Linked Data' refers to a set of best practices, introduced by Tim Berners-lee, for publishing and interlinking structured data on the Web, popularly called Linked Data principles [1]". Linked Data principles put forth by Semantic community has encouraged data providers to publish the data in structured format (machine-readable format), enabling sharing and exchanging of information. This ongoing effort from Semantic Web Community to link the different datasets, across different domains, has led to the formation of Linked Open Data Cloud (also known as Web of Data). Figure 1 denotes the current state of 'Web of Data'. Each node in this cloud diagram represents a distinct data set published as Linked data, as of January 2017. Each arc indicates the existence of link between entities in the two connected data sets. In recent years, the amount of Semantic data published on the Web has increased significantly. "Linked Open Data (LOD) is a pragmatic approach of realizing the Semantic Web vision of making the Web, a global, distributed data space called *–the Web of Data"*[2]. Today, the Linked Data paradigm has emerged as a potential enabler for shift of current Web of documents to Web of interlinked Data.

Resources on the 'Web of Data' are identified using Uniform Resource Identifiers (URIs), which are unique on the Web. Today, this global data space (Web of Linked Data) contains billions of triples and interlinks hundreds of datasets. Most of these datasets provide SPARQL endpoints for querying the datasets. In order to exploit the full value of information on the 'Web of Data', as many users as possible, with diverse background and skills need to be benefitted, not just the Semantic Web users.

However, with the growing amount of structured data, it has become a difficult task for the lay users (with little or no knowledge of the Semantic Web technologies) to access, review and explore the datasets of their interest on the 'Web of Data'. While the Linked Data is aimed at targeting machine processing agents, human agents ultimately need easy-to-interface tools to navigate and query datasets for consumption. However, there are considerable challenges in designing the browsers and Visualization tools for browsing, exploring and navigating linked data, as the requirements for browsing 'Web of Data' are different from browsing the Web of documents.

The remaining portion of the paper is structured as follows. In section 2, motivating facts to embrace the benefits of Linked Data are provided. In section 3, the challenges identified for designing the modern visualization and analysis tools that support easy navigation and exploration of Linked Data are presented. In section 4, the abstract Linked Data Visualization Model and its workflow are presented. In section 5, the existing tools are surveyed and their features are presented. In section 6, the comparative features under each category are presented. Finally, the paper is concluded with future direction of research.

II. MOTIVATION

"The Linked Data paradigm has emerged as a powerful promoter for publishing, enriching, and sharing data, information and knowledge on the Web [3]". Today, a vast variety of the application domains spanning commerce, entertainment, research, bioinformatics, tourism and society in particular are getting benefitted by Linked Data exploration and analysis.

The result of this effort is the creation of the Linked Open Data Cloud, which is a huge repository containing more than 35 billions of RDF triples and interlinks datasets, having around 504 million links [3]. Despite having such an impressive wealth of semantically enriched data, Web of Data fails to reach more users, especially the non-expert users who do not have in-depth knowledge of Semantic Web technologies. Though SPARQL endpoints provide enormous flexibility regarding the querying of

Linked Data, there are several challenges posed, making the consumption of data difficult:

i. Data contained in Linked Data repository is usually accessible for users in Semantic Web technologies having expertise in RDF programming and writing SPARQL queries.
ii. At times, it is quite laborious task even for experienced users to write complex SPARQL queries for navigating and exploring unacquainted SPARQL endpoints.

To better enable the users to query, explore, navigate and analyze the Linked Data in user friendly manner, visualization tools need to address the aforementioned challenges which are surfaced due to the vast influx of structured data by organizations.

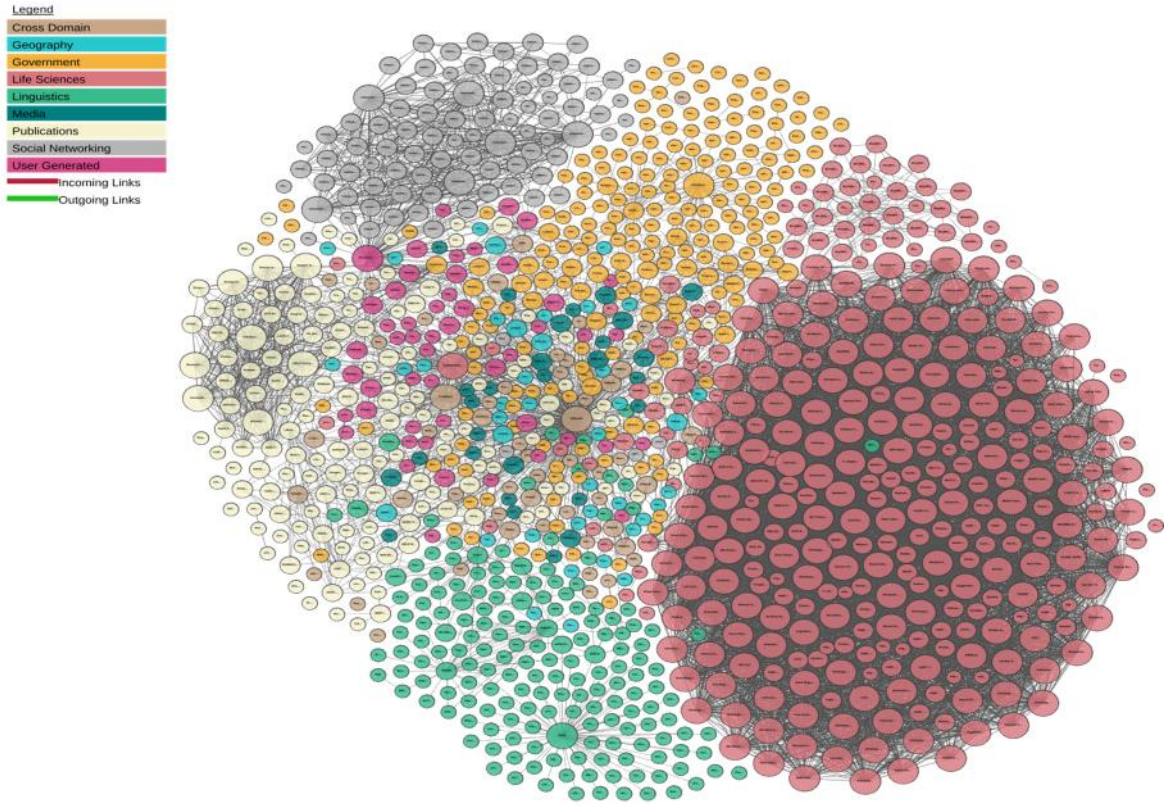

Figure 1. Linked Open Data Cloud [4]

III. Linked Data Visualization Challenges

The Domain of Linked Data poses some challenges in the context of Linked Data Visualization.

Scalability: Scalability issue is foreseen as the frontier challenge, especially when the datasets are large. The data of interest, for example the data returned from the SPARQL query on the dataset could be enormous. The Visualization techniques opted should address the scalability issue also while exploring the dataset.

Time scale: The Visualization tools also need to be efficient enough to render the information within an acceptable timeline. One way to tackle this issue is to support user interaction facility to the end-user.

Reusability: Linked Data Visualization and software applications used in developing them, should be reusable. Developing tools to implement maps and timelines involve lot of effort. Therefore reusability of tools plays a significant role in Linked Data Visualizations.

Heterogeneity of Information: The data of interest may be present in different repositories, say for example, a SPARQL query may involve more than one dataset. Integration of data and visualization, from multiple datasets, has to deal with the heterogeneity of information, semantics and schema format issues.

Multiple Datasets, Modeling the same concepts in different ways: Data accessed from multiple data repositories i.e., integrated heterogeneous data, may

surface the problem of modeling the concepts in different alternate ways.

Missing Data: Visualization techniques used should be able to handle the level of missing data and should indicate the user data that cannot be represented by the visualization tools.

Dadzie and Rowe [5], in their survey work, identified the major requirements for consuming and publishing the Linked Data. Their analysis follows the approach of Shneiderman [6], who broadly classified users into three types: Lay users, Technical users and Domain experts for which the visualization tools are meant.

IV. LINKED DATA VISUALIZATION MODEL

"Visualizing and interacting with Linked Data has been an issue that has been recognized from the beginning of the Semantic Web [2]". Adopting Information Visualization techniques in Semantic Web Applications can equip users with exploration and interaction capabilities and aid in better understanding of the data. Visualization models are useful for obtaining an overview of the datasets, their main types, properties and relationship between them. The Linked Data Visualization Model (LDVM) presented in [7], provides an abstract visualization process of Linked datasets. It allows user to connect different linked datasets with different visualization types in dynamic way. The model was adopted by many data Visualization tools in transforming structured data into graphical form.

The Visualization process follows a four stage workflow, originating with raw RDF data and ending with the Visualization. Figure 2 presents a high level overview of the process.

1. **RDF Data**: The raw data, which adheres to RDF data model, e.g. instance data, vocabularies, ontologies, taxonomies.
2. **Analytical extraction:** Data extractions obtained from raw data, such as aggregate values.
3. **Visualization abstraction:** Information is processed using visualization techniques.
4. **View:** presentation of the results of the process in graphical representation, e.g. plot, Treemap, Timelines, and Maps etc.

While data is propagated through different stages, different transformation operators are applied. Data transformation, visual transformation and visual mapping transformation are three different operators applied correspondingly. An example scenario showing the visualization workflow involved in LDVM is shown in figure 3. The RDF data is fetched from the SPARQL endpoint posing the SPARQL query. LOD Visualization tool is the prototype of the Linked Data Visualization Model.

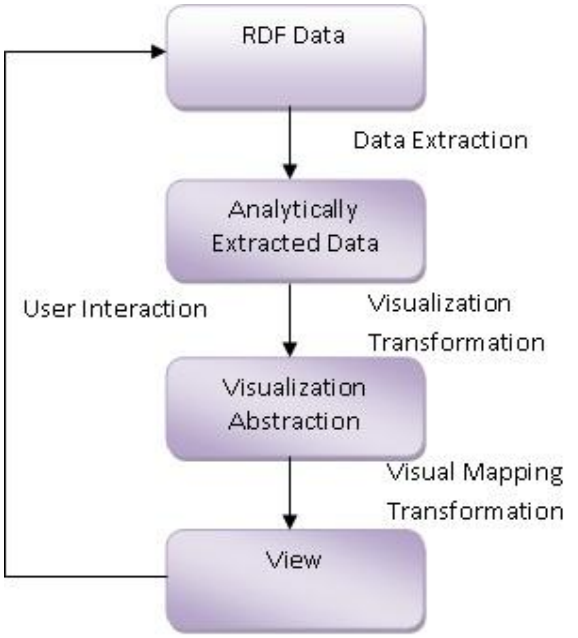

Figure 2. High level overview of the Linked Data Visualization Model

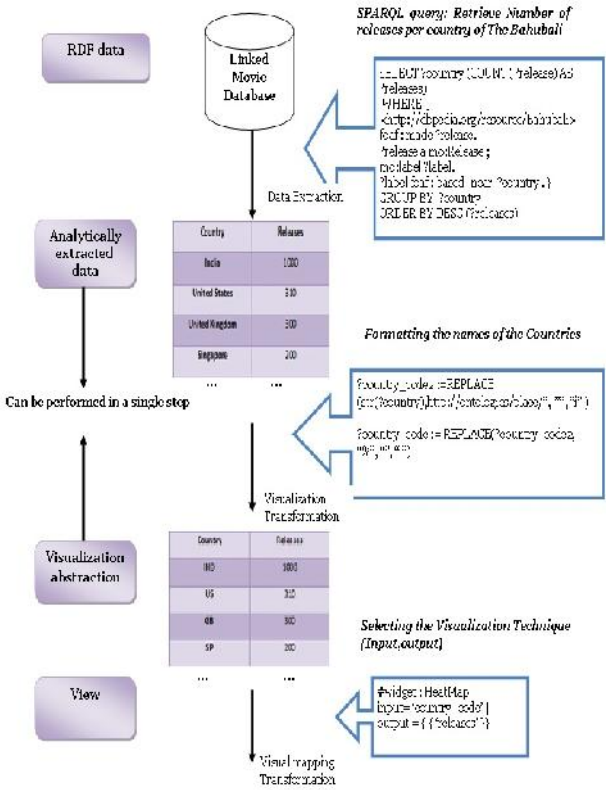

Figure 3. Example scenario showing the Visualization Workflow of the LDVM

V. LINKED DATA VISUALIZATION TOOLS

Linked Data is made available to users via the SPARQL endpoints or Data repositories (Data dump). In recent years there has been an increased amount of literature on Linked Data exploration and visualization tools, focusing on the features, benefits and their limitations.

In what follows, we categorize these works into following classes: (1) Linked Data browsers with text-based representations, (2) Generic Linked Data Visualization Systems, (3) Graph-based Linked Data Visualization systems, (4) Visualization Libraries and (5) Domain and Vocabulary specific Visualization Systems.

A. Linked Data browsers supporting text-based representation

These browsers use textual structures such as lists and tables to render the Linked Data entities, properties and relationship between them. Some of these browsers also provide faceted browsing to support intuitive rendering and navigation of data as surveyed in [8].

The *Disco* [9] is a hyper data browser that renders all the information present in RDF resource as HTML table with property-value pairs. It follows an approach of the traditional Web browsers to navigate the Linked data resources between RDF links and can be seen as a direct application of the hypertext navigation paradigm to the Web of Data. It supports navigation between Semantic Web resources by dereferencing HTTP URIs and by following the *rdfs:seeAlso* links.

Sig.ma [10] (**S**emantic **I**nformation **MA**shups) is a text based browser, which allows user to explore datasets by giving URI as input. It also supports simple free text search. *Sig.ma* is built on top of *Sindice* [11], a semantic search engine that allows user to search for resource description. A snapshot of *Sig.ma* linked Data browser is shown in figure 4. *Piggy Bank* [12] is a Web browser plug-in which converts the standard HTML content into Semantic Web content. It uses a series of customized screen scrapers to turn HTML into structured code.

URI Burner [13] is a service that retrieves structured data about Web resources by generating an RDF graph of the retrieved RDF data. It exploits the ontologies and background knowledge of the web resources, while retrieving the data.

Zitgist Data Viewer [14] is a RDF browser. This tool is a sort of information shape-filter, provides different shapes based on the data at hand, giving a better interface and browsing experience. *Marbles* [15] formats the RDF triples using the Fresnel Vocabulary (a Vocabulary that renders RDF resources as HTML). Also it supports the retrieval of information about a resource using the Semantic Web indexes and Search engines. *Dipper* [16] provides a public interface to retrieve and browse Linked Data resources from a set of repositories stored on the Talis platform and present the retrieved data in a human readable format.

Figure 4. Sig.ma Linked Data browser

B. Generic Linked Data Visualization Systems

In this section, we outline the best known generic visualization frameworks, which are offering a wide range of visualization types and operations.

The Linked Data Visualization Model (LDVM) is an abstract model for visualizing RDF data. A detailed discussion on LDVM is given in section 4. *Payola* [17, 18] is a generic framework for Linked Data visualization and analysis. It provides an elegant implementation of LDVM and offers a large number of domain specific visualization techniques and plug-ins to support the visualization of RDF based data. It was experimented on Czech LOD cloud for generating visualization. Payola tool provides a support for customizing the visualization by referring the ontologies defined for the resulting dataset.

Rhizomer [19] provides Semantic Data exploration using zooms and filter workflows. It also offers different types of visualizations such as maps, treemaps, timelines and charts. *VisBoard* [20, 21, 22] is an information visualization workbench for Linked Data that is build on mashup platform, presents the RDF data in dashboard-like interactive visualization.

SynopsViz [23, 24] is a Web-based visualization tool built on top of generic tree-based model. It supports multilevel exploration of data by performing hierarchical aggregation over large RDF datasets. *VisWizard* [25] is a Web based Visualization tool that exploits semantics of the underlying dataset to simplify the visualization process. It supports analysis of multiple datasets using brushing and linking methods. Similarly *LinkDaViz* [26] finds the appropriate visualization for the given part of a dataset. It facilitates the automatic binding between data and visualization options by employing the visualization model and performing heuristic data analysis. *LODWheel* [27] is a Web based visualization tool that enables the visualization of RDF data in graphical form by making use of the Java script libraries. *SemLens* [28] is a visualization tool that offers a visual discovery of correlations and patterns in data by combining the features of scatter plots and semantic lenses.

Comparative features of various Generic Linked Data visualization tools are well presented in table 1.

C. Graph based Linked Data Visualization Systems

These browsers use visual or graphics structures such as maps, timelines, images and graphs (individually or in combination) to represent Linked Data. We outline the best tools in this category.

DBpedia Mobile [29] is a location-centric DBpedia client application for mobile phone use. It allows user to query and access the real world entities such as cities, streets and landmarks that have described and asserted in DBpedia knowledge base, using his current location as input. It also allows users to access other resources linked from DBpedia. Based on the current GPS location of the mobile device, it renders a map indicating the locations of different objects nearby to user's current location, which are accessible from the DBpedia datasets.

IsaViz [30] is an interactive RDF browser and editor, allowing user to browse and edit RDF data as graph objects. It allows user to zoom, filter and navigate over the RDF graphs. It enables user to interact with RDF graphs, such as by clicking on a vertex node of the RDF graph, textual descriptions of the vertex is rendered. Features such as addition and deletion of RDF graph nodes and links is well supported by this application. In the same context *graphVizdb* [31, 32] is built on top of the spatial and database techniques, allows interactive visualizations over large RDF graphs. *RDF graph Visualizer* [33] employed a node-centric approach to visualize RDF graphs.

Open Link Data Explorer (ODE) [34] is a Web based RDF data browser, preferred mainly for performing search of RDF documents by taking resolvable URI or text string (for which it will attempt to match the resource URI) as input. It also supports extracting metadata from the RDF document. It provides a number of perspectives (or views) to facilitate user with more number of navigational features. *When, grid view, SVG graph, image, tag cloud* are some of the views. *RDF Gravity* [35] visualizes RDF and OWL data. It offers services like keyword search, filtering and manipulating the RDF graphs. It offers the user the flexibility to change the color of the nodes of the RDF graph. It also allows the user to visualize the ontologies. *Relfinder* [36] is a web based application, that supports discovery of graph covering relationships between two Linked Data objects of interest and visualizes them in a force-directed graph layout. It provides user interaction mechanism like previewing, filtering and highlighting the relationships found. *Tabulator* [37] is a RDF browser and editor. It supports browsing and exploring of RDF data. It allows RDF data providers to visualize, how their data interacts with the rest of the Semantic Web. Additionally it also provides Maps and Timelines visualizations.

Information Workbench [38] is a platform supporting the whole life cycle of Linked Data application development including integration, managing, analyzing and exploring the Linked Data. It is enriched with a large set of widgets supporting navigation, data authoring, data access, visualization as well as data mashups with different external linked data sources.

The main advantage offered by this tool is that the structure and behavior of user interfaces can be easily customized to build domain specific applications. Further the tool supports rich user interaction capabilities and provides a number of visualization techniques such a Google maps, timelines, pie charts, bar charts etc.

Code Linked Data Query wizard [39] provides a Web based interface to access, explore, filter and navigate Linked Data available through SPARQL endpoints. The main advantage offered by this tool is that it converts the Linked Data graph into tabular form and provides easy-to-use interaction possibilities to end user. *CODE Linked Data Vis Wizard* [40] enables a visual analysis of Linked Data and supports the user in automating the visualization process. Further the tool suggests visualization channels for the already analyzed data for representation. A snapshot of *CODE- Linked Data Vis Wizard* is shown in figure 5.

LODLive [41] and *Fenfire* [42] are exploratory tools that allow users to browse Linked Data resources using interactive graphs. Starting from a seed URL, the user can explore other resources using links. *LODLive* also allow users to have, live access to SPARQL endpoints. *LODVisualization* allows users to create visual hierarchies of data, fetched via SPARQL endpoint. Treemaps, maps and timelines are graph structures used in RDF visualization. Comparative features of various graph based Linked Data visualization systems are presented in table 2.

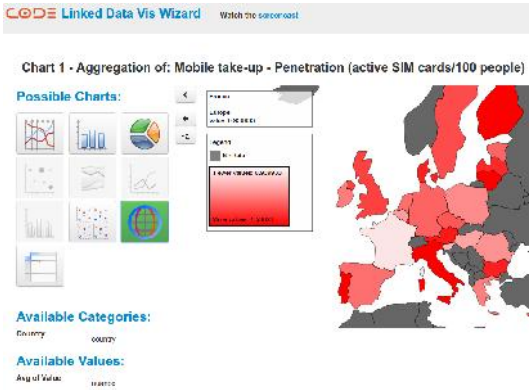

Figure 5. CODE Linked Data Vis Wizard

D. Visualization Libraries

Sgvizler [43] is a JavaScript library that allows SPARQL query results to be embedded in HTML elements. It uses Google Charts to offer numerous types of visualizations for SPARQL results such as graphs, charts, treemaps and timelines.

VisualBox [44] provides a novel interface for building and debugging SPARQL queries for retrieving Linked Data. It recommends visualization templates for visualizing results. It uses libraries like Google charts and D3 [45]. It offers nearly 14 various types of visualization.

TABLE I.
GENERIC LINKED DATA VISUALIZATION SYSTEMS

System	Data Types*	Vis.Types**	Visual Recomm#	Domain	Application Types	SPARQL Query support	Vis.Cust.***	Target users##
LDVM	S	H,B,M,T	✓	Generic	Web	✓	✓	L,T,E
VizBoard	N	H,S,C	✓	Generic	Web		✓	L
LODWheel	N,S	G,C,M,P		Generic	Web			T,E
Payola	N,T,S	H, G,T,TL,C,CI,M		Generic	Web	✓	✓	L,T,E
Rhizomer	N,T,S	H, G,C,M,T,TL	✓	Generic	Web			L,T,E
LinkDaViz	N,S,T	B,C,M,P,S	✓	Generic	Web			L,T,E
LDVizWiz	S	H, G,M,P	✓	Generic	Web	✓		L,E
SynopsViz	N,T	H,P,TL	✓	Generic	Web		✓	E
VisWizard	N,S,T	B,C,M,P,S	✓	Generic	Web		✓	E
SemLens	N	S		Generic	Web			E

*Data Types- N: Numeric, S: Spatial, T: Temporal;
**Vis.Types (Visualization Types) - CI: Circle, C: Chart, B: Bubble Chart, G: Graph, S: Scatter Plot, SG: Stream Graph, M: Map, T: Treemap, H: Hierarchical, TL: Timeline; #Visual Recomm- Visual Recommendation; ***VisCust- Visualization Customization;
##Target users- L: Lay Users, T: Technical Users, E: Domain Experts;

TABLE II.
GRAPH BASED LINKED DATA VISUALIZATION SYSTEMS

System	Keyword	Filter	Visualization type	Domain*	Application Type**	Detail on Demand
DBpedia Mobile	✓	✓	Graph	Generic	Web (Mobile)	✓
OpenLink Data Explorer	✓	✓	Graph, Grid view, Map View	Generic	Web	✓
IsaViz	✓	✓	Graph	Generic	Desktop	✓
Fenfire			Graph	Generic	Desktop	✓
RelFinder	✓		Graph	Generic	Web	✓
ZoomRDF			Graph	Generic	Desktop	✓
LODlive	✓		Graph	Generic	Web	✓
graphVizdb	✓	✓	Graph	Generic	Web	✓
RDF Graph Visualizer	✓		Graph	Generic	Desktop	✓
RDF-Gravity	✓	✓	Graph	Generic	Desktop	✓
Tabulator	✓		Map, Timelines	Generic	Web	✓

*Domain- Generic / ontology/ specific domain; **Application type – Web based / Desktop

E. Domain and Vocabulary specific Visualization Systems

These systems provide visualizations according to the types of data, domains and RDF vocabularies of the data at hand.
In literature there are several systems focusing on exploration and visualization of geo-spatial linked data. *Map4rdf* [46] is a faceted browsing tool that enables the visualization of the RDF datasets using Google maps. The *LinkedGeoData* browser [47] is a faceted browser and editor used for manipulating and visualizing linked geo data. *DBpedia Atlas* [48] also offers exploration over the DBpedia dataset by making use of the dataset's spatial data. *SexTant* [49] and *SpaceTime* [50] are tools that focus on exploration and visualization of time-related geo-spatial data.
VISUalization Playground [51] is an interactive tool for exploring and visualizing Linked University data. It offers a novel SPARQL interface for querying the data and uses Google charts for visualizing the query results. *CubeViz* [52] and *OpenCube Toolkit* [53] are tools used for exploring and visualizing statistical Linked data. The Open Cube Map view (part of *Open Cube Toolkit*) offers map based visualizations of RDF data cubes based on their geo-spatial dimensions.

VI. Discussion

In this section, we highlight the relative capabilities of the Linked Data tools with regard to the handling, exploration and visualization of different types of data in a qualitative way, catering to all categories of users.

Our reviews regarding text–based browsers found that these browsers are unbound to RDF visualizations and provide only HTML representation of RDF Data. However, some degree of detailed exploration of the data at hand is supported by almost all the text-based browsers. In comparison to the remaining text-based browsers under review, *Marbles* additionally supports the feature of highlighting of links across selected data, adopting visual paradigm. It showcases the color marbles to differentiate among data sources under view.

Other browsers like *URI Burner*, *Disco* and *Zitgist* presents the RDF data in the form of "Entity-attribute-value" pairs. We conclude that the text description does not provide a good level of support for generation of overviews, compared to visual clues. It is evident from table 1, that generic linked data visualization systems support several of data types (e.g., numeric, spatial, temporal, graph) and supports a plethora of visualization features. Additionally some systems such as *LinkDaViz*, *LDVM*, *VizWizard*, *VisBoard* and *SynopsViz* support recommendation mechanisms also. Particularly, these systems mainly recommend the most suitable visualization types considering the selected data. Though SynopsViz offers five types of charts, timelines and treemaps for visualization of data, it has intricate interface that is not so user-friendly for lay users to interact with it. Systems like *Payola*, *LDVizWiz* benefits all type of users (lay, technical and domain experts) in exploring and visualizing the linked data.

An overview of the main features of Graph-based Linked Data Visualization Systems is presented in Table 2. When compared to other visualization tools, this group of tools provides more user interaction capabilities. They support various types of graph structures, visual sharing, visual recommendations, and visual customizations in addition to providing access for SPARQL queries.

Map4rdf, *DBpedia Atlas* and *LinkedGeoData* are domain specific faceted browsers, supporting manipulation and visualization of geo-spatial linked data. *SexTant* and *Spacetime* focus on visualizing time-evolving geo-spatial linked data. *CubeViz* and *OpenCube Toolkit* are tools dedicated for visualizing and exploring statistical linked data.

Sgvizler and *Visualbox* expect user to have knowledge on SPARQL language to retrieve and visualize the data in HTML pages.

VII. Conclusions

In order to realize the Semantic Web vision, many communities under the realm of World Wide Web are advocating the use of RDF data and Linked data as standard formats for publishing the data on the Web. This has provided an easy path for integration and sharing of heterogeneous data on the Web. However, the rising popularity of Linked Data is posing new challenges, related to visualization and exploration of Linked data.

Several ongoing research efforts have offered a wide range of tools for exploration and visualization of linked data. The paper surveys the most common Linked Data Visualization tools proposed in the literature. The main aim of this work is to present the different features provided by various tools in literature, related to user interaction, in particular those features which benefit the lay-users and technical users, in exploring and consuming the Linked Data.
Finally, considering users' perspectives, beyond visualization recommendations, modern Linked data tools should employ smart techniques that capture users' preferences and assist them throughout exploration and analysis tasks.

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A Classification of MapReduce Schedulers in Heterogeneous Environments

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***Abstract*—MapReduce is an essential framework for distributed storage and parallel processing for large-scale data-intensive jobs proposed in recent times. Intelligent scheduling decisions can potentially help in significantly minimizing the overall runtime of jobs. Hadoop default scheduler assumes a homogeneous environment. This assumption of homogeneity does not work at all times in practice and limits the MapReduce performance. In heterogeneous environments, the job completion times do not synchronize. Data locality is essentially moving computation closer (faster access) to the input data. Fundamentally, MapReduce does not always look into the heterogeneity from a data locality perspective. Improving data locality for MapReduce framework is an important issue to improve the performance of large-scale Hadoop clusters.**

This paper primarily provides an overview of the evaluation of Hadoop and introduces the MapReduce framework in detail. This paper also describes some relevant literature work on some recent developments in MapReduce scheduling algorithms in heterogeneous environments.

***Index Terms* -Hadoop, MapReduce, Job Scheduler, JobTracker, TaskTracker and Heterogeneous Environments.**

I. Introduction

The era of distributed and parallel computing had begun in the mid 1960s. During that period, to increase the computational speed, parallel processors were introduced. Later, Ethernet came into the picture that would transform the way data was distributed in a network with nodes working as processors of the parallel machine [1]. As the sequential architectures could not enhance the performance, there was a need for parallel and distributed architectures. In addition to this, the cost of hardware was also to be considered. Usually, it is better to introduce much cheaper parallel-working processors/multiple single-processor connected systems than making a single processor faster.

Nowadays, distributed systems replaced supercomputers as they are cheaper and became better alternatives for faster processing. A distributed system is a collection of multiple, single or multi-core, computers connected to a network that shares data and processing power to solve a given task effectively and efficiently. The motto of the distributed system is that the completion of the task becomes faster if it is shared among multiple processors than a single processor. It is important to observe that a distributed system can complete a task by executing it in the parallel fashion which is not possible with a single processor system [2].

MapReduce is now one of the most popular computational frameworks for large-scale data processing and analysis for parallel and distributed computing systems. MapReduce schedulers perform task assignment to available resources in the cluster. The common goal of MapReduce scheduling is to minimize the overall completion time of a job by appropriately assigning tasks to the available nodes [3].

The rest of this paper is structured as follows. Overview of Hadoop framework is presented in Section II. Section III presents a classification of MapReduce schedulers in heterogeneous environments. Different MapReduce scheduling problems are presented in Section IV. Finally, conclude the paper in Section V.

II. Overview of Hadoop Framework

Big Data depends very much on the capabilities of the systems for storage and processing. Traditional systems like Relational Database are not designed to handle smooth processing of Big Data [4]. In particular, the challenges of big data are those of processing and capturing of unstructured data. It is said many issues exist related to problems associated with sharing, transferring, analyzing, and visualizing of big data [5]. In traditional database systems, data is structured and is stored in tables with fixed number of columns. Each column has the particular data type. However, Big Data have a variety of data formats like audio, video, and text that does not fit in the table sizes.

Data-intensive applications are the ones that can process big data to get useful data [5]. To conduct the activities of data-intensive applications in parallel, requests devoting their time in the movement and manipulation of data are to be made. Movement of data involves the flow of data between two different nodes of a network for further processing.

However, as there is a lot of unstructured data growth, there is much demand for new processing frameworks to deal with it. For this purpose, several solutions emerge, including MapReduce. MapReduce is a framework for large-scale data processing developed by Jeffrey Dean and Sanjay Ghemawat [6] at Google. Now, it is one of the most popular frameworks for large-scale data processing and analysis.

Google trends show an increasing trend for the search term Hadoop worldwide [7]. The growing trend of Hadoop is caused by companies adopting this technology into their technology stack. Companies are now migrating towards Hadoop technology (eco-system) as it provides an easy and straightforward approach to access the data and to get the "Value" from Big Data.

In particular, the MapReduce framework [8] made a significant impact by demonstrating a simple, flexible and generic way of storing and processing large distributed datasets. MapReduce programs are written in a particular functional style and may be executed within a framework that automatically enables distributed and highly parallel execution. MapReduce was quickly embraced as a new paradigm for data-intensive computing and widely adopted by other companies working with web-scale data sets. For example, Hadoop is currently used by major companies such as Amazon, eBay, Facebook, Twitter, Yahoo! and many others [10].

A. Hadoop

The importance of Hadoop is due to its large scale adoption in clusters with commodity systems. Use of Hadoop has spread from large corporations with expensive server farms to small business and academia for research and other data processing tasks. It also indicates a shift from homogeneous to heterogeneous computing environments that are small or medium scale and thrifty.

Figure 1 depicts the general Hadoop cluster. It is composed of nodes, racks, and switches. All nodes in a rack are connected to a rack switch, and all rack-switches are then connected via bandwidth links to the core switch. There are two branches of Hadoop releases, i.e. Hadoop1 and Hadoop2. Hadoop1 is the most famous for batch processing and shows the potential value of Big Data distributed processing. Hadoop2 or YARN (Yet Another Resource Negotiator) [11] provides a unified resource management framework for different data processing platforms. Similar to the original Hadoop framework, the YARN framework also has a centralized manager node running the Resource Manager (RM) daemon and multiple distributed working nodes running the Node Manager (NM) daemons.

However, there are two main differences between the design of YARN and original Hadoop. First, the Resource Manager (RM) in YARN no longer monitors and coordinates job execution as the *JobTracker* of traditional Hadoop do. An Application Master (AM) is generated for each application in YARN, which generates resource requests, negotiates resources from the scheduler of RM and works with the Node Managers to execute and to monitor the similar application tasks.

The Hadoop1 framework contains two components [12]: 1. HDFS (Hadoop Distributed File System), which stores the input data 2. MapReduce engine, which processes the data blocks stored in different nodes of a cluster. HDFS contains a *NameNode* and *DataNodes* in a cluster. *NameNode* is a master node which contains the meta-data information of the data

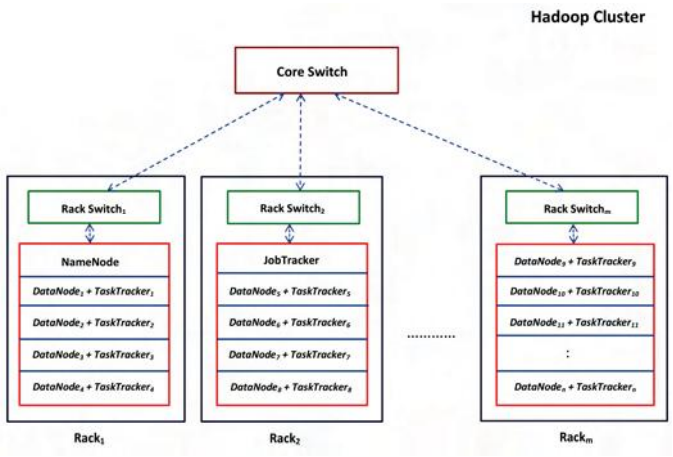

Figure 1. A simplified schematic of a general Hadoop cluster [9]

block locations in a cluster. *DataNodes* are slave nodes, which store the data blocks within a cluster. MapReduce contains a *JobTracker* and multiple *TaskTrackers*. *JobTracker* deals with job scheduling and assigns tasks to *TaskTrackers* within a cluster depending on the slot availability. *TaskTrackers* process the *map* and *reduce* tasks on the corresponding nodes in the cluster.

B. MapReduce

MapReduce framework was inspired from the functional programming languages [14]. The input and output data have a particular format of (*key*, *value*) pairs. The Users define an application using two functions: the *Map* function and the *Reduce* function. The *Map* function repeats over a set of the input (*key*, *value*) pairs and produces intermediate output (*key*, *value*) pairs. The MapReduce library groups all *intermediate values* by *key* and gives them to the *Reduce* function. The *Reduce* function iterates over the *intermediate values* associated with the same *key*. Then it produces zero or more output (*key*, *value*) pairs.

MapReduce framework is most widely used across the industry and academia. It has been in practice in many domains of data-intensive applications such as web data mining, machine learning, health care data analysis, and scientific simulation. MapReduce is highly scalable and enables thousands of commodity computers to be used as an efficient computing platform. The framework detects and handles node failures automatically without allowing the overall execution process to be affected.

MapReduce framework follows a simple master-slave architecture, where *JobTracker* is the master node and *TaskTrackers* are the slave nodes. The *JobTracker* handles scheduling decisions for the MapReduce jobs. The *JobTracker* in Hadoop is designed in such a way that the schedulers can be pluggable in and out. The *JobTracker* and *TaskTrackers* communicate with each other through heartbeat messages. Through these messages, the *TaskTracker* indicates to the *JobTracker* that it is alive. As a part of the heartbeat message, the *TaskTracker*

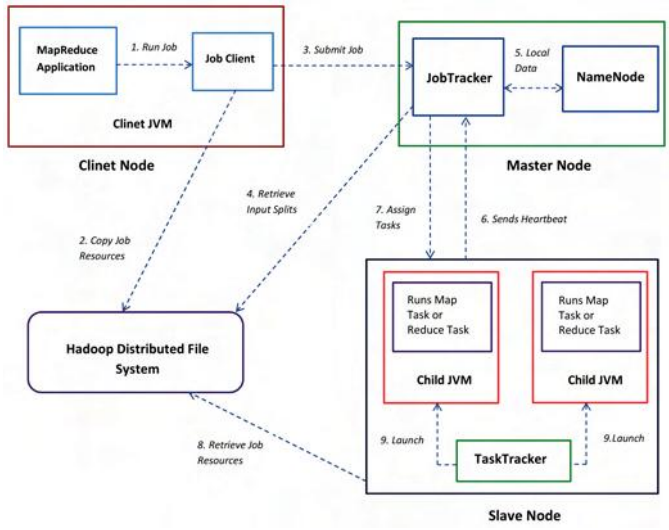

Figure 2. Hadoop MapReduce workflow [13]

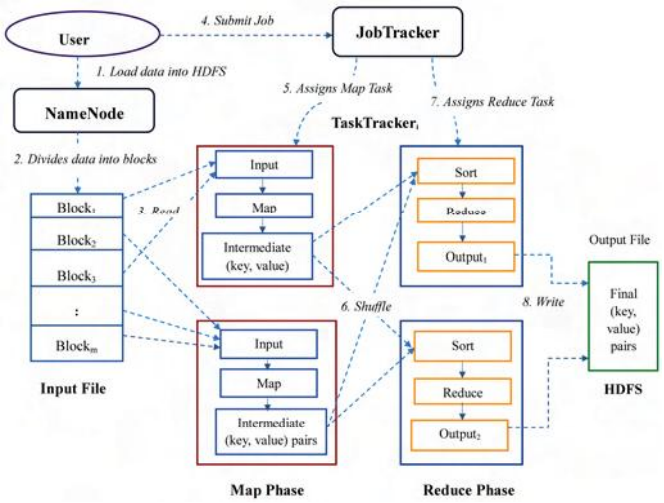

Figure 3. MapReduce Jobflow [15]

also indicate whether it is ready to accept a new task and other related information. The client application submits jobs to the *JobTracker*. The *JobTracker* communicates to *NameNode* to find the data location. The *JobTracker* then creates a *map* task for each data block. These tasks are queued up in the *JobTracker* as per the scheduling algorithm. Whenever the *TaskTracker* requests for a task, the *JobTracker* submits a task to it as a return value. The *TaskTracker* launches each task in a new Java Virtual Machine. A *TaskTracker* can run multiple tasks at an instant which can be configured through the configuration parameters. Once all the job tasks are finished execution, then the output is stored back in HDFS.

We broadly describe MapReduce workflow as shown in Figure 2 with the following sequence of steps.

1) The client submits the MapReduce job to the *JobClient*.
2) The *JobClient* copies the information regarding the job resources to HDFS.
3) The *JobClinet* internally submits the job to the *JobTracker*.
4) The *JobTracker* retrieves corresponding input data blocks of the job.
5) The *JobTracker* interacts with the *NameNode* for metadata information of the input data.
6) The *TaskTracker* periodically sends the heartbeat information regarding the availability of slots and task progress to the *JobTracker*.
7) The *JobTracker* assigns tasks to the *TaskTrackers*.
8) The *TaskTracker* retrieves job resources from the HDFS.
9) Finally, *TaskTracker* launches the child JVM, and it executes the *map* or *reduce* task.

MapReduce contains the following stages [15] when scheduling a job from the master node to the slave nodes as shown in Figure 3.

1) User submits input data to the *NameNode*
2) The *NameNode* divides the data into m blocks of the same size. r copies (replicas) of every block are produced for fault tolerance. (r is the replication factor).
3) The master node picks up the idle slave nodes to schedule map and $reduce$ tasks.
4) User submits a job to the *JobTracker* for processing corresponding data blocks.
5) A slave node that is executing a map task parses the data block and assigns each (key, $value$) pair to the Map function. The intermediate (key, $value$) pairs are buffered in memory at corresponding nodes.
6) The buffered (key, $value$) pairs are written to the data residing nodes at fixed intervals and divided into R sections by means of a (configurable) partition function (default is *hash (intermediate key) mod R)*. The identical (key, $value$) pairs go to the same partition. When the task completes, the slave node sends the location information of partition to the master node.
7) The node which contains $Reducer$ function reads the data using remote procedure calls. It sorts and groups the data by *intermediate key* so that all values of the same key are grouped. It is called shuffling of the task.
8) The master node produces the final output after execution of all map and $reduce$ tasks.

In the MapReduce framework, the job execution process has two phases, namely, a *Map* phase and a *Reduce* phase. The *Map* phase assigns each *map* task to a block of the input data. The number of data blocks determines the number of *map* tasks. Execution of a *map* task consists of the following steps [16]:

1) The task's slice is read and organized into records (*key, value*) pairs, and the *Map* function are applied to each block.
2) After the *Map* function's completion, the *commit* phase registers the final output with the *TaskTracker*, which

notifies the *JobTracker* about the task's completion.

3) The Output Collector stores the *Map* output in *Intermediate keys*
4) The Output Collector 'spills' this information to the disks. A spill of the in-memory buffer contains sorted records; first by partition number, and second by (*key, value*) pairs. The buffer information is written to a local file system as a data file and an index file.
5) In the commit phase, the final output of a *map* task is produced by integrating all the split files created by this *map* task into a single pair of data and index files.

These files are recorded with the *TaskTracker* before the task is completed. *TaskTracker* reads these files to service requests from *reduce* tasks.

Reduce phase contains following three stages: shuffle, sort, and reduce.

1) In the *shuffle* stage, the intermediate output produced by the *Map* phase is collected. Every *reduce* task is allotted a part of the intermediate output with a static *key* range.
2) In the *sort* stage, output with the same *key* are grouped together to be processed by the *reduce* stage.
3) In the *reduce* stage, the user-defined *Reduce* function is applied to every *key* and corresponding list of *values*.

III. Scheduling Algorithms for Hadoop MapReduce

We present a mathematical model to describe general scheduling problems in a Distributed Environment.

Let $M = \{M_1, M_2, ..., M_m\}$ be the set of machines or computer nodes which have to process n jobs represented by the set $J = \{J_1, J_2, ..., J_n\}$. A job J_i usually consists of several tasks $T_1, T_2, ..., T_k$. Each task T_i consists of n_i operations $O_{i1}, O_{i2}, ..., O_{in}$. To every O_{ij} a process requirement p_{ij} is associated. Each operation O_{ij} is associated with a set of parallel machines M_{ij}.

The goal is to design a scheduler, which is responsible for making decisions to execute a task at some time and on some machine. The most common objective of scheduling is to reduce the completion time of a parallel application by properly assigning the tasks to the processors. Inappropriate scheduling of tasks would fail to exploit the true potential of the system [17].

The MapReduce task scheduling is an NP-Hard problem [19] as it needs to achieve a balance between the job performance, data locality, user fairness or priority, resource utilization, network congestion, and reliability. If the scheduling policy considers data locality for selecting a task, it may have to compromise on the fairness as the node available may have data of some job, which is not on head-of-line as per the fairness policy. Similarly, if a task is scheduled based on job's priority, it is not necessary that it would have local data on the available node. It would impact job performance and network utilization. Some data centers or users want to achieve higher performance; some want high data locality, some want to improve resource utilization and so on. The scheduling policies need to be designed differently for achieving different objectives in different scenarios.

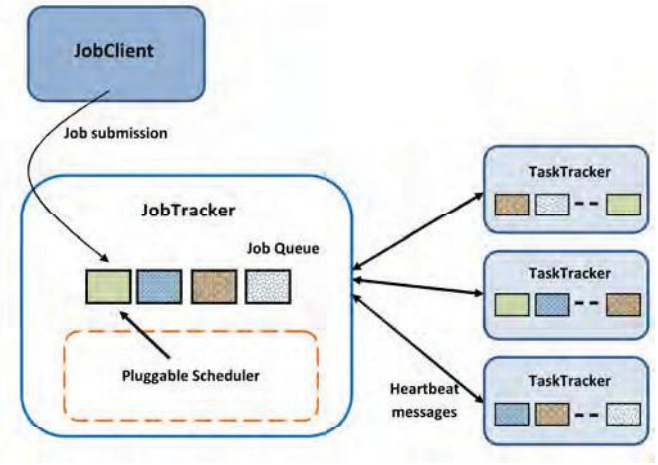

Figure 4. Adding pluggable scheduler [19]

The demand for scheduling adaptation in MapReduce comes from following points: the heterogeneity of cluster nodes, the data locality-awareness, and the diversity of job execution times. Job scheduling or task scheduling in the MapReduce is employed to manage workload efficiently between the computing nodes and effectively share the resources of a Hadoop cluster among various jobs and nodes [18]. The performance of the Hadoop framework can be affected by the imbalance workload distribution and partial resources sharing because of not having a sophisticated scheduling mechanism.

At each heartbeat, the *TaskTracker* notifies the *JobTracker* the number of available slots it currently has. MapReduce slots define the maximum number of *map* and *reduce* tasks that can run in parallel on a cluster node. The number of slots depends on the number of cores on that node. The *JobTracker* assigns tasks depending on job's priority, the number of non-running tasks and potentially other criteria. Since bug report Hadoop-3412, Hadoop has been modified to accept pluggable schedulers as shown in Figure 4 that allows the use of new scheduling algorithms to help optimize jobs with different specific characteristics.

A. Taxonomy for MapReduce Scheduling Algorithms

A significant characteristic of scheduling algorithms is their runtime performance. It means just how schedulers adapt to the heterogeneous cluster. Schedulers can run in a static (non-adaptive) or dynamic (adaptive) environments at runtime [9]. The dynamic nature of MapReduce framework is centered on several things, like resource, data, workload, and the job. We categorize the scheduling algorithms into adaptive and non-adaptive based on their runtime flexibility. The classification of MapReduce schedulers is as shown in Figure 5.

In **Non-adaptive** algorithms, scheduling, order for users,

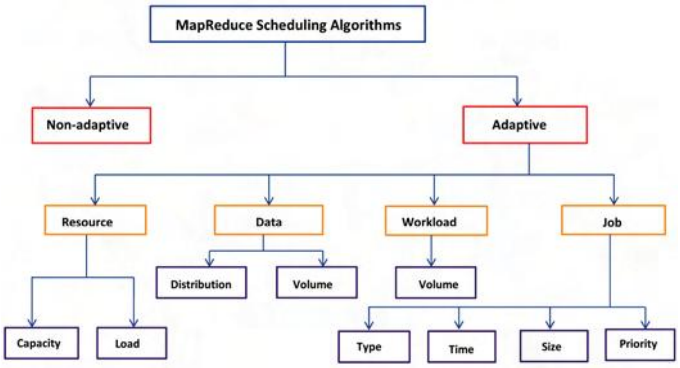

Figure 5. Taxonomy for MapReduce scheduling algorithms

jobs and tasks are static at runtime based on predefined policies. For example, The Hadoop first-in-first-out and priority-based schedulers practice predefined policies for scheduling jobs or tasks in order.

In a MapReduce system, the features of the data, physical resources, and workload vary at runtime. An **Adaptive** scheduling algorithm assigns a task to a node based on the availability, capacity, and load on nodes in the cluster at runtime. It may additionally choose an ideal task assignment approach predicated on the dynamic arrival attributes of the workload. We further categorize the algorithms based on the runtime features of the MapReduce framework.

1) Resource-Adaptive: The resources existing in a Hadoop cluster have distinct features. A CPU resource can be categorized by its processing speed, network bandwidth, and a system can be considered by grouping its CPU speed, RAM, and disk storage capacity. An additional essential characteristic of a resource is the processing load. Processing load of a resource is used to decide the available capacity of the resource. Some of the schedulers execute tasks based on the nodes according to their speeds to guarantee fast execution and approximately based on the existing capacity to avoid resource conflicts.

a) Resource Capacity: The capacity of a system contains the resources like the size of RAM, the number of CPUs, and disk capacity along with their processing speed. The systems used in heterogeneous clusters may have a varied capacity of these resources. Therefore, a scheduler has to reflect this while launching different kinds of tasks on them.

b) Resource Load: Overloading of systems usually has consequences of longer execution times and failures as a result of resource conflicts. Overloading moreover raises the temperature of the system and consumption of power. Therefore, schedulers have to adapt to decrease overloading and avoid resource skewness.

2) Data-Adaptive : To minimize the data transfers delays and network conflicts, a scheduler has to perform a significant part in getting the execution of a task nearer to the data residing node. Therefore, while scheduling tasks, a scheduler is necessary to be responsive to the data location and the data volume.

a) Data Distribution: The Hadoop distributed file system divides the input data into multiple blocks and distributes various replicas of blocks across existing nodes. The MapReduce framework executes a task in parallel on these distributed data blocks. The MapReduce scheduler requires being responsive to the location of data blocks to exploit the data local task executions. The scheduling of the *reduce* task has to be done based on the intermediate data locations. Therefore, the nodes that run local *map* tasks of the job must be set preference.

b) Data Volume: The MapReduce jobs are executed on the nodes of the cluster that store a massive amount of data. If a scheduler recognizes the nodes having the input data of a given job correctly, then the performance of a job can be enhanced. The chances of identifying a right data block on a node are less if the amount of data to be processed is enormous. Hence, to quickly recognize the local data nodes for a job, the scheduler has to be adaptive in nature.

3) Workload-Volume-Adaptive: In distributed and parallel environments several jobs are executed at a time. The volume of data turns out to be important to ensure Quality of Service necessities of response time and throughput.

4) Job-Adaptive: The important features of a MapReduce job are its type, priority, size, and execution time. A scheduler can adapt to one or more features as job contains a *map* and *reduce* tasks, its type and time are resulting from the corresponding task features.

a) Job Type: A job can be I/O-intensive or CPU-intensive, or a combination of both. If the *map* tasks of two CPU-intensive jobs are scheduled on a node, then both the jobs will contend for the allocation of CPU, and it can take a longer execution time. However, if the tasks of a CPU and I/O-intensive jobs are scheduled on a node, they can execute in parallel.

b) Job Time: A scheduler has to confirm that at least a few tasks of a job are continuously executed in the cluster. For that, it has to consider the response time, task execution time, and the actual response time with different task schedules.

c) Job Size: The job sizes are characteristically measured as the number of *map* and *reduce* tasks essential to complete that job. These tasks are subject to the size of data to be executed by that job. The scheduler decides each job task be scheduled based on their size.

d) Job Priority: The MapReduce framework runs different job types. Scheduling algorithms should be capable of scheduling jobs and tasks depending on their priorities. These priorities can be fixed by the administrator depending on the user inputs. In a few circumstances, priorities can be identified by the scheduler depending on further requests, for instance, fairness and response times.

IV. MapReduce Scheduling Issues

This section defines data locality, speculative execution, and heterogeneity regarding the MapReduce framework because these are the important performance issues for MapReduce

scheduling algorithms. We present the classification of literature as shown in Figure 6.

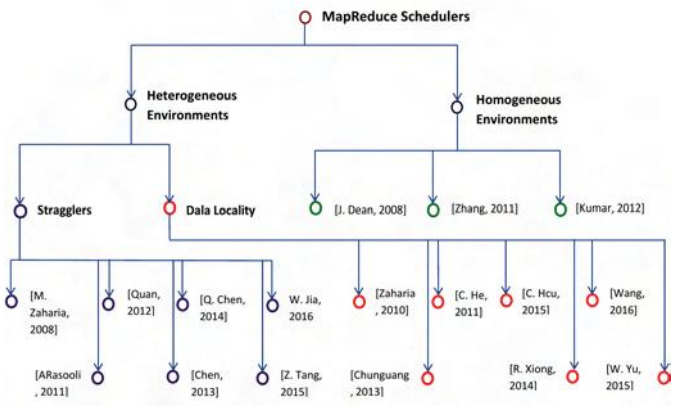

Figure 6. A Classification Literature of MapReduce Scheduling Approaches

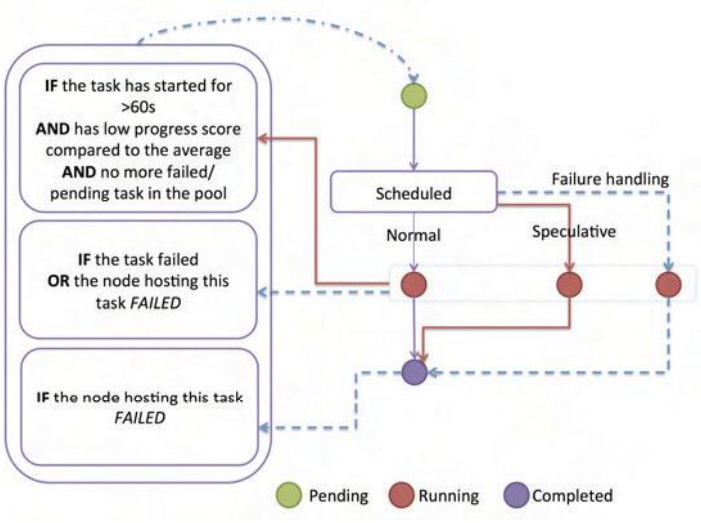

Figure 7. Life cycle of a task in Hadoop

A. Data locality

To process an enormous amount of data, Hadoop has to provide an efficient data locality scheduling approach for improving its performance in a heterogeneous environment. One of the Hadoop principles is that moving computation is cheaper than moving data [17]. This principle says that it is better to move the computation close to data location rather than to move data to the computing node. It applies in particular when the data size is vast because the moving of computation minimizes the network congestion and enhances the system performance. Data locality is about executing tasks to their input data as close as possible. These days clusters have many nodes and transmit large data that enforce network load and create congestion. Therefore, designing a scheduler that can avoid unnecessary data transmission in the Hadoop cluster is a crucial factor for the MapReduce performance as network bandwidth is a scarce resource for these systems.

For each node, all tasks are categorized according to the distance between the input data node and computation node. The best efficient locality is where the task processing is done on the same node with corresponding input data block named as node-level locality. When a task cannot achieve the node level locality, then scheduler executes the task on the node where the processing node and data node located in the same rack named as rack-level locality. If the task still fails to achieve the rack-level locality, then the scheduler schedules the task on a node in another rack which is named after off-rack-level locality. If the data locality is not accomplished, transferring of data and I/O cost can adversely affect the performance due to shared network bandwidth.

B. Speculative Execution

One of the common causes that prolong the execution of a MapReduce job is a "straggler". A Straggler in simple terms is a task (*map* or *reduce*) that takes longer execution time as compared to other tasks in the cluster. Straggler tasks can cause resource wastage and hamper the performance of a job in the cluster, i.e. if a single task is delayed it affects the execution time of the whole job. It is commonly seen that the longer that a job runs, the chances of its getting delayed increase. The causes can be many; malfunctioning of hardware, bugs in software and configurations, different hardware and dynamic aspects like CPU time variability, network traffic, disk contention, etc. These can be difficult to identify as in most of the cases; jobs execute effectively. As the stragglers may take longer execution time, MapReduce goes for a redundant speculative execution on other nodes in an attempt to minimize job execution time as shown in Figure 7.

MapReduce executes a speculative copy of its task (also called a backup task) on another node to finish the computation faster. The objective of speculative execution is to minimize the job execution time. A speculative task is executed based on a simple heuristic that compares each task progress to the average progress of a job. If the *JobTracker* finds that the task is running very slow (about other tasks of the same job) or showing minimal progress over time, it schedules a copy of the same task on another node without suspending the initial task. Moreover, both the tasks run simultaneously and separately. When a task executes well, then any duplicate tasks that are running are dismissed as they are not required. Therefore, if the original task completes its execution before the speculative task, then the speculative task is terminated. Conversely, if the speculative task finishes first, then the original task is terminated, which is termed as speculative execution.

Scheduling of speculative tasks is complicated as it is difficult to differentiate the tasks that are marginally slower than the average completion time, especially in heterogeneous environments. If straggler tasks are identified initially, then the completion time of a job can be minimized. Even though MapReduce schedulers attempt to launch backup tasks for

stragglers, they fail to identify correct straggler tasks because of errors and difficulties in estimating the remaining execution time of tasks. Wrong identification of straggler tasks eventually gives rise to two problems; First, the execution times of real stragglers are extended because launching a backup task for wrongly identified stragglers will not improve the MapReduce performance. Second, the system resources are misused when launching backup tasks for wrong stragglers. Straggler tasks are undesirable since they extend the job execution time and thus degrade the performance of the MapReduce framework.

C. Heterogeneity

Hadoop was initially aimed for homogeneous cluster environments, but now it is commonly used in various heterogeneous environments [19]. The homogeneity assumption is that all the nodes in the cluster will have the same processing capacity. This assumption can degrade the MapReduce performance because there is certain diversity in the hardware. In current day scenarios, financially constrained entities like universities and colleges would like to have a cluster with a mix of legacy hardware with newer ones. Advancement of hardware technology is another practical reason for heterogeneous clusters to increase, as hardware sourced at different times in technology cycles can be brought together in a better way. Therefore, coping with heterogeneous cluster hardware would be a major goal to increase the scope of MapReduce. In a heterogeneous environment, it is important to schedule a job with proper resources to achieve high performance. MapReduce jobs have heterogeneous resource demands as jobs may be CPU or I/O-intensive.

Heterogeneity is categorized as below which is increasing in both workloads and cluster configurations.

1) In Heterogeneous environments, each node in the cluster can have different physical parameters such as processing speed and disk capacity.
2) MapReduce jobs can be heterogeneous on various task features such as data, the number of tasks, job execution times, and computation requirements.

However, current MapReduce schedulers are not correctly adapted for heterogeneous systems. Research in this paper is originally motivated by addressing the scheduling challenges arising due to increase in the heterogeneity of distributed systems. This system introduces novel scheduling challenges and directly affects the system performance.

V. Conclusions

This paper presented background work on the evaluation of Hadoop framework. A detailed explanation of the MapReduce framework is given and presented a taxonomy of MapReduce scheduling algorithms. This paper also reviewed some of the MapReduce scheduling approaches for heterogeneous environments which are related to the job or task scheduling, speculative execution, and data locality.

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Cloud Armor: A Trusty Supporting Reputation-based Management for Cloud Services

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***Abstract*: Trust controlling may be a standout among the primary tough matter for the effort and development of cloud computing. The very dynamic, scattered, and non-transparent nature of cloud facilities ends up in several difficult problems like privacy, security, and handiness. Saving consumers' privacy isn't a simple task attributable to the direction concerned within the communications between customers and also the trust controlling service. Protective cloud services against their spiteful shoppers (e.g., such shoppers could provide dishonorable feedback to inconvenience a selected cloud service) may be a sophisticated issue. Attributable to the dynamic nature of cloud environments, reassuring the provision of the trust management service may be a problematic issue. during this article, we incline to describe the planning and application of Cloud Armor, a reputation-based trust management system that provides a conference of functionalities to deliver Trust as a Service (TaaS), which joins i) a completely unique convention to demonstrate the quality of trust inputs and save clients' security, ii) a flexible and sturdy quality model for measurement the quality of trust feedbacks to stay cloud services from malicious shoppers and to investigate the Irresponsibleness of cloud services, associated iii) an handiness model to manage the accessibility of the suburbanized usage of the trust management service. The possibility and assistances of our methodology are tried by a model and take a look at studies utilizing a set of true trust feedbacks on cloud services.**

***Index terms*: Cloud computing, trust controlling, repute, authority, security, secrecy.**

I. INTRODUCTION

Cloud computing [6] refers to pool of services that square measure offered to a client on pay per use basis. It helps IT firms to specialize in their business or strategic comes instead of technical aspects. It elevates the necessity of shopping for pricey servers. Users needn't to hassle concerning installation and package maintenance. in the main 3 service model square measure offered by cloud that square measure Infrastructure as a service (IaaS), Platform as a Service (PaaS) and package as a service (SaaS). At SaaS level applications square measure hosted by suppliers on network, these services square measure utilized by customers over web on demand basis. an online browser is employed to access totally different software's from the cloud suppliers. A user needn't to put in package on his machine, solely Associate in Nursing instance of package is required. For instance Google Apps, SQL Azure. In PaaS model as name implies it provides platform to create numerous applications. numerous facilities offered by PaaS to deploy applications embrace application planning, development, testing and hosting [10]. Suppliers offer servers and network for application preparation while not shopping for actual hardware and package. The downfall of PaaS is movable-ness drawback. Users got to pay high price if he desires to migrate from one supplier to a different. Iaas is model during which solely hardware is employed by services for his or her operation. Users needn't to buy pricey servers; they'll rent server and network house, memory, cupboard space etc. This reduces hardware maintenance at native level. a number of IaaS vendors square measure Amazon straightforward Storage Service (S3) for information backup, Amazon Elastic Cloud Computing (EC2), Go Grid, VMW square measure etc.

A. Cloud Security:

As companies are placing more information on cloud, threats are increasing about the safety of environment. Security and data protection are one of serious concern in cloud development and adoption. Restricted manipulation on data can cause miscellaneous security problems which include data outflow, unprotected interface, resource sharing, data availability and inner attacks [9]. As all aware cloud is increasingly accepted, but still people have certain confusion in their mind that their data might not be secure at other end. Security in cloud computing is one of big matter because equipment used to deliver services does not own by users. The consumers have no authority, nor any knowledge of, what is happening with their data. Service Provider Layer have various security concerns some of them are Data transmission, Privacy, People and Identity, Audit and Compliance, integrity and Binding problems. Security difficulties faced by Virtual Machine Layer are VM Escape, VM Sprawl, Insecure VM migration, Malicious VM Creation, Cloud legal and Regularity complains Identity and Access management. Data Centre are vulnerable to different type of attack at Physical and Network level.

B. Overview of Trust is a social problem:

There are lots of definitions of trust. Basically trust refers to confidence or belief of one entity on other. One cannot build trust in a day. It is normally based upon provider's position in market. As users are putting their resources on provider's datacenters so there is major concern about the trustworthiness of providers and services. Two parties are

involved in any trusted relationship: one is trusting party (i.etrustor) and other party to be trusted (i.e trustee) [1-5], [7]. Various risks are involved: location security risk, data disclosure problem, data misplacement issue, data investigation concern. In cloud environment hostile user can add malicious code and take CPU space, resources and time. To model attractive cloud computing, trust should be introduced and there should be some trustworthy regions where users can deploy their applications and use resources safely.

II. Related Work

Trust is one amongst the foremost involved problems for the acceptance and growth of cloud computing. Though many solutions are expected recently in managing trust feedbacks in cloud environments, the way to confirm the believability of trust feedbacks is generally neglected. During this project the system projected a Cloud Armor, a reputation-based trust management outline that gives a collection of functionalities to deliver Trust as a Service (TaaS). "Trust as a Service" (TaaS) framework to enhance ways in which on trust management in cloud environments. The approaches are valid by the epitome system and experimental results. Here, it provides some drawbacks are, it's common that a cloud service involvements malicious behaviors from its users, it's undecided whether or not they will trust the cloud suppliers, It not convincing enough for the customers, SLAs don't seem to be consistent among the cloud suppliers albeit they provide services with similar practicality, Customers don't seem to be certain whether or not they will establish a trustworthy cloud supplier solely supported its SLA. During this project the system projected a Cloud Armor, a reputation-based trust management framework that gives a collection of functionalities to deliver Trust as a Service (TaaS). "Trust [11], [12] as a Service" (TaaS) framework to enhance ways in which on trust management in cloud environments. specifically, the system introduce associate degree adaptation believability model that distinguishes between credible trust feedbacks and malicious feedbacks by considering cloud service consumers' capability and majority agreement of their feedbacks. The approaches are valid by the epitome system and experimental results. The system proposes a framework mistreatment the Service orientating design (SOA) to deliver trust as a service. Here it includes some edges are, It not solely preserves the consumers' privacy, however conjointly permits the TMS to prove the believability of a selected consumer's feedback, It conjointly has the flexibility to discover strategic and occasional behaviors of collusion attacks, Load equalization techniques are exploited to share the employment, thereby invariably maintaining a desired accessibility level, This metric exploits particle filtering techniques to exactly predict the provision of every node, Cloud Armor exploits techniques to spot credible feedbacks from malicious ones.

III. Proposed System

A. Trust Management

Long back, Trust applied in scientific correction for constructing individual association and currently it's necessary additional for forming security device in distributed computing atmospheres. Trust management has several security qualities like dependableness, irresponsibleness, self-assurance, honest, belief, honesties, security, ability [8]. There are 2 variations of trust 1) trust and 2) Indirect Trust [8]. Trust is predicated on personal expertise and indirect trust state that once anyone has no any direct knowledge then he's have faith in others trust. This kind of trust is implicit indirect Trust. In cloud setting varied service supplier is obtainable. Hence, it's vital to spot trustworthy service dealer. Trust is advanced relationship among totally different cloud unit and since trust is additional particular, context dependent, non-rhombohedra and inexact. There are varied ways that of analysis of trust. In e-commerce sector, we will measure the trait by feedback submitted by cloud users. Once trust is calculated supported feedback scores of cloud users there could probability varied feedback base attacks. Next section need the assorted attainable attack on reaction primarily based trust evaluation.

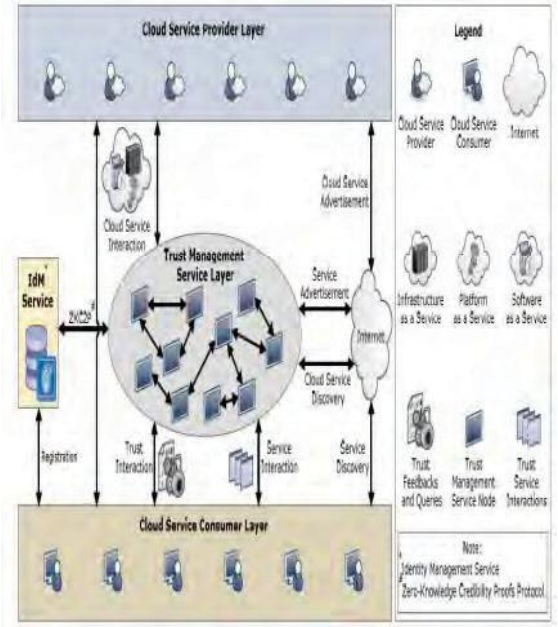

Figure 1. System architecture

B. Implementation

i. User Registration:

Users are the important entities in our scheme. Initially the user wants to register their credentials in the corresponding system. These credentials are including some personal information about users like, name, date of birth, address, contact number etc... This personal information is stored in Identity Management Services. This acts like a database in this manner. After this registration only, the user can use all the services provide from cloud. But this information is

stored very securely. We need to protect the user's privacy from unauthorized activities.

ii. Upload Services:

Cloud service provider is responsible for provide useful services to the user. Their services are classified into three categories. These are, Infrastructure As a service, Platform As a Service, Software As a Service. Under these three categories, the CSP upload the services for users. These details are stored in Identity management Service. Services detail information shown in Figure 3.

iii. Send Feedback:

After uploading the services, the user can use these services from the cloud. To use these services, the user needs to store their credentials in IDM services. Then the user can share their opinion to the cloud regarding to the services, shown in Figure 4. This feedback also stored in the identity management Services. This IDM service sore the user details and product details as shown in the Figure 2, according to their feedback service.

iv. Feedback Collusion Detection:

Trust Management Service is the one, which use all the details stored in the IDM for check the user's credibility. Users have a limit to send the feedback for a service. There is a threshold value for that. If they cross the limit, we can identify if they are trying to increase/decrease the service rate. Suppose they cross the limit, the trust management service separate them from the users list. This process is called as feedback collusion detection.

v. Sybil Attack Detection:

Some users are very brilliant. Because they know, if we cross the limit, we would catch. So they use the different accounts for increase/decrease the service rate. In our system, their credentials also stored in identity management service this record are viewed by trust management service. Our TMS service cross checking the user's credentials. Some credential of user's are cannot to change like date of birth, mobile number, mail id. Using that similarity, the TMS can found the unauthorized users. This is called as Sybil attack detection.

Figure 2. Product details

Figure 3. Services page

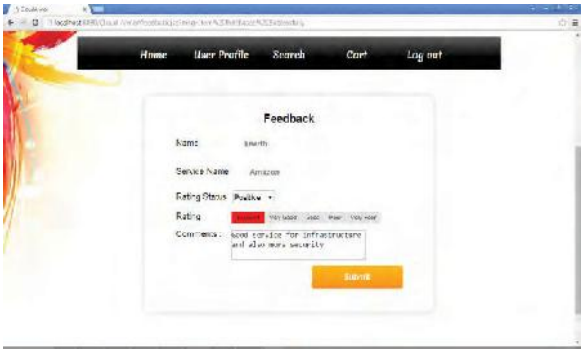

Figure 4. Feedback

IV. Conclusions

Cloud computing source many consecrations but still there are a unit many difficulties in cloud supported practice of cloud. A most tough issue that required to surrender focus in cloud computing is security and trust controlling, due to dynamic nature of cloud atmosphere, that area unit very important part of cloud security. Once trust result appraised by responses of cloud user then there may chance of malicious feedback submission. It is significant to identify the feedback base attacks as a outcomes of less submission of fake feedbacks might negotiation the entire trait of service provider. In future, we'd wish to hunt down the other gettable attacks on feedback collection, feedback analysis and account the thanks to forestall and notice those attacks efficiently by strong trust model.

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DNS Cache Poisoning Attack Analysis and Detection Using Packet Header

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***Abstract*- DNS is the most critical component in the internet and its security is crucially challenged. The normal operation of DNS is to acquire the correct domain to IP address mapping to browse the web and sending emails etc. DNS cache poisoning is an attack strategy that diverts the network traffic to attacker's computer by exploiting the vulnerabilities in the DNS server. The web server is susceptible to many kinds of attacks. One such attack called DNS cache poisoning attack is discussed here. The attack procedure of the DNS cache is briefly narrated so that the algorithmic solution is easily developed by following an IF then Else conditional rules. In this paper, we developed an algorithm to detect DNS cache poisoning attack based on packet header analysis. The DNS packets are captured through ETHEREAL software and stored in a log after dissection of the packet header. The logged packets are analyzed and processed through an algorithm in order to detect the possibility of DNS Cache Poisoning attack.**

***Index Terms*- DNS Cache Poisoning Attack, DNS reply, TTL, Request transaction ID, Reply transaction ID**

I. Introduction

The most vulnerable layers among the seven layers of OSI reference model are the network layer and the transport layer [1]. There are many attacks on these two layers by the third party attacker either intentionally or due to misconception. We assume that the network is susceptible to many such attacks where a system or server is compromised. These attacks [2] greatly affect the system performance and destroying the valuable information on the web server. It is not easy to detect or prevent some of the attacks due to the intelligence of third party attackers. The attackers violate all the security rules [3] and also remove the trespassing activity on the web from the server logs. Therefore the network traffic has to be monitored and a suitable method has to be developed for countering the attack.

The simple way of monitoring the network traffic is to look at the server log files. The log files contain the activities related to their trespassing i.e. date, time, IP address, HTTP status, bytes sent, bytes received etc. The log files are the most important documents to the security professionals where the histories of certain attacks are found. In this paper, we also look at the log files at server for the entries of DNS traffic and devise an algorithm to detect DNS Cache Poisoning attack.

II. Background

The domain names are converted to IP addresses in the case of DNS and it is the bridge between the client and the server. There is an analytical model which defines the DNS infrastructure along with the selection of DNS parameters [4]. Similarly, they have compared the performances of DNS security solutions using cryptographically approach and collaborative overlay approach.

The DNSSEC (DNS SECurity) is essential for DNS cache poisoning attack as the attacker redirects the communications to adversarial servers. DNS cache poisoning attack indirectly allows interception of original contents and modification [5].

It is a considerable threat to the security of internet users which has to be detected at the earliest. Some such detection methods are implemented by using Kalman filter and the entropy of query packet [6]. Another mechanism called security proxy is also implemented, the schemes to prevent the DNS cache poisoning attack are the selective requery and the security level communication [7]. There is a novel solution to DNS cache poisoning attacks called WSEC DNS (Wild card SECure DNS) which depends on existing DNS protocol but with a wild card domain name.

A system or server in a network is susceptible to many attacks. The attacks [8] can be of different types which may include the attacks done intentionally by the third party. Firewall does not protect the system from such attacks. Some of the existing software and techniques are discussed hereunder.

- *Basic Entry Log Auditing Software*

A Basic Entry system allows you or a log auditor to enter the logs manually onto the system and the software indicates if there is Hours of Service (HOS) violation and so forth. The auditor will be allowed to deduct points off the driver if he has for example; not calculated his hours correctly, missing remarks, etc. From there you have a reporting package that will highlight all the drivers' mistakes and give him a rating percentage for any violation that he/she has done.

The software comes with one rule set (Canadian or American), Manual Event Tracking, Initial 50 Active Drivers and a Reporting package.

- *Automated Scanning & Log Auditing Software*

An automated system will take a scan able log and do the auditing for you. The software will take all the information from the drivers log and red flag any logs with violations. If 100 logs were to be scanned in to the system and 20 of the logs had violations on them. You will only be auditing the 20 logs that were red flagged.

The software comes with Driver & Vehicle Profiles, Timed Events Verification Module, Full Reporting Package, Initial 50 Active Drivers and Four hours of internet based installation and training assistance.

- *Electronic Log Auditing*

Laptop application with complete rule sets and voice prompts (alerting the driver of pending violations before they happen, based on each driver's individual duty cycle). E-logs will reduce audit review and help enhance communication with corporate offices. It also eliminates paper logs, log editing and HOS violations giving the company and the driver peace of mind to.

- *Network Traffic Monitor Analysis*

Packet Analyzer enterprise edition is an advanced network monitoring, analysis and reporting tool. It captures and analyzes traffic in realtime. It also presents comprehensive and graphic reports for many technical and business applications. All information is displayed in simple English with easy to use interface for anyone to master the tool with minutes of self training.

- *PC-Based Data Logging and Recording Techniques*

Data logging and recording is a very common measurement application. In its most basic form, data logging is the measurement and recording of physical or electrical parameters over a period of time. The data can be temperature, strain, displacement, flow, pressure, voltage, current, resistance, power, or any of a wide range of other parameters. Real-world data logging applications are typically more involved than just acquiring and recording signals, typically involving some combination of online analysis, offline analysis, display, report generation, and data sharing. Moreover, several data logging applications are beginning to require the acquisition and storage of other types of data, such as recording sound and video in conjunction with the other parameters measured during an automobile crash test.

Data logging is used in a broad spectrum of applications. Chemists record data such as temperature, pH, and pressure when performing experiments in a lab. Design engineers log performance parameters such as vibration, temperature, and battery level to evaluate product designs. Civil engineers record strain and load on bridges over time to evaluate safety. Geologists use data logging to determine mineral formations when drilling for oil. Breweries log the conditions of their storage and brewing facilities to maintain quality.

- *Google security tool uses Google to scan sites for vulnerabilities*

Google Scanner is a Web auditing tool released by the hacker group Cult of Dead Cows. The tool uses the prowess of the search engine to surface vulnerabilities on Web sites.

III. DNS Cache Poisoning Attack

Normally a computer uses DNS (Domain Name System) server [9] to find the domain name of a site. The DNS server responds with one or more IP addresses where a computer can reach to the site. Afterwards a computer connects directly to that numerical IP address. The role of DNS is to convert human-readable addresses like "google.com" to computer readable IP addresses like "173.194.67.102".

DNS cache poisoning [10] is an attack strategy that diverts the network traffic to attacker's computer by exploiting the vulnerabilities in the DNS server. It is also called as DNS Spoofing which corrupts DNS data and returns an incorrect IP address to a computer. Whenever a computer asks for an IP address of a domain name, if the server does not know then it will ask another server and the process continues until it finds. To increase performance the server cache these translations for certain amount of time to make use in future. Now if the server receives same kind of request then it can reply from the cache without asking other servers until the cache expires. But what if a computer receives a false translation and caches for performance optimization then it is considered as poisoned. As the DNS server is poisoned, it replies an incorrect IP address that diverts the network traffic to attacker's computer.

An attacker takes advantage of the loop holes of the DNS software by poisoning the cache and makes it accept incorrect information. If the DNS server does not properly validate the DNS response from an authoritative source then the server will cache the incorrect entries. Now server will reply to users the same incorrect entries for the same kind of request. In this process the attackers get the diverted network traffic and may control the users.

To perform a cache poisoning attack [11], the attacker exploits a flaw in the DNS (Domain Name Server) software that can make it accept incorrect information. If the server does not correctly validate DNS responses to ensure that they have come from an authoritative source, the server will end up caching the incorrect entries locally and serve them to users that make the same request.

This technique can be used to replace arbitrary content for a set of victims with content of an attacker's choice. For example, an attacker poisons the IP address in the DNS entries for a target website on a given DNS server,

replacing them with the IP address of a server he controls. He then creates fake entries for files on the server they control with names matching those on the target server. These files could contain malicious content, such as a worm or a virus. A user whose computer has referenced the poisoned DNS server would be tricked into thinking that the content comes from the target server and unknowingly downloads malicious content.

We studied the behavior of the DNS Cache Poisoning attack and formulated the algorithm based on packet header to detect the threat. The information about the attack is maintained in a log for the evidentiary purpose in the court of law. Hence the work is embodied with the appropriate results.

Attack Procedure

1. Host requests message to DNS with domain name of destination
2. DNS redirects the request message to sub domains.
3. Attacker captures the request message and finds the transaction ID.
4. Attacker replies with same transaction ID, his own IP address and TTL is set to a greater value.
5. When original reply comes, DNS sees this and thinks that this is a Duplicate and discards it.
6. DNS attack is successful.
7. End.

IV. ANALYSIS OF DNS PACKET

The DNS packet is composed of four important header formats such as MAC header, IP header, UDP header and DNS header as shown in table 1. The details of the header with respect to the DNS request are shown in table 2 and the DNS reply is shown in table 3.

TABLE 1.
THE DNS PACKET FORMAT

MAC Header	IP Header	UDP Header	DNS Section

TABLE 2.
DNS REQUEST PACKET FORMAT

Identification (Transaction ID)	Parameters (Flags)	No. of questions	No. of answers	No. of authority
No. of additional	Query domain name	Query type	Query class	

TABLE 3.
DNS REPLY PACKET FORMAT

Identification (Transaction ID)	Parameters (Flags)	No. of questions	No. of answers	No. of authority
No. of additional	DNS Query section	Answers section	Authoritative Name servers	Additional records

A. DNS Request packet

We have captured the DNS request packet using the Ethereal software and the details of the packet dissection are given below.

HEX packet format:
0000 00 11 85 c2 82 e6 00 16 76 89 b2 58 08 00 45 00
0010 00 41 19 31 00 00 80 11 50 b5 c0 a8 14 89 cb 99
0020 2f fb 04 39 00 35 00 2d 70 c9 ab cd 01 00 00 01
0030 00 00 00 00 00 00 04 61 75 74 6f 06 73 65 61 72
0040 63 68 03 6d 73 6e 03 63 6f 6d 00 00 01 00 01

Ethernet II:

- 6 bytes destination address: 00: 11: 85: c2: 82: e6
- 6 bytes source address: 00: 16: 76: 89: b2: 58(192.168.20.137)
- Type: IP (0X0800)08 00

Internet protocol:

- The IP version is IPV4: 4 (45)
- 1 byte differentiated services field: 0x00 (00)
- 2 bytes of total length: 65 (00 41)
- 2 bytes identification: 0x1931 (19 31)
- 1 byte for flags: 0x00 (00)
- 2 bytes of fragment offset: 0 (00 00)
- 1 byte is for time to live:128 (80)
- 1 byte to indicate the protocol: udp (0x11) (11)
- 2 bytes for header checksum: 0x50b5 (50 b5)
- 4 bytes used for source address: 192.168.20.137 (c0 a8 14 89)

- 4 bytes for destination address: 203:153:47:251 (cb 99 2f fb)
- User datagram protocol:
- Source port is of 2 bytes: 1081 (04 39)
- Destination port is of 2 bytes: domain (53) (00 35)
- Length: 45 (00 2d)
- Checksum: 0x70c9 (70 c9)

Domain Name System: Query

- The transaction id is 2 bytes: 0xabcd (abcd)
- Flags is of 2 bytes: 0x0100 (01 00)
- Questions is 2 bytes: 1 (00 01)
- Answers is 2 bytes R Rs: 0 (00 00)
- Authority is of 2 bytes: 0 (00 00)
- Additional: 0 (00 00)

Queries:

- Name: auto.search.msn.com (04 61 75 74 6f 06 73 65 61 72 63 68 03 6d 73 6e 03 63 6f 6d 00)
- Type: host address (00 01)
- Class: inet (00 01)

IV. IMPLEMENTATION

We capture the DNS packets using Ethereal software. After capturing the packets, we store the packets in the database. We store both the request as well as response packets in the database. The request transaction ID is compared with the response transaction ID, if both are equal then check the TTL field in the response answer section. If TTL field is greater than 1 day, then we conclude that there is a DNS Cache poisoning attack.

A. DNS_Cache_Poisoning Detection Algorithm

[DNS_DB refers to database of DNS traffic, PKT refers to a DNS packet, DNS_REQ refers to request packet of DNS cache traffic, DNS_REP refers to reply packet of DNS cache traffic, REQ_TR_ID refers to transaction ID of request packet, REQ_IP_ADD refers to IP address of request packet, REQ_DOM_NAME refers to domain name request packet, REP_TR_ID refers to transaction ID reply packet, REP_TTL refers to TTL in the answer section of reply packet, REP_IP_ADD refers to IP address of reply packet.]

1. Capture all packets
   {
   FILTER DNS cache packets;
   STORE in DNS_DB;
   }
2. If (PKT=DNS_REQ)
3. {
4. GET REQ_TR_ID, REQ_IP_ADD, REQ_DOM_NAME;
5. }.
6. If (PKT=DNS_REP)
7. {
8. GET REP_TR_ID, REP_TTL, REP_IP_ADD;
9. }
10. If REQ_TR_ID = REP_TR_ID then
    {
      If Ans_TTL >1 day Then
    {
    DETECT as “DNS Cache poisoning attack”
    DISCARD the packet
    STORE the REQ_IP_ADD, REP_TTL, REQ_TR_ID, DATE, TIME in DNS_FORENSIC_LOG.
    }
    }
    ELSE
{
   If REP_TTL <1 DAY Then
    SEND REPLY
}
11. End

B. Results

We have captured the DNS packets by using the freeware ETHEREAL Network Analyzer and the details are shown in fig. 1.

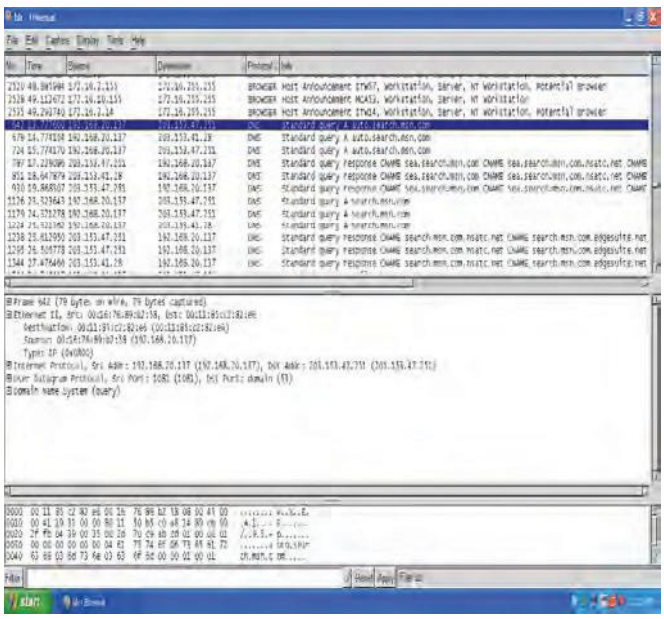

Figure1. Frame which captures the DNS packets

The DNS packets are dissected and the required header fields are stored in the MySQL database for further analysis of attack and detection as shown in fig. 2.

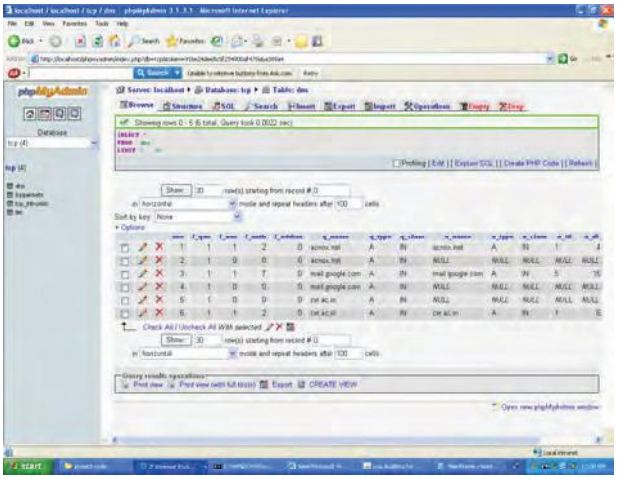

Figure 2. Stored packets in MySQL database

The detected intrusion packets are stored in the DNS_INTRUSION database for the purpose of future evidentiary purpose by the law enforcement agencies as shown in fig. 3.

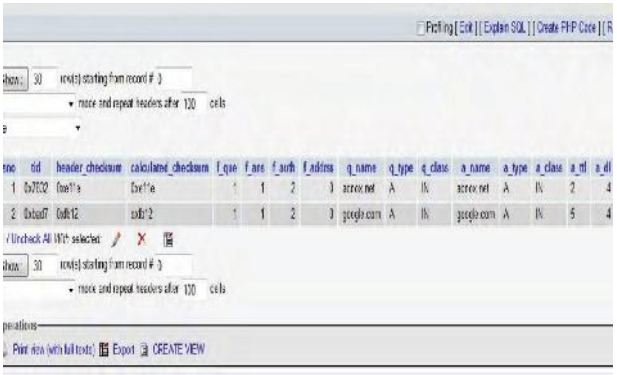

Figure 3. DNS intrusion database

V. CONCLUSIONS

It is observed that the network traffic entering into the system must be carefully analyzed. With the increase in emerging technologies, there has always been a scope for hackers to trespass into the others system in an innovative way. Therefore in this paper, we have effectively detected the DNS cache poisoning attack and these attacks affect the integrity of the data, and the authentication of the user. Though there are several ways to study or analyze a packet, we study the header format and perform the actions accordingly. Research is also being done in detecting the errors by performing correlation analysis and discriminating the packets.

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Contextual Customization of Reusable Components for High Cohesiveness in Robust Software Development

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Abstract: **Developers generally prefer reusable code in software development. Writing reusable code is not about developing generic, monolithic modules. It is about writing focused, com-posable modules with high cohesion and loose coupling. Reusing generic, monolithic modules which are non-cohesive makes a fragile software which in turn increases development and maintenance costs. Proper customisation of a generic monolithic module in a context enhances cohesiveness of the module. Customisation for cohesiveness makes the module reliable and robust which in turn reduces the development and maintenance cost.**

***Index Terms*—robust programming, cohesion, monolithic design, generic components, contextual customisation**

I. Introduction

Being generic is a basic requirement for a module to be reusable [1]. In the quest for writing reusable software, it's a common mistake to make software too generic. Making software too generic causes its usability to suffer. Reusable module is not about designing a module to be a single, flexible, monolithic component which is applicable in an extremely broad range of use cases and environments[2]. It's about designing a cohesive com-posable component.

Preferring reusability over cohesiveness makes a module less robust which in turn affects the development and maintenance cost. Robustness is the ability of computer to cope up with errors during execution and cope with erroneous input[3]. Robust programs generally need to deal with 3 kinds of exceptional conditions: user errors - when invalid input is passed to the program; exhaustion - when program tries to acquire shared resources; internal errors - due to bugs.

A robust program ideally detects or prevents these conditions and deals with them in a safe and intelligent way.

Let's take a c code-snippet and elaborate upon the concepts of reusability and cohesiveness. Let's take a simple c program to calculate sum of 2 real numbers

vamshi-macbook:researchvamshi$mate sum2Floats.c

```
#include <stdio.h>

float readFloat(void);
float sumFloat(float, float);

int main(void){
        float number1;
        float number2;
        float result;

        number1 = readFloat();
        number2 = readFloat();

        result  =sumFloat(number1, number2);

        printf("\n\nSum  : %f", result);

        return 0;
}

float readFloat(){

        float number;

        printf("\nEnter a Real Number : ");
        scanf(" %f", &number);

        return number;
}

float sumFloat(float number1, float number2){
        return number1 + number2;
}
```

vamshi-macbook:researchvamshi$gcc sum2Floats.c
vamshi-macbook:researchvamshi$./a.out

Enter a Real Number : 123
Enter a Real Number : 234

Sum : 357.000000
vamshi-macbook:researchvamshi$./a.out
Enter a Real Number : 123a45
Enter a Real Number :

Sum : 246.000000
vamshi-macbook:researchvamshi$

We get in-consistent result because *readFloat* is not cohesive in nature. It is making use of *scanf* function which is reusable module but not cohesive. There should be clear

II. Proposed Strategy

We are proposing a design methodology where we neither sacrifice reusability aspect nor neglect cohesive aspect of the module being developed. We customize reusable components to enhance its cohesive nature which enhances its robustness [4].

Certain key-points in framing our cohesive modules

- Maximizing genericity complicates use
- Excessive reusability breaks abstraction.
- Favor Composability over monolithic design
- Favor Composability over reusability
- Customise Reusable Components to enhance cohesion.

For example, generic *scanf* function is used to read data of different types. It's very generic nature creates the problem of robustness. Typo in entering an integer using *scanf* forces the integer variable to carry garbage value.

Because of excessive genericity of *scanf* function, it's difficult to modify the existing functionality to facilitate robustness.

It's better to design our own module using existing *scanf* function to deal with the context appropriately.

A developer should neither code from scratch, nor use existing re-usable components blindly. He should customise the existing components to enhance cohesiveness.

Let's understand the above aspects through the case studies given below

III. Case Study

Let's modify *sum2Floats.c* to enhance cohesive aspect of *readFloat* function which in turn makes the module robust.

vamshi-macbook:researchvamshi$mate cohesiveSum2Floats.c

```
#include <stdio.h>
#include <stdbool.h>
#include <ctype.h>
#include <stdlib.h>

float readFloat(const char* prompt);
float sumFloat(float, float);

int main(void){

float number1;
float number2;
float result;

number1 = readFloat("\nEnter Number1 : ");
number2 = readFloat("\nEnter Number2 : ");

result  =sumFloat(number1, number2);

printf("\nResult : %f", result);

printf("\n\n");
return 0;
}
float readFloat(char* prompt){

float number;
bool successFlag = false;

do{
        char ch;
        intextraCharacterCount = 0;

        printf("\n%s", prompt);
        if(scanf(" %f", &number) != 0){
        while((ch = getchar())!='\n')
                extraCharacterCount++;

        successFlag = extraCharacterCount?false :
                                        true;
        }
        else
                successFlag = false;

        if(!successFlag&&extraCharacterCount){
        printf("\nInvalid Input");
        continue;
        }


        else if(!successFlag){
        while(getchar()!='\n');
                printf("\nInvalid Input");
        }

}while(!successFlag);

return number;
}

float sumFloat(float number1, float number2){
        return number1 + number2;
}
```

vamshi-macbook:researchvamshi$gcc cohesiveSum2Floats.c
vamshi-macbook:researchvamshi$./a.out

```
Enter Number1 : 123a45
Invalid Input
Enter Number1 :abc
Invalid Input
Enter Number1 : 123

Enter Number2 : 234.56a
Invalid Input
Enter Number2 : 234.56

Sum  : 357.559998
vamshi-macbook:researchvamshi$
```

Although, we can write *readFloat* module from scratch to be cohesive, we brought about cohesiveness by customising the reusable component *scanf* function. Along with cohesiveness, we enhanced reusable aspect of *readFloat* module by prompting user to provide a contextual prompt.

We can better appreciate the robustness brought about by *readFloat*module if it's being frequently used as part of another module which dramatically makes the new module under development very robust. The code-snippet given below communicates the power of customised cohesive module design.

vamshi-macbook:researchvamshi$matecohesiveSumStudentMarks.c

```
intreadInteger(const char* prompt);
intreadArraySize(const char* prompt, int capacity);
float readFloat(char* prompt);

void readFloatArray(const char*, float* numbers, int size);
void displayFloatArray(const char*, float* numbers, int size);

int main(void){

int capacity = 10;
float subjects[capacity];
intnoOfSubjects;

noOfSubjects = readArraySize("\nEnter the No.of Subjects : ", capacity);
readFloatArray("\nEnter %d Subject Marks\n", subjects, noOfSubjects);
displayFloatArray("\n%d Subject Marks are\n", subjects, noOfSubjects);

printf("\n\n");
return 0;
}

void readFloatArray(const char* prompt, float* numbers, int size){

int index;

printf(prompt, size);
for(index = 0; index < size; ++index)
        numbers[index] = readInteger("\n");

return;
}

intreadArraySize(const char* prompt, int capacity){

intarraySize;
bool successFlag = true;
do{
        arraySize = readInteger(prompt);
        if(arraySize> capacity)
        successFlag = false;
        else
        successFlag = true;
}while(!successFlag);

return arraySize;
}

void displayFloatArray(const char* prompt, float* numbers, int size){

int index;

printf(prompt,size);
for(index = 0; index < size; ++index)
printf(" %f", numbers[index]);

return;
}
```

vamshi-macbook:researchvamshi$gcccohesiveSumStudentMarks.c

vamshi-macbook:researchvamshi$./a.out

```
Enter the No. of Subjects : 5

Enter 5 Subject Marks
85
abc
Invalid Input
83
82
83a
Invalid Input
84
86

5 Subject Marks are
85.00000 83.00000 82.00000 84.00000 86.000000
```

vamshi-macbook:researchvamshi$

In the above application, we need to read 5 subject marks. If their is at least 1 typo, the entire data becomes invalid. The *readFloatArray* function internally invokes*readFloat* cohesive function which in turn makes the *readFloatArray* cohesive. This in turn makes the *readFloatArray* module very robust.

IV. Conclusions

Although robust programming is an established programming methodology, developers tend to design cohesive modules from scratch or tend to re-use existing components overlooking cohesion.

Customising Re-usable components for cohesion increases productivity of developer along with robustness of the module. Proper customisation of modules dramatically reduces development and maintenance costs.

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Design and Implementation of Low Power Finite Impulse Response Filters

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***Abstract*— The Finite Impulse Response (FIR) filter is widely used in mobile and wireless applications. For these applications, the low power and low complexity FIR filter architectures are required. The FIR filter is most commonly used hardware block for signal processing in the above applications. The performance improvement of FIR filter is a great challenge. The researchers have proposed many FIR filters to meet above design specifications. In this paper, two different but efficient methods have been implemented in Xilinx software to improve the performance metrics in terms of speed, area and power. The target device is Spartan-3 Field Programmable Gate Array.**

The first FIR filter is implemented using a variable precision two dimensional fine grain pipeline technique. This technique is developed to improve the performance of the existing two dimensional pipeline gating. The second type of FIR filter is based on the technique of a Data transition Power Diminution Technique (DPDT). In this technique, the effective dynamic data ranges are determined and the unused functional blocks are not activated based on the input data. Due to the unused functional blocks, the power consumption is reduced.

***Index Terms* – FIR, DPDT, Low power, Pipeline gating, pipelining.**

I. Introduction

Finite-Impulse Response filters are important building blocks in many digital signal processing systems such as portable wireless systems, mobile phones and battery operated multimedia devices. The design metrics power, area and speed are considered as important parameters for Very Large Scale Integration (VLSI) architectures. The design methodology for high speed and low power is essential in the implementation of all Digital Signal Processing ICs. Generally, the power dissipation can be analyzed at different levels of the design process, such as algorithmic, architecture, circuit and device levels. The minimization of power dissipation depends on the selection of appropriate algorithms and mapping on to suitable architecture. The great extent of power can be reduced by the elimination of redundant and irrelevant computations in the particular system. The proposed architectures are implemented to reduce power dissipation, increasing the speed of operation and minimizing the area of the chip. The total power consumption of CMOS circuit is a combination of static power and dynamic power. Static power defined as the power consumed when the input signal is a constant value.

The dynamic power consumption is the power consumed when the transistors are active and the input signal change the state of the transistors frequently [1]. In the existing methods of FIR filters, lot of power is consumed because of the switching activities in the circuit. The dynamic power can be reduced by proper identification and suppressing the unnecessary activities in the circuit. The speed of the any architecture depends on the longest path delay of the combinational circuit, setup time of the sequential circuits and clock skew. This paper presents two efficient architectures for the solution of the above problems. Variable precision two dimensional fine- grain pipeline gating and Data transition power diminution techniques are working on the reduction of unwanted switching activities to reduce power consumption.

II. Variable Precision Two-Dimensional Fine Grain Pipeline

The variable precision two-dimensional fine-grain pipeline technique is used to reduce the power by decreasing the switching activities in the circuit. In this technique, pipelining is applied to the horizontal and vertical registers. The corresponding register clocks only gated using this pipelining method.

A) Two-dimensional pipeline gating

The two–dimensional pipeline gating technique is an earlier method of the variable precision pipeline gating technique [2]. In this technique, only horizontal clock gating is used to reduce the power consumption in the pipeline digital system. In the two-dimensional pipeline gating technique discussed by Di et al [3], clock gating is used in data path direction in the pipeline. This two- dimensional pipeline gating provides power awareness in the digital system. The global clock or system clock is distributed to the different blocks as a sub clock. This sub clock is based on the input data precision and is connected to one pipeline stage. Each sub clock is driven the registers, which are placed in the pipeline stage. The pipeline gating method based on the input data, disabling the stages, which are not used in the calculation. Those results are diverted to the final output by using multiplexer is shown in the figure.1. This technique decreases the pipeline latency and the power consumption. The power consumption is reduced due to the no transition in the masked pipeline stage. This technique disable the blocks according to the data flow. Here the delay is not fixed, so the gating cannot be applied for overall pipeline system. The pipeline system is implemented for

fixed latency using clock gating in vertical and horizontal directions to reduce the further power reduction in the digital system. This technique is called variable precision two-dimensional fine grain pipeline gating.

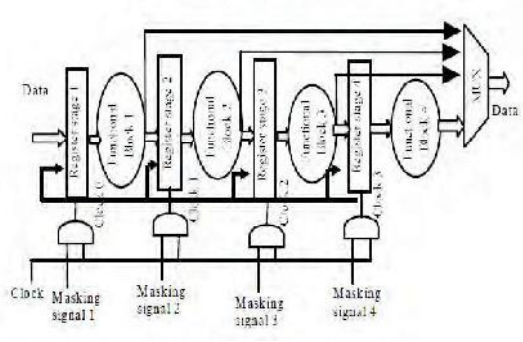

Figure. 1.Two-Dimensional Pipeline Gating Technique.

B) Variable precision two dimensional fine grain pipeline technique for FIR filter

In the variable precision pipeline method two extra features are considered, sub blocks pipelining to maintain the fixed latency and intra pipeline stage gating using variable precision. The variable precision pipeline requires similar additional hardware as conventional pipeline gating technique and with same latency reduction. This section presents the variable precision pipeline fine grain clock gating for multiplier and further FIR filters to reduce the power consumption. The figure. 2 present the variable precision fine grain pipelining for the multiplier. In the multiplier, the zero output-partial products are disabled based on the input combinations. In such case the registers connected to those blocks will not function during multiplication result calculation. The multiplexer selects the correct outputs from the corresponding stages only and remaining blocks clocks are disabled.

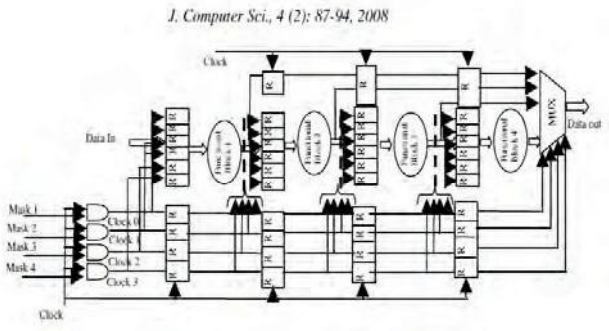

Figure. 2. Variable precision pipeline gating for multiplier.

A set of 8-bit variable precision fine grain pipeline multipliers were used to implement the 8- tap FIR filter and corresponding simulated output windows are shown in figures. 3&4.. In pipelining system, low power and high speed are two main advantages. In the FIR filters, multipliers and adders to be pipelined to improve the throughput [4]. The multiplication time (TM) much larger than the adder time (TA). Hence, proper balancing is required in pipelining stages to get the shorter critical path.

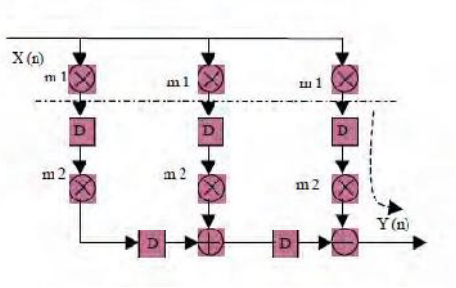

Figure. 3. FIR filter architecture using variable precision Adders and Multipliers.

In the FIR filter architecture, every multiplier is partitioned into two pipeline stages and some extra registers inserted between the sub stage multiplier. The multiplier time TM is divided by TM1 and TM2 and adder time is denoted by TA. If the input data length and the coefficients are small, then TA is enough to operate the filter in high sampling frequency. But, now a days, the FIR filter lengths are 8 to 16 bits and 32 to 64 bits also. For the long word length inputs, the adder also takes considerable time. Now, the pipeline adders are required with including pipeline multipliers for the FIR filter implementation. The pipelining of one adder alters the timing relationship between the two inputs of the next adder. But in the multipliers the relative timing sequence will not change. The pipelining adders are just adding the delay elements between the paths of adders. Hence, extra delay elements are inserted between the pipelined multiplier and its corresponding next adder..

A set of 8–tap variable precision pipelining FIR filter is designed. The variable precision multipliers and adders are used. The overall power consumption is reduced by using two dimensional fine grain adders and multipliers in FIR filter. These results are compared existing pipelining design in [4].

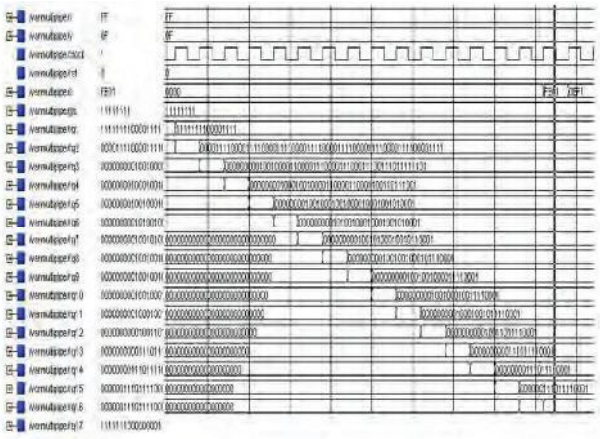

Figure. 4. Simulation Window of Variable Precision Two-Dimensional Pipeline Gating Multiplier

III. THE DATA TRANSISTION POWER DIMINUTION TECHNIQUE IN FIR FILTER

In this method, the data transition power diminution technique for adder, multiplier and FIR filters is introduced. This work is mainly based on the effective data range of arithmetic units. For this method, the Dynamic data range

determination technique was proposed by Oscal et al [5], is used to reduce the switching activities and corresponding power in the arithmetic units.

The signal or bit switching activities of the two input data, changing from x(n-1) and y(n-1) to x(n) and y(n) respectively cause the switching power. Based upon the each input data, the input data can be divided into effective bits and non effective bits with respect to dynamic range. The entire switching activities are classified into four types, EE- Effective to Effective bits, EN-Effective to Non effective bits, NE- Non effective to Effective and NN- Non effective to Non effective bits. These switching activity styles are always represented in 2's compliment form. The EE, EN, and NE activities are represented in sign magnitude and hybrid, where as NN is represented in only sign magnitude form, because there is no sign extension bits. This proposed work is used to reduce the switching activities of EN and NN styles. [5].

The DRD technique for an adder is presented in the figure. 4. This method can be realized in the 2` compliment representation and sign magnitude representations. Initially, the effective dynamic ranges of every input date can be calculated and higher effective dynamic range will be considered. Hence few blocks of an adder used for the addition process and the result is scaled down for the matching of original word length according to its numerical representation. The less dynamic power is consumed by unused blocks of the adder. Here, the input bits of the unused adder blocks are unchanged states.

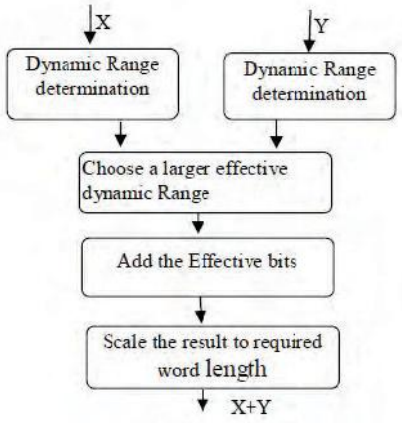

Figure 5. The DPDT for Addition.

For the case of NN, no switching activity and no switching power due to non effective bits of the side by side data are 0 only. The EE, EN, NE, and NN can have the switching activities in 2's compliment representation. The EE and NE are mainly for the DRD technique in the representation of 2's compliment form for the realization of sign magnitude. The NN origination from sign extension bits for the sign change. In the EN case, the switching activities are reduced . These are cannot be eliminated.

A) DPDT Adder Design

The next proposed technique is Data Transition Power Diminution technique (DPDT), which reduces the dynamic power dissipation by reducing the switching activity. The DPDT separates the entire designed circuit into two parts are MSP and LSP. These are most significant part and Least significant part. The MSP circuit turns off whenever they do not affect the results. The 16-bit two's complement adder using DPDT, shown in the figure. 5. In this, the 16-bit 2's complement adder is divided into MSP and LSP at the place between 8^{th} and 9^{th} bits. To control the input data of the MSP some latches are placed in the circuit. When the MSP is turned on, there is no change in the input data. If the MSP is turned off, the previous value is as input. This concept reduces the glitching power consumption. A control logic is required to know whether the MSP affects the computation results or not. This control logic helps to detect the effective ranges of the inputs.

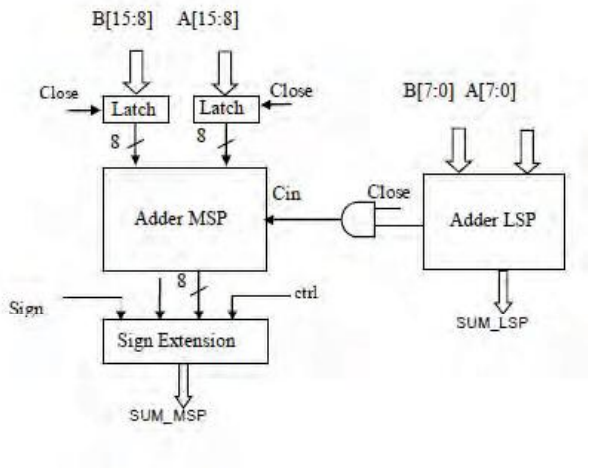

Figure 6. Two's Complement Adder based on DPDT.

B) Multiplier using DPDT

The multiplier design using DPDT is illustrated in the figure. 6(a) and 6(b). According to the Booth encoder, the partial product generator generates the five different partial products, i.e (-2A, -A, 0, A, 2A). These operations are selected and performed on operand B using the Booth encoding method. The partial products, P0 to P7 are accumulated by the adders A1, A2, D1 and D2. Here, the adders A1 and A2 are normal adders used in LSP. The D1 and D2 are DPDT adders, which are used in MSP. The second partial input to all adders are left shifted by 2 bits. The outputs are sign extended by 2bits [6].

The output of the first stage is given as input to the second stage. The output of this stage is sign extended to 4 bits. The output of the second stage is given as input to the third stage. The output of this stage is sign extended to 6 bits. If the Booth encoded value is the small absolute value, then the power dissipation due to data transition will be minimized in the compression tree. According to concept of the redundancy, some of the adders in the multiplier compression tree are replaced with the DPDT adders. The bit-widths of the LSP and MSP are indicated in fraction values nearing the corresponding adder in figure. 6 (b).

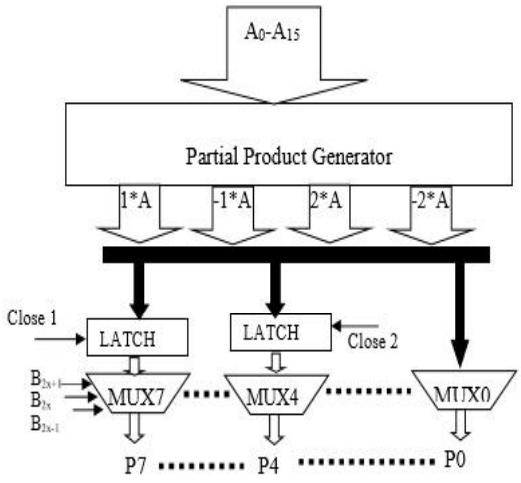

Figure. 7 (a) Booth multiplier using DPDT

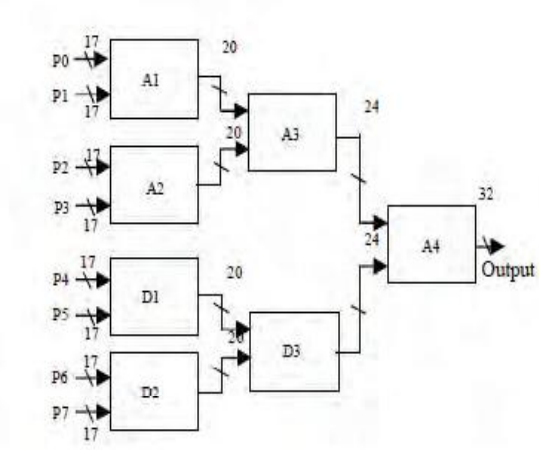

Figure. 7 (b). Low Power Multiplier using DPDT

C) Low-power digital filter design

The FIR filter is implemented using mainly three hardware elements namely, adder, multiplier and unit delay. The function of the unit delay is updating its output once per every sample period. The figure. 7 represents the DPDT low power direct form structure, which is implemented using DPDT adders and DPDT multipliers. The input sequence x(n) is first multiplied by the coefficient h0 using DPDT equipped multiplier [7]. The input sequence is then delayed by unit delay element. After being subjected to each delay, the input sequence gets multiplied by the other coefficients viz. from h1 to hM-1. The multiplied values are then added, to give the output y(n).

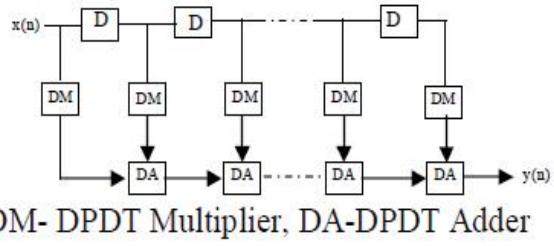

Figure 8. Direct Form Filter Structure using DPDT.

The figures 9 and 10 represents the simulated outputs for the 16 bit adder and FIR filter using DPDT technique.

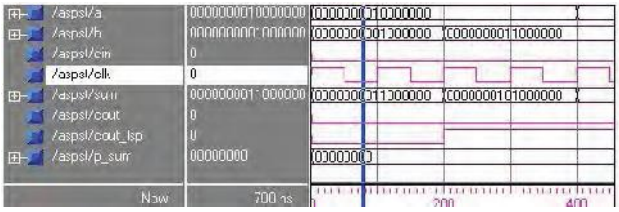

Figure 9. Simulation Result for 16Bit Adder using DPDT

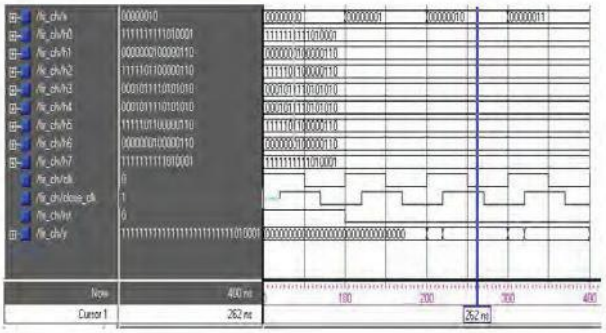

Figure 10. Simulation Result for FIR Filter with Booth multiplier using DPDT

IV. RESULTS

These methods are validated for the target device of Spartan-3 FPGA. The techniques are simulated and synthesized in Xilinx software. The significant high speed and power reduction over traditional Distributed Arithmetic based techniques. The results listed in the table. 1 depicts the performance metrics. Those are frequency, power, delay and area of the different efficient FIR filter architectures.

The bar graph shown in the figure. 11 represents the comparison of the FIR filter parameters. In this, the operating frequency of the variable precision fine grain pipelining FIR filter is comparatively high and delay is very less. The power consumption of this architecture is more than the DPDT FIR filter.

The area of the DPDT fir filter is larger than the Variable precision pipelining FIR filter architecture is shown in the figure. 12.

TABLE.I
COMPARISON BETWEEN DIFFERENT FIR FILTER PARAMETERS.

	Variable precision pipelining FIR	DPDT FIR
Frequency (MHz)	81.6	25
Power (mW)	350	326
Delay (nS)	12.25	81.21
Area	12036 gate count	27622 gate count

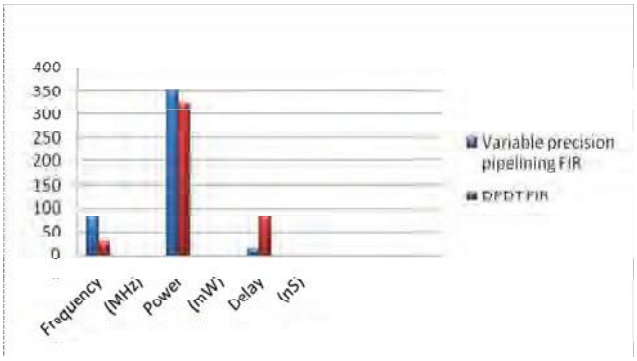

Figure.11 Bar graph for design parametrs of two FIR architectures.

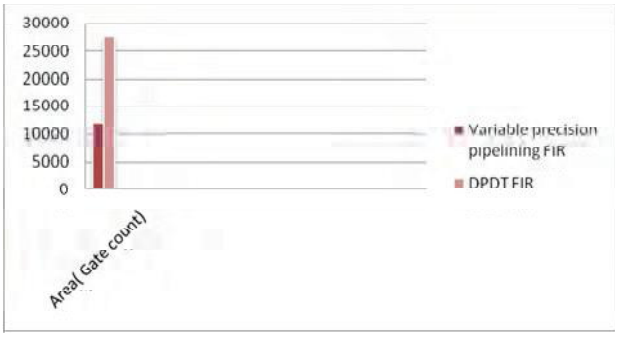

Figure.12 Bar graph for Area comparison of two FIR architectures.

V. CONCLUSIONS

In this paper, two types of efficient performance VLSI architectures required for digital signal processing are designed with different implementation techniques.

The variable precision two-dimensional fine grain pipelining in the FIR filter is discussed. The results-in comparison with the conventional existing techniques make it clear that the variable precision method reduces the power consumption by 18% with 3% additional area. But delay is very much less comparatively with other method. In the area wise, It is the second best architecture.

The second method, called data transition power diminution technique has been applied on adders, multipliers and FIR filter to reduce the power consumption. This FIR filter, using a Booth multiplier with DPDT has been implemented in FPGA. There is a decrease in power consumption, area and delay by 31%, 17.9% and 3%, respectively, when compared to the existing FIR filter, using normal Booth multipliers and normal adders.

For minimum power and high speed applications, the variable precision two dimensional fine–grain pipelining architecture can be preferred. Designing low power System-on-Chip (SoC) for multi-media applications where the less signal correlations, the DPDT is a better method. As DSP continues to make a major impact in many key areas of technology, the two methods have vast opportunities for expansion.

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Synthesis and Anticancer Molecular Docking Studies of Phenothiazine Derivatives

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Abstract: **Phenothiazine incorporated pyran derivatives are prepared by using N-alkyl-phenothiazine-3-carbaldehydes under ultrasonic/reflux condition by one step synthesis. Improvement in yield is observed when the reaction is carried out under ultrasonic condition compared to classical synthetic method. The synthesized compounds are characterized by using FT-IR, ^{1}H NMR, ^{13}C NMR and mass spectral data. Anticancer docking studies are carried out for the synthesized compounds and different cancer target proteins namely lung cancer, colon cancer, breast cancer and pancreatic cancer and the results are reported.**

***Index Terms*— Phenothiazine, Pyran, Anticancer docking and Ultrasonic Irradiation.**

I. Introduction

Hetero aromatic compound containing Nitrogen and Sulfur atom in their backbone is being pursued as a thrust area of research in Chemistry due to its potential applications of these derivatives are used in pharma field. The combination of two or more pharmacophores in one molecule is an idea involved in designing of new biologically active chemical compound including natural alkaloids. Phenothiazine, a hetero aromatic tricyclic compound containing nitrogen and sulfur hetero atom in their ring has been well known for a period of hundred years. The first parent compound of unsubstituted phenothiazine was synthesized in 1883 by a synthetic chemist Bernthsen.

These derivatives were used in treatment of psychopathy for the first time and to get better results. Phenothiazine is a heterocyclic compound of possess lots of pharmaceutical applications such as antifungal [1], antibacterial [2-3], anti-inflammatory [4], anti-malarial [5], anti-psychotropic [6], antimicrobial [7], antitubercular [8-9] activities. It is reported that these derivatives have a few significant anticancer activities. These characteristics have generated a great interest in formulating and synthesizing new phenothiazine to investigate their anticancer activities. [10-11].

Phenothiazine derivatives also act as human cholinesterase inhibitors and on several occasions, these derivatives have been characterized as multidrug resistance (MDR) reversal agents [12-13]. The literature reports have shown that the anticancer activity of phenothiazine derivatives are determined by the substituents linked to Carbon-2 position of phenothiazine ring, extent of alkyl group connecting nitrogen atom attached at position (N-10) of the cyclic ring, also the terminal N-H group present in ring [14-15]. This activity is firmly bound to the nature of substituents attached to phenothiazine ring rather than nature of side chain present [16].

Phenothiazine derivatives are used as neuroleptic drugs because they cross the blood brain barrier possess a strong affinity to lipid-rich tissues and lipid bilayers in neurons because of high degree of lipophilicity of phenothiazine derivatives [17]. In order to get active neuroleptic agents containing hydrogen atoms attached to nitrogen N-10 carbon-2 atoms are replaced by different groups attached at N-10 position such, as piperidin, aliphatic side chain and piperazine derivatives are given in literature [18]. They are also used as antipsychotic drugs because of their easily interaction with various receptors in central nervous system particularly which blocks the dopaminergic receptors [19].

A. Experimental procedure

General: All the chemicals were purchased from SD Fine Chemicals (India), Sisco Research Laboratory and Sigma-Aldrich (USA). Open capillary tubes were used to determine melting point of reported compound by a Buchi-530 melting point apparatus and the results were uncorrected. Perkin Elmer of FT-IR 1600 RX1 spectrophotometer used for recording FT-Infra Red spectra and potassium bromide used as discs. Proton and Carbon NMR were recorded using AV-400MHz and Bruker DPX 400 MHz spectrometer using deuterated chloroform and dimethyl sulphoxide a solvent by using an internal reference of Tetramethylsilane (TMS). Mass spectra were obtained using HR mass spectrometer and the compounds were dried under vacuum before analysis.

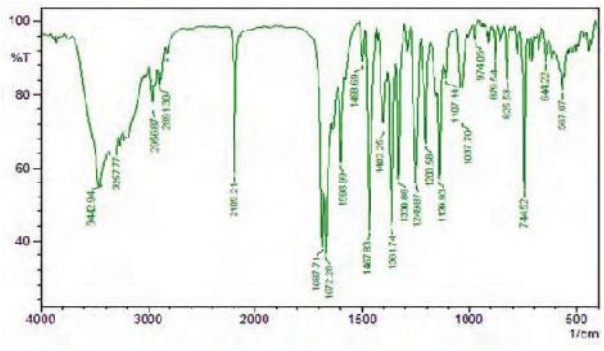
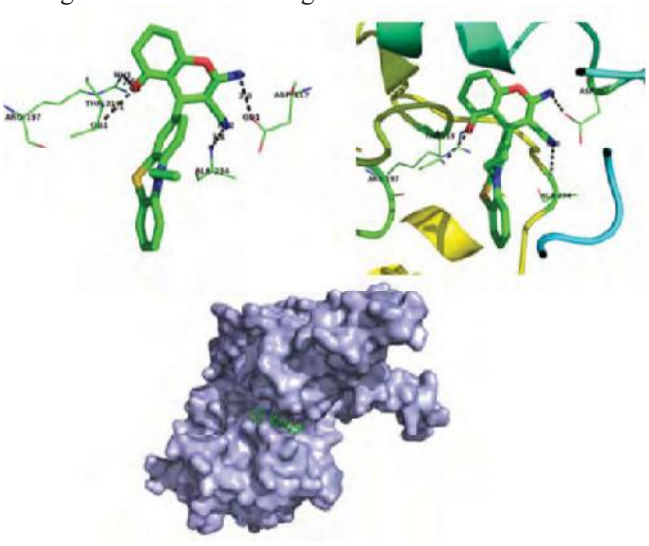


Figure 1. IR spectrum of compound **4a**.

B. Docking Analysis

Geometry optimized structures for all new synthesized derivatives were obtained using iGEMDOCK automated docking program. The 3-dimensional coordinates of different target cancer proteins were selected from protein

data bank (PDB). The PDB id of pancreatic cancer (1SVC), lung cancer (1MOX), colon cancer (4FLH), and breast cancer (2DSQ) were chosen for docking study. The 3D structure of ligand molecules and therapeutic target proteins were executed through GEMDOCK graphical interface. Before starting docking analysis, the output path was set. The default parameters were included such as population size (n=200), number of solutions (s=10) and generation (g=70) to compute the feasible binding mechanism of ligand moiety for each target protein. The docking run was initiated through GEMDOCK scoring function.



Figur. 2. Active sites of Rho-associated protein kinase 1 of compound **4d** by docking studies.

The binding pose of every ligand molecule was observed after docking analysis and their affinity with target proteins were analyzed. Binding geometries are predicted by visual examination which contributes essentially further development of a new compound. The best binding pose and total energy of each ligand molecules were analyzed using post docking analysis and the details were saved in output folder. Pymol automated docking software used to analyzed and visualized the protein-ligand binding site [20-21].

Protocol for the preparation of compound 2(a-b):

In a 50 mL two-necked RB flask a mixture of Phenothiazine (1.0 mmol), ethyl or methyl iodide (3.0 mmol) and DMF (25 mL) were taken. The solution was heated in an oil bath at 75°C, potassium tert-butoxide was added (1.5 mmol) and stirred for 24 hours. Completion of reaction was observed through thin layer chromatography, and cooled to room temperature and transferred into ice cooled water, the reaction mixture was extracted using chloroform and dried using sodium sulphate salt to get crude product. The impure products were subjected to column chromatography using hexane/ethyl ethanoate (4.5:0.5) to get pure compound as a colourless solid (yield: 81-83%).

Spectral data of compound 2a: mp. 96-98 ºC; IR (KBr) νmax: 1130, 1280, 1327, 1384, 1440, 1483, 1570, 1591, 1788, 1899, 2826, 2937, 2981, 3053 3053, cm^{-1}; ^1H NMR (500 MHz, ppm, $CDCl_3$), δ_H 3.40 (s, 3H, CH_3), 6.84 (d, 2H, *J* 8.0 Hz, C_3, C_6- Ph-H), 6.95-7.28 (m, 6H, Ph-H); ^{13}C NMR (125.787 MHz, ppm, $CDCl_3$), δ_C 35.3, 114.0, 122.4, 123.4, 127.4, 145.8; Mass (EI): *m/z* [M^+] calculated for $C_{13}H_{11}NS$: 212.0612; obtained: 212.2038.

Spectral data of compound 2b: mp. 102-104ºC; IR (KBr) νmax: 1107, 1136, 1163, 1259, 1286, 1330, 1456, 1489, 1568, 2816, 2879, 2960, 3055 cm-1; 1H NMR (500 MHz, ppm, $CDCl_3$), δ_H 1.46 (t, 3H, *J* 5.4Hz, CH_3), 3.96 (d, 2H, *J* 5.7Hz, CH_2), 6.90-7.28 (m, 8H, Ph-H); ^{13}C NMR (125.787 MHz, ppm, $CDCl_3$), δ_C 13.7, 41.6, 115.1, 122.3, 124.5, 127.2, 127.4, 145.0; Mass (EI): m/z [M^+] calculated. for $C_{14}H_{13}NS$: 227.0769; obtained: 227.1685.

Protocol for the preparation of compound 3(a-b):

In a two necked RB flask a solution of $POCl_3$ (4.1 mmol) and freshly distilled dry DMF (4.7 mmol) was added drop wise at 0°C under inert or nitrogen atmospheric condition. The compound **2(a-b)** (1.0 mmol) dissolved in 40 mL of DCM and the solution was added dropwise to the $POCl_3$/DMF complex at 30°C. The reaction mixture was stirred at 80°C in an oil bath for 16 hours. Completion of the reaction was monitored through thin layer chromatography and then cooled to room temperature and poured it to 200 grams of ice crystals. The reaction mixture was neutralized by adding sodium bicarbonate solution, then extracted with chloroform, dried using sodium sulphate salt and the excess solvent was evaporated using vacuum distillation to get crude product. The impure product was subjected to column chromatography hexane/ethyl ethanoate solvent; to get pure yellow coloured compound, yield obtained was 79-82%.

Spectral data of compound 3a: mp. 106-108 ºC; IR (KBr) νmax: 1036, 1144, 1288, 1327, 1566, 1595, 1641, 1678, 2884, 3056 cm^{-1}; ^1H NMR (400 MHz, ppm, $CDCl_3$), δ_H 3.37 (s, 3H, CH_3), 7.00-7.74 (m, 7H, Ph-H), 9.79 (s, 1H, CHO); ^{13}C NMR (100.602 MHz, ppm, $CDCl_3$), δ_C 35.6, 114.5, 115.4, 121.1, 122.3, 123.5, 126.9, 127.2, 128.0, 130.4, 130.8, 143.6, 150.4, 190.6; Mass (EI): *m/z* [M+] calculated. for $C_{14}H_{11}NOS$: 241.0351; obtained: 241.0187.

Spectral data of compound 3b: mp. 109-111 ºC; IR (KBr) νmax: 1042, 1135, 1199, 1238, 1310, 1466, 1552, 1572, 1669, 2738, 2827, 2931, 2977, 3057 cm^{-1}; ^1H NMR (400 MHz, ppm, $CDCl_3$), δ_H 1.45 (d, 3H, *J* 6.4Hz, CH_3), 3.97 (d, 2H, *J* 6.4Hz, CH_2), 7.62 (d, 1H, *J* 8.4Hz, C_7-Ph-H), 7.56 (s, 1H, C8- Ph-H), 6.89-7.26 (m, 5H, Ph-H), 9.78 (s, 1H, CHO); ^{13}C NMR (100.602 MHz, ppm, $CDCl_3$), δ_C 12.8, 42.4, 114.4, 115.6, 123.2, 124.4, 127.6, 128.2, 130.2, 143.0, 150.3, 190.0; Mass (EI): *m/z* [M^+] calculated. for $C_{15}H_{13}NOS$: 255.1688; obtained: 255.1798.

Protocol for the preparation of compound 4(a-d).

Conventional method: In a 100 mL RB flask a mixture of compound **3a-b** (1.0 mmol), 1,3-diketone (1.0 mmol), malononitrile 1.0 mmol, K_3PO_4 (15 mmol%) and 20% ethanol (5 ml) were refluxed with constant stirring at 80°C in an oil bath for the period of time listed in Table. 1 (completion of reaction monitored by thin layer chromatography using hexane/ethyl ethanoate as eluent). The reaction mixture on cooling to get precipitated crude

product and the solid obtained was filtered and recrystallization process was done by using ethanol solvent to get pure product.

Ultrasonic method: In a 25 mL beaker, a mixture of compound **3a-b** (1.0 mmol), 1,3-diketones 1.0 mmol, malononitrile (1.0 mmol) in the presence of K_3PO_4 catalyst 15 mmol% and 20% ethanol (5 ml) were sonicated using ultrasonic probe at frequency range of 22 kHz for the given periods of time listed in Table. Completion of the reaction observed by thin layer chromatography, the precipitate obtained was filtered using funnel and washed with large amount of water and purified by recrystallization process using ethanol solvent.

Spectral data of compound 4a: mp. 194-196 ºC; IR (KBr) νmax: 1037, 1103, 1203, 1249, 1330, 1361, 1402, 1467, 1598, 2189, 2891, 2958, 3257, 3442 cm^{-1}; ^1H NMR (400 MHz, ppm, $CDCl_3$), δ_H 0.97 (s, 3H, CH_3), 1.03 (s, 3H, CH_3), 2.37 (q, 2H, *J* 7.8Hz, CH_2), 3.27 (s, 3H, N-CH_3), 4.25 (s, 1H, CH) 4.49 (s, 2H, NH_2), 6.67 (d, 1H, *J* 7.6Hz, C_4- Ph-H), 2.14 (q, 2H, *J* 6.6Hz, CH_2), 6.71 (d, 1H, *J* 7.6Hz, C_2-Ar-H), 6.84-7.20 (m, 5H, Ph-H); ^{13}C NMR (100.602 MHz, ppm, $CDCl_3$), δ_C 27.8, 28.6, 32.2, 34.6, 35.2, 40.4, 50.7, 63.2, 113.7, 118.5, 122.3., 123.0, 123.5, 125.8, 127.2, 127.4, 137.5, 144.8, 145.7, 157.4, 161.3, 195.8; Mass (EI): *m/z* [M^+] calculated for $C_{25}H_{23}N_3O_2S$: 429.1511, obtained: 429.1514.

Spectral data of compound 4b: mp. 161-163 ºC; IR (KBr) νmax: 1035, 1215, 1251, 1385, 1485, 1606, 1680, 2191, 2933, 2958, 3170, 3255, 3352 cm^{-1}; ^1H NMR (400 MHz, ppm, $CDCl_3$), δ_H 0.99 (s, CH_3, 3H), 1.03 (s, CH_3, 3H), 1.32 (s, 3H, CH_3), 2.15 (s, 2H, CH_2), 2.37 (q, 2H, *J* 7.6Hz, CH_2), 3.82 (s, 2H, N-CH_2), 4.24 (s, 1H, CH), 4.45 (s, 2H, NH_2), 6.82-7.20 (m, 5H, Ph-H), 6.71 (d, 1H, *J* 7.3Hz, C_2-Ar-H), 6.75 (d, 1H, *J* 6.8Hz, C_2-Ar-H); ^{13}C NMR (100.602 MHz, ppm, $CDCl_3$), δ_C 12.9, 27.9, 28.6, 32.2, 34.5, 40.6, 41.7, 50.6, 63.4, 113.3, 14.8, 118.5, 122.1, 124.0, 126.1, 126.9, 127.1, 137.3, 144.1, 144.8, 157.3, 161.3, 195.8; Mass (EI): *m/z* [M^+] calculated for $C_{26}H_{25}N_3O_2S$: 443.1667, obtained: 443.1663.

Spectral data of compound 4c: mp. 150-152 ºC; IR (KBr) νmax: 1125, 1260, 1334, 1365, 1485, 1566, 1606, 1647, 1680, 2191, 2203, 2922, 3360 cm^{-1}; ^1H NMR (400 MHz, ppm, $CDCl_3$), δ_H 2.02-2.20 (m, CH_2, 2H), 2.28-2.35 (m, 2H, CH_2), 2.40-2.59 (m, CH_2, 2H), 3.32 (s, 3H, *N*-CH_3), 4.34 (s, 1H, CH), 4.52 (s, 2H, NH_2), 6.74 (d, 1H, *J* 7.2Hz, 4- Ph-H), 6.85 (d, 1H, *J* 7.5Hz, C_2- Ph-H), 6.91-7.23 (m, 6H, Ph-H); ^{13}C NMR (100.602 MHz, ppm, $CDCl_3$), δ_C 20.0, 26.8, 35.9, 36.7, 401., 60.5, 114.0, 114.5, 121.9, 122.3, 124.1, 124.3, 125.3, 125.8, 127.3, 127.8, 129.0, 131.6, 143..2, 151.2, 157.4, 194.2; Mass (EI): *m/z* [M^+] calculated for $C_{23}H_{19}N_3O_2S$: 401.1198, obtained: 401.1192.

Spectral data of compound 4d: mp. 143-145 ºC; IR (KBr) νmax: 1120, 1271, 1365, 1483, 1576, 1600, 1648, 1679, 2190, 2922, 3268, 3382 cm^{-1}; ^1H NMR (400 MHz, ppm, $CDCl_3$), δ_H 1.25 (s, CH_3, 3H), 1.46-1.55 (m, CH_2, 2H), 2.02 (m, 2H, CH_2), 2.57 (q, 2H, *J* 6.6Hz, CH_2), 3.48 (s, 2H, N-CH_2), 4.33 (s, 1H, CH), 4.50 (s, 2H, NH_2), 6.74 (d, 1H, *J* 8.1Hz, C_4- Ph-H), 6.82 (d, 1H, *J* 8.1Hz, C_2- Ph-H), 6.93-7.25 (m, 5H, Ph-H); ^{13}C NMR (100.602 MHz, ppm, $CDCl_3$), δ_C 13.1, 20.2, 27.1, 36.9, 41.8, 42.8, 59.8, 114.5, 114.9, 115.3, 124.2, 127.3, 127.6, 127.9, 129.4, 131.6, 144.2, 150.4, 157.5, 194.4; Mass (EI): *m/z* [M^+] calculated for $C_{24}H_{21}N_3O_2S$: 415.1534, obtained: 415.1530.

II. RESULTS AND DISCUSSION

Phenothiazine (1) was treated with methyl, ethyl iodide using potassium tertiary but-oxide catalyst and dry DMF used as a solvent and heated in an oil bath around 80 ºC for 24 hours to yield alkyl substituted phenothiazine **2a-b** (Scheme 1). The compound **2a** showed a singlet peak at δ 3.40 ppm in ^1H NMR spectrum of corresponds to methyl group which is an evidence for the compound **2a** formation. The disintegration of N-H band at 3420 cm^{-1} in IR spectra of **2a** supporting the formation of alkyl phenothiazine. The compound **2b** showed a quartet peak at δ 3.96 ppm and triplet peak at δ 1.47 ppm in ^1H NMR spectrum indicating the formation of CH_2 and CH_3 protons which is an evidence for compound **2b** formation. The compound **2b** showed peaks at δ 41.76 and 14.09 ppm in ^{13}C NMR spectrum indicated the presence of CH_3 and CH_2 carbons in compound **2b**.

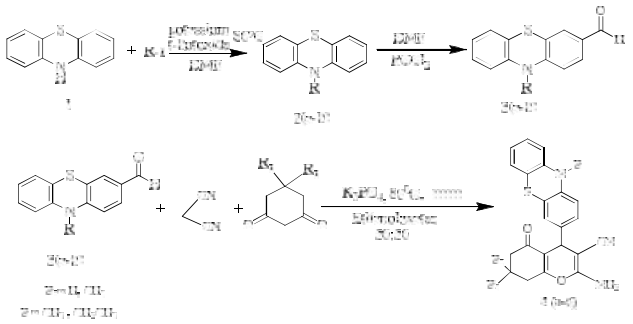
TABLE I
PHYSICAL DATA OF SYNTHESIZED COMPOUNDS

Compound	R	R_1	Reaction Time [a] (min)	Yield[a,b](%)	m.p. (°C)
4a	CH_3	CH_3	165/7	85/87	195-197
4b	CH_2-CH_3	CH_3	170/8	83/86	160-162
4c	CH_3	H	175/8	84/86	152-155
4d	CH_2-CH_3	H	180/9	81/83	145-147

[a]At reflux temperature/ ultrasonic irradiation; [b]Isolated yields

The compound **2a-b** on treatment with Vilsmeier Hack reaction to get compound **3a-b** with a yield of 78-80%. The compound **3a** and **3b** showed a singlet peak at δ 9.76 and 9.78 ppm observed in ^1H NMR spectra indicating the formation of aldehyde hydrogen and the peaks at δ 190.68 and 190.10 ppm in ^{13}C NMR spectra also confirming the presence of aldehyde carbon. The compound **3a** and **3b** showed the absorption peak at 1679 and 1665 cm^{-1} in IR spectra indicated the presence of aldehyde carbonyl group which is also an evidence for the formation of **3a** and **3b**.
The compound **4(a-d)** was prepared by one step multi constituent reaction of dimedone, malono nitrile, **3(a-b)** and K_3PO_4 catalyst were heated at 100 °C with equal ratio of Et-OH and water was used as a solvent for a given period of time listed in table and the same reaction was carried out using ultra sonication. The compound **4a** showed absorption frequency at 3432 and 3263 cm^{-1} in IR spectra due to amine group at 2187 cm^{-1} due to CN and 1686 cm^{-1} (Figure. 1) due to ketonic group which is also supporting the compound **4a** formation.

SCHEME I
SYNTHETIC PROTOCOL OF COMPOUND **4a-d**.



The compound **4a** shows two singlet peaks at δ 1.02, 0.98 ppm corresponds to CH_3 hydrogens of cyclomethone, while CH_2 hydrogen of cyclomethone appeared as quartet peak δ 2.39, 2.13 and CH_3 hydrogen attached to nitrogen appeared at δ 3.29 as a singlet. The peak at δ 4.25 ppm belongs to benzylic methyl hydrogen and the singlet peak at δ 4.49 ppm belongs to -NH_2 hydrogen and which is clearly indicating the compound **4a** formation. The structures of all the synthesized derivatives were conformed through spectral techniques such as IR, ^1H, ^{13}C NMR and mass spectra. The physical data of all the newly reported derivatives were summarized in Table 1.

C. Molecular docking studies

Docking studies of synthesized pyran derivatives have been studied to find out the best drug moiety giving an insight into substituted and configurational needs for perfect receptor pit which cause the evolution of best pharmacophore moiety. These models are achieved to get more precise and consistent picture of the potentially active biological molecules at the atomic level and also produce new insights that could be used to develop new therapeutic agents.

In anticancer docking results, only best conformers were chosen and dock value for every ligand listed in Table 2. Most stable receptor ligand complex form is the one which has low dock value. The best docked conformer of every ligand and receptor were joined together and their complexes were optimized energetically after docking execution by define a radius of 10A° measured from the docked ligand. Step by step optimization energy was done by using first hydrogen, side chains attached and finally the backbone of receptor molecule.

Fig. 2, shows the binding relationship between compound **4d** and protein kinase 1 active site residues interact with Arg 197, Thr 219, Asp117 and Ala 234.

TABLE II
DOCKING SCORES OF THE SYNTHESIZED COMPOUNDS.

Compound	Docking score (Binding energy)			
	Breast Cancer	Colon Cancer	Lung Cancer	Pancreatic Cancer
4a	-93.04	-86.24	-90.09	-83.87
4b	-93.55	-92.00	-83.92	-83.54
4c	-97.29	-94.78	-78.13	-78.34
4d	-104.89	-89.55	-91.56	-86.26

Important hydrogen bonding interaction takes place between Thr 219 and the (C=O) oxygen atom of pyran ring, another strong bonding takes place between Asp117 and Ala 234 and the nitrogen atom attached to the pyran ring.

III. CONCLUSIONS

In conclusion, it is found that a simple and efficient method for the synthesis of phenothiazine substituted different pyran derivatives under conventional heating and ultrasonic method. The main advantages of ultrasonic irradiation are those which include yield improvement, short reaction times, easy reaction set-up and use of very little amount of solvents or without solvents. The synthesized phenothiazine derivatives were subjected to anticancer molecular docking studies using four dissimilar cancer target proteins. The results of anticancer docking studies showed that the synthesized compound **4d** possess significant binding energy with breast cancer when comparing with other compound.

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In the next issue (Vol 13, December, 2017)

1.	**SPMSM Drive Controlled by Diode Clamped Multilevel Inverters**	*Dr. G. Sree Lakshmi*
2.	**Study of Star Connected Cascaded H-Bridge STATCOM using Different PWM Techniques**	*Ch. Lokeshwar Reddy, P. Rajesh Kumar*
3.	**MUTAWEB – Mutation Testing Tool for Servlet based Web Applications**	*S.Suguna Mallika,Samuel Vineeth, Rohith Rangaraju, Shabana Begum*
4.	**Labview based Greenhouse Automation**	*S.Harivardhagini*

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Abstract: **These instructions give you basic guidelines for preparing camera-ready papers for CVR College journal Publications. Your cooperation in this matter will help in producing a high quality journal.**

***Index Terms*—first term, second term, third term, fourth term, fifth term, sixth term**

I. Introduction

Your goal is to simulate the usual appearance of papers in a Journal Publication of the CVR College. We are requesting that you follow these guidelines as closely as possible. It should be original work. Format must be done as per the template specified. Diagrams with good clarity with relevant reference within the text are to be given. References are to be cited within the body of the paper. Number of pages must not be less than five, but not more than eight.

A. Full-Sized Camera-Ready (CR) Copy

Prepare your CR paper in full-size format, on A4 paper (210 x 297 mm, 8.27 x 11.69 in). No header or footer, no page number.

Type sizes and typefaces: Follow the type sizes specified in Table I. As an aid in gauging type size, 1 point is about 0.35 mm. The size of the lowercase letter "j" will give the point size. Times New Roman has to be the font for main text. Paper should be single spaced.

Margins: top = 30mm (1.18 in), bottom, left and right = 20 mm (0.79 in). The column width is 82mm (3.23 in). The space between the two columns is 6mm (0.24 in). Paragraph indentation is 3.7 mm (0.15 in).

Left- and right-justify your columns. Use tables and figures to adjust column length. On the last page of your paper, adjust the lengths of the columns so that they are equal. Use automatic hyphenation and check spelling. Digitize or paste down figures.

For the Title use 24-point Times New Roman font, an initial capital letter for each word. Its paragraph description should be set so that the line spacing is single with 6-point spacing before and 6-point spacing after. Use two additional line spacings of 10 points before the beginning of the double column section, as shown above.

Each major section begins with a Heading in 10 point Times New Roman font centered within the column and numbered using Roman numerals (except for ACKNOWLEDGEMENT and REFERENCES), followed by a period, two spaces, and the title using an initial capital letter for each word. The remaining letters are in SMALL CAPITALS (8 point). The paragraph description of the section heading line should be set for 12 points before and 6 points after.

TABLE I.
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8	Section titles, tables, table names, first letters in table captions, figure captions, footnotes, text subscripts, and superscripts		
9	References, authors' biographies	Abstract	
10	Authors' affiliations, main text, equations, first letters in section titles		Subheading
11	Authors' names		
24	Paper title		

Subheadings should be 10 point, italic, left justified, and numbered with letters (A, B, …), followed by a period, two spaces, and the title using an initial capital letter for each word. The paragraph description of the subheading line should be set for 6 points before and 3 points after.

For main text, paragraph spacing should be single spaced, no space between paragraphs. Paragraph indentation should be 3.7mm/0.21in, but no indentation for abstract & index terms.

II. Helpful Hints

A. Figures and Tables

Position figures and tables at the tops and bottoms of columns. Avoid placing them in the middle of columns. Large figures and tables may span across both columns. Leave sufficient room between the figures/tables and the main text. Figure captions should be centered below the figures; table captions should be centered above. Avoid placing figures and tables before their first mention in the text. Use the abbreviation "Fig. 1," even at the beginning of a sentence.

To figure axis labels, use words rather than symbols.

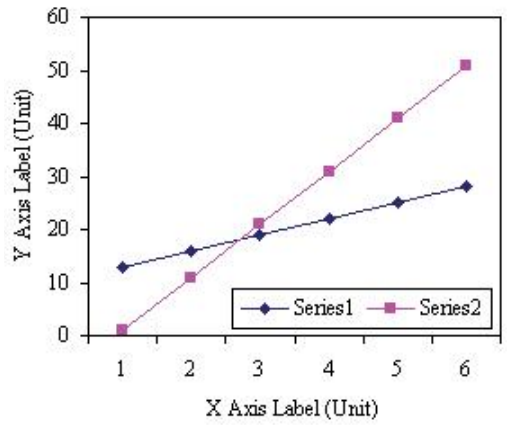

Figure 2. Note how the caption is centered in the column.

Do not label axes only with units. Do not label axes with a ratio of quantities and units. Figure labels should be legible, about 9-point type.

Color figures will be appearing only in online publication. All figures will be black and white graphs in print publication.

B. References

Number citations consecutively in square brackets [1]. Punctuation follows the bracket [2]. Use "Ref. [3]" or "Reference [3]" at the beginning of a sentence:

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C. Footnotes

Number footnotes separately in superscripts [1, 2, …]. Place the actual footnote at the bottom of the column in which it was cited, as in this column. See first page footnote as an example.

D. Abbreviations and Acronyms

Define abbreviations and acronyms the first time they are used in the text, even after they have been defined in the abstract. Do not use abbreviations in the title unless they are unavoidable.

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Equations should be left justified in the column. The paragraph description of the line containing the equation should be set for 6 points before and 6 points after. Number equations consecutively with equation numbers in parentheses flush with the right margin, as in (1). Italicize Roman symbols for quantities and variables, but not Greek symbols. Punctuate equations with commas or periods when they are part of a sentence, as in

$$a + b = c \ . \qquad (1)$$

Symbols in your equation should be defined before the equation appears or immediately following. Use "(1)," not "Eq. (1)" or "equation (1)," except at the beginning of a sentence: "Equation (1) is ..."

F. Other Recommendations

Use either SI (MKS) or CGS as primary units. (SI units are encouraged.) If your native language is not English, try to get a native English-speaking colleague to proofread your paper. Do not add page numbers.

III. Conclusions

The authors can conclude on the topic discussed and proposed, future enhancement of research work can also be briefed here.

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CVR College of Engineering (A UGC Autonomous Institution) was established in the year 2001, and its Thirteenth batch of students graduated from the College. This college is on a roll with the recent ***NIRF*** *ranking within the* ***top 4 colleges*** *in the state of* ***Telangana****, followed by record placements and now with the setting up of a new* ***Apple lab****. The new lab consists of state of the art iMacs that enables students to develop new applications on the Apple devices. With the Make in India initiative and the expected manufacturing and increased sales of Apple devices in the country, new applications need to be developed for our needs and this lab will* ***transform students into developers****.*

The College was the ***first*** *college in Telangana that was promoted by NRI technology professionals resident in the US. The NRI promoters are associated with cutting-edge technologies of the computer and electronics industry. They also have strong associations with other leading NRI professionals working for world-renowned companies like IBM, Intel, Cisco, Motorola, AT&T, Lucent and Nortel who have agreed to associate with the College with a vision and passion to make the College a state-of-the-art engineering institution.*

The college has many accomplishments and to name a few, it obtained ***NBA Tier -1 accreditation*** *for four UG programs,* ***NAAC 'A' grade****,* ***UGC autonomous status****,* ***National Employability Award for*** *sixth year in a row and got a very high rating by several ranking agencies including the most recent EducationWorld ranking of third best college in Telangana and Outlook magazine rating CVR one among the* ***top 100 colleges in the country.***

Placements at the college continue to create a ***record year after year*** *with average salary going up to a record Rs. 3.90 Lakhs and a record 20 students getting offers of above Rs. 10 Lakhs and another 160+ students above Rs. 4 Lakhs with a total of about 610 job offers. 10 students have offers of Rs. 16 Lakhs, which is the highest. CVR has made huge progressin a short span of time and will be preferred by the students and parents among* ***the top 4 colleges*** *in the state during the EAMCET counseling this year.*

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